High efficiency polycrystalline CdS/CdTe solar cells on buffered commercial TCO-coated glass

E. Colegrove[1,2], R. Banai[1], C. Blissett[1], C. Buurma[1], J. Ellsworth[1], M. Morley[1], S. Barnes[1], C. Gilmore[1], J. Bergeson[1], R. Dhere[3], M. Scott[3], T. Gessert[3] and Siva Sivananthan[1,2]

[1]EPIR Technologies Inc., Bolingbrook, IL 60440
[2]University of Illinois at Chicago, Chicago, IL 60607
[3]National Renewable Energy Laboratory, Golden, CO 80401

Contact: Mr. Eric Colegrove
Email: ecoleg2@uic.edu

Abstract

Multiple polycrystalline CdS/CdTe solar cells with efficiencies greater than 15% were produced on buffered, commercially-available Pilkington TEC Glass^{TM} at EPIR Technologies, Inc. (EPIR) and verified by the National Renewable Energy Laboratory (NREL). n-CdS and p-CdTe were grown by chemical bath deposition (CBD) and close space sublimation, respectively. Samples with sputter-deposited CdS were also investigated. Initial results indicate that this is a viable dry-process alternative to CBD for production-scale processing. Published results for polycrystalline CdS/CdTe solar cells with high efficiencies are typically based upon cells utilizing research-grade transparent conducting oxides (TCOs) requiring high-temperature processing inconducive to low-cost manufacturing. EPIR's results for cells on commercial glass were obtained by implementing a high resistivity SnO_2 buffer layer and optimizing the CdS window layer thickness. The high resistivity buffer layer prevents the formation of CdTe-TCO junctions, thereby maintaining a high open circuit voltage and fill factor; while using a thin CdS layer reduces absorption losses and improves the short circuit current density. EPIR's best device demonstrated an NREL-verified efficiency of 15.3%. The mean efficiency of hundreds of cells produced with a buffer layer between December 2010 and June 2011 is 14.4%. Quantum efficiency results are presented to demonstrate EPIR's progress toward NREL's best-published results.

Key Words: CdTe, CdS, polycrystalline, solar, buffer layer, TCO, commercial

Introduction

Disparities in efficiencies (η) between commercial modules and lab-scale cells are prevalent throughout the solar industry. This gap is particularly pronounced in the thin-film CdTe market. The CdS/CdTe solar cell has a maximum theoretical efficiency of approximately 30%, with a more conservative practical limit of around 20% [1,2]. The industry leader in CdTe solar now reports record module efficiencies of 13.4% and a record lab-cell efficiency of 17.3% [3]. Narrowing this gap is one of EPIR Technologies, Inc.'s (EPIR's) primary research interests.

EPIR's research to narrow the gap between lab and module efficiencies has two general aspects: 1) improving the cell efficiency while using materials and processes conducive to low-cost manufacturing, and 2) improving the reproducibility of high cell efficiencies. The focus of the research presented here is on improving the efficiency of cells fabricated on commercially available transparent-conducting-oxide (TCO) coated glass by optimizing the CdS material quality and using a high-resistivity buffer layer to allow the CdS layer to be made thinner. Thinning the CdS enhances the short circuit current (J_{sc}) by increasing the amount of light reaching the junction. However, film uniformity can become a problem when thinning CdS, and pinholes or other areas of incomplete coverage can lead to localized shorts between the CdTe and the TCO. TCO roughness has to be considered for avoiding TCO/CdTe shorts, e.g. a smooth TCO will require minimal CdS whereas rough TCO requires certain thickness to cover entire surface. Shunting paths between CdTe and the TCO greatly reduce the open circuit voltage (V_{oc}). A thin buffer layer, with resistivity much higher than that of the TCO, can minimize the influence of these shunting paths on the cell performance by isolating the CdTe from the TCO. The use of a buffer layer to improve device performance with thin CdS has been investigated as early as 1998 [4,5]. Significant work has been done additionally in the mid-2000's [6]. EPIR uses an undoped SnO_2 layer to serve this purpose. EPIR has seen not only a substantial efficiency gain through implementation of the buffer layer, but also a great improvement in the yield of higher-efficiency cells. This is particularly interesting considering the use of a commercially available glass/TCO and potential for these relatively simple and scalable improvements to achieve such impressive gains.

Typically, EPIR uses chemical bath deposition (CBD) to grow CdS. This is a slow, batch-style process that generates a substantial amount of waste, making it more difficult to scale to production levels than alternate dry deposition methods. While excellent results have been achieved with the CBD process, EPIR is exploring sputtered CdS as an alternate dry-deposition method that is more easily scalable and more conducive to in-line processing. Sputtered CdS has shown promising results elsewhere [7,8]. Some of EPIR's preliminary results from this work are presented here.

Methods

EPIR uses a typical polycrystalline CdS/CdTe device structure (Figure 1) with commercially available Pilkington TEC Glass™ as a superstrate. This superstrate is a soda lime glass with fluorine doped SnO_2 (SnO_2:F) as a TCO. After a simple solvent clean, a thin SnO_2 buffer layer is grown by chemical vapor deposition (CVD) at NREL. We have chosen to prepare the un-doped SnO_2 layer ourselves for improved process control at the lab scale however the CVD process is highly scalable [9]. Oxygenated CdS is then grown by CBD. The thickness, oxygen content and quality of the CdS layer are optimized by controlling the deposition rate, the precursors and the deposition time. Because CBD is a batch process, a witness sample with nearly identical CdS material properties can be analyzed alongside wafers that have undergone further processing. CdTe is grown by close space sublimation (CSS) in a helium and oxygen environment, where oxygen facilitates CdTe nucleation on the CdS surface [10]. A second CSS chamber is then used for a dry $CdCl_2$ annealing process. Photolithography followed by a nitric phosphoric (NP) etch is then performed prior to a proprietary back-contact deposition and anneal. The NP etch

creates a highly p-type region near the back contact for improved contact quality. Wafers are comprised of sixteen 0.5 cm × 0.5 cm cells. EPIR's sputtered CdS cells undergo identical processing steps except that the CdS is deposited in a sputtering chamber at NREL as opposed to being deposited by CBD at EPIR.

Current-voltage (I-V) characteristics are obtained from all completed devices using EPIR's solar simulator (Newport Oriel), which is equipped with an AM1.5g spectral filter. Devices of particular interest are sent to NREL for certification. In addition to 1st (η) and 2nd (fill factor (FF), V_{oc}, J_{sc}) level metrics, additional device parameters are extracted through further modeling of I-V characteristics. The model developed at EPIR initially segments the I-V curve into regions where certain behaviors are expected to dominate. The model then iteratively fits the entire curve starting by weighting the parameters dominant in each region appropriately and fitting them all simultaneously through the Levenburg-Marquardt technique [11,12]. Only the results shown here as being NREL-verified are from samples sent to NREL. However, when comparing results from cells sent to NREL, the relative difference between the NREL results and those obtained at EPIR was less than 2%. Quantum efficiency (QE), capacitance-voltage (C-V), and time resolved photoluminescence (TRPL) measurements were also performed at NREL for some of the devices to gain more detailed information about the device performances and the limitations on their performance. EPIR measured the transmittance and reflectance of the CdS witness films with a Perkin Elmer LAMBDA 950 spectrophotometer to gain insights into the CdS layer quality prior to any further processing.

Results

Using the device architecture described previously and a series of focused process optimizations, EPIR has produced multiple polycrystalline CdS/CdTe solar cells on commercially available TCO coated glass with efficiencies above 15%. The best device without an antireflection coating (ARC) exhibited an NREL-verified efficiency of 15.3%. The I-V characteristic and measured device parameters for this cell are shown in Figure 2.

The implementation of a buffer layer has been crucial in achieving these results. Table 1 shows the I-V characteristic parameters and certification dates of the NREL-verified cells. The NREL deposited buffer layer was implemented after the 12.02% cell was tested. Within the next 6 months the obtained cell efficiencies increased 3.2 absolute percentage points, and further improvements are expected. The values obtained for J_{sc}, V_{oc} and FF all increased. The J_{sc} increase was directly related to the thinning of the CdS, which reduced absorption losses in the window layer. The FF and V_{oc} values were maintained and even increased through implementation of the buffer layer.

A comparison of QE data for a production module from a large scale manufacturer, NREL's best lab cell, and EPIR's 15.3% cell is shown in Figure 3 [1]. In addition to an ARC, NREL's best lab cell used a high-quality, high-temperature, TCO. The overall lower QE of EPIR's cell compared to that of NREL is primarily an effect of decreased glass transmission, a lower quality TCO and the absence of an ARC. The higher-quality TCO and glass utilized in the NREL device have a lower light absorption over the entire spectral range of interest, so the NREL device shows a 5%-10% higher QE across this entire range. The thinning of the CdS layer is significant predominantly in the short wavelength region, as light absorption in the CdS occurs primarily in that region. This effect is observed most significantly when comparing EPIR's cell to the production module. EPIR's cell has far better QE in this short wavelength region. This is an indication that the production module had a thick CdS layer. If a buffer layer was not implemented, thick CdS is a good way to improve repeatability. A buffer layer can account for this repeatability issue as well and is discussed below. Maintaining a high V_{oc} and FF with the devices utilizing thin CdS deposited by CBD was only possible after the implementation of the resistive SnO_2 buffer layer. These results are among the best reported CdS/CdTe solar cell efficiencies utilizing commercial TCO-coated soda lime glass. Previous publications have

reported devices produced on TCO-coated soda lime glass with efficiencies on the order of 15%, but these have not been independently verified[13,14].

Analysis of C-V measurements on the EPIR devices indicates an average loss of about 10 mV in the built-in voltage (V_{bi}) of the junction from thicker to thinner CdS samples with a buffer layer. This loss in V_{bi} is vastly outweighed by the enhanced J_{sc} of the device resulting in an improved overall efficiency of the cells with a thinner CdS layer and a buffer layer. Minority carrier recombination lifetimes derived from TRPL measurements were generally between 1 and 2 ns with no significant differences between devices with and without a thinner CdS layer and buffer layer.

Demonstrating good performance in a single cell is important as a proof of concept for the possibility of improving module efficiencies, but obtaining uniformly high-performance cells is also a primary concern. The mean efficiency of all of the hundreds of cells produced at EPIR with a buffer layer between December 2010 and June 2011 is 14.4%. The distribution of cell efficiencies is given in Figure 4. The standard deviation for this distribution is 0.6 percentage points. This result indicates that the implementation of a buffer layer not only improved individual cell performances, but also facilitated impressive reproducibility of that improved performance. This consistency is necessary for the manufacturing of solar modules.

Device models developed at EPIR described above were applied to hundreds of cells with and without buffer layers and the resulting fits were analyzed. The results indicate that increases in both the diffusion current in the bulk region of the CdTe layer (I_d) and the series resistance (R_s) correlate to the presence of the buffer layer. Assuming absorption and carrier generation occur predominantly in the depletion region, electrons and holes can quickly be swept out of the junction by the built in potential. The electrons then quickly reach the buffer and back contact considering comparatively thin CdS. The presence of a buffer layer will account for the increase in R_s. The potential loss in the FF due to an increased R_s can be compensated for by a vastly improved shunt resistance. The observed improvement in V_{oc} for cells with a buffer cannot come from the R_s improvement, but rather can be attributed to the improved I_d seeing as the holes must traverse the bulk CdTe region to reach the back contact. The observed increase in I_d may be due to a higher quality CdTe associated with the buffered superstrate, but further investigation would be required. These results indicate that some of the improvements in our 2nd level metrics may also be attributed to this unexpected improvement in I_d.

In keeping with the goal of addressing the discrepancy between module and lab cell performance, EPIR is also investigating cells with CdS deposited by sputtering, as sputtering is a much more readily scalable process than CBD. In an initial experiment targeting sputtered CdS thickness, a 14.8% efficient cell was produced with a CdS thickness similar to that of the CBD-deposited CdS used for the 15.3% EPIR cell. This result was obtained without any process optimization specific to sputtered CdS and hence is highly promising. The sputtered CdS grain size is believed to be strongly related to the oxygen level in the CdS [7]. Oxygen also influences CdS-CdTe inter-diffusion, which can greatly influence device performance [15]. This means that the process optimization performed for CBD CdS could be largely irrelevant for sputtered CdS. These preliminary results in device performance indicate that using sputter-deposited CdS as an alternative to CBD CdS is a viable option and with further process optimization could yield cells with higher efficiencies.

Conclusions

EPIR has produced high efficiency polycrystalline CdS/CdTe solar cells on commercial TCO-coated soda lime glass through the implementation of a buffer layer between the TCO and the CdS and the optimization of the CdS material quality and thickness. Not only did the buffer lead to improved device performance, but it also greatly improved yield, reproducibility, and consistency. These results show progress in some of the typical problems that lead to the

difference between module and lab scale cell efficiencies. Finally, preliminary results for sputtered CdS indicate that it may well be a possible dry-deposition alternative to CBD.

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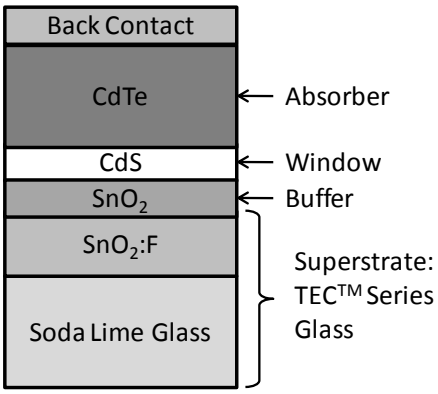

Figure 1 Polycrystalline CdTe solar cell device structure

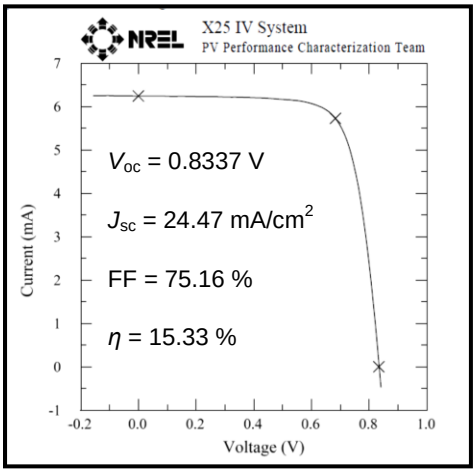

Figure 2 I-V curve and derived parameters of an NREL-verified EPIR-produced high efficiency polycrystalline CdTe solar cell.

Table 1 NREL verified I-V Characteristic parameters and certification dates

Month of Certification	η	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF
Jul-2010	12.02 %	802	21.97	68.19 %
Dec-2010	15.21 %	815	24.03	77.64 %
Apr-2011	15.08 %	829	23.87	76.16 %
Apr-2011	15.33 %	834	24.47	75.16 %

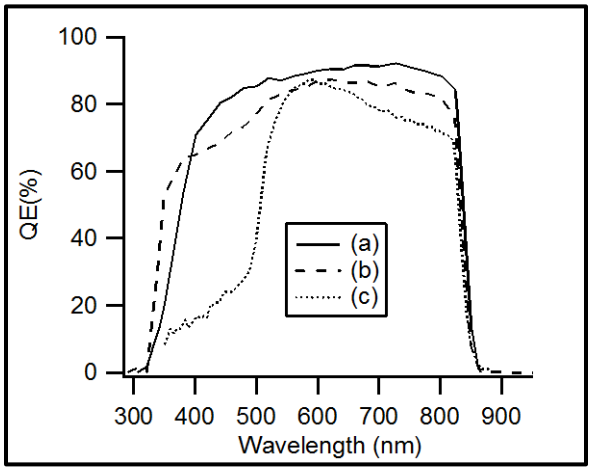

Figure 3 QE comparing (a) NREL's best lab cell[1], (b) a 15% cell produced at EPIR measured by NREL, and (c) a sample production cell (not produced by EPIR)[1].

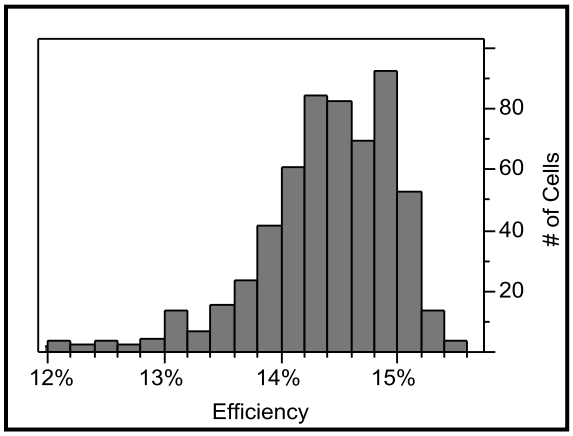

Figure 4 Distribution histogram of devices with a buffer layer produced at EPIR between December 2010 and June 2011.

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