2D-Materials: Synthesis and Investigation of Electrical and Thermal Properties

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THESIS

Submitted as partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Mechanical Engineering
to the Graduate College of the
University of Illinois at Chicago, 2018

Chicago, Illinois

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To parents

and to my friends.

ACKNOWLEDGMENTS

This thesis paper could not be written without the help and support of Prof. Amin Salehi-Khojin, who served as my supervisor, gave me support and assistance, and provided me with motivation and encouragement throughout the entire period of my research thus far at the Nanomaterials and Energy Systems Laboratory. My deepest gratitude goes also to my family and friends for their moral support. I also wish to particularly thank Mohammad Asadi, Poya Yasaei, Zahra Hemmat and all my collaborators who helped me to complete this thesis.

CONTRIBUTION OF AUTHORS

Main parts of the results and discussions in this thesis are taken from my published or submitted papers with written permission from the journals (see Appendix). Below, the contributions of all the co-authors are listed:

Authors' contributions in chapter 2 (taken from reference [1]**):** A.Salehi-Khojin and A.Behranginia conceived the idea. A.Salehi-Khojin led the material synthesis, device fabrications, electrical measurements and device characterizations. A.Behranginia synthesized the MoS_2-graphene lateral heterostructure and performed electrical experiments. A.Behranginia and P.Yasaei carried out device fabrications and characterizations. P.Yasaei and T.Foroozan synthesized the CVD graphene. A.K.Majee performed band structure alignment, mobility, and interfacial resistance calculations. V.K.Sangwan performed 1/f noise and breakdown measurements and analysis. C.J.Foss carried out DFT and transmission coefficient calculations. Z.Aksamija conceived and supervised the calculations. M.C.Hersam supervised the 1/f noise and breakdown measurements and analysis. F.Long performed KPFM measurements and R.Shahbazian-Yassar supervised him. S.Fuladi helped in DFT calculations. M.R.Hantehzadeh helped in CVD MoS_2 and graphene synthesis.

Authors' contributions in chapter 3 (Accepted in ACS Applied Materials & Interfaces): A.S.K. and A.B. conceived the idea. A.S.K. led the fabrication and experiments. Z.A. developed the BTE model and led the first principles calculations. A.B. developed the fabrication process, experimental setup, and thermal analyses. A.B. and Z.H. fabricated all the devices. A.B., P.Y. and Z.H. performed Raman thermometry measurements and thermal analysis. C.J.F. performed the numerical calculations and A.K.M. derived phonon interaction rates. All authors contributed to the write up of the manuscript.

Authors' contributions in chapter 4 (taken from reference [2]**):** A.Salehi-Khojin and P.Yasaei conceived the idea. A.Salehi-Khojin led the synthesis, fabrication, characterization, and experiments. C.D.Foster led the FE modeling. P.Yasaei, A.Behranginia, and Z.Hemmat synthesized the graphene flakes. P.Yasaei fabricated all the devices and performed the experiments. A.El-Ghandour developed the FE model and carried out the parameter optimization and data extraction process (with P.Yasaei). All authors contributed to the write up of the manuscript.

SUMMARY

This dissertation presents a study of (1) the growth of in-plane MoS_2-graphene heterostructure together with its electrical characterizations, (2) the power dissipation of the WSe_2 FET as a representative of 2D-material FETs (Field effect transistors), and (3) thermal dissipation across monolayer CVD graphene, as a representative of 2D-materials, on different technologically-viable substrates.

First, the in-plane MoS_2-graphene heterostructure is grown by the CVD method for large-scale applications. Electrical characterizations and 1/f noise measurements of this heterostructure reveal an order of magnitude higher electron mobility and lower noise amplitude for this heterostructure compared to conventional metal-contact MoS_2 devices. The KPFM (Kelvin Probe Force Microscop) study is performed to map the surface potential distribution across the MoS_2-graphene interface and visualizes the reduction of the MoS_2-graphene interface resistance at positive gate voltages. The DFT (Density Functional Theory) calculations demonstrate that the role of this interface resistance is less than 1% of the overall device resistance at gate voltages above 60 V. Similar failure modes and electrostatic breakdown fields for MoS_2-graphene and MoS_2-metal devices are also observed by electrostatic breakdown measurements.

Second, the power dissipation of the WSe_2 FET, as a representative of the 2D-materials, is investigated by the Raman thermometry method. The low-frequency $E_{2g}{}^2$ peak of WSe_2 material is used to measure the temperature rise of the device versus different the applied electrical powers. The interface resistance measurement between WSe_2 and SiO_2/Si substrate reveals that their interface TBC (Thermal Boundary Conductance) is in the low range of the solid-solid interfaces, proving the importance of the interface resistances for thermal dissipation of 2D-FETs.

Finally,to shed light on the role of the interface resistance of 2D-materials with different substrates, thermal dissipation of CVD graphene on different technologically-viable

substrates is investigated. The interface resistances between graphene and different tested substrates reveal that the overall thermal dissipation performance on AlN is better than on diamond substrate, although the thermal conductance of the AlN is significantly lower than that diamond material. These results confirm that the thermal conductance of the substrate is not the only key factor which is important for thermal dissipation of the 2D-material devices and that the role of the boundary resistance between 2D-material and substrate is very crucial.

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ΔT	temperature rise
2D	two-dimensional
3ω	3-Omega
AFM	atomic force microscopy
Al_2O_3	aluminum oxide
ALD	atomic layer deposition
AlN	aluminum nitride
AP-CVD	atmospheric pressure chemical vapor deposition
Ar	argon
Au	gold
BeO	beryllium oxide
BP	black phosphorus
BTE	Boltzmann transport equation
CI	charged-impurity
CLS	classical least square
Cu	copper
CVD	chemical vapor deposition
DFT	density functional theory
EBL	electron beam lithography
FDTR	frequency domain thermoreflectance
FE	finite element
FET	field-effect transistor
FFT	fast Fourier transform
G/A	thermal conductance per unit area
GB	grain boundary
GNR	graphene nano-ribbon
h-BN	hexagonal boron nitride
HOPG	highly ordered pyrolytic graphite
HRTEM	high-resolution transmission electron microscopy
I_{2D}	intensity of the 2D Raman peak in graphene
I_d	drain current
I_G	intensity of the G Raman peak in graphene

IPA	isopropyl alcohol
IR	infra-red
K	bulk thermal conductivity
K/mW	Kelvin per milliwatt
KPFM	Kelvin probe force microscopy
MD	molecular dynamics
MoO_3	molybdenum trioxide
MoS_2	molybdenum disulfide
NEMD	non-equilibrium molecular dynamics
rms	root mean square
R_{square}	linear regression
R_{TH}	thermal resistance
RWM	Rayleigh wave mode
SAED	selected area electron diffraction
SEM	scanning electron microscopy
Si	silicon
SiN	silicon nitride
SiO_2	silicon dioxide
SJEM	scanning Joule expansion microscopy
SO	surface optical
SThM	scanning thermal microscopy
STM	scanning tunneling microscopy
TBC	thermal boundary conductance
TBR	thermal boundary resistance
TDTR	time domain thermoreflectance
TEM	transmission electron microscopy
Ti	titanium
TMD	transition metal dichalcogenides
V_{ds}	drain-source voltage
V_g	gate voltage
ZA	flexural (out-of-plane) acoustic
Φ_B	Schottky barrier height

CHAPTER 1

INTRODUCTION

1.1. The Importance of Two-Dimensional Materials and their Heterostructures

Since conventional bulk materials have reached their geometrical limitation, miniaturization of the electronic devices has faced a formidable challenge. There are substantial efforts over the last decades to explore new materials as a subsequent of bulk materials for future electronic/optoelectronic devices. Using Two-dimensional (2D) materials, which are one atom thick, as channel and electrodes of the future electronic devices provide the chance of controlling the thickness of these devices at the atomic scale. These materials have shown astonishing electronic, optical and mechanical properties which make them proper candidates for future applications. For instance, it is possible to simply tune their electronic properties by changing the number of their layers[3], [4]. Or their outstanding mechanical bendability makes them applicable for flexible electronic applications[5], [6].Their ultrahigh optical transparency makes them auspicious for transparent electronic systems[7], [8]. Also, one of the important effects of utilizing these novel materials in ultrathin electronic devices is reducing the issue of the short-channel effect[9].

Rediscovery of the 2D-materials has ignited by the Exfoliation of the graphene, a zero bandgap semiconductor, from bulk graphite at 2004 by the Manchester group[9]–[11]. This material has shown a semi-metallic behavior with high carrier mobility at room temperature, admirable thermal and mechanical properties. However, the absence

of the bandgap in graphene makes it inapplicable for transistor applications. Hence, semiconducting materials like transition metal dichalcogenides (TMDs) are needed to be able to make field effect transistors (FETs), with high current on/off ratio, from 2D-materials. These materials have a hexagonal crystal structure consisting of transition metal atoms and chalcogen atoms which have a strong covalent intralayer and weak van der Waals interlayer bonding[12]. Based on the dimension of the metal atom and chalcogen atom, the bonding length between these atoms is from 3.15 A° to 4.03 A° and the TMDs single layer thickness is around 6 to 7 A°[13], [14]. One of their astonishing advantages is the ability of tuning their bandgap by changing the number of their layers, making different compositions between transition metal atoms and chalcogen atoms as well as applying mechanical strain to them[9], [15], [16]. To build all 2D circuitries, it is also needed to have insulating materials like hexagonal boron nitride (h-BN) which can be used as a gate dielectric for nanoelectronics devices. Therefore, 2D-materials will cover a wide range of material types from insulators with large bandgaps to metals[15]–[20] which are very promising for future industry.

As it is mentioned in previous paragraphs, 2D-materials have wide variety of properties and they behave notably different from each other. Each of these materials has some disadvantages which could limit the performance of its device. For example, Molybdenum disulfide (MoS_2) which is a famous member of the TMDs, has shown high on/off ratio making it a promising candidate to be used as a channel of the transistor in future devices. However, it has also shown that there is a Schottky barrier formation at its

interface with metal electrodes downgrading its performance significantly[21]. Or some of the 2D-materials like WTe_2 are instable at ambient conditions[22] and they need to be combined with other 2D-materials to be applicable for the industry applications. Thus, making the heterostructures of 2D-materials will open a plenty of opportunities to combine the advantage of each 2D-material together and eliminate its disadvantages. These heterostructures can be made by stacking or growing the 2D-materials on top of each other or next to each other. For instances, stacking a layer of graphene on top of h-BN substrate results in almost an order of magnitude higher mobility, less doping and enhanced chemical stability due to almost absence of the charge trappings at the surface of the h-BN and its atomically flat surface[23], [24]. Also in another work, Behranginia et al. have grown three dimensional(3D) MoS_2 on top of the graphene films and demonstrated that the charge transferred to 3D structured MoS_2 grown on top of the graphene film has improved significantly compared to 3D structured MoS_2 grown on top of the bare glassy carbon substrate[25].In addition, there has been a huge demand in recent years for flexible electronic devices and manufacturing all-2D circuitries can make it possible to achieve this dream. For example, Lee et al.[26] fabricated a flexible and transparent FET by stacking 2D-materials on top of 127 μm thick polyethylene naphthalate (PEN) substrate. In this work, MoS_2, h-BN and graphene materials have been used as a channel of the transistor, gate dielectric and gate electrode respectively. This vertical heterostructure has been made by mechanical stacking method and its performance has not changed up to 1.5 % induced strain. They could achieve a high

mobility of 29 $cm^2/V.S$ and operating gate voltage of 5V before bending the device. In another work, Das et al. [27] have made all-2D WSe_2 transistor on top of the flexible polyethylene terephthalate (PET) substrate with the mobility of 45 $cm^2/V.S$ and current on/off ratio of 10^7. In this work, WSe_2 and h-BN have been used as a transistor channel and gate dielectric respectively. Also, graphene material has been used as both gate electrode and source-drain electrode. The device performance did not change up to 2% applied strain and it was remarkably stable over wide range of temperature from 77 K to 400 K.

1.2.Preparation of 2D-materials and their heterostructures

There are different methods to make 2D-materials. Mechanical exfoliation method is the first method which has been used for fundamental studies about physical and chemical properties of these materials. In this method 2D-materials exfoliates from their bulk crystals by using scotch tapes[10]. The yields of this method to achieve large single layer flakes are low, but the flakes exfoliated by this method are pristine and almost free of defects. So, due to inapplicability of this method for mass production, other methods like chemical exfoliation and chemical vapor deposition (CVD) techniques have been used to produce single and few-layer of 2D-Materials for large-scale production. To chemically exfoliate 2D-materials, scientists have used different approaches like electrochemical exfoliation[28], [29] and liquid exfoliation techniques[30], [31]. These various approaches can produce 2D nanosheets with different qualities from almost defect free nanosheets to completely degraded nanoflakes[32]. These methods of 2D-

material production could be very cost-effective and simple. For example, Varrla et al.[33] have used Kitchen blender and household detergent to produce high quality graphene flakes. Also, preparing 2D-materials via chemical exfoliation technique brings the opportunity of making 2D-material inks for low-cost printed electronic circuits[34]. However, controlling the uniformity, lateral size and thickness of the flakes produced by these approaches are very challenging[23]. Till now, different techniques have been used by scientists for in situ measurement of the thickness and size of the 2D-material-nanosheets dispersed in the solution to have a better control on the uniformity of the exfoliated flakes[32], [35], [36]. There are an extensive range of liquids which can be used for chemical exfoliation of 2D-matrials resulting in having 2D materials with wide range of lateral sizes from 100 nm to 100 μm and thicknesses from monolayer to few layers. The dispersed liquid could be quite stable and have variety range of concentrations[32].

CVD method is another technique for large-scale production of 2D-Materials. Generally, there are two different approaches for the growth of the 2D-matrials by CVD technique. In the first approach, a thin layer of the metal atom will be deposited on top of the substrate by the means of metal evaporation technique or sputtering one. Then, the chalcogen atom will react with the deposited layer at elevated temperatures. Zhan et al. and Kong et al. were the scientists who used this approach to synthesize atomically thin MoS_2 film and vertically aligned MoS_2 layers respectively[37], [38]. Reaching uniform layers with very thin thicknesses is one of the difficult challenges of this approach[14].

The second approach is the reaction of the metal atom with the chalcogen atom at the vapor phase at elevated temperatures. Basically, in this method, people use a noble gas as a carrier gas inside the CVD chamber and a metal oxide source and a chalcogen precursor is used as the sources of the metal and chalcogen atom for the reaction respectively. Some scientists also used hydrogen gas as an reducing agent for the growth of the TMDs too [39], [40]. The temperature of the growth is from 500 $^{\circ}$C to ~ 1000 $^{\circ}$C depends on the melting temperature of the metal oxide precursor and the quality of the crystallinity of the grown material which is needed for that specific application. The growth could be done in both atmospheric pressure and low pressure. It was at 2012 and 2013 that different groups have started to grow CVD MoS_2 flakes by sulfurization of the MoO_3 precursor at high temperatures[38], [41], [42]. It is possible to grow single layer MoS_2 flakes on arbitrary substrates by using this approach and substrate treatment is one of the key factors in the growth of the TMDs by this method. For instance, performing an oxygen plasma treatment on the SiO_2 substrate, making it a hydrophilic substrate, before the growth will result in the growth of the MoS_2 flakes with larger flake sizes and better uniformity on top of the SiO_2 substrate[1]. There are many reports on the growth of the different TMDs by CVD approach[25], [40], [43]–[49] which shows that it is an auspicious approach for the large scale production of TMDs. For example, Eichfeld et al. [50] have reported the first scalable synthesis method of mono and few-layer WSe_2 material via metal-organic CVD method. In this work, they have used tungsten hexacarbonyl (W(CO)6) as a source of the tungsten material and dimethylselenium

((CH3)2Se) as a source of the selenium material and the growth happened at a wide range of temperatures from 600 ℃ to 900 ℃. A mixture of the hydrogen and nitrogen gas has been used as a carrier gas and the reaction happened in a vertical cold-wall reactor system. The WSe_2 material has been grown on top of the four different substrates including epitaxial graphene, CVD graphene, sapphire and amorphous boron nitride and the results of the growth were distinct for all these substrates from the point of the morphologies and thicknesses of the grown WSe_2 material. They could have achieved lateral size of 5-8 μm for WSe_2 flakes grown on top of the sapphire substrate. Or on the other work by Kang et al.[51], wafer scale multilayer films of MoS_2 and tungsten sulfide (WS_2) material have been grown directly on top of the SiO_2 substrate with the excellent uniformity over the entire film. They have used Molybdenum hexacarbonyl (MHC), tungsten hexacarbonyl (THC) and diethyl sulphide (DES) as a source of molybdenum, tungsten and sulfur respectively. These precursors purged into the reaction tube in a gas-phase condition. H_2 and Ar gases have also been used as carrier gases during the growth procedure and the growth time and temperature were 26 hr and 550 ℃ respectively. They could have achieved to the high mobility of 30 $cm^2/V.S$ for the grown MoS_2 film with 99% device yield.

1.3. Potential application of 2D-materials and their heterostructures

The unique properties of 2D-materials and their heterostructures such as transparency, mechanical flexibility, high surface to volume ratio and high electrical and thermal conductivity make them good candidates for wide variety of applications. Field

effect transistors, light emitting diodes, transparent electronics devices, sensors, and energy conversion/storage systems are the devices [23], [34], [52], [53] which can be revolutionized by 2D-materials and their heterostructures. Some of these applications for 2D-materials are briefly discussed in the following subsections.

1.3.1. Field effect transistors

Graphene was one of the first 2D-material which was used for transistor application due to its high carrier mobility. However, future FETs needs the on/off ratio of larger than 10^4[9] and the absence of the band gap in graphene results in having very low on/off current ratio and large off current. Scientists have tried to improve this disadvantage by using bilayer graphene[54], [55], graphene nanoribbons[56] and nanostructures[57], but it results in lowering the mobility of graphene[58]. Therefore, scientists tried to use other 2D-materials like TMDCs which mostly have a band gap between 1-2 eV. These materials have low off currents resulting in lowering the power consumption when the system is in the standby mode[9]. MoS_2 was one of the 2D-materials which has been used as the channel of the transistor and shows high on/off ratio[42]. However, due to the Schottky barrier formation at the metal electrode junction, it shows lower extrinsic mobility value than the theoretically estimated one[9]. Das et al. [59] have shown the formation of the Schottky barrier at the interface of the MoS_2 with four different low work function metals. In this study, scandium has shown the lowest Schottky barrier height (30 meV) and platinum has shown the highest Schottky barrier height (230 meV) at its interface with MoS_2. They claim that fermi level pining has a strong impact on the

interface of the metal and MoS_2. Hence to reduce the Schottky barrier height at the interface of the 2D-materials with metals, have high on/off ratio and high mobility, scientist have tried to develop in-plane and vertical heterostructures of 2D-materials. One of the ideas was to open a band gap in graphene by making a vertical heterostructure of GR/hBN/GR or Gr/MoS_2/GR which was developed by Britnell et al.[60]. The on/off ratio of this tunneling transistor at room temperature was almost an order of magnitude larger than previous graphene FETs[61]–[65], but still it was not enough for future applications. Then, Georgiou et.al.[66] came up with the idea of using WSe_2 as a barrier instead of hBN material for vertical graphene heterostructure. This heterostructure could switche between tunneling and thermionic transport behavior and shows high on/off ratio ($\sim 10^6$)[58]. Roy et al. [58] reported all-2D FET in which the graphene is utilized as source/drain as well as top gate electrodes, hBN as the gate dielectric and MoS_2 as a channel of the transistor. This heterostructure shows the on/off ratio of $>10^6$ and the mobility of 33 $cm^2V^{-1}S^{-1}$. Also, Behranginia et al. [1] have reported in-plane heterostructure of GR/MoS_2 for future transistor applications. This heterostructure shows higher mobility and lower noise metric compared to metal/MoS_2 transistors.

1.3.2. Optoelectronic Devices

Photoresponsivity and light absorption are the critical parameters for optoelectronic devices. Combination of the TMDC materials, which have direct band gap and high absorption coefficient, with graphene, which has high mobility, can provide fast response time and strong light absorption for the optoelectronic devices which are made out of the

Gr/TMDCs heterostructures[23], [58]. Zhang et al.[67] reported a photogain larger than 10^8 by stacking a layer of graphene on top of the layer of MoS_2. In this vertical heterostructure, in contradiction to the conventional metal/MoS_2 contact, the excited photoelectrons in the MoS_2 layer are injected to the graphene layer rather than trapping into the MoS_2 layer in the presence of the perpendicular electric field across the heterostructure[67]. Also, sandwiching a WS_2 material, as a light absorber, between two graphene layers, as a carrier separators, results in achieving the photoresponsivity of 0.1 AW^{-1} and quantum efficiency of above 30%[68]. The optoelectronic devices can also be made from p-n junctions. Lee et al.[69] reported the electronic and optoelectronic characteristic of the p-type WSe_2 and n-type MoS_2 vertical heterostructure. Their results exhibit diode-like current rectification behavior and photovoltaic response across WSe_2/MoS_2 junction. Their calculated diffusion time for the majority carriers to leave the junction was ~1μs resulting in almost high interlayer recombination losses. To improve this diffusion time, they have sandwiched the junction between two graphene electrodes to directly collect the charge carriers in the vertical direction resulting in increasing the collection rate of the charge carriers generated by the light absorption.

1.3.3. Sensor Devices

2D-materials have been used for different sensor applications such as humidity sensors[70], biosensors[71], [72] and etc. due to their high sensitivity and large surface to volume ratio[23]. Yasaei et al. have reported ultrahigh sensitivity of the black phosphorus(BP) film to the humidity. They have coated the BP nanoflakes in the form of

stacked films on top of the hydrophilic polytetrafluoroethylene (PTFE) filter papers and their results shows almost 4 orders of magnitude change in the drain current by changing the relative humidity from 10% to 85%. They have explored that the modulation in the leakage ionic current is the operation principle of their sensors. MoS_2 is the other 2D-material which has been used for DNA detection, but due to its sensitivity to moisture and oxygen its application is restricted for aqueous solution. To overcome this challenge, Loan et al. [73] stacked a layer of graphene on top of the MoS_2 layer providing ultra-sensitive structure for detection of the DNA hybridization. Stacking graphene layer on top of the MoS_2 layer brought two benefits for this sensor. First, biocompatibility of the graphene with DNA makes graphene a suitable host for the DNA[73]. Second, the presence of the graphene on top of the MoS_2 layers results in protecting the MoS_2 layer from the moisture[23].

1.4. Thermal transport of 2D-materials

Due to the small size of the 2D-material electronic devices, these devices can suffer from sophisticated thermal challenges which could significantly limit their practical applications[74], [75]. The temperature distribution in these devices can be significantly non-uniform across the channel of the transistor resulting in creating hot spots with temperatures noticeably higher than the average temperature of the channel[75], [76]. Without having a considerable progress in electronic circuit cooling technology, the power density of the new electronic devices could reach the level resulting in unreliable operation of these devices. This phenomena makes the thermal management of the

individual nanoscale-transistors a formidable challenge for future device designers[76]. Higher operation temperature of thin-film transistors with the channel thicknesses lower than phonon mean free path could also reduce the efficiency of these devices significantly. This phenomena is due to the phonon confinement and boundary scattering which results in increasing the thermal resistance of these devices[76]. Electron-phonon scattering is the main scattering mechanism which results in the heating of this devices. In more detail, absorbing the energy of the electron by lattice results in increasing the temperature of these devices and affecting the electron mobility of them[76].Hence, complete understanding of the thermal properties of 2D-materials and their interfaces is needed to be able to design and fabricate 2D-material deices with higher efficiency and better performances. Various thermal measurement techniques such as 3ω[77], time-domain thermoreflectance (TDTR)[52], suspended micro-bridge[78] and optothermal Raman[79] methods have been developed during passed decades to investigate thermophysical properties of 2D-material devices. The first two methods are appropriate for cross-plane thermal transport measurement and the last two ones are developed for intrinsic in-plane thermal transport measurement[74].

Basically, in 3ω method the material will be suspended with four electrical contacts. The Ac current with 1ω angular frequency will apply between the two farthest electrodes and the voltage drop will be measured between the two closest ones. Applying 1ω sinusoidal current will results in temperature variation at 2ω frequency and voltage drop with a 3ω component. Finally, thermal conductivity and thermal time constant can be

calculated based on the measured voltage drop. The specific heat and diffusivity of the material can also be measured by this method[80].

TDTR technique is based on measuring the thermoreflected signals from the material as a result of the localized temperature increase. Generally, in this technique, the material will be heated by the pulse laser which results in increasing the temperature of the material locally and inducing the thermal stress to the sample. The acoustic strain pulses will be generated because of this thermal stress. Finally, the thermoreflected signals will be measured by photodiode and will be amplified by a RF lock-in amplifier. Then, the thermal conductivity of the material will be extracted from the ratio of the in phase and out of phase of the lock in amplifier signal[80]–[82].

The micro-bridge method has been used by many scientists to measure thermal conductivity and seebeck coefficient of the different materials including 2D-materials[83]–[89]. Basically, in this method, heater and sensor electrodes are fabricated on top of the silicon nitride membrane and the desire material is suspended between the heater and sensor. So, the huge part of the generated heat at the heater is conducted to the sensor electrodes through the suspended material by joule heating mechanism. And finally, the heat will be dissipated through the silicon nitride beams to the heat sinks. By knowing the amount of the generated heat at the heater and measuring the temperature of the two ends of the sample (T_{hot} and T_{cold}), it is possible to measure the thermal conductivity of the desired material. To perform this measurement, the sample will be loaded inside the vacuum chamber to be able to ignore the heat transfer through the

convention and radiation. Transferring the desired material to this platform and sophisticated fabrication process are the challenges which limit the implication of this method for thermal measurements. There are two methods to transfer the low dimensional materials to this platform. The first is using the sharp tip to pick up the material and transfer it to the platform which has been found very challenging for the materials with the thicknesses less than the 50 nm[74], [87]. Another method is to use the polymer-assisted transfer process which could leave the residue on the sample resulting in changing its thermal properties[90] and damaging the device. Also, having a correct evaluation of the interface thermal resistance between 2D-materials and silicon nitride membrane is another challenge of this method to extract the correct value of the thermal conductivity of the 2D-material[74]. Shi et al.[78] were the first group who used this technique to measure the thermal conductivity of the carbon nanotube (CNT) material. They deposited platinum electrodes as a heater and sensor on top of the silicon nitride membrane. They have used two different methods to transfer their material on top of the platform. In the first one, they spun the solution containing the CNT material on the substrate with many suspended structures and then anneal the device at 300 °C to improve the contact between the platinum electrode and the deposited material. In the second one, they spun coat the solution containing the precursors for the CVD growth of the CNT material and then placed the substrate into the CVD furnace. They used the methane gas as the source of the carbon material and the temperature of the growth was 900 °C. Their measurements reveal that the thermal conductivity of the single-wall CNT

is lower than individual multi-wall CNT which could be due to the scatterings at the defects. Lee et al. [91] also used the same method to measure the thermal conductivity of the few layer black phosphorus. They have shown that there is a large anisotropy in the thermal conductivity of the black phosphorus nanoribbons and their thermal conductivity reduces by decreasing the thickness of the nanoribbons. Temperature and thickness dependent thermoelectric properties of bismuth telluride (Bi_2Te_3) is also investigated by Pettes et al. [86] by using the micro-bridge platform. Their results exhibit that the seebeck coefficient of Bi_2Te_3 will significantly reduce by decreasing the thickness of this material.

Optothermal Raman technique is another approach with simple sample fabrication and measurement process for investigation of the thermal properties of 2D-materials.This method has been used by many groups during the past decades[4], [34], [79]. By using this method, it is possible to measure the thermal conductivity of 2D-materials and the temperature of their devices under the operation at different applied powers. Basically, in this method, the fabricated sample will be placed on the stage which has the temperature control and can heat/cool the device in a wide range of temperatures. Then, the temperature coefficient of the Raman peaks of the material will be extracted by acquiring Raman spectra of the sample at various temperatures. To find out the thermal conductivity of the sample, the laser light with a desirable wavelength will be focused on the middle of the 2D-material, which is suspended over a trench, to heat the device. Next, the generated heat will be dissipated through the 2D-material to the heat sinks. Finally,

the thermal conductivity of the sample can be calculated by knowing the laser power, thickness of the sample and temperature gradient of the sample. Inaccuracy in measuring the absorbed laser power and the Raman peak shift are the challenges of this measurement method. Also, this method is not applicable for the 2D-materials which have Raman peaks with weak intensity and temperature independency[74]. This method was used by Balandin et al.[79] to measure the thermal conductivity of the suspended graphene for the first time. They extracted the temperature coefficient of the G Raman peak of the graphene and heated the graphene by using the 488 nm wavelength laser. Faugeras et al.[92] were another group which measured the thermal conductivity of the graphene by Raman thermometry technique. They have reported the thermal conductivity of the 630 $Wm^{-1}K^{-1}$ for graphene which was lower than 5300 $Wm^{-1}K^{-1}$ value reported by Balandin et al[79]. The reason that Faugeras reported lower value than Balandin was that they considered lower value for the absorption of the laser power by graphene based on the latest results on the transmission and reflectivity of the graphene. It is also worth mentioning that, Faugeras used the ratio of the stokes to anti-stokes Raman signal instead of considering the Raman peak shift at different temperatures. There were also other reports on the thermal conductivity of the graphene ranging from 600 $Wm^{-1}K^{-1}$ to 2500 $Wm^{-1}K^{-1}$ [93]–[95]. Pop et al.[96] also use Raman thermometry technique to investigate the energy dissipation of MoS_2 transistors under the operation. They used both CVD MoS_2 and mechanically exfoliated MoS_2 as a channel of the transistor for this measurement. Their study revealed that the average temperature rises for both

Mechanically exfoliated and CVD grown MoS_2 is almost the same resulting in showing the same behavior in energy dissipation. Their temperature mapping measurements also shows that the nonuniformity in the MoS_2 layer would not cause significant self-heating in the small bilayer region. Their measurement also disclosed that the thermal boundary conductance between MoS_2 layer and its SiO_2 substrate is an order of magnitude larger than previously reported values[97]–[99]. On the other work, Engel et al. [100] used the anti-stokes-to stokes Raman peak intensity ratio to measure the temperature rise of the 50 nm black phosphorus transistor under the applied bias. Their measurement shows the breakdown temperature of the 757 K for this material.

CHAPTER 2

Direct Growth of High Mobility and Low Noise Lateral MoS2-Graphene Heterostructure Electronics

(Most parts of this chapter are taken from the published paper with the following citation:

Amirhossein Behranginia, Poya Yasaei, Arnab K. Majee, Vinod K. Sangwan, Fei Long, Cameron J. Foss, Tara Foroozan, Shadi Fuladi, Mohammad Reza Hantehzadeh, Reza Shahbazian-Yassar, Mark C. Hersam, Zlatan Aksamija, Amin Salehi-Khojin "Direct Growth of High Mobility and Low Noise Lateral MoS_2-Graphene Heterostructure Electronics" Small, 2017.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

2.1. Introduction

According to Moore's law, the transistor count per chip doubles every two years[101]. The continuing shrinkage in size is pushing the silicon-based industry toward its physical limitations. Numerous efforts are now being dedicated to the development of two-dimensional (2D) materials for future electronic/optoelectronic devices[20], [31], [39], [102]–[105]. Transition metal dichalcogenides (TMDs) are a family of layered crystals that are opening the possibility of developing systems with reduced dimensionality and a range of unique properties[105]. The most abundant member of this family is molybdenum disulfide (MoS2), which shows interesting semiconducting properties[106], [107] that make it a promising candidate for digital electronic circuitry applications. On the downside, the electrical performance of MoS2 field-effect transistors

(FETs) has been limited by the performance of the MoS2 junction with the metal contact electrodes[21]. In particular, due to Fermi level pinning, nearly all metals form a Schottky barrier upon contact with MoS2, which results in large contact resistances on the extrinsic (2-probe) performance of MoS2-based devices[21]. Additionally, metals do not possess sufficient mechanical bendability for use in flexible structures. Thus, significant research has been invested in finding a replacement for conventional metal electrodes that will allow the fabrication of intrinsically 2D devices with improved device metrics[108]–[113]. Du et al. [114] have been fabricated the first Gr/Metal hetero-contact MoS_2 FET to improve the electron coupling between the metal and MoS_2. In this work, mechanically exfoliated MoS_2 has been used as the channel of the transistor and monolayer graphene is transferred on top of the MoS_2 layer before deposition of the source and drain metal electrodes. They have measured the extrinsic field effect mobility of 32.3 $cm^2/V.S$ and on/off current ratio of 10^7 for this hetero-contact device. Their contact resistance has improved significantly (3.3 times) compared to conventional metal/MoS_2 FET. They claimed that this improvement is because of the gate-enhanced electron injection from graphene into the conduction band of the MoS_2.

In this section, I present the seed-free consecutive CVD processes to synthesize lateral MoS2-graphene interfaces with large crystal domain sizes and high interface quality. Device-level experiments reveal that the extrinsic mobility of MoS2-graphene FETs is improved by an order of magnitude compared with the MoS2-metal FETs because of energy band rearrangement and smaller Schottky barrier height at the

contacts, especially in the accumulation region (large positive gate voltages). For direct verification of the device-level measurements and to gain more insight into the role of the interface on the overall resistance of the device, Kelvin probe force microscopy (KPFM) is employed to map the surface potential distribution of a biased MoS2-graphene heterojunction under applied gate potentials. Low frequency 1/f noise metrics of the MoS2-graphene FETs are also extensively studied in both subthreshold and accumulation regions to identify the origins of signal fluctuations in lateral MoS2-graphene devices. The results show that the mobility fluctuations are the dominant origin of the noise in the accumulation region, while the overall noise amplitude is an order of magnitude lower than MoS2-metal FETs. Additionally, electrostatic breakdown measurements are performed on both MoS2-graphene and MoS2-metal devices to study the failure modes of the devices under high-power operation. To gain insight into the physics of the observed improvements, the interfacial resistance is modeled using a combination of first-principles band structure calculations, followed by calculation of the transmission coefficient and interfacial conductance in the Landauer formalism. Overall, this work establishes the superlative electronic properties of directly grown MoS2-graphene lateral heterostructures.

2.2. RESULTS and DISCUSSION

In our method, a graphene film with partial (or full) coverage is initially synthesized on a copper substrate in an atmospheric pressure chemical vapor deposition (AP-CVD) process and then transferred to a silicon (SiO_2/Si) substrate, similar to our previous

reports[115], [116]. Figure 1 shows our CVD setup for the growth of the graphene and MoS_2 material.

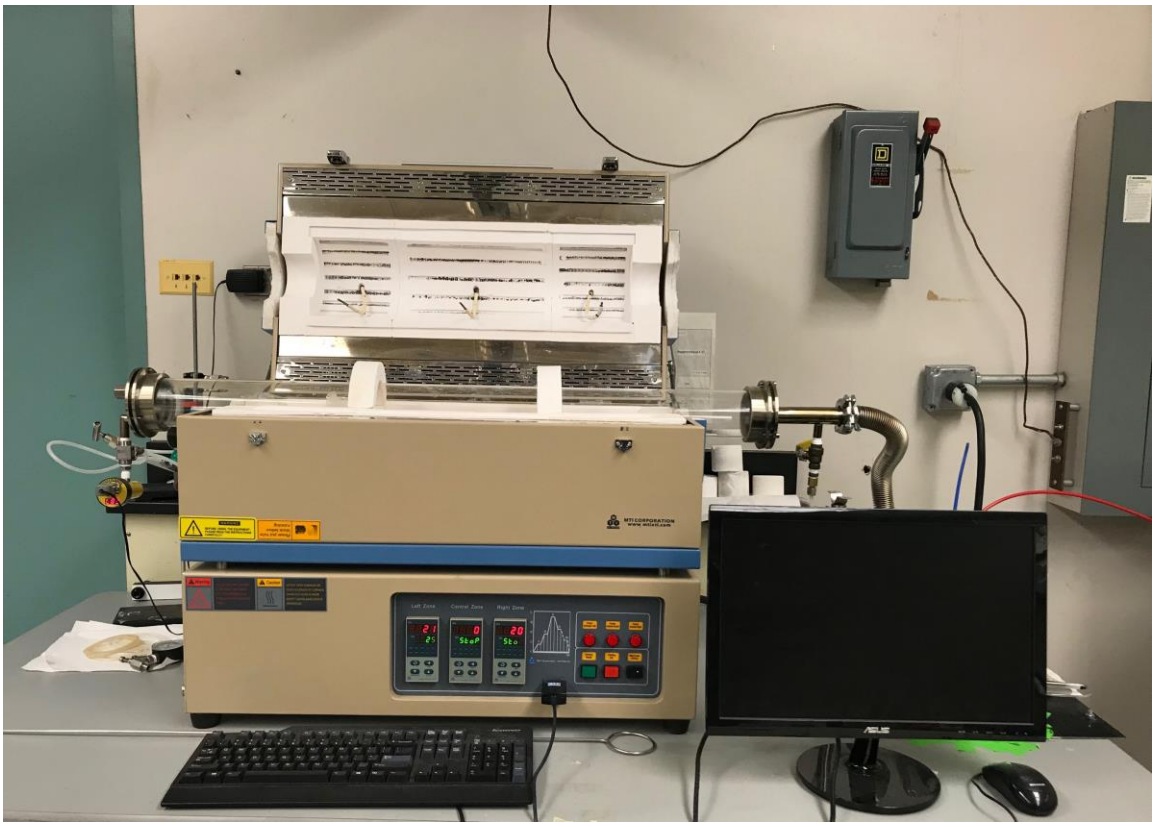

Figure 1. CVD Setup: three zones CVD furnace which is used for the growth of the graphene and MoS_2 materials.

The samples are then transferred to another AP-CVD chamber to synthesize MoS_2 through the reaction of sulfur and molybdenum trioxide (MoO_3) precursors. **Figure 2a-b** shows the CVD-grown MoS_2 triangular single crystalline flakes making a lateral junction with graphene domains. We note that even without any specific surface treatment (e.g., use of seed promoters), the growth of MoS_2 is more favorable on a bare oxide substrate compared to graphene films. This observation may be explained by the relative scarcity

of nucleation sites on graphene compared to SiO_2. The preferential deposition on SiO_2 causes the growth of MoS_2 to stop right at the edge of the graphene film, resulting in a lateral (in-plane) heterojunction. We note that due to the lattice mismatch between graphene and MoS_2, an atomically sharp interface is not likely to form, but due to the self-limiting growth process (deposition selectivity), the overlapped region remains quite small (2 to 30 nm) [117]. Next, to investigate the scalability of this method, we have increased the growth time of the graphene flakes to grow a continuous graphene film on top of the cupper substrate. Then, uniform grown graphene film was transferred to the SiO_2 substrate by PMMA assisted transfer method. The graphene film is patterned to small squares by using photolithography process and the unwanted areas are etched a way by using 5 minutes oxygen plasma. Finally, the patterned graphene films are loaded into the MoS_2 CVD furnace to grow uniform films of MoS_2 on the bare area of SiO_2 substrate. We found that a uniform MoS_2 film can fill arbitrary-shaped patterns in the graphene films and form lateral interfaces (Figure 2c). This process shows that it is possible to grow MoS_2-graphene in-plane heterostructures in large scales for future industry applications.

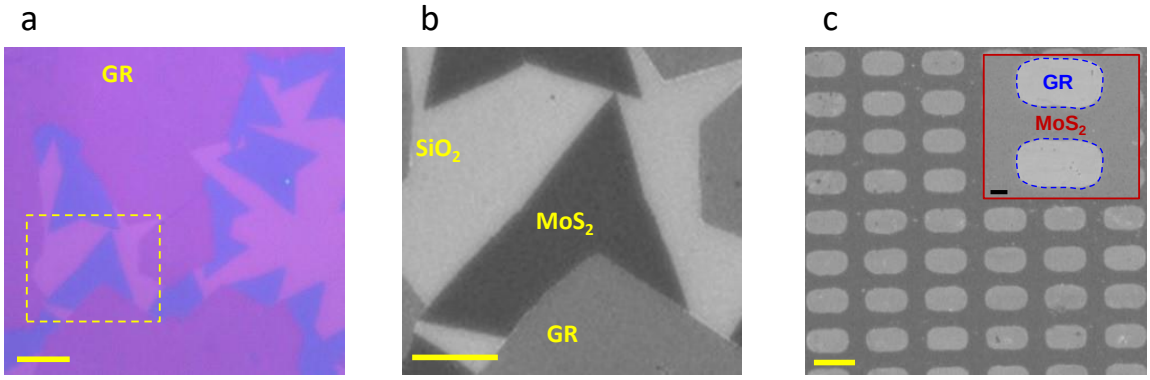

Figure 2. Optical and SEM characterization images of MoS_2-Graphene heterostructure: (a) Optical image of the partially covered MoS_2 triangular flakes next to the graphene flakes (scale bar 10 µm). **(b)** SEM image of the MoS_2-graphene in-plane heterostructure from the selected area in (a) (scale bar 5 µm). **(c)** SEM image of a large scale patterned MoS_2-graphene in-plane heterostructure (scale bar 10 µm) the inset magnifies the same image (Scale bar in inset 2 µm).

Atomic force microscopy (AFM) characterization (Figure 3) also shows an overlapped region between MoS_2 and graphene domains which is smaller than 30 nm over the entire interface length.

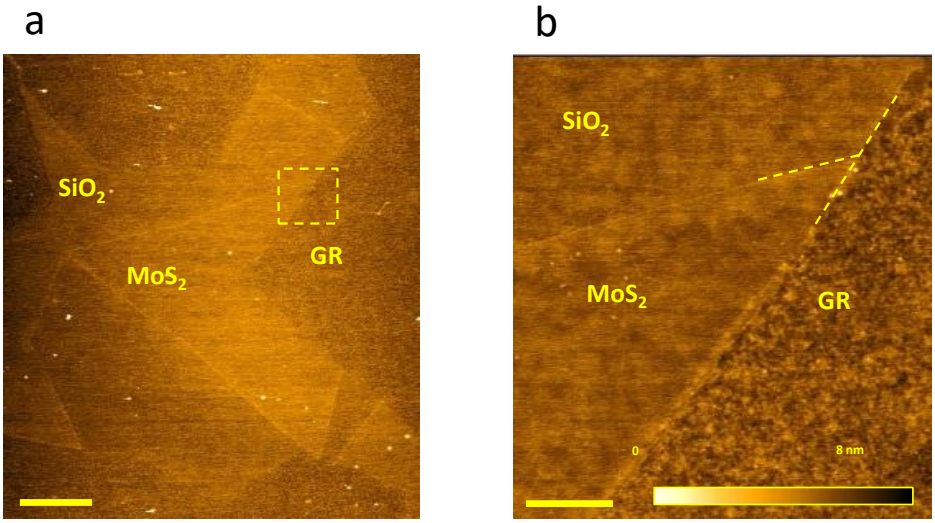

Figure 3. AFM Characterization of MoS_2-Graphene junction: (a) AFM image of the MoS2-graphene in-plane heterostructure. **(b)** Higher magnification AFM image of the MoS2-graphene interface.

Raman point spectroscopy on a patterned MoS_2-graphene interface shows the characteristic peaks of MoS_2 and graphene next to the silicon peaks from the substrate (Figure 4). E^2_g and A^1_g peaks are the in-plane and out-of-plane Raman representative peaks of MoS_2 respectively and the G peak and 2D peaks are the Raman representative peaks of graphene. The inset of Figure 4 shows the spatial distributions of the graphene and MoS_2 Raman peaks, which reveal the formation of a lateral interface without a noticeable gap or overlap. The classical least-square (CLS) fitting was used to analyze the obtained hyper-spectra, including the E^2_g and A^1_g peaks of the MoS_2 (coded as green in Figure 4) and the G peak of the graphene (coded as red).

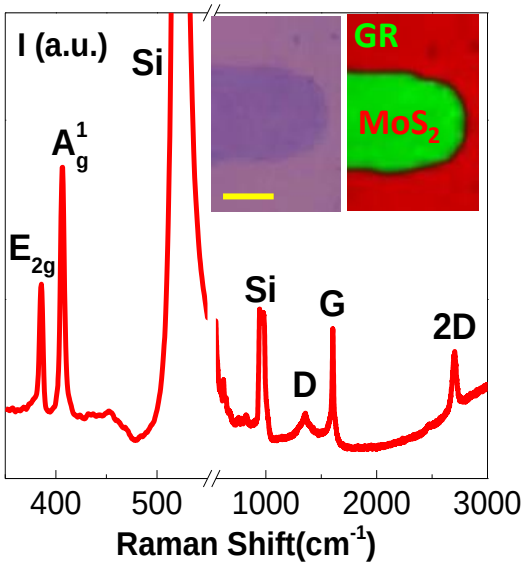

Figure 4. Raman Characterization of MoS_2-Graphene junction: A representative Raman point spectrum from the MoS_2-graphene interface area. The inset shows optical image and Raman mapping of a patterned MoS_2-graphene heterostructure. The scale bar is 2 μm.

To make MoS_2-Gr and MoS_2-metal field-effect transistors (FETs), We first transferred the MoS_2-Gr heterostructure and MoS_2-metal structure from the grown substrate to the new SiO_2/Si substrate. For this process, we coated a Poly (methyl methacrylate) (PMMA) layer on top of the substrate and let it dry in the air for four hours. Then, we floated the coated substrate on the diluted Potassium hydroxide (KOH) etchant till the PMMA layer detach from the old substrate. The detached layer floated on top of two bath of water for four hours and then transferred to new SiO_2/Si substrate. The reason of transferring the structures from the old substrate to the new one is the leakage of the gate oxide due to the reaction of the sulfur with SiO_2 layer during the growth process. Next, the transferred structures are etched to the desire shape by electron-beam

lithography (EBL) process followed by oxygen plasma etching. Finally, the metal electrodes deposited by metal evaporation process after patterning the electrodes by EBL process (Figure 5a-b).

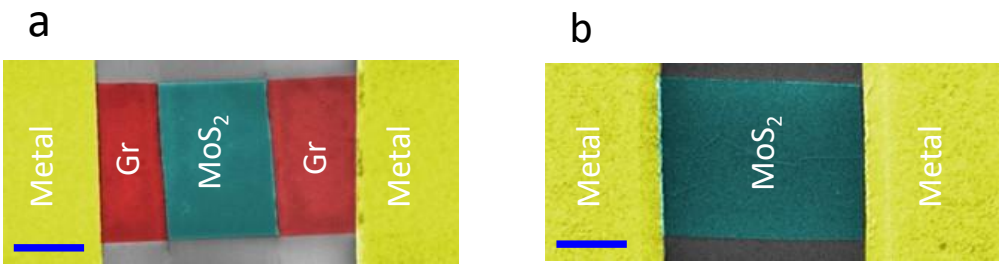

Figure 5. Colorful SEM image of the MoS_2-Gr and MoS_2-Metal FET structures: (a-b) SEM images of the MoS_2-graphene and MoS_2-metal FETs, respectively (scale bars 2 µm and 1 µm, respectively).

An optical cryogenic refrigerator (from Janis, model: CCS-450) was used to carry out our electrical measurements at different temperatures (Figure 6). The operation temperature range of the system is from 10 K to 500 K and a closed loop Helium compressor is used to bring down the temperature of the device to the lower temperatures. The temperature controlling unit (Lakeshore 335) is also used to precisely control the temperature of the system. To reduce the heat losses by convection heat transfer mechanism and eliminating the effect of the moisture on the performance of the device, a turbo pump is connected to the system to pump down the pressure of the unit to ultra-high vacuum pressures (~10^{-7} mbar). The electrical connections are established through a chip-carrier to the device and the chip-carrier is mounted on top of the cold finger. Prior to mounting the chip carrier on top of the cold finger, enough vacuum

compatible thermally conductive grease is applied to it to make sure about the proper heat conduction from the cold finger to the device. A keithley 2612A source meter is also used to apply bias between the source and drain of the device and measure the current across the MoS_2-Gr transistor channel.

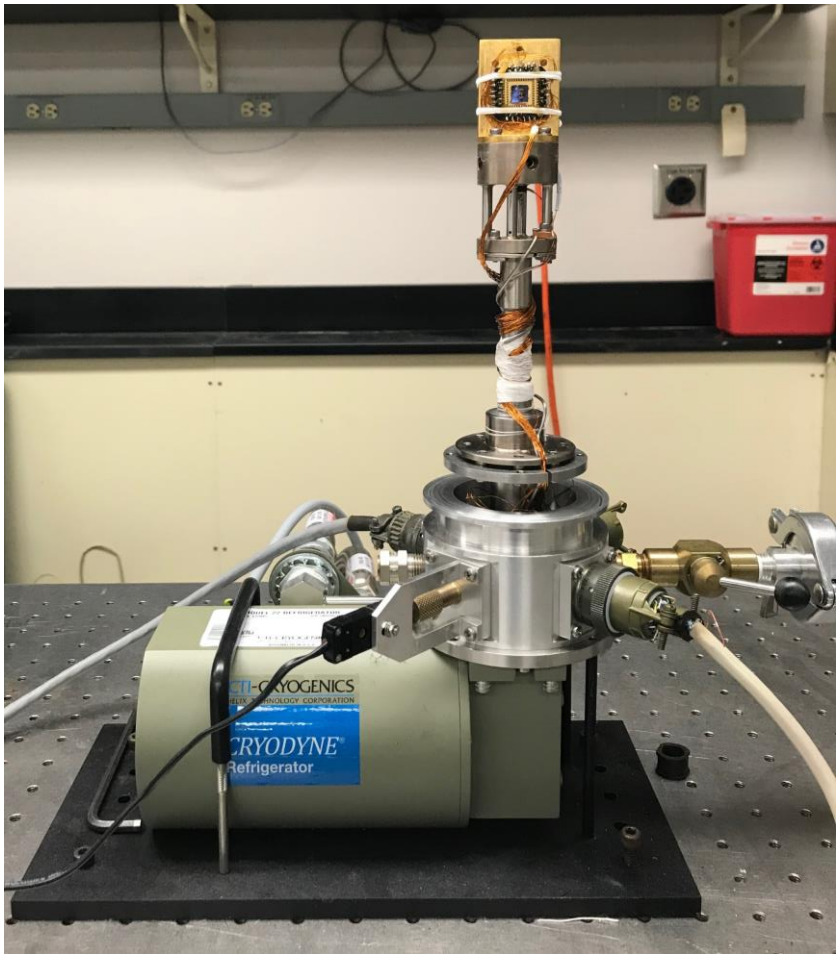

Figure 6. Optical image of the cryogenic system. Cryogenic system which is used for temperature study of the electrical performance of the MoS_2-Gr device.

Figure 7 shows the two-probe current-voltage (I_d-V_{ds}) measurements at the back gate bias (V_g) of 60 V for different temperatures.

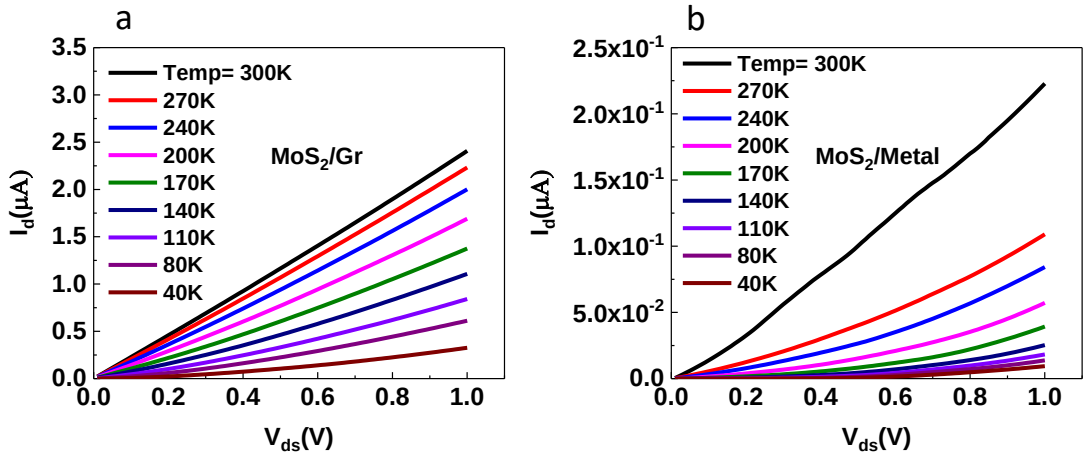

Figure 7. Two-probe current-voltage (Id-Vds) characterization at different temperatures: Output characteristic at different temperatures for **(a)** MoS_2-Gr **(b)** MoS_2-Metal FETs.

To compare the linearity of the I_d-V_{ds} trends in the MoS_2-graphene and MoS_2-metal FETs, the normalized I_d-V_{ds} trends (Y axis: $I_d/I_{d@Vsd=1V}$) at temperature 270 K are shown as an inset to Figure 8. Unlike the MoS_2-metal device, the MoS_2-graphene FET shows a linear behavior. The correlation coefficient of the linear regression (R_{square}) in the I_d-V_{ds} is also calculated for both devices at different temperatures (see Figure 8). The R_{square} of the MoS_2-graphene FET starts from 1 at room temperature and goes to 0.970 at 40 K. However, the R_{square} of the MoS_2-metal transistor shows greater temperature dependence (0.998 to 0.799). The larger non-linearity in the I_d-V_{ds} curve of the MoS_2-metal device compared to the MoS_2-graphene device – especially at low temperatures – suggests that a larger Schottky barrier is present for the metal-contacted MoS_2 device.

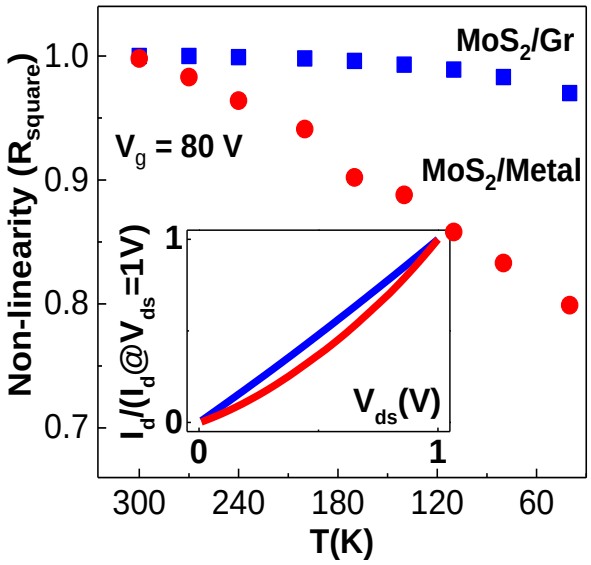

Figure 8. Linear Regression of I_d-V_{ds} : The linear regression (R_{square}) of the I_d-V_{sd} at different temperatures for the MoS_2-graphene and MoS_2-metal FETs (The inset shows normalized I_d-V_{sd} characteristics of the both devices – normalized with their respective I_d at V_{sd}=1V).

The output characteristics for both devices at different gate biases for different temperatures are also shown in Figure 9. For this measurement, the temperature of the cryogenic setup kept constant at a specific temperature and then I_d-V_{ds} measurements are performed for different applied gate voltages. The measurement is done at vacuum pressure of ~ 10^{-6} Torr. These measurements show that MoS_2-graphene FET almost keep its linearity at the three different measured temperatures (300K, 240K and 200K) under different applied gate biases. While, MoS_2-metal FET show significant non-linearity for temperatures lower than the room temperature at different applied gate biases.

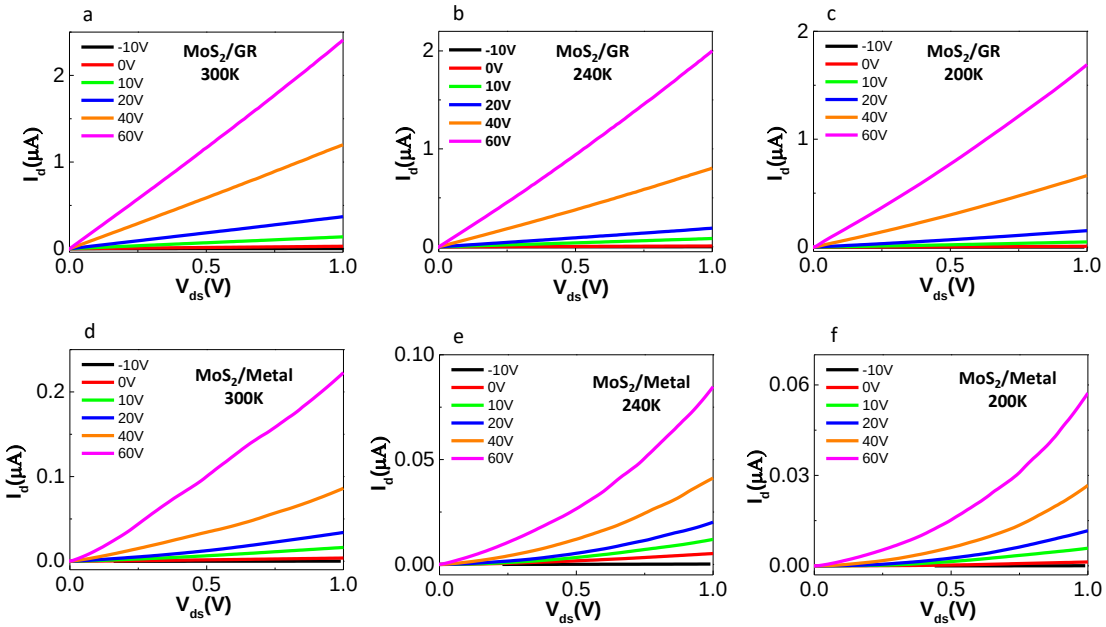

Figure 9. Two-probe I_d-V_{ds} characterization at different applied gate biases :(a-f) I_d-V_{ds} measurements under different applied gate voltages for MoS2/Gr and MoS2/Metal FETs at 300 K, 240 K, and 200 K respectively.

Moreover, the electrical transfer characteristics (I_d-V_g) were measured at different temperatures (Figure 10) and a typical n-type semiconducting behavior was obtained for both devices.

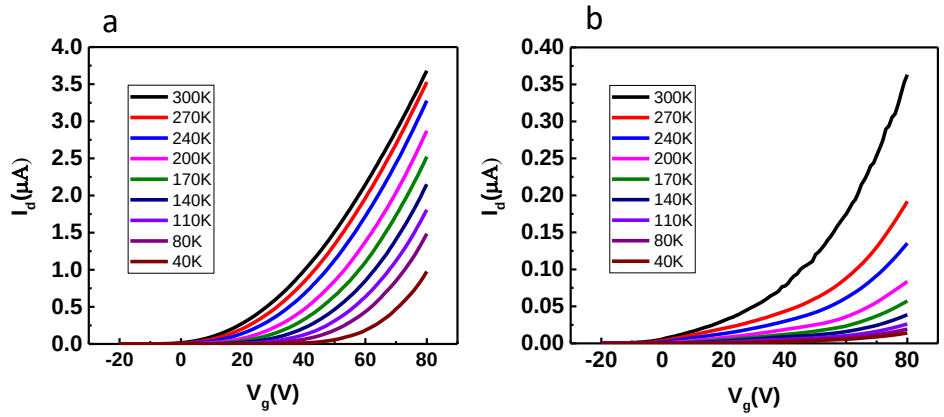

Figure 10. Two-Probe Electrical Transfer characteristic at different temperatures: I_d-V_g measurements at different temperatures for **(a)** MoS_2/Gr and **(b)** MoS_2/Metal FETs.

The I_d-V_g results at 270 K (Figure 11) indicate that the current density ($I_d \times \frac{L}{W}$) at V_g = 80 V for the MoS_2-graphene FET is 20 times higher than the MoS_2-metal FET. This ratio becomes even larger at low temperatures and approaches ~74 times at 40 K (Figure 11 inset), which is attributed to a smaller barrier for thermally induced charge carriers in the MoS_2-graphene in-plane heterostructure. These measurements also performed at cryogenic setup and the vacuum pressure of ~ 10^{-6} Torr. It is worth mentioning that performing the measurements in the ambient conditions results in lowering the current density of the FETs significantly which is due to the high sensitivity of the MoS_2 to the humidity.

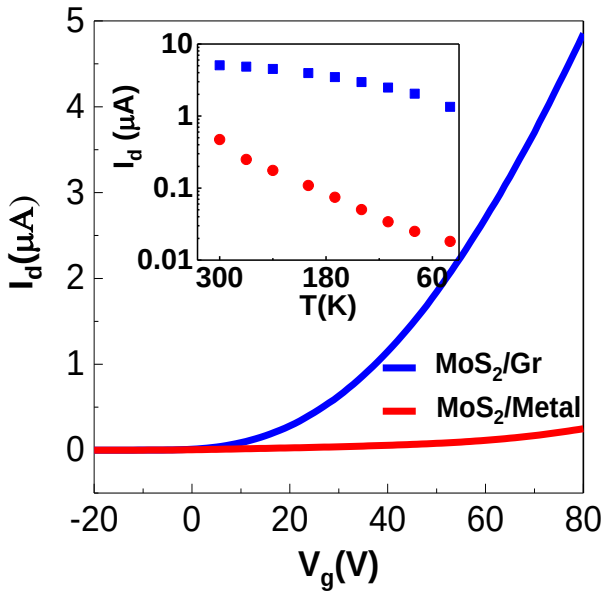

Figure 11. Two-Probe Electrical Transfer characteristic at Vg=80V: I_d-V_g characteristics of the MoS_2-graphene and MoS_2-metal FETs at 270 K (the inset shows the drain current at V_g=80V with respect to temperature).

The extrinsic field-effect mobility is also calculated for both structures at room temperature and different back gate voltages (Figure 12a). Both transistors are completely turned OFF at large negative gate biases and turned ON at a threshold voltage of 55 V and 40 V with an ON/OFF ratio of 10^4 and 10^5 for MoS_2-metal and MoS_2-graphene, respectively. The linear field-effect mobility is calculated as ~11.5 cm^2/V.S for MoS_2-graphene and ~1.5 cm^2/V.S for MoS_2-metal at V_g = 80 V. It should be noted that the field-effect mobility of the MoS_2-metal devices is consistent with the previously reported mobility of monolayer CVD MoS_2 without top-gate dielectrics.[109] However, higher extrinsic mobility values can be achieved by using multilayer MoS_2[118] or using

high-k dielectric substrates/overcoats.[119] Our temperature-dependent measurements show that the mobility of the MoS_2-metal FET is reduced by 95% as the temperature is decreased to 40 K, while the MoS_2-graphene FET shows almost constant mobility down to 160 K and then 30% reduction in the mobility at 40 K (Figure 12b). This temperature dependence is also demonstrated in the inset of Figure 4h in which the drain current of the MoS_2-graphene device reduces by ~4 times, while that of the MoS_2-metal device decreases by ~26 times.

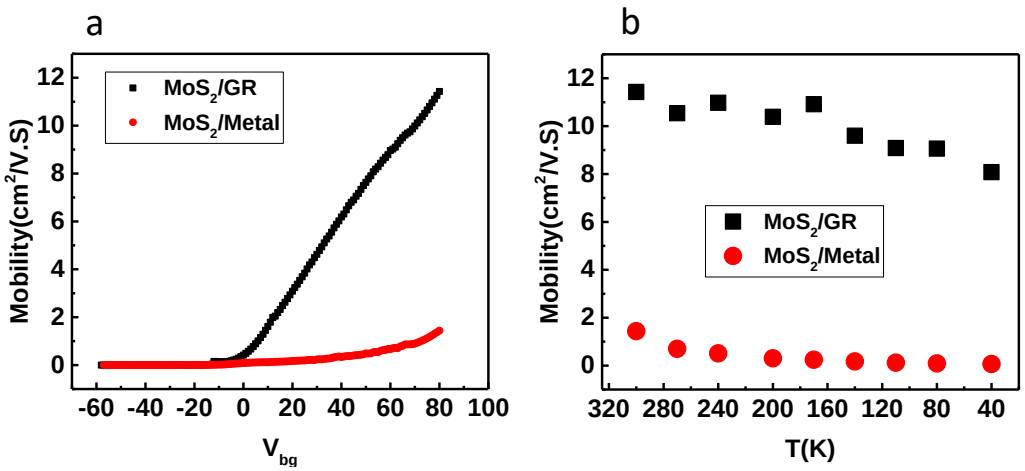

Figure 12. Mobility measurements: mobility vs. **(a)** gate voltage at T = 300 K, and **(b)** the temperature at $V_g = 80$ V.

To study the Schottky barrier height of the devices, a 2D thermionic equation $I_d=AT^{3/2}\exp\left(\frac{-q(\Phi_B-\frac{V_{ds}}{n})}{K_BT}\right)$ is used in which I_d is source-drain current, T is temperature, q is electron charge, K_B is Boltzmann constant, Φ_B is Schottky barrier height, V_{ds} is Source-drain current, n is Schottky diode non-ideality factor, and A is Richardson's

constant[120], [121]. Figure 13a and b shows the logarithmic plots of ($I_d/T^{3/2}$) versus (1000/T) for the MoS_2-graphene and MoS_2-metal interfaces at different V_{ds}.

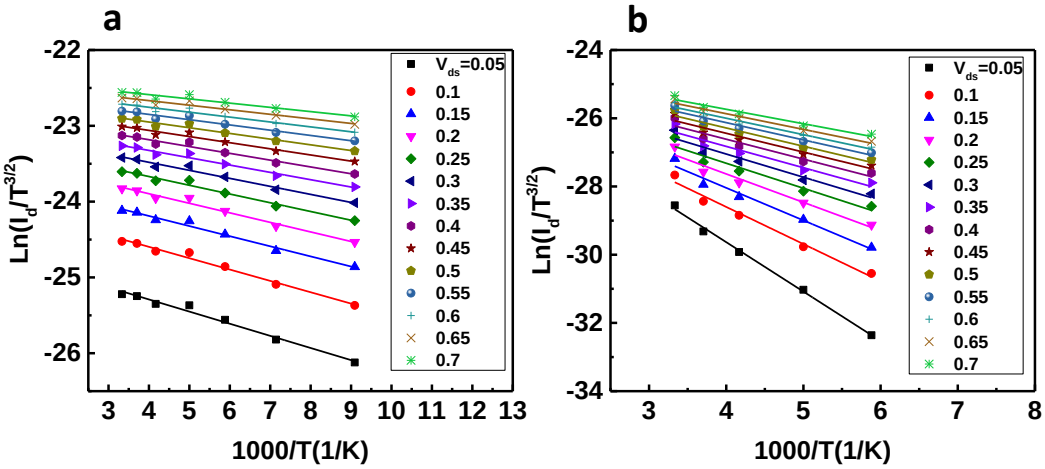

Figure 13. Arrhenius characterization for different applied source-drain biases: Arrhenius measurements for **(a),** MoS_2/Gr **(b),** MoS_2/Metal transistors at V_g=40V for different applied V_{ds}. **(c)** Slope of the Arrhenius graph as a function of the V_{ds} at gate 40 V.

The slope of figure 10a ($\frac{-q(\Phi_B-\frac{V_{ds}}{n})}{K_BT}$) at each source-drain bias for V_g=40 V is derived and plotted in Fig 14 for the MoS_2/Gr in-plane heterostructure.

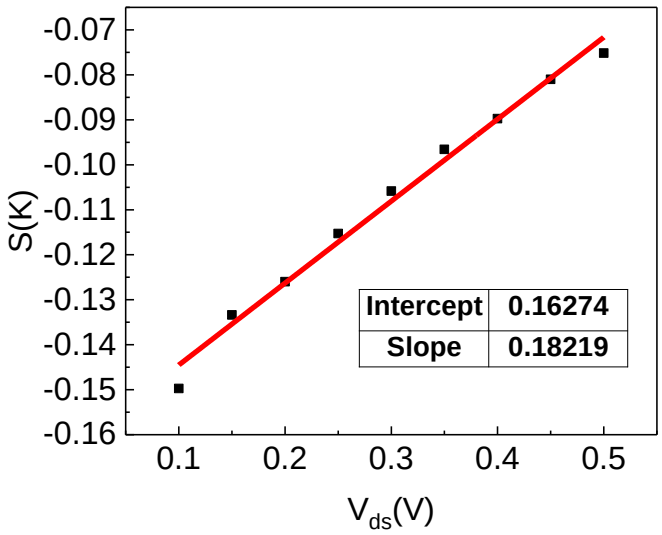

Figure 14. Slope of the Arrhenius graph as a function of the V_{ds} at gate bias of 40 V.

The Schottky barrier height (Φ_B) is calculated at the intercept of Fig. 14 with the Y axis, where the V_{ds} is zero[120]. Figure 15 further shows the derived Schottky barrier height of both structures at room temperature for different applied gate voltages. The Schottky barrier height for the MoS_2-metal structure is about 88 meV at V_g = 10 V and decreases to 60 meV for V_g = 60 V, while the MoS_2-graphene in-plane heterostructure starts at ~58 meV at V_g = 10 V and fades to zero at V_g = 60 V. The presence of the schottkey barrier height for MoS_2-metal structure even at high gate biases shows the importance of the choosing of appropriate metal contact for 2D-material semiconductors. This huge Schottky barrier results in decreasing the extrinsic mobility of these semiconductors and downgrading their performance for future applications significantly.

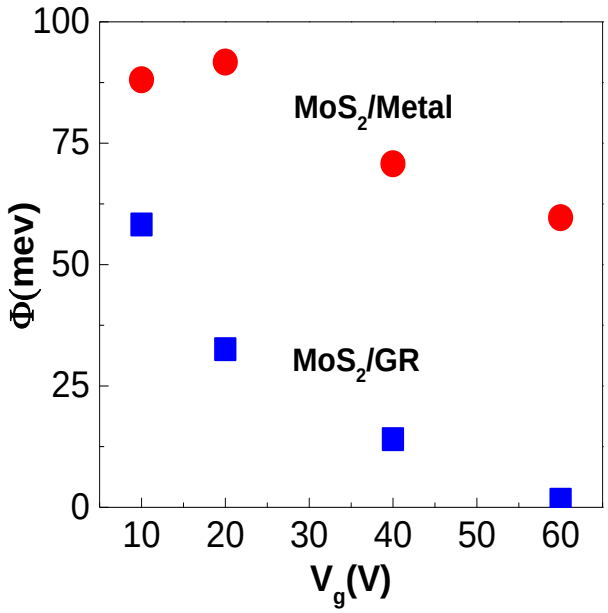

Figure 15. Extracted Schottky barrier height: extracted Schottky barrier height from Arrhenius measurements as a function of V_g for the MoS_2-graphene and MoS_2-metal FETs.

We also performed Kelvin probe force microscopy (KPFM) experiments to map the surface potential distribution across the MoS_2-graphene interface under applied source-drain and gate voltages. This technique enables us to spatially map the local potential drops in the MoS_2-graphene lateral heterojunction and in the MoS_2 and graphene films under device operational conditions to gain insight into their relative contributions to the overall resistance of the device. Figure 16a shows the KPFM mapping of the device at V_{ds} = 0 V and V_g = 0 V. We also mapped the change in the surface potential along the entire length of the device at V_{ds} = 1V and at different gate voltages (Figure 16b-c). As the gate voltage increases from -20 V to +20 V, the potential drop across the interface decreases from 455 mV to 201 mV (Figure 16d). This observation implies that the

contribution of the resistive potential drop across the interface relative to the total resistance of the device decreases as one increases the gate voltage. In other words, the MoS_2-graphene contact resistance has a negligible contribution to the overall device resistance at larger gate voltages.

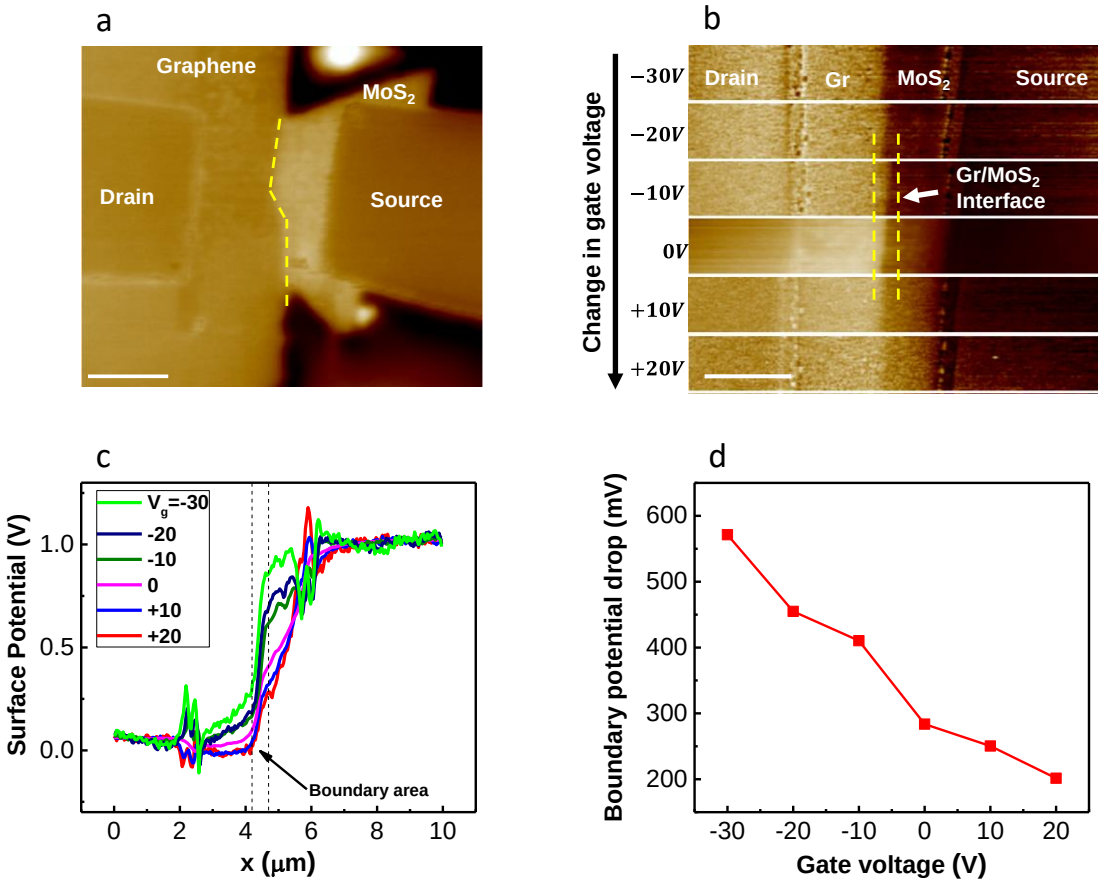

Figure 16. KPFM measurements: (a) KPFM mapping of the MoS_2-graphene transistor with $V_{gate} = 0\,V$ and $V_{sd} = 0\,V$. The interface between graphene and MoS_2 is highlighted with yellow dashed line (scale bar 2 μm). **(b)** KPFM mapping of the interface area from a selected region shown in (a) by keeping $V_{sd} = 1\,V$ and changing V_{gate} from $-20\,V$ to $+20\,V$ with $10\,V$ increments (Scale bar 2 μm). The dashed lines show the interface area. **(c)** Corresponding surface

potential profiles across the interface area. **(d)** The potential drop at the interface area as a function of the applied gate voltages.

Next, a systematic study of 1/f noise was performed in the MoS_2-graphene and MoS_2-metal devices in a vacuum (pressure < 10^{-5} Torr). Low frequency 1/f noise has the potential to severely limit the performance of nanoscale materials because 1/f noise increases with decreasing number of carriers (i.e., device size). Recently, it has been shown that metal contacts can play a significant role in 1/f noise in CVD-grown MoS_2. Thus, 1/f noise is an important metric to gauge the quality and viability of lateral graphene-MoS_2 heterojunctions. Regardless of the fundamental sources of 1/f noise (i.e., mobility fluctuation versus carrier number fluctuation), the noise power spectral density S_I can be described empirically as:

$$S_I = \frac{AI^\gamma}{f^\beta}$$

where I is mean drain current, f is frequency, A is noise amplitude, and exponents β and γ are expected to be close to ideal values of 1 and 2, respectively. Figure 17a shows $1/f^\beta$ dependence of noise spectral density for a MoS_2-graphene device with $\beta = 1.02 \pm 0.002$ over four decades of frequency.

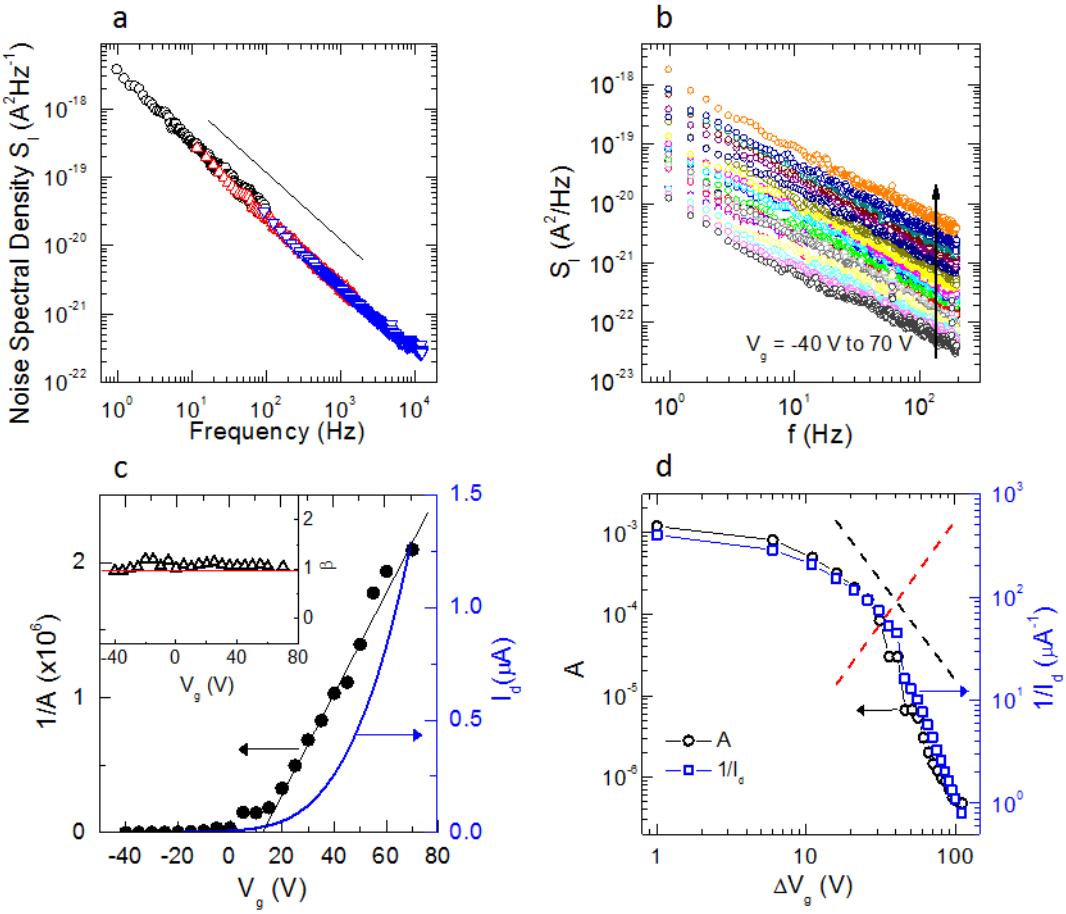

Figure 17. Noise spectral density measurements: (a) Noise spectral density (S_I) as a function of frequency for a MoS_2-graphene FET at V_g = 60 V and V_d = 4 V showing $1/f^{\beta}$ behavior with β = 1.02 ± 0.002. The black line shows ideal $1/f$ behavior. **(b)** S_I versus frequency of the device at V_g varying from -40 V to 70 V at V_d = 2 V. **(c)** Inverse of noise amplitude (1/A) versus V_g compared with transfer characteristics (device current (I_d) versus V_g) from the data in (c). The inset shows β as a function of V_g. **(d)** Log-Log plot of A and $1/I_d$ versus ΔV_g (= V_g + 41) where V_g is ranging from -40 to 70 V. Black and red dashed lines show V_g^{-2} and V_g^{2} dependence for purely channel and purely contact effects on $1/f$ noise, respectively.

We also studied the gate-dependence of 1/f noise characteristics to understand the origins of the low frequency fluctuations and the relative role of contacts in MoS_2-

graphene and MoS_2-metal devices. Figure 17b shows 1/f behavior of a MoS_2-graphene device for V_g = -40 to 70 V. Noise spectral density shows $1/f^{\beta}$ behavior ($\beta = 0.97 – 1.2$) with no clear dependence on V_g over the entire range (see inset of Figure 17c). Transfer characteristics ($I_d – V_g$) of this device show a threshold voltage V_{th} = 40 V (Figure 17c), and thus measurements cover both accumulation ($V > V_g – V_{th}$) and sub-threshold regions ($V < V_g – V_{th}$). The noise amplitude A was extracted from the plots of I^2/S_I versus frequency with the V_g dependence analyzed in Figure 17c,d. First, 1/A varies linearly with V_g in the accumulation region (Figure 17c), even though I_d follows a super-linear behavior with V_g in accumulation. Note that $I \sim V_g^m$ ($m = 1 – 2$) behavior arises from reduced screening effect in a two-dimensional material with parabolic band structure and has been described in experimental findings[122] and in analytical calculations[123]. Within Hooge's mobility fluctuation model, the noise amplitude A is related to the carrier number (N) according to $A = \alpha_H/N$, where α_H is Hooge's parameter and $N = C_g/(V_g – V_{th})/q$ in the accumulation region, where C_g is total gate oxide capacitance and q is electronic charge. Thus, the linear $1/A \sim V_g$ dependence in the accumulation regime in Figure 17c and strong correlation between noise amplitude and current throughout the whole range of V_g suggests mobility fluctuation or correlated mobility-number fluctuation as the dominant source of current fluctuations in the accumulation region, in agreement with previous 1/f noise studies conducted on exfoliated MoS_2 transistors[124]. The number fluctuation model predicts the correlation between A and $(g_m/I)^2$, where g_m is the transconductance. [125]–[128] In the absence of

such correlation in these devices, we rule out the number fluctuation model. The Hooge parameter for this device was extracted as α_H = 0.21, which is comparable to previous CVD-grown MoS_2[129] but larger than high quality exfoliated MoS_2 by up to 2 orders of magnitude[124]. Indeed, the average Hooge parameter of six measured devices is 0.33 ± 0.08.

Now we consider the role of contacts in the 1/f noise behavior in graphene-MoS_2 and metal-MoS_2 devices. In the case of significant Schottky barriers at the contacts, fluctuations in both channel resistance (R_{ch}) and contact resistance (R_c) can contribute to the overall noise in the transistor. Thus, the normalized noise spectral density can be written as:

$$\frac{S_I}{I^2} = \frac{S_{R_c}}{{R_c}^2}\frac{R_c^2}{(R_{ch}+R_c)^2} + \frac{S_{R_{ch}}}{{R_{ch}}^2}\frac{R_{ch}^2}{(R_{ch}+R_c)^2}$$

where S_{Rc} and S_{Rch} are power spectral density originating solely from the contacts and the channel, respectively. Based on this equation for the number fluctuation model, in the case of dominant channel resistance, noise A (and S_I/I^2) would vary as $\sim V_g^2$, and in the case of dominant contact resistance, the noise would result in $\sim V_g^{-2}$ dependence in the accumulation region. Note that a log-log plot of A versus ΔV_g overestimates the exponent *m* in Figure 17d. However, the A versus V_g behavior is starkly different from the $\sim V_g^2$ behavior expected for dominant contact resistance that has been seen in previous CVD-grown MoS_2 transistors[130]. Thus, we can conclude that the MoS_2-graphene interface is not the dominant source of 1/f noise in our devices.

Finally, we compare the normalized noise amplitude ($A \sim 1/N$) with the total number of carriers (i.e., channel area $L \times W$) for all measured MoS_2-graphene and MoS_2-metal devices (Figure 18). V_g dependence of normalized noise amplitude shows overall decreased noise in MoS_2-graphene. Furthermore, channel area-scaling results in a tighter distribution of noise metrics for MoS_2-graphene devices (Figure 18), suggesting MoS_2-metal has a larger contribution of noise from the contacts. Furthermore, the overall V_g dependence is more well-defined ($A \sim 1/V_g$) in MoS_2-graphene devices, again corroborating the dominance of channel resistance fluctuations compared to contact resistance fluctuations.

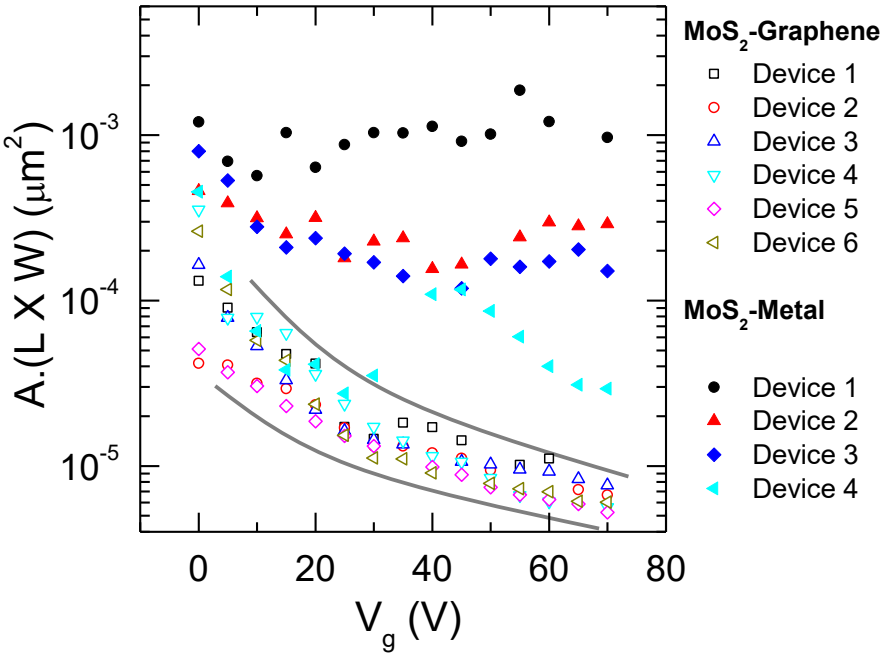

Figure 18. Noise amplitude measurements. Comparison of area-normalized noise amplitude (A. (L X W)) of MoS_2-graphene and MoS_2-metal FETs as a function of V_g. Two gray lines show upper and lower bonds of noise amplitude for MoS_2-graphene devices.

For reliable electronics, it is also critical to achieve mechanically and electrostatically robust contacts. The present MoS_2-graphene devices have essentially a 1D interface between two 2D materials. Thus far, electrostatic breakdown of a lateral heterojunction of this type has not been probed. Figure 19a, b shows current-voltage characteristics of a MoS_2-graphene and a MoS_2-metal device for V_d = 75 to -75 V (sweep rate = 1 V/s) under vacuum (pressure < 10^{-5} torr). Both devices show qualitatively similar behavior of electrostatic breakdown. In particular, the current decreases irreversibly by more than 2 orders of magnitude within 1 V. Interestingly, both MoS_2-graphene and MoS_2-metal

devices show comparable maximum width-normalized drain current (~40 μA/μm) just before breakdown, roughly an order of magnitude lower current density than high quality exfoliated monolayer MoS_2.[131] The breakdown field of the two devices is also comparable (~38 MV/m). Scanning electron microscopy of the broken devices was conducted to probe morphological evidence of the failure mode (inset of Figure 19a and b). A significant portion of CVD MoS_2 was found missing near the drain contacts in both of the devices. This suggests a similar failure mechanism irrespective of metal or lateral graphene contacts. Thus, direct growth of the MoS_2-graphene heterojunction does not significantly affect the electrostatic breakdown characteristics of the devices.

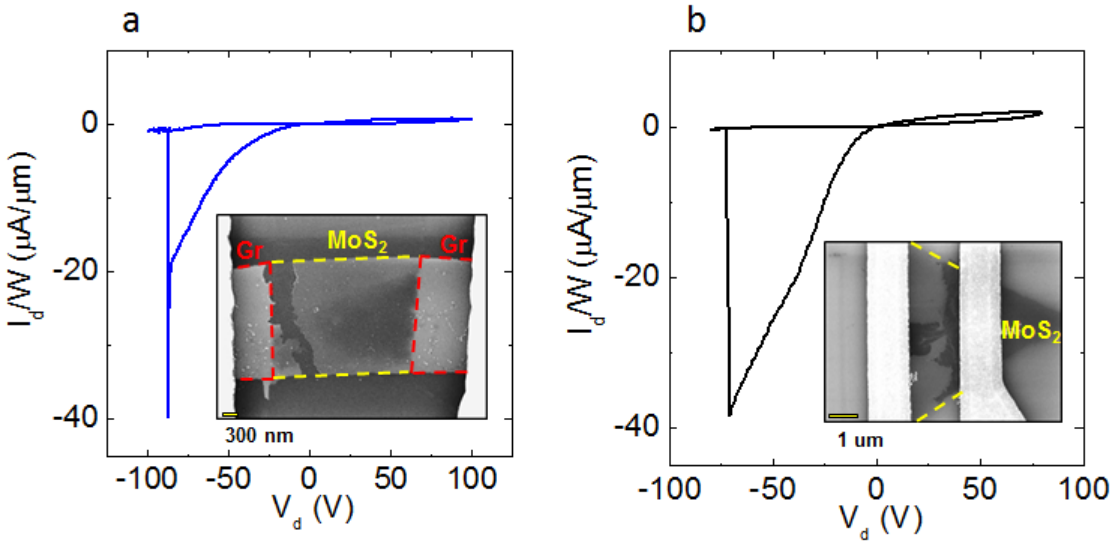

Figure 19. Breakdown test: (a), (b) Current-voltage characteristics of a MoS_2-graphene and MoS_2-metal FET, respectively, at V_g = 0 V showing irreversible breakdown at large V_d. The current was normalized to the channel width. The insets of figure (a) and (b) show scanning electron microscopy micrographs of the MoS_2-graphene and MoS_2-metal FETs after the breakdown, respectively.

To shed light on the origin of the improved electrical performance of the MoS_2-graphene devices, we perform bandstructure, band alignment, and transport calculations. The total resistance (R_{tot}) of the device between source and drain is comprised of the series resistances from the graphene grains (R_{grap}, forming source and drain), resistance of MoS_2 grain (R_{MoS_2}, constituting the channel) and resistances of the interfaces ($R_{int.}$) between graphene and MoS_2. We calculate the series grain resistances of graphene and MoS_2 sections from the general expression– $R_{2D} = \rho\frac{L}{W}$, where ρ is the resistivity of the material (sheet resistance in this case) and $\frac{L}{W}$ is the aspect ratio of the sample. The conductivity ($\sigma = \frac{1}{\rho}$) of graphene and MoS_2 grain is calculated from $\sigma = qn\mu$, where n is the sheet charge density, μ is the carrier mobility.

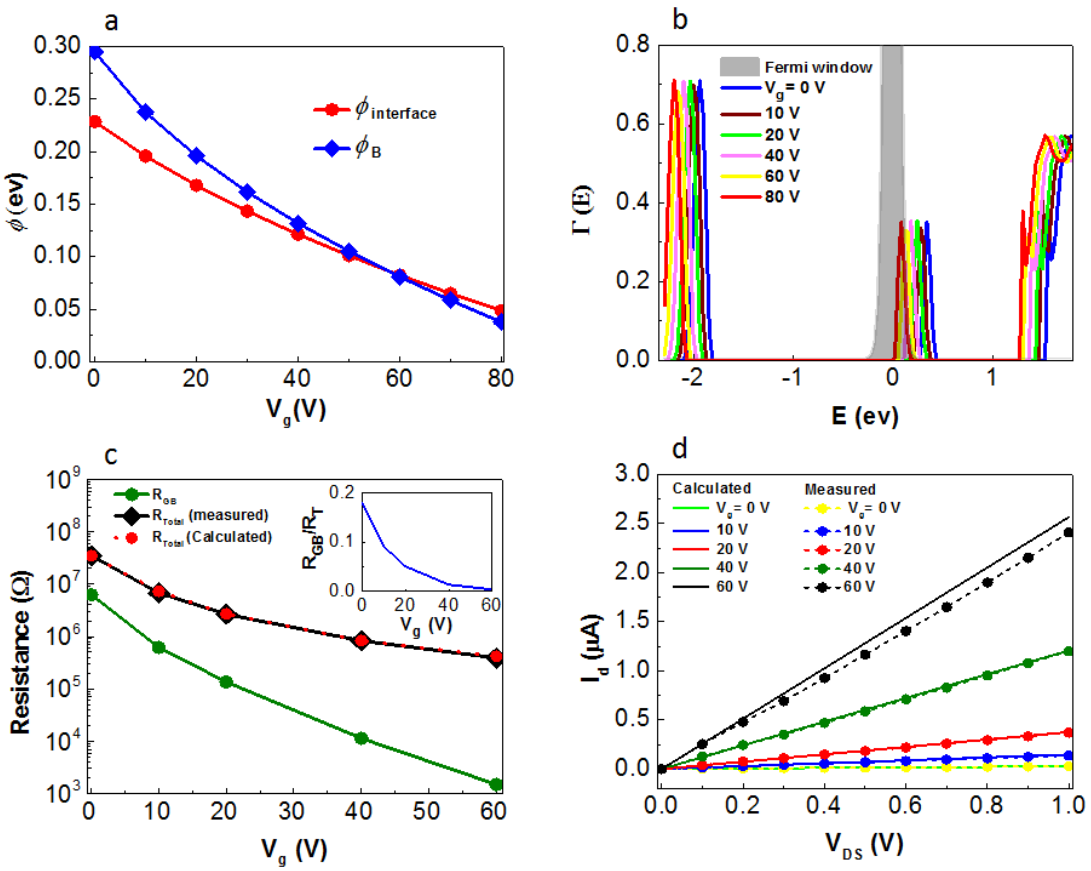

Figure 20. DFT calculations: (a) Variation in interfacial Schottky potential barrier height — from graphene to MoS_2 (ϕ_B) and from MoS_2 to graphene ($\phi_{interface}$) — with gate voltage (V_g). **(b)** Resulting shift in transmission coefficient with gate voltage, such that with the increasing V_g a larger part of $\Gamma(E)$ overlaps with the Fermi window (shown by the grey area in the plot) resulting in increased conductance. **(c)** Interfacial resistance ($R_{int.}$) and the total resistance (R_{tot}) — both measured (red line with red markers) and calculated (black line with black markers) — against gate voltage. The inset shows the percentage contribution of interfacial resistance ($R_{int.}$) towards the total resistance (R_{tot}) of the device at different gate voltages, in good agreement with KPFM measurements. **(d)** Drain current (I_D) vs. drain-source voltage (V_{DS}) calculated both experimentally and by numerical simulation showing good agreement between numerical and experimental results.

In the case of a finite gate voltage and zero drain bias, the Fermi levels in both graphene and MoS_2 away from the interface shift relative to their position at zero gate voltage in response to the induced charge in the 2-dimensional layers, as shown in Figure 18a. Consequently, the energy bands on both sides of the interface rearrange themselves to maintain the equilibrium condition. However, the shift in the bands on the two sides is not identical because the two materials have different densities of states, leading to an increase in band bending in the MoS_2 with increasing gate bias. The transmission coefficient of electrons across the interface, however, depends on the alignment of energy bands of graphene and MoS_2 at the interface. For example, states near the Fermi level in graphene cannot typically be transmitted because there are no available states at the same energy in MoS_2 as energies near the Fermi level fall inside the bandgap. Increasing the gate bias increases the sheet charge density in both graphene and MoS_2; in response, the barrier height at the junction of the two domains decreases with increasing gate voltages (Figure 20a), in agreement with the electrical measurements in Figure 15.

Because of band rearrangement and barrier lowering, the transmission Γ(E) also shows a dependence on gate voltages. It can be seen in Figure 20b that with increasing gate voltages, the transmission coefficient Γ(E) shifts towards the left resulting in larger overlap between Γ(E) and the so-called Fermi window$\left(-\frac{df}{dE}\right)$, centered at the Fermi level. An increase in overlap between the transmission Γ(E) and the Fermi window corresponds to a reduction in interfacial resistance. In addition to the reduction in interfacial resistance with gate voltage, we obtain a reduction in the resistance of the

MoS_2 due to the increase in sheet charge density and mobility with gate voltage. The simultaneous reduction in interfacial resistance and MoS_2 resistance with gate bias leads to an overall decrease in the total resistance (R_{tot}), as can be seen in Figure 20c. We find that the contribution of the interfacial resistance to the total resistance of the combined MoS_2+interface+graphene system (R_{tot}) decreases with increasing gate voltages, starting at around 25% of the total in the intrinsic case (zero gate bias), and rapidly dropping below 1% at gate voltage of 60 V, as shown in the inset of Figure 20c, further corroborating the KPFM measurements at the interface. The agreement between measured and calculated total resistances of the device, mathematically written as $\mathrm{R_{tot}} = 2\mathrm{R_{grap}} + \mathrm{R_{MoS_2}} + 2\mathrm{R_{int.}}$ and shown in Figure 20d, indicates that the measured resistances are well reproduced by the model. We also show that at large non-zero gate biases, the interface contributes very little to the overall resistance, leading to Ohmic behavior.

2.3. Details of Material Synthesis, Characterization, Device Fabrication, KPFM Measurement, Noise measurement and DFT Calculation

2.3.1. Graphene Growth Procedure

The Three-Zone MTI CVD furnace is used for graphene growth. The partially and fully covered graphene films are grown on the copper substrate (Alfa Aesar, product no. 46365) by using atmospheric pressure CVD growth process. The copper substrate is immersed inside of the hydrochloric acid for 15 minutes to remove the local surface oxides and then rinsed with acetone and isopropanol. Next, the copper substrate was

placed inside of the CVD furnace and then the chamber was evacuated to the 1 mTorr vacuum pressure to remove the unwanted gasses. The chamber was then restored to atmospheric pressure by filling it with 5% hydrogen diluted in argon gas. The growth procedure consists of three main steps. The first step was annealing, in which the maximum temperature of the furnace is set to 1050 ^{o}C and the annealing time was 1 hour for the growth of both partially and fully covered graphene films. In the second step, the furnace was filled with 20 p.p.m methane gas and the growth time was 60 minutes for partial coverage graphene and 90 minutes for full coverage graphene film. The third step was cooling in which the furnace is cooled down to room temperature by force cooling and the methane gas also was stopped from flowing into the furnace. Figure 21a shows the scanning electron microscopy (SEM) image of the partially grown graphene flakes on cupper substrate and figure 21b exhibits the optical image of the graphene flakes transferred to silicon substrate.

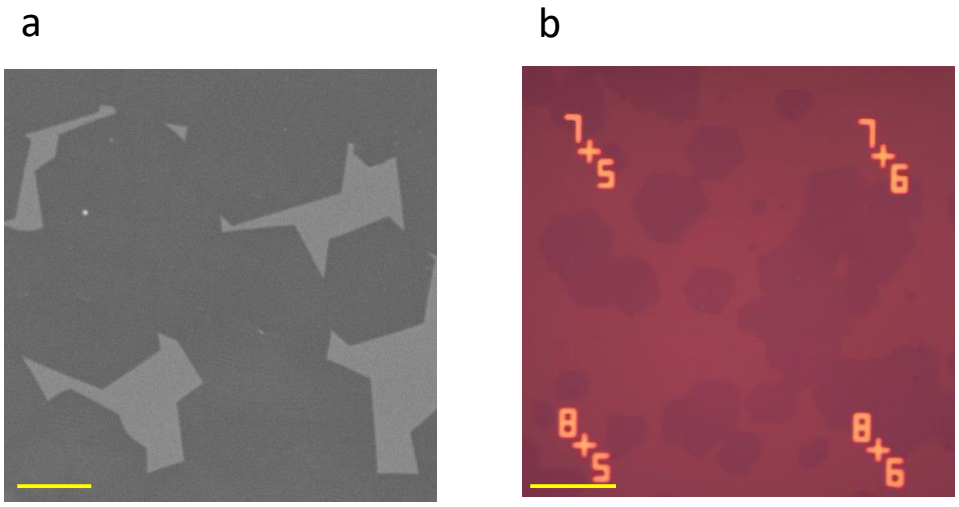

Figure 21. Optical and SEM Characterization of the graphene flakes: (a) SEM images of the partially grown graphene flakes on cupper substrate (scale bar is 10 μm). (b) Optical image of the partially grown graphene flakes transferred to silicon substrate (scale bar is 15 μm).

2.3.2. MoS_2-Graphene Growth Procedure

The oxygen plasma treatment is performed on SiO2/Silicon substrate for two minutes to make the substrate hydrophilic, which helps with the transfer of the graphene film and the growth of MoS2 on the substrate. After transferring the partial coverage graphene film onto the SiO2/Silicon substrate, the substrate is annealed at 400 ºC for 8 hours. The 5% diluted hydrogen in argon gas was also continuously supplied during the annealing process to remove the residue of the transfer process. Then, the substrate is placed inside of the MoS2 CVD chamber together with 2 milligrams of Molybdenum trioxides and 1 gram of sulfur as precursors for the MoS2 growth. The chamber temperature increased to 550 oC in 30 minutes and then it was increased to 850 oC in 60 minutes. The growth time was 10 minutes and then furnace was cooled down to the room temperature by

natural cooling. It is worth mentioning that increasing the time of the MoS2 growth or the amount of the MoO3 powder will result in the growth of the MoS2 film on top of the graphene film.[132] Figure 22 shows the optical image of the polycrystaline MoS2 film grown next to the graphene flakes.

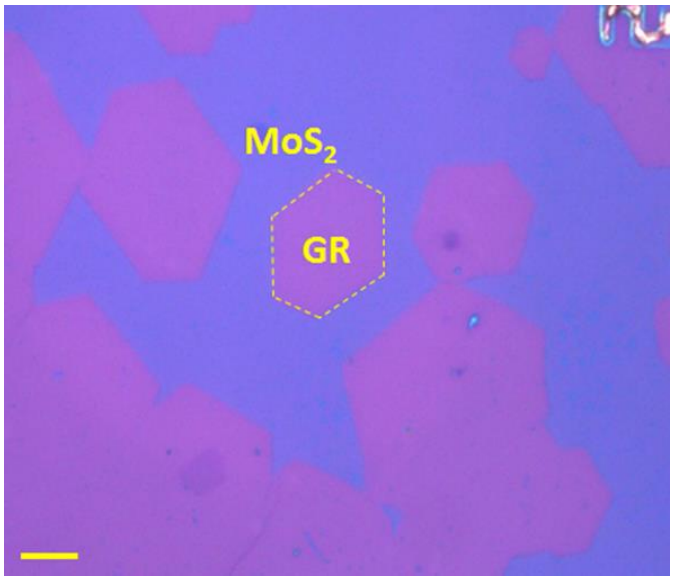

Figure 22. Optical characterization of the MoS_2 film next to the graphene flakes: Optical image of the Polycrystalline MoS_2 film grown next to the graphene flakes (scale bar 10 μm).

2.3.3. Fabrication of MoS_2-Graphene Field Effect Transistor

After the graphene film was transferred onto the SiO2 substrate, it was patterned into rectangles by a photolithography process followed by oxygen plasma etching. Next, MoS2-graphene heterostructure was synthesized, and the metal electrodes were patterned on the MoS2-graphene FETs and on the MoS2 FETs by an electron beam lithography method. Finally, 10 nm Titanium and 60 nm Gold were deposited on the devices by an electron beam evaporation process.

2.3.4. KPFM Measurement

All AFM experiments were carried out with a Dimension ICON system (Bruker, CA) in ambient conditions. PFQNE-AL cantilevers (Bruker, CA) were selected for improved spatial resolution in surface potential measurements. The nominal spring constant is 0.8 N/m and the resonant frequency is 300 kHz. Two-pass technique (also known as 'lift mode') was applied in KPFM experiments. During scanning, the sample was grounded, while a bias $\Delta V = V_{DC} + V_{AC}$ was applied to the AFM cantilever, where the V_{DC} and V_{AC} are the DC and AC component, respectively. The frequency of V_{AC} was chosen at the resonant frequency of the cantilever. The AFM controller nulled the cantilever amplitude due to periodic electrostatic force by adjusting V_{DC}. If the work function of the cantilever tip Φ_{tip} is known, then the sample work function Φ_s can be given as $\Phi_s = \Phi_{tip} - eV_{DC}$. Φ_s and V_{DC} are opposite in sign, so the work function Φ_s has inverse contrast with KPFM mapping. All AFM data were analyzed with Nanoscope Analysis software (Bruker, CA). Figure 23 shows the KPFM setup.

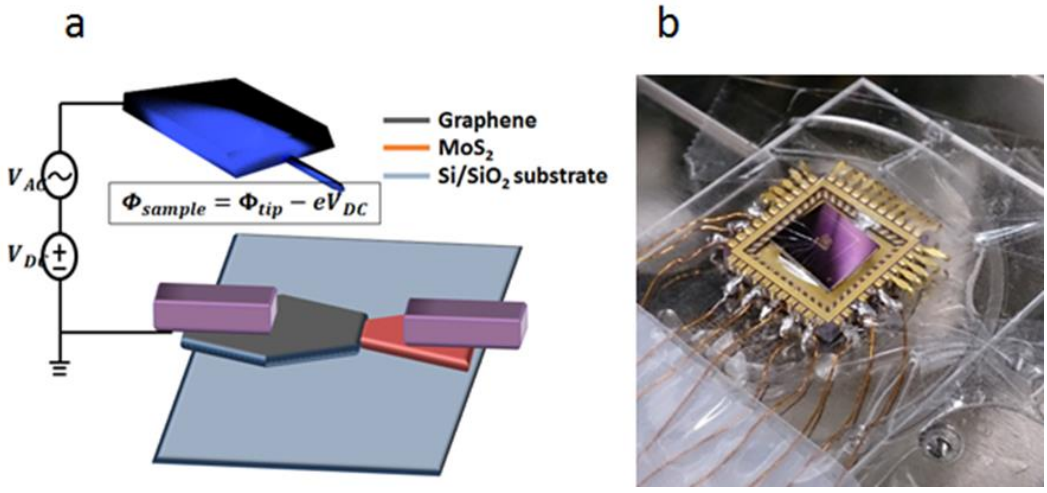

Figure 23. KPFM setup: (a) Schematic of the KPFM setup. **(b)** Device optical image mounted on the KPFM setup.

2.3.5. 1/f Noise and Breakdown Measurements

All 1/f noise and breakdown measurements were carried out under vacuum (pressure ~105 torr) using a LakeShore CRX 4K probe station. The current fluctuations were amplified with a low-noise voltage amplifier (DL Instruments 1212) and power spectral density was captured with a spectrum analyzer (Stanford Research SR780). Drain and gate voltage were controlled by Keithley Instruments 2400 source-meters and homemade LabView programs. Power spectral density in devices powered by stand-alone batteries and source-meters was found to be comparable, thus confirming that the measurement apparatus does not contribute to the measured noise.

2.3.6. Raman Mapping

Raman mapping: The Swift mode Raman mapping with a 500 nm scanning step size is performed for two different ranges with the total number of 1824 collected spectrums.

The first range was from 100 cm-1 to 900 cm-1 and the second one was from 800 cm-1 to 1700 cm-1.The classical least-square (CLS) fitting was used to analyze the Raman data, which includes the E2g and A1g peaks of the MoS2 and the G peak of the graphene.

2.3.7. DFT Calculation

Density functional theory calculation of the electronic structures: We performed self-consistent Density Functional Theory (DFT) calculations with the open-source software Quantum-Espresso (www.quantum-espresso.org). For graphene, we used a scalar relativistic, norm-conserving pseudopotential (NCPP) which uses a direct-fit Von Barth-Car method with a Perdew-Zunger (LDA) exchange-correlation functional. For MoS_2, we used a non-relativistic NCPP for Mo and a scalar relativistic NCPP for S. Both potentials employed a Martins-Troullier method with a Perdew-Wang (LDA) exchange-correlation. The lattice constants are a=2.459 Å for graphene and a=3.125 Å, z=3.11 Å for MoS2, where z is the S-S distance. The band structures produced by these parameters can be found in Figure S13. To capture the monolayer band structure, planes of single-layer graphene or tri-layered MoS2 are separated by a 20 Å vacuum. The cutoff energy for plane waves was 120 Ry for graphene and 140 Ry for MoS2. We used a convergence threshold of 10-16 on a Monkhorst-Pack grid sizes of 8 × 8 × 1 for graphene and 6 × 6 × 4 for MoS2 for the initial total energy calculation and then performed a bands calculation on a dense grid of 126,040 k-points with a convergence threshold of 10-12. We use the central difference method to obtain the band velocities per band which in turn is used to

determine the electronic DOS and other transport properties including interfacial transmission and resistance of the interface.

Mobility calculation in MoS2: The carrier mobility in graphene, which depends on its carrier concentration, is taken from the work by Dorgan et al.[133] In addition to intrinsic phonon-limited carrier mobility in MoS2 (μ_{ph}~ 410 cm2/V-s[134]), the mobility is also influenced by factors like charged impurities, surface optical (SO) phonons and other short range scattering mechanisms. However, it has been reported that the electron mobility in MoS2 is largely affected by the charged-impurity (CI) scattering.[135], [135], [136] An empirical expression for CI-limited mobility for MoS2 has been adopted and modified from the work by Ma and Jena[135] and is given as: $\mu_{CI} \approx \frac{45}{n_{imp}/10^{11}\ cm^{-2}}\left(A(\epsilon) + \left(\frac{C_{oxide}V_g + n_{imp}}{10^{13}\ cm^{-2}}\right)^{1.2}\right)$, where $A(\epsilon)$=0.036 is a fitting constant depending on the dielectric constant of SiO2 (oxide layer), C_{oxide} is the capacitance per unit area of the gate oxide, and n_{imp} is the charged-impurity density. The impurity density equals sheet charge density ($n_C = C_{oxide}V_g + n_{imp}$) at zero gate voltage. We use an impurity concentration of $5.5 \times 10^{11}\ cm^{-2}$, which is found by fitting the finite resistance at zero gate voltage obtained from experimentally measured $I_d - V_{DS}$ data. In the presence of multiple scattering mechanisms, the mobility of the free carriers can be represented by Matthiessen's rule and is given as: $\mu_{MoS_2} = \left(\mu_{ph}{}^{-1} + \mu_{CI}{}^{-1} + \mu_{SR}{}^{-1}\right)^{-1}$, where μ_{SR} is the mobility due to short range effects[136].

2.4. Summary and Conclusion

In conclusion, we report seed-free synthesis of graphene and MoS_2 lateral heterojunctions through the CVD method, which exhibit improved electrical performance compared to conventional metal-contact MoS_2 devices. This method makes in-plane MoS_2-graphene heterostructures promising for the large-scale production of electronic and logic circuits from all-2D materials for next generation device applications. Temperature-dependent electrical characterization shows Ohmic behavior for the MoS_2-graphene FET devices at back-gate voltages above 60 V, verifying a high-quality lateral interface between MoS_2 and graphene. KPFM results also visualize the reduction of the MoS_2-graphene in-plane junction resistance at positive gate voltages. We further present the first study of 1/f noise in 2D lateral heterojunction electronic circuits. MoS_2-graphene devices show up to an order of magnitude lower noise amplitude in comparison to MoS_2-metal devices fabricated under similar conditions. A systematic study of 1/f noise by varying gate bias and area-scaling revealed the dominant origin of noise as mobility fluctuations in the accumulation region. We also conducted the first electrostatic breakdown study of lateral MoS_2-graphene heterojunctions. In this case, MoS_2-graphene and MoS_2-metal devices showed comparable current density, breakdown fields, and similar failure modes through microscopic visualization. Our numerical calculations reveal that both the barrier at the interface as well as the resulting interfacial resistance decrease as sheet charge is increased in response to the external gate voltage, matching the KPFM results. At gate voltages above 60 V, the interface contributes less than 1% to

the overall device resistance despite the appreciable electron mobility in MoS_2, resulting in the observed linear (Ohmic) behavior.

CHAPTER 3

Power Dissipation of WSe_2 FET using Low-Frequency Raman Peak

(Most parts of this chapter are taken from the Accepted paper with the following citation:

Amirhossein Behranginia, Zahra Hemmat, Arnab K. Majee, Cameron J. Foss, Poya Yasaei, Zlatan Aksamija, Amin Salehi-Khojin1"Power Dissipation of WSe_2 Field Effect Transistors Probed by Low-Frequency Raman" ACS Applied Materials & Interfaces, 2018.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

3.1. Introduction

Thermal management of the modern electronic circuits is going to be a formidable challenge by continuing the miniaturization of the electronic devices. The operating voltage of the new generation electronic systems needs to be reduced to balance out their power dissipation[137]. Scaling down of these devices results in moving toward the subcontinuum regime in which both electron and phonon transport follows ballistic condition. The electron-phonon interactions are the main reason of the heating of these devices and could be energetically and spatially nonuniform[76]. Future nanoelectronic devices with gate length <5nm needs the transistor channel thickness less than one-third of the gate length[138].Also, the demands for thinner electronic devices with higher speeds and preventing the short channel effect in these future nanoelectronic devices push scientists to discover new materials with characteristic superior to conventional ones. The recent discovered 2D-materials are very promising to be used for future nanotransistors due to their unique mechanical, physical and chemical properties at their

atomic thicknesses. The single layer of these materials is highly flexible, transparent and robust. They have a pristine surface which results in reducing the surface roughness scattering and interface traps[139]. Also, controlling the charge carriers of 2D-materials,by applying gate biases, is easier than controlling the charge carriers in conventional bulk materials due to their atomic thicknesses[139]. These materials cover a wide range of electronic properties from insulating material to semiconductors and conductors. One of the semiconductor family of 2D-materials are Transition metal dichalcogenides (TMDs) with an indirect bandgap which could be changed to direct one by reducing their thickness to the monolayer structure[4], [42]. This family of 2D-materials have shown promising results in wide range of applications such as electronics[1], [137], [138], optoelectronics[140], sensing[70], energy conversion[25], [141], [142] and storage systems[143]. Tungsten diselenide (WSe_2) is one of the TMDs' members with ambipolar transport behavior. The crystal structure of this material consists of stack layers in which one tungsten atom is sandwiched by two selenium atoms. The bulk structure of this material has an indirect bandgap of 1.2 eV[144] and its single layer has a direct bandgap of 1.65 eV[145]. The hole mobility of 500 $cm^2/V.S$ for bulk WSe_2 and the extrinsic back-gate electron mobility of 142 $cm^2/V.S$ for single layer WSe_2 is reported by Podzorov et al.[146] and Liu et al.[139] respectively. This is a high extrinsic back-gate mobility which results in high potential of using this semiconductor as a channel of the future nanotransistors. Interlayer van der walls (vdW) bonding of this material facilitates the thinning process of this material to atomic thicknesses. Hence,

thin structure of this material can easily be made from its bulk structure by using mechanical exfoliation or chemical exfoliation method. But this interlayer bonding also results in weaker thermal and electrical conductivity of this material between its layers compared to through its layers. Also, large surface to volume ratio of this material results in significantly increasing the role of its boundary thermal resistances. Chiritescu et al. [147] have reported the cross plane thermal conductivity of 0.05 W/m.K for disordered thin films of WSe_2, which is one of the lowest thermal conductivities observed in a fully dense solid materials. Kim et al. [148] also reported the thermal conductivity of less than 1 W/m.K for poly crystalline WSe_2 material. Hence, heat removal from the devices made from this material is more complicated and needs the complete understanding of its thermal physics which does not follow the classical diffusion theory prediction for the heat generation regions[76]. Scientists are also very interested to investigate the thermoelectric properties of WSe_2 material due to its high electrical conductivity and low thermal conductivity. Recently, Wang et al. [149] have done a study on the thermoelectric properties of WSe_2 nanoribbons using first-principle calculations to find out about the ZT values of the armchair and zigzag WSe_2 material. They have claimed that the ZT value of the armchair WSe_2 nanoribbons (1.4) is seven times higher than that of zigzag WSe_2 nanoribbons at room temperature. This value will be increased to 2.4 at the temperature of 500 K due to reaching to the minimum value of its thermal conductance at this temperature. There is still a lack of enough understanding about the

power dissipation of WSe_2 material under the applied biases which will be furthered discussed in this work.

3.2. Results and Discussion

In this work, we exfoliated WSe_2 flakes from its powder (Alfa Aesar Company) by standard mechanical exfoliation method onto the silicon substrate with 300 nm oxide layer. Then, the substrate was left into the Acetone bath for one hour followed by 2 hours annealing at 200 °C in Argon environment to remove the exfoliation residues. Tapping mode of Dimension ICON system (Bruker, CA) is used to take the Atomic force microscopy (AFM) image from the exfoliated flake. Figure 24 shows the representative AFM image of the WSe_2 flake with thickness of ~7nm.

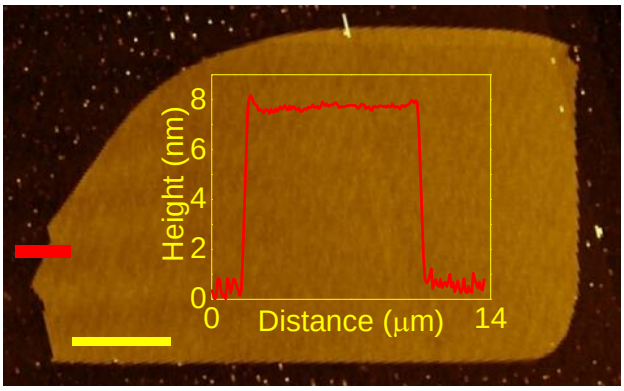

Figure 24. AFM Characterization: AFM image of the exfoliated WSe_2 flake (inset shows the AFM height profile). The scale bar is 2.5 μm.

Next, source-drain metal electrodes are patterned by e-beam lithography method and 5 nm silver (Ag) and 35 nm gold (Au) are deposited as metal electrodes. The reason of choosing Ag material as metal contact is based on previous study by Liu et al[139]. In

this study they have compared the performance of the WSe_2 FETs by depositing four different metals (Aluminum (Al), titanium (Ti), Ag and indium (In)). Among these metals In and Ag contacts have shown the best results with mobility of 142 and 44 $cm^2/V.S$ respectively. But the weak adhesion of the In metal to the 2D-materials make us choose Ag metal for this project which provides enough mobility for measuring the power dissipation of the WSe_2 material. Figure 25a shows the optical image of the fabricated device with a length and width of 6.5 μm and ~8.5 μm respectively. Then, the electrical transfer characteristics (I_d-V_g) were measured at room temperature and vacuum condition. The applied source-drain bias was 1V and gate voltage was changed from -60 V to +60 V. We increased the source-drain bias from 1 V to 10 V to perform current annealing on the device and remove the absorbed moisture, which results in decreasing the current density and mobility of some of the devices. Figure 25b exhibits the I_d-V_g results at V_{ds}=1V before and after current annealing for WSe_2 FET. The measurements indicate an ambipolar behavior with small hole current at high negative gate voltages (2 orders of magnitude lower than that of the electrons). The extrinsic back-gate field effect mobility of the device is extracted from the linear region of the I_d-V_g curve and calculated based on the following formula:

$$\mu=(dI_d/dV_g)\times(L/(W\times V_{ds}\times C_g)$$

In which I_d is the drain current, V_g is the gate bias, L and W are the length and width of the device, respectively, V_{ds} is the drain voltage and C_g is the gate capacitance. The

mobility of this device was ~ 65 cm^2/V.S before current annealing and was consistent, however, the drain current increased by a small amount after current annealing. It is worth mentioning that current annealing helps to improve the mobility of some of our devices by a factor of 2 (figure 25c). Our back-gated extrinsic mobility values for different fabricated devices are ranging from ~20 cm^2/V.S to ~70 cm^2/V.S with I_{on}/I_{off} $>10^6$. The I_d-V_{ds} measurements at three different applied gate biases (Figure 25d) shows linear behavior. This proves the ohmic contact between Ag electrodes and WSe_2 material, consistent with the previous study[139].

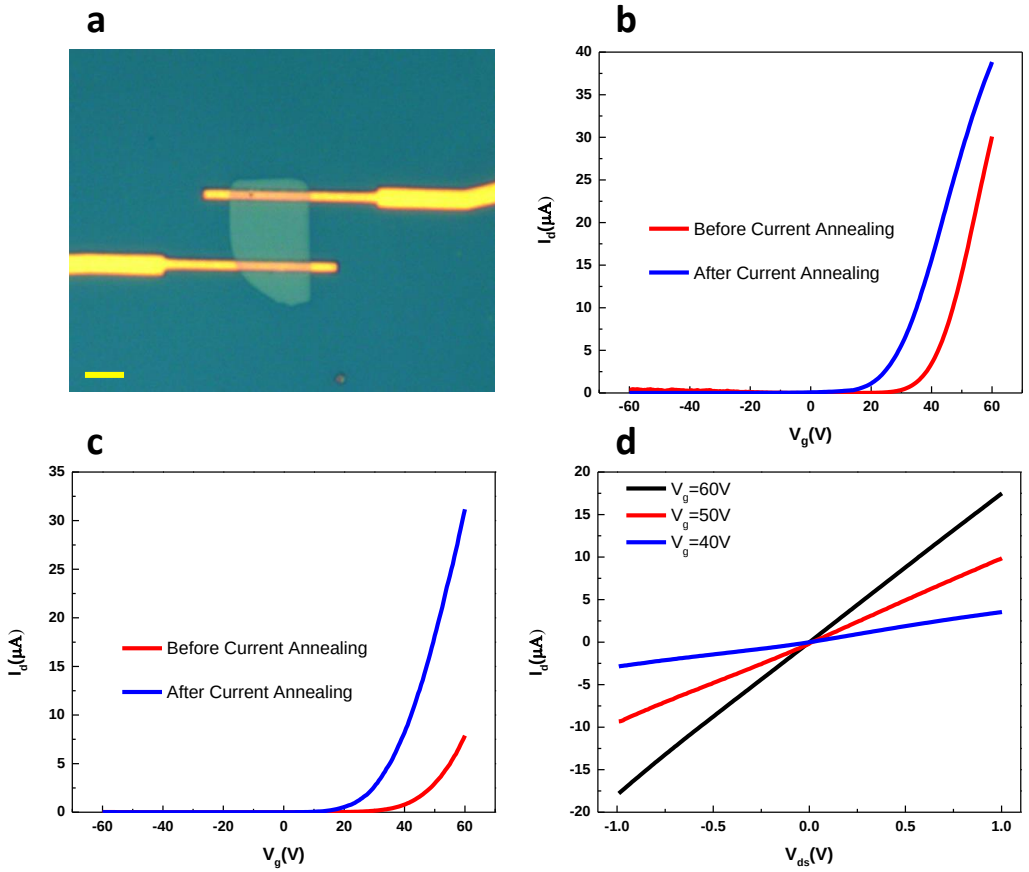

Figure 25. Optical and electrical characterizations of WSe_2 FET: (a) Optical image of the WSe_2 FET (scale bar is 4 μm). **(b) and (c)** Electrical transfer characteristic for WSe_2 FET. **(d)** Electrical transport characteristic of WSe_2 FET.

To be able to perform Raman thermometry on our device we need to operate the device in the air environment instead of the vacuum environment. The I_d-V_g measurement of WSe_2 FET without encapsulation in air (Figure 26) shows that the current of the device reduces about three orders of magnetite which results in significantly decreasing the mobility of the device. Instability of the device (without encapsulation) and its mobility reduction in the air environment prevented us from

measuring its power dissipation with Raman thermometry. So, we needed to deposit a layer as a passivation layer to be able to perform the measurement in the air environment.

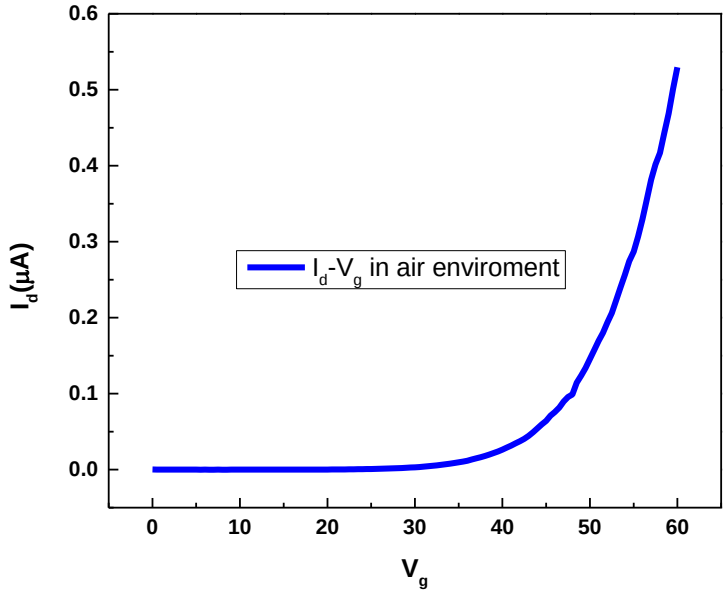

Figure 26. Transfer characteristic of bare WSe_2 FET in the air: I_d-V_g measurements of bare WSe_2 FET with length of 6.5 μm and width of 8.4 μm in the air environment.

To deposit a passivation layer on WSe_2 flakes, we first tried to deposit this layer directly on top the WSe_2 flakes. The Savannah-atomic layer deposition system was used for this process. Figure 27 shows the optical image of this system. The system was connected to the vacuum pump to be able to perform the ALD deposition at low pressures. The uniformity of the deposition by this system for AL_2O_3 layer is less than 1% and the average time of the cycles are about 2 seconds. The WSe_2 samples were transferred to the atomic layer deposition (ALD) chamber directly after exfoliation and annealing at 200 °C in the presence of the argon gas. The system pumped down

immediately to remove the unwanted gases from the deposition chamber. Then, 20 nm Al_2O_3 layer was deposited on top of the flakes by using water as an oxygen source and trimethylaluminum(TMA) as an aluminum source. During the process, the TMA was purged into the chamber by a pulse time of 0.015 s and after 8 seconds waiting the water was also purged into the chamber by a pulse time of 0.018 s. During the hole process 5 SCCM nitrogen gas was purged inside of the chamber as a carrier and venting gas.

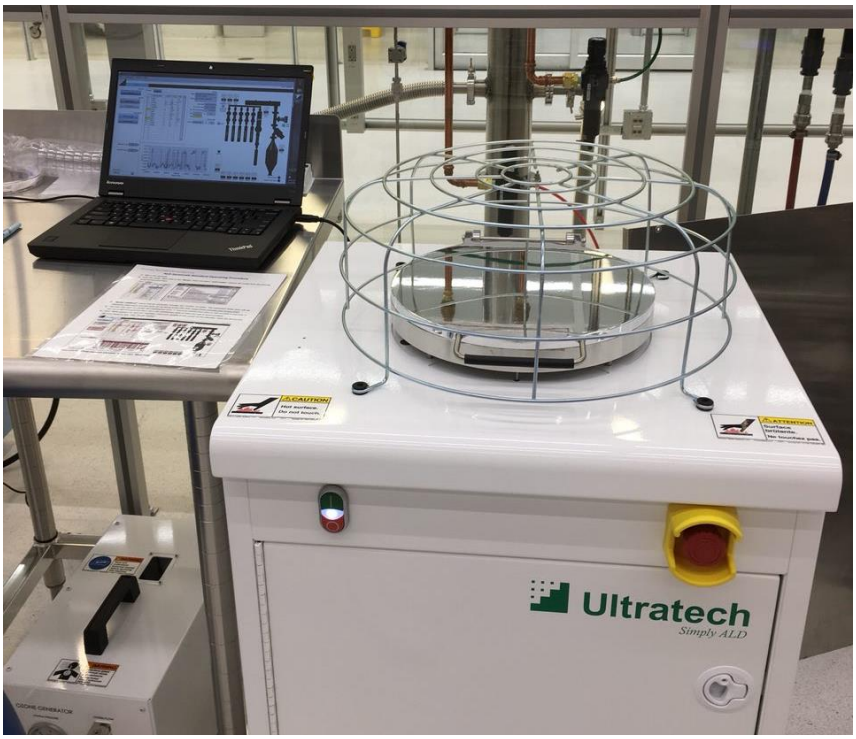

Figure 27. Savannah standard ALD System: ALD system which is used for the deposition of the Al_2O_3 layer on top of the WSe_2 flakes.

Figure 28a shows atomic force microscopy (AFM) image of the Al_2O_3 layer deposited at 150 ℃ on top of the WSe_2 flake. The height profile from the surface of this

flake shows nonuniform deposition of Al_2O_3 layer on top of it with many pinholes which results in instability of the device performance under air exposure. Increasing the temperature of the growth from 150 ℃ to 200 ℃ does not improve the quality of the deposition and results in increasing the nonuniformity of the deposition significantly (Figure 28b).

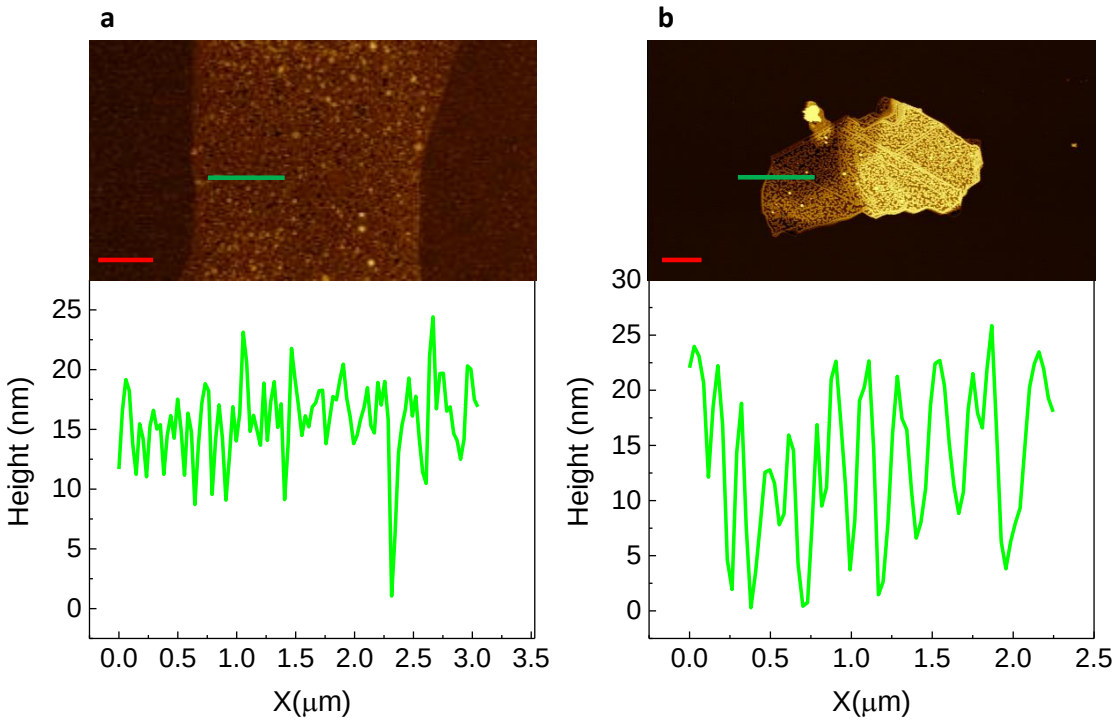

Figure 28. AFM characteristic of Al_2O_3 deposited on WSe_2: AFM image of Al_2O_3 layer deposited on WSe_2 flakes at **(a)** 150 ℃ (scale bar is 0.7 μm) **(b)** 200 ℃ (scale bar is 1 μm)**.**

This nonuniformity of the Al_2O_3 layer can be due to lack of the dangling bonds on the surface of this material[150].Previously to have a uniform deposition of the Al_2O_3 layer , Park et al.[151] have deposited Monolayer of titanyl phthalocyanine (TiOPc) as a seeding layer on the surface of WSe_2 material by molecular beam epitaxy (MBE) method

prior to ALD deposition of the Al_2O_3 layer. Here, instead of using MBE method, we have deposited 1 nm of SiO_x layer as a seeding layer by e-beam evaporation method and then the samples are transferred to ALD chamber for deposition of the Al_2O_3 layer. 20 nm Al_2O_3 layer was then deposited at 150 ℃ with the recipe same as the one which is mentioned for no seeding deposition. The AFM image (Figure 29) from the surface of the WSe_2 flake shows a very uniform deposition of the AL_2O_3 layer with roughness of ~1.5nm.

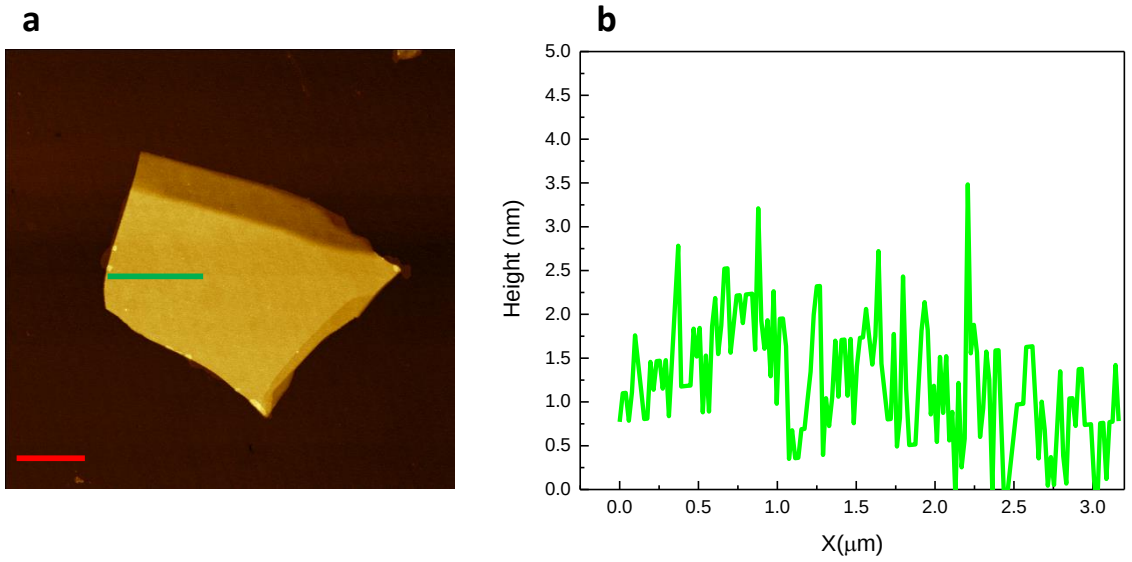

Figure 29. AFM characteristic of Al_2O_3 deposited on WSe_2 with 1nm SiOx seeding layer: (a) AFM image of Al_2O_3 layer deposited on WSe_2 flakes at 150 ℃ after 1 nm deposition of SiO_x seeding layer by e-beam evaporation technique (scale bar is 0.8 μm). **(b)** AFM height profile from the surface of the WSe_2 shown in image (a).

After successful uniform deposition of the AL_2O_3 layer on WSe_2 flake, we deposited 20 nm AL_2O_3 layer on the WSe_2 FET which is shown in figure 25a. Next, we performed

the transfer characteristic measurements on the device in the presence of the air environment to make sure about the stability of the device. The I_d-V_g measurement results are shown in figure 30 at V_{ds}=1V before and after current annealing. The current annealing did not have a significant improvement on the performance of this device and the mobility of the device was almost the same as the mobility of the device in vacuum environment without the passivation layer (Figure 25b). Furthermore, the maximum current of the device at V_g=60 V is decreased by a factor of ~2 compared to the vacuum environment but it is still high enough to be able to run the Raman thermometry measurement. This excellent performance of the device in the air environment after deposition of the AL_2O_3 passivation layer also confirms that 1 nm deposition of the SiO_x layer, as a seeding layer, helped to the uniform deposition of this passivation layer. If it was any nonuniformity on the deposition of the passivation layer, the air molecules could adsorb on the surface of WSe_2 flake and decrease the performance of the FET significantly as it was shown in figure 26.

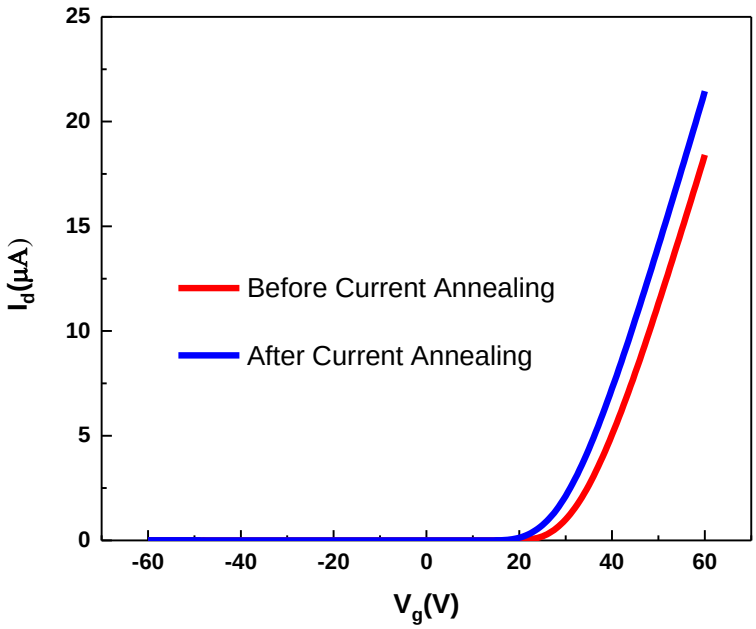

Figure 30. Transfer Characteristic of WSe_2 FET in the air environment: I_d-V_g measurement of WSe_2 FET at V_{ds}=1V in the presence of the air environment.

To establish an electrical connection to the device after the deposition of the AL_2O_3 layer, we need to etch the layer from the gold-pad areas. The Plasma-Therm ICP Chlorine Etch system (Figure 31) was used for this process. 5 sccm Boron trichloride (BCl3) gas was used to etch the Al_2O_3 layer and the power of the system was set at 100 W. 15 sccm argon gas was also flown during the entire process and it took about 6 minutes to etch 20 nm Al_2O_3 layer. Then the sample was wire bonded to the chip carrier for Raman thermometry measurements.

Figure 31. Plasma-Therm ICP Chlorine Etch System. Etching system which is used to etch the AL_2O_3 layer.

Next, The Acton TriVista CRS confocal Raman with 10 µw power and 1.3 µm spot size was utilized to get Raman spectra from the WSe_2 flake at thermal equilibrium condition. Figure 32 exhibits the characteristic Raman peaks of the WSe_2[152] flake with the thickness of ~ 7nm. The E_{2g}^1, A_{1g} and E_{2g}^2 peaks corresponding to the in-plane, out-of-plane and interlayer vibration of atoms respectively.

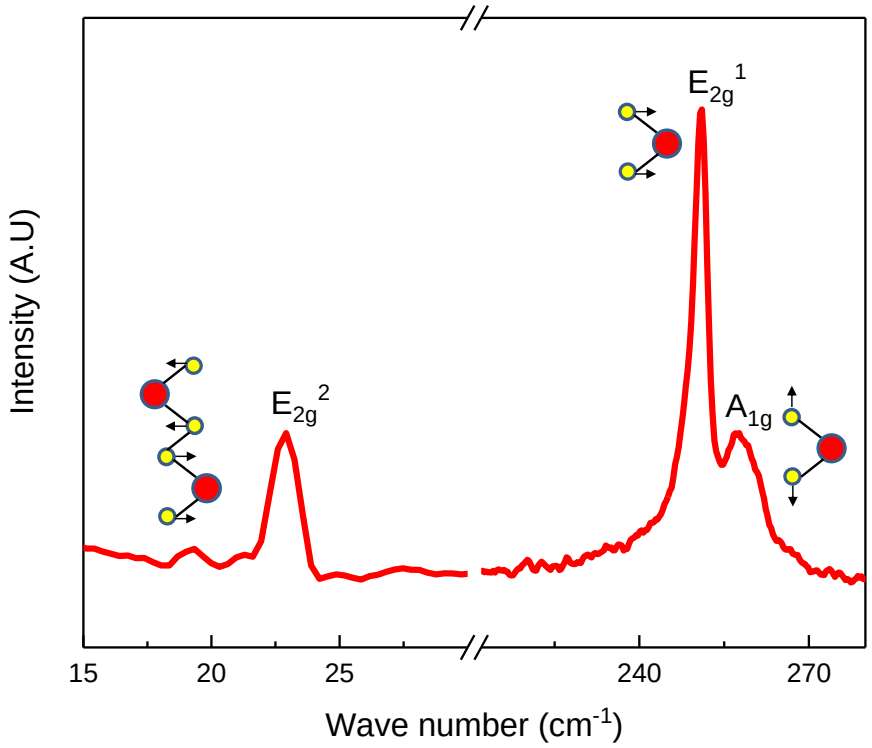

Figure 32. Raman characteristic of WSe_2 flake: Representative Raman peaks of mechanically exfoliated WSe_2 flake with thickness of ~8nm.

Since the temperature of the device will be extracted based on the shift in the Raman peaks, it is important to find out the dependency of the peak shifts to the applied gate voltages. For this, we have applied 60 V gate bias to the WSe_2 FET (shown in figure 25a) while the source-drain bias is kept at 0 V. Figure 33a and b shows the Raman shifts for WSe_2 after applying gate biases (All the peaks were fitted by Gaussian distribution). All the peaks had red shifts by increasing the gate bias. We also wanted to experimentally investigate the temperature distribution of the substrate, which is Silicon wafer. Therefore, the effect of the applied gate bias is also investigated on the silicon Raman peak (Figure 33c). The silicon peak also had redshift. These shifts will be deducted from

the total peak shifts of the device because of the applied electrical power, to deconvolute the effect of the thermal shift from the effect of the carrier concentration shift.

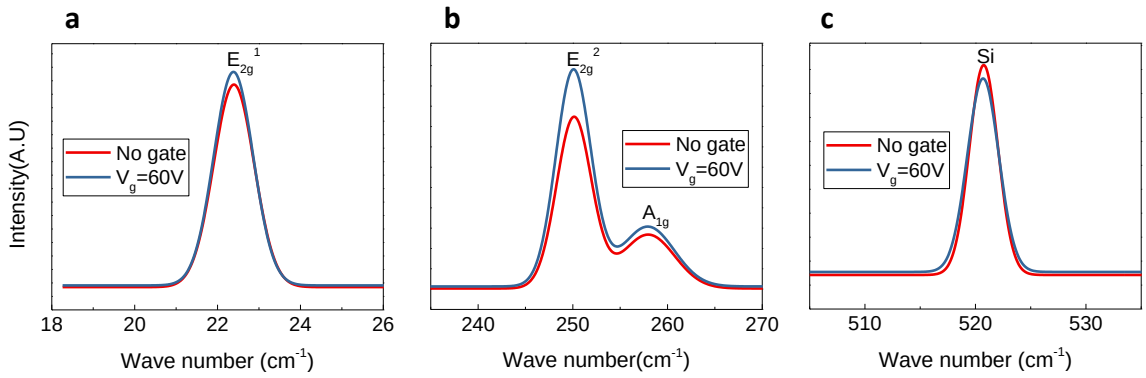

Figure 33. Raman peak shifts because of applied gate bias: Raman peak shift of (a) E_{2g}^1 (b) E_{2g}^2 as well as A_{1g} and (c) silicon peak at V_g=60 V and V_{ds}=1V.

To perform Raman temperature measurement, we first needed to calibrate the Raman peak shift with temperature. To do this, the WSe_2 flake is placed on top of the hotplate and the Raman spectra was acquired at different temperatures. Figure 34a exhibits the temperature dependency of WSe_2 E_{2g}^1 and A_{1g} peaks (the peaks were fitted with Gaussian distribution). This measurement reveals that temperature increase results in not only widening of these two peaks but also reducing the intensity of them significantly. This phenomenon could result in significant error in the thermometry measurements. On the other hand, increasing the temperature did not have any effect on widening of E_{2g}^2 peak (figure 34b) and its intensity was almost constant by increasing the temperature.

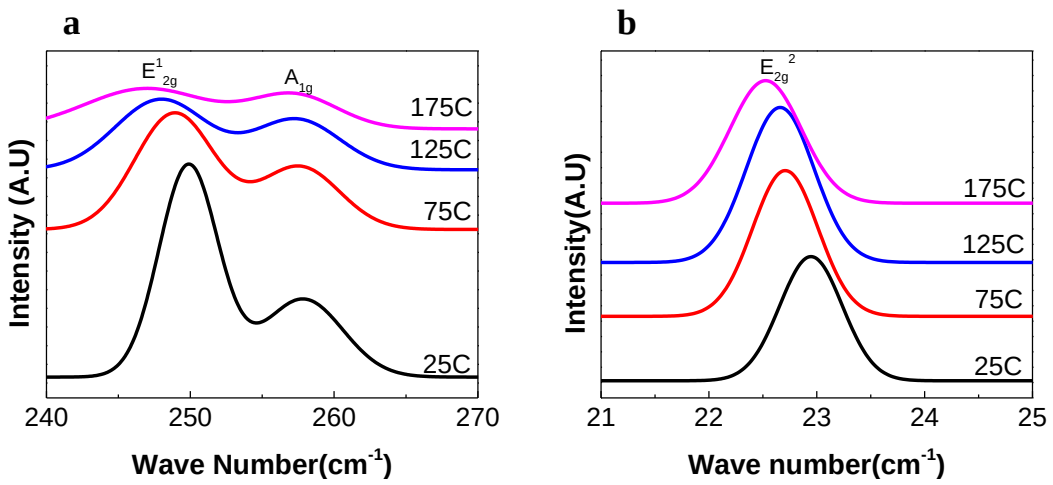

Figure 34. Raman peak shifts VS temp: Raman shifts of (a) $E_{2g}{}^1$ and A_{1g} (b) $E_{2g}{}^2$ peaks of WSe_2 at different temperatures from 25 ℃ to 175 ℃.

Next, we have loaded our WSe_2 FET on top of the hot plate and performed the same measurement to extract the temperature dependency of the peaks. But, this time we only increased the temperature to 125 ℃ to have a better quality of the $E_{2g}{}^1$ and A_{1g} peaks. We have used the laser power of <10 µW with the laser spot size of 1.3 µm. The acquisition and RTD time were set for 20 and 3 seconds respectively. The accumulated data was also averaged by 12 times. Figure 35a show the calibration curve for $E_{2g}{}^2$ WSe_2 Raman Peaks. Also, Raman peak shift of the silicon (figure 35b) is measured. both peaks had redshift by increasing the temperature.

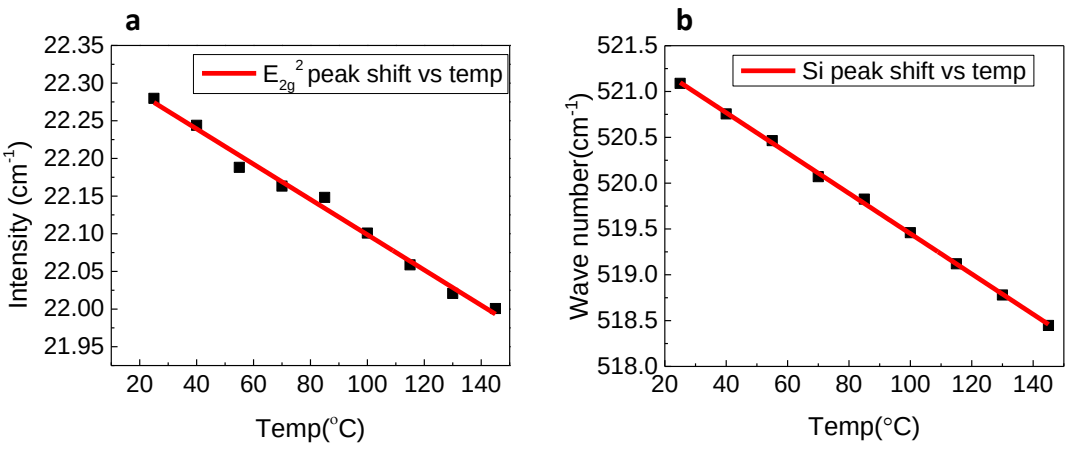

Figure 35. Extracted Raman shift VS temp: $E_{2g}{}^2$ Raman peak shift of WSe_2 FET and (b) Si Raman peak shift of silicon substrate at different temperatures.

To measure the temperature of the WSe_2 FET under the operation, we have mounted the device on the chip carrier and the source-drain voltage was applied to the device by using Keithley source-meter instrument (figure 36).

Figure 36. Optical image of the Keithley source meter.

We have applied different source-drain voltages and measured the current across the transistor channel. The applied power density is calculated based on the formula of P=IV/A where P is power density, I is current, V is the source-drain voltage and A is the area of the device. Here, the channel length and width were 6.5 µm and 8.5 µm respectively (figure 25a). The Raman spectra of the WSe_2 FET and the silicon substrate were acquired simultaneously at each applied power to prevent from any assumption for the temperature of the substrate. As discussed previously, $E_{2g}{}^1$, and A_{1g} peaks of WSe_2 are not appropriate for Raman thermometry measurement due to weak intensity and broadening at elevated temperatures. So, we have plotted the temperature rise of the WSe_2 FET based on $E_{2g}{}^2$ Raman peak shift. Figure 37a and b exhibits the temperature

rise of the WSe_2 FET and silicon substrate based on $E_{2g}{}^2$ Raman peak of WSe_2 and the silicon Raman peak respectively.

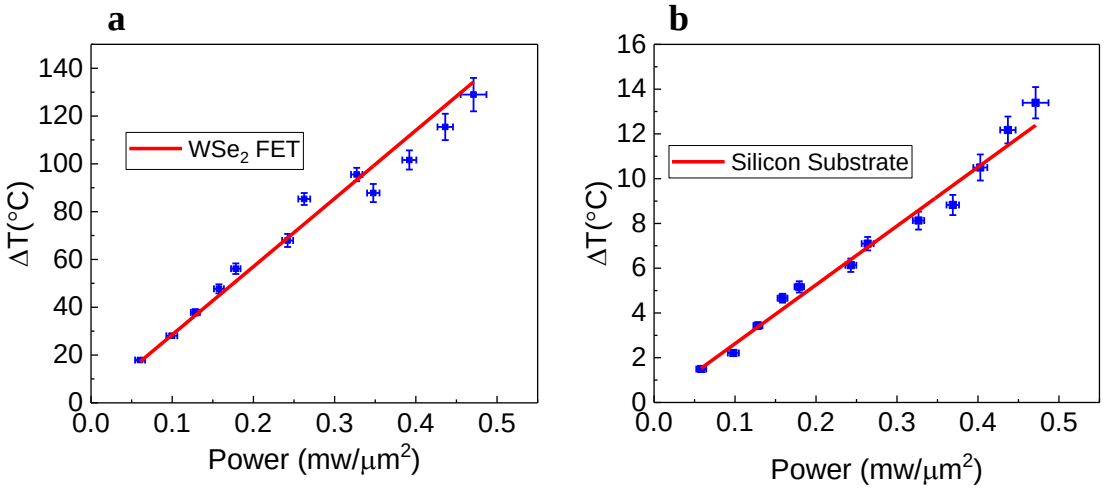

Figure 37. Applied Power VS temp rise: Temperature rise of the (a) WSe_2 FET (b) Silicon substrate versus electrical applied power.

To find out thermal boundary conductance between the WSe_2 flake and the substrate, we considered equivalent thermal circuit from WSe_2 flake to the silicon substrate (Figure38). The total thermal resistance between the hot and cold zones is the sum of the thermal resistances between WSe_2 flake and SiO_2 substrate (R_{int}), thermal resistance of SiO_2 (R_{SiO2}) and thermal resistance of Silicon (R_{Si}). It is worth noting that, the resistance between Si and SiO_2 can be neglected due to the very high thermal boundary conductance between these two layers[96], [153], [154]. The total thermal resistance ($R_{th}=\Delta T/P$) is extracted from the slope of the figure 37a.

The calculated in-plane thermal resistance is 5 orders of magnitude larger than the total out-of-plane thermal resistance measured from the slope of the figure 37a, proving that in-plane power dissipation is negligible in this device. Also the thermal resistance of the silicon substrate can be calculated based on either the slope of the figure 37b [96]or the known value for thermal conductivity of the silicon.

$$R_{si}= \left(\frac{1}{4K_{si}^2 LW_{eff}}\right)^{1/2} \qquad (1)$$

In which K_{si} is the thermal conductivity of silicon, L is the channel length and W_{eff} is the effective width of heat dissipation through the silicon substrate. To calculate the thermal resistance of the SiO_2 layer, the thermal dependency of its thermal conductivity is also considered based on the following formula[156], [157]:

$$K_{ox}=\mathrm{Ln}(T_{ox}^{0.52})-1.687 \qquad (2)$$

In which T_{ox} is the average temperature of the hot zone and cold zone. Then the resistance of the SiO_2 layer is calculated based on formula (3)[156].

$$R_{SiO2}= \frac{1}{L}\left(\frac{\pi K_{ox}}{Ln\left(6\frac{T_{ox}}{W+1}\right)} + \frac{K_{ox}}{T_{ox}}W\right)^{-1} \qquad (3)$$

The resistance of the interface can be calculated based on formula (4).

$$R_{int}= R_{th}-(R_{Si}+R_{SiO2}) \qquad (4)$$

And finally, by knowing the area of the device, TBC can be calculated.

We found that TBC values for six tested devices with the same thicknesses (~7 nm) vary in the range of 10-32 MW/m^{2}K. This value of TBC between the interface of the WSe_2 material and SiO_2/Si substrate is consistent with the recent report on the TBC between MoS_2 material and SiO_2/Si substrate[96] and is an order of magnitude higher than the reported MoS_2 TBC value measured by optical heating[97]–[99]. This difference could be due to the better quality of the interface between WSe_2 material and SiO_2 substrate after the deposition of the Al_2O_3 passivation layer or the challenges in optical heating method such as induced Raman shift as a result of the using high laser powers[96]–[99].

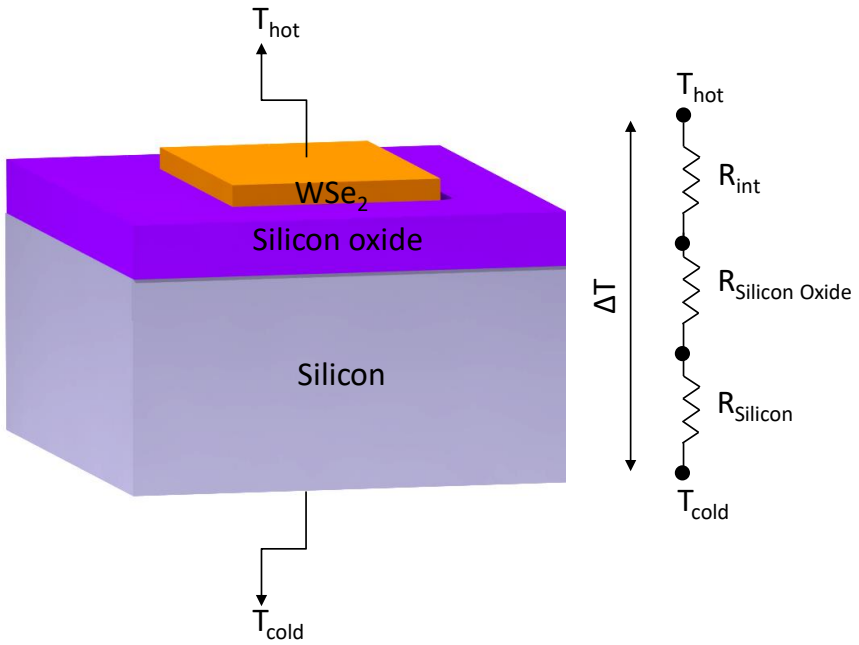

Figure 38. Thermal resistances between hot and cold zone: Schematic image of the device fabricated on SiO_2/Si substrate with its equivalent thermal circuit.

3.3. Summary and conclusion

In summary, we have investigated the power dissipation of the WSe_2 FET under the electrical operation by using the Raman thermometry method. Electrical heating coefficients for E_{2g}^1, A_{1g} and E_{2g}^2 Raman peaks of WSe_2 material is measured and our experimental results reveal that $E_{2g}^1$and A_{1g} Raman peaks of WSe_2 material cannot be used for Raman thermometry due to peak broadening at elevated temperatures. Hence, the E_{2g}^2 Raman peak, which is a very low-frequency peak, is used to measure the operating temperatures for a multilayer WSe_2 FET as a function of the dissipated electrical powers. Also, the measured value for TBC between WSe_2 material and SiO_2/Si substrate reveal that the interface thermal resistance between this material and its substrate is very high and plays a limiting role on the thermal dissipation of the WSe_2 FET. These results show that substrates with higher thermal conductances and better thermal interfaces must be chosen for future 2D-material FETs; otherwise, their performance will be degraded significantly due to the poor thermal dissipation at their interfaces.

CHAPTER 4

QUANTIFYING THE LIMITS OF THROUGH-PLANE THERMAL DISSIPATION IN 2D-MATERIAL-BASED SYSTEMS

(Most parts of this chapter are taken from the published paper with the following citation:

Poya Yasaei, Amirhossein Behranginia, Zahra Hemmat, Ahmed El-Ghandour, Craig D. Foster, Amin Salehi-Khojin "Quantifying the limits of through-plane thermal dissipation in 2D-material-based systems," *2D Mater.*, vol. 4, no. 3, p. 35027, Aug. 2017.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

4.1. Introduction

Through-plane thermal transport accounts for a major fraction of heat dissipation from hot-spots in many existing devices made of two-dimensional (2D) materials. In this report, we performed a set of electrical thermometry measurements and 3D finite element analyses to quantify the limits of power dissipation in monolayer graphene, a representative of 2D materials, fabricated on various technologically viable substrates such as chemical vapor deposited (CVD) diamond, tape-casted (sintered) aluminum nitride (AlN), and single crystalline c-plane sapphire as well as silicon with different oxide layers. We demonstrate that the heat dissipation through graphene on AlN substrate near room temperature outperforms those of CVD diamond and other studied substrates, owing to its superior thermal boundary conductance (TBC). At room temperature, our measurements reveal a TBC of 33.5 $MW.m^{-2}.K^{-1}$ for graphene on AlN compared to 6.2 $MW.m^{-2}.K^{-1}$ on diamond. This study highlights the importance of

simultaneous optimization of the interfaces and the substrate and provides a route to maximize the heat removal capability of 2D-material-based devices.

Since their discovery, two-dimensional (2D) materials have enabled the design of nanoscale devices with unique functionalities that are otherwise unavailable in conventional 3D systems.[9], [105], [158]–[163] In these applications, heat dissipation and thermal management are crucial for the design and operation of 2D nano-devices, in which overheating could lead to premature failure. While 2D materials offer excellent intrinsic thermal properties, the heat dissipation performance of devices based on these materials will be affected by the thermal characteristics of the enabling infrastructures, such as interconnects and substrates as well as their junctions and interfaces.[24], [74], [98], [164]–[177] Thus, a system-level analysis is essential to quantify the thermal dissipation limits in 2D material-based structures to realize their competitive advantage over their 3D counterparts .[75], [79], [166], [172], [173], [178]–[182]

Heat generated in the hot-spots of 2D circuitry generally spreads within the plane of the 2D materials and ultimately dissipates through the substrate and the contact electrodes.[181] The contributions of in-plane and through-plane transport on the overall thermal resistance (R_{TH}) is determined by a combination of geometrical dimensions as well as thermal properties of the materials and interfaces.[169], [181] In many device architectures (e.g., devices with characteristic lengths>100nm), the through-plane thermal transport predominantly defines the R_{TH}.[181] In these cases, optimizing the R_{TH} requires a high-conductance substrate as well as a good thermal interface. One major

challenge is that the heat in high-conductance substrates such as diamond is usually carried by high-frequency phonons which transmit poorly through the Van der Waals interfaces that bind 2D materials.[183], [184] In other words, a practical trade-off seems to exist between the bulk thermal conductivity of existing substrates and the interfacial conductance at their junction with the 2D materials. On top of this criterion, the microscopic details of the interface such as coupling (adhesion) forces, surface roughness, and presence of potential contaminants also affect the thermal boundary resistances (TBRs) and consequently the R_{TH}. Thus, it is necessary to consider all the thermal resistances and their decisive parameters simultaneously in the design of the 2D-based systems, in order to maximize the overall thermal dissipation.

4.2. Results and Discussion

In this report, we utilized an electrical thermometry platform to measure through-plane thermal transport in representative 2D-based devices fabricated on the substrates with the highest available thermal conductances, e.g., CVD diamond (K~1500 $W.m^{-1}.K^{-1}$at room temperature), tape-casted (sintered) aluminum nitride (AlN - K~170 $W.m^{-1}.K^{-1}$), and single crystalline c-plane sapphire (K~31 $W.m^{-1}.K^{-1}$). We note that beryllium oxide (BeO) (K~250 $W.m^{-1}.K^{-1}$) is another high-conductance substrate, but we declined to test it due to its toxicity, which has caused a ban on its use in many industries.[185], [186] We also tested the Si/SiO_2 (270nm oxide thickness) as a reference point for comparison, as it is the most frequently used substrate for devices based on 2D materials. The Si/SiO_2 and sapphire substrates are single crystalline with a surface roughness of <1nm. Diamond

and AlN substrates are polycrystalline and are polished to <10nm roughness. It is worth noting that, we used commercially available CVD diamond and tape-casted aluminum nitride (AlN) substrates with an advertised roughness of <10nm and <1µ-in (~25.4nm), respectively. Optical images of the as-received diamond and AlN substrates are respectively shown in Figure 39a-b. The AFM images of diamond and AlN are also respectively shown in Figure 39c-d and a representative height profile is shown in the insets. Surface analyses show that diamond has a root mean square (rms) roughness of Rq=5.21nm and Rq=3.72nm before and after waviness removal, respectively. AlN is more wavy than rough, as evidenced by Rq=24.6nm and Rq=2.3nm before and after waviness removal, respectively.

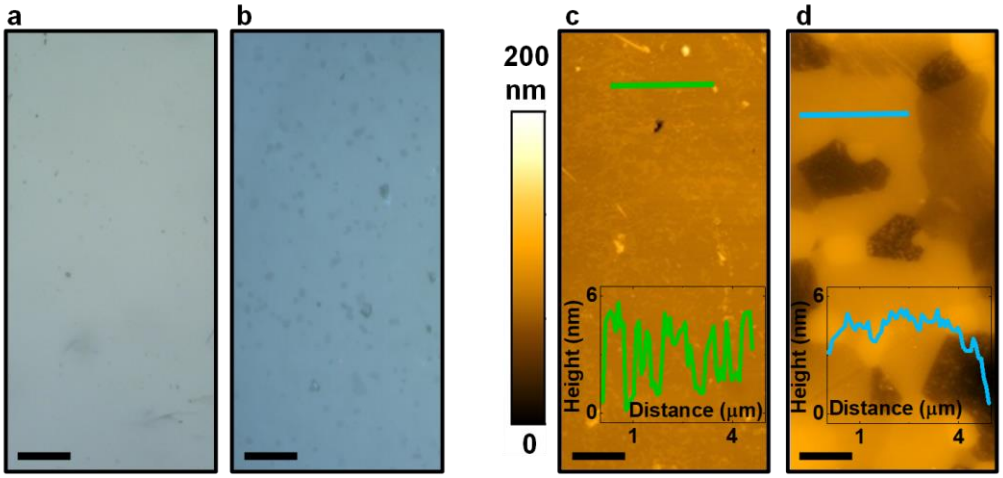

Figure 39. Characterization of Diamond and AlN Substrates. (a-b) Optical image of an as-received diamond and AlN substrates, respectively. The scale bars are 15 µm. **(c-d)** AFM images of the diamond and AlN substrates, respectively. The scale bars are 2 µm. The inset shows the height profile along the green and blue lines. Detailed analyses were performed to quantify the limits of through-plane heat dissipation in the tested devices and to identify the best structure from a thermal management perspective.

We used monolayer CVD graphene as a model for 2D materials throughout this study. The graphene growth process and characterization can be found in our previous reports[115], [187], [188]. After the synthesis of graphene on copper foils, a typical polymer-assisted wet etching process was used to transfer the monolayer flakes to the target substrates[189].For the through-plane thermal transport measurements, we employed a serpentine-shape electrical thermometry platform, as shown in Figure 40.

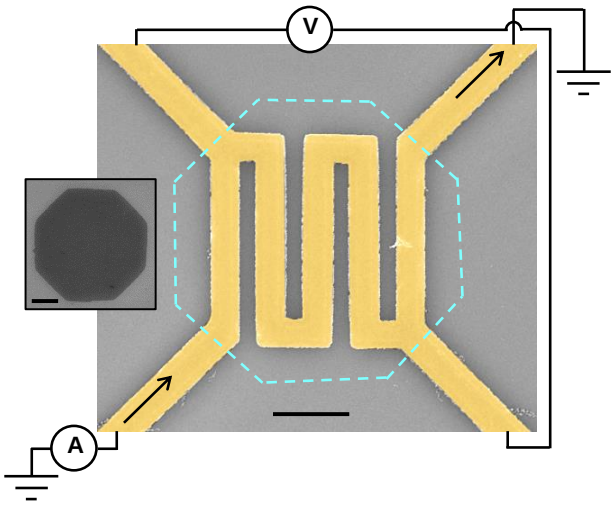

Figure 40. SEM image of the electrical thermometry platform: False-Colored scanning electron microscopy (SEM) image of the thermometry platform. The inset shows the graphene flake defined into a symmetric octagon before electrode patterning/deposition and plasma etching. The dashed lines indicate the graphene borders under the metal electrodes. The scale bar is 2μm.

The thermometry experiments were performed in a cryogenic refrigerator (Janis LLC, model: CCS-450) in high vacuum (~10-7 mbar). The system has a nominal temperature reading error of 0.01 K and an operating temperature range of 10 to ~450 K.

The temperature drift between the cold finger and the tested chips is measured to be negligible down to 35K, using vacuum compatible grease and conductive epoxy. In the thermometry experiments, the temperature of the cold finger is used as the cold source temperature (TC) and the temperature reading using the heater/sensor thermometry electrode is used as the hot source temperature (TH). Due to small thermal capacity of the platform, the transient time constants are in the order of few seconds, hence, a 100s measurement duration is enough to assure steady-state heat transport conditions. In our measurements, the uncertainty of the measured temperature is less than 50 mK in all the tested structures, as measured by the fluctuations in the measured resistance and the calibration coefficient.

The resistance of the four-probe heater/sensor electrode, which is patterned on a monolayer graphene (or a bare substrate for control experiments), was initially calibrated at different temperatures (25K to 295K) (inset of Figure 41a). The base temperature is then held constant and various levels of electrical power (Joule heating) were applied to the platform, while the resistance was being monitored (Figure 41a shows a representative dataset for graphene on SiO_2/Si with 270nm oxide thickness). Using the calibration data in Figure 41a, the change in the resistance was used to precisely measure the temperature rise (ΔT) of the platform at different applied powers (P) (Figure 41b). The slope of the ΔT versus P plot represents the overall thermal resistance (R_{TH}) to the environment. The R_{TH} characterizes the temperature rise of the device at a given applied power and determines how efficiently a certain structure can dissipate the heat from the

electrode. In our measurements, the structure consists of a monolayer graphene sheet capped with an Au/Ti (50/5 nm) electrode and supported by different substrates. The temperature-dependent R_{TH} values of these structures with graphene are shown in Figure 41c (Unit: K/mW - Kelvin per milliwatt). The error bars in Figure 41c represent the standard deviations of at least 3 measurements in identical conditions (same in all R_{TH}-T plots hereafter). As shown in Figure 41c, the highest R_{TH} throughout the temperature range is obtained for the Au/Ti/Gr/SiO_2/Si (270nm oxide) structure, which increases from 8.72 K/mW at 295K to 15.55 K/mW at 85K. Remarkably, the lowest R_{TH} values near the room temperature are recorded for the Au/Ti/Gr/AlN structure (1.75 K/mW at 295K). At low temperatures, the Au/Ti/Gr/Sapphire stack provides the lowest R_{TH} (1.77 K/mW at 85K).

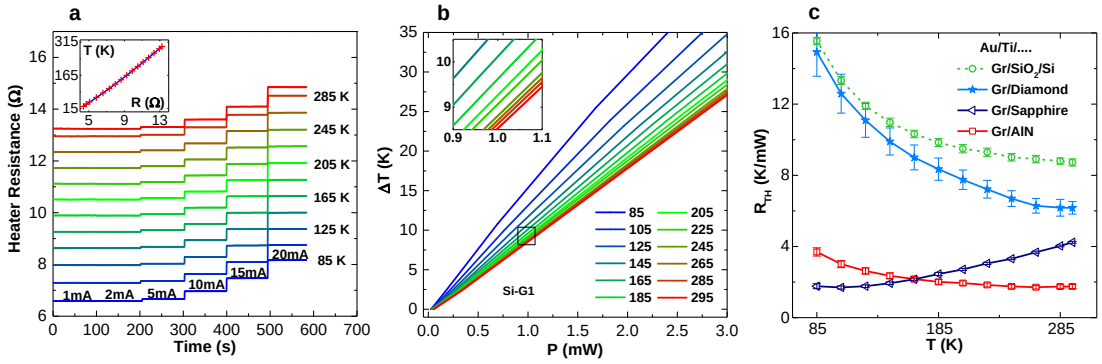

Figure 41. Thermometry measurements on different substrates: (a) Hyperspectral data for the electrical resistances of the heater versus time at different temperatures and applied powers. The inset shows the calibration curve with a 3rd order polynomial fitting. **(b)** The temperature rise (ΔT) versus applied power (P) at different base temperatures. **(c)** Temperature-dependent overall thermal resistance to the environment (R_{TH}) of the tested structures. The error bars indicate the standard deviation of at least 3 experiments in identical conditions.

For all the tested structures incorporating a monolayer graphene in this work, we have also performed a control experiment in which the metal electrodes are directly deposited on the substrates. Supplementary Figure 42 shows the full data set for the R_{TH} and extracted TBC values for the diamond, sapphire, AlN, and Si/SiO_2 (270nm) substrates. It is noteworthy that the R_{TH} for the Au/Ti/Gr/Diamond structure is quite large, despite the very high lattice thermal conductivity of diamond. For the Au/Ti/Diamond stack (control experiment), the R_{TH} at 295K is ~1.78 K/mW, which increases to 5.41 K/mW at 85K. For the Au/Ti/Gr/Diamond stack, the R_{TH} is 6.17 K/mW and 14.93 K/mW at 295K and 85K, respectively. This enormous surge in the R_{TH} upon incorporating the graphene monolayer in the stack implies that the thermal boundary resistance (TBR) significantly contributes to the R_{TH} of the Au/Ti/Gr/Diamond structure.

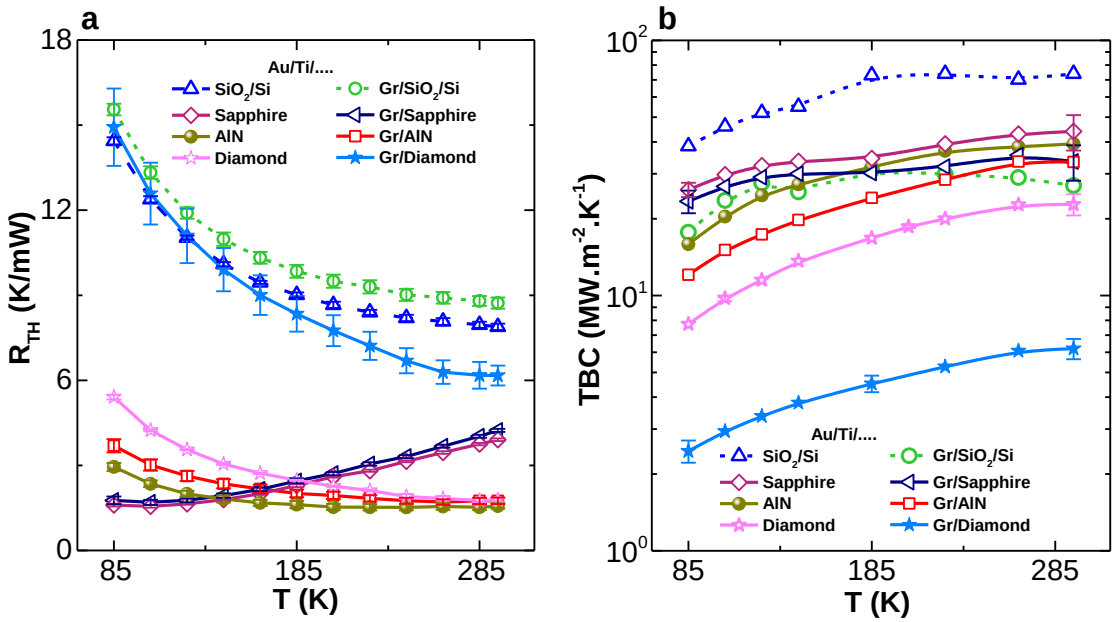

Figure 42. Experimental data for the R_{th} and TBC of tested substrates: (a) R_{TH} and **(b)** TBC for the diamond, sapphire, AlN, and Si/SiO_2 (270nm) substrates at the temperature range of 85-295K.

To extract the interfacial thermal properties of these structures, the thermometry results are analyzed in a 3D finite element (FE) model with the exact geometrical dimensions of the fabricated platform. In the FE model, we used the previously measured thermal conductivity of the materials[172], [190]–[193] as input parameters and iteratively matched the lumped thermal boundary resistance (TBR) between the metal electrode and the substrate. Figure 43a shows the calculated effective thermal conductivity of the Au/Ti metal electrode. We used an average Lorentz number L = 2.7×10^{-8} $W.\Omega.K^{-2}$ in the Wiedemann-Franz law[172], [193] to obtain the thermal conductivities shown in Figure 43a. Figure 43b shows the thermal conductivity values

for single crystalline Si and sapphire substrates which are respectively obtained from the reports by Glassbrenner *et al.*[191] and Dobrovinskaya *et al.*[192]. For the thermal conductivity of SiO_2 layer, the report by Bae *et al.*[172] is used (Figure 43c). For the CVD diamond (Figure 43d), the thermal conductivity data from Hebei Co. (manufacturer of the diamond substrates used in this study) in the range of 298 – 433 K is extrapolated down to 200 K using the trends in the report by Vandersande *et al.* (1994)[190] for diamond with the closest thermal conductivities. It worth noting that the sensitivity of the extracted TBCs for diamond experiments to the thermal conductivity of the diamond are found to be very low (weak function) because the diamond substrate resistance has a very minor contribution on the overall R_{TH}. Hence, the error in the extrapolation would not notably affect the extracted TBC values. This allowed us to further extrapolate the trends down to 75K (in Orange) and still the overall uncertainty in the extracted TBC values remain less than 3%, considering ±500 $W.m^{-1}.K^{-1}$ uncertainty for the diamond thermal conductivity in low temperatures. Regarding the bulk aluminum nitride (AlN), Figure 43e shows the available data for pure AlN by Slack *et al.*[194] as well as the data for AlN-170 (used in this study) by Toshiba Corp. published in 1989. For aluminum oxide thin films by ALD, since a reliable temperature-dependent data was not found in the literature, we directly used our experiments to estimate the thermal conductivity. In more details, we attributed the difference in the R_{TH} of the control experiment data on Si/Al_2O_3 (12nm) and Si/Al_2O_3 (25nm) to the 13nm difference in the oxide thickness. Knowing the geometry of the device, the K at different temperatures are calculated and shown in

Figure 43f. These values are slightly higher than the sputtered amorphous Al_2O_3 thin films measured by Lee *et al.*,[195] but the temperature-dependent trends are very consistent.

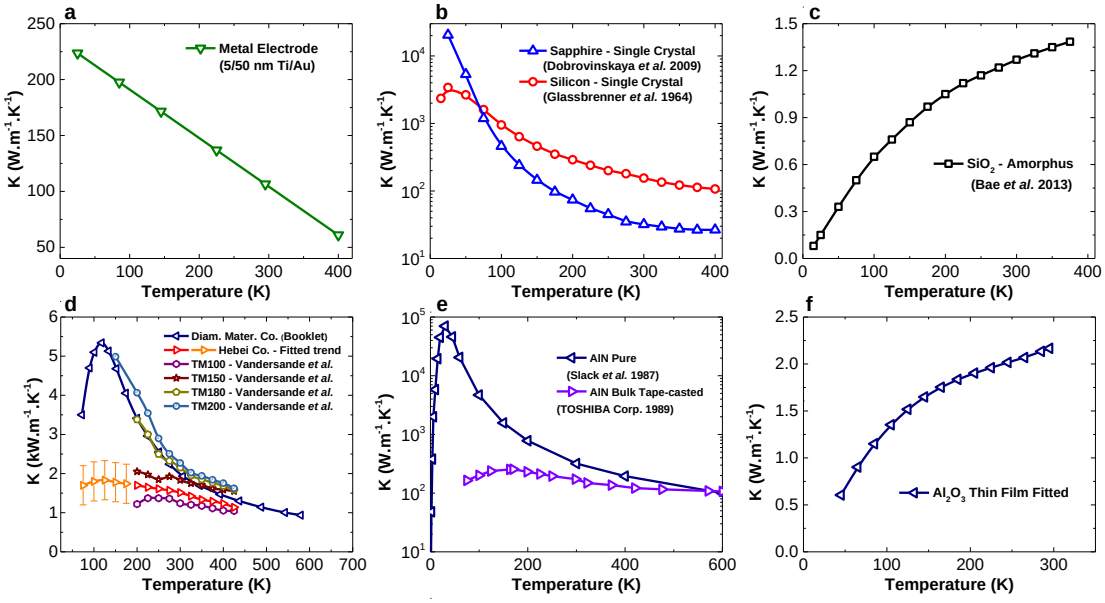

Figure 43. Thermal conductivities of the materials vs. temperature: (a) Metal electrode through Wiedemann-Franz law[172], [193], **(b)** Silicon[191] and sapphire[192] single crystals, **(c)** Silicon oxide[172] (SiO_2), **(d)** Diamond[190], **(e)** Aluminum nitride[194] (AlN), **(f)** Aluminum oxide (Al_2O_3) thin film.

Figure 44a shows the temperature distribution of a representative FE model for the Au/Ti/Gr/SiO_2/Si stack (270nm SiO_2 thickness) at 2mW applied power at 295 K. Figure 44b exhibits the extracted TBC values for the tested structures. For the case of Au/Ti/Gr/SiO_2/Si the TBC at 295K is 27 $MW.m^{-2}.K^{-1}$, nearly half of the TBC for the Au/Ti/SiO_2/Si stack (74 $MW.m^{-2}.K^{-1}$). These values are consistent with the well-established results by Koh *et al.* on the same structures using time-domain

thermoreflectance (TDTR) technique.[173] In our measurements, the highest TBC at 295K was obtained for the sapphire and AlN substrates (~33.5 $MW.m^{-2}.K^{-1}$). Sapphire also exhibits the highest TBC at low temperatures (23.4 $MW.m^{-2}.K^{-1}$ at 85K). The lowest values of TBC in the tested temperature range were obtained for the Au/Ti/Gr/Diamond stack (6.2 $MW.m^{-2}.K^{-1}$ at 295K and 2.46 $MW.m^{-2}.K^{-1}$ at 85K). The TBC for the Au/Ti/diamond stack is also the lowest among the tested control samples (22.78 $MW.m^{-2}.K^{-1}$ at 295 and 7.74 $MW.m^{-2}.K^{-1}$ at 85K). This is in agreement with the previously reported metal/diamond TBC values[169], [183]. The low TBC in diamond interfaces is attributed to the very high Debye temperature of diamond (2200K), which is highly mismatched with most of the metals and the 2D materials (in the out-of-plane direction)[183], [184], [196]. This imposes serious challenges for the use of diamond for thermal management in 2D-based applications.

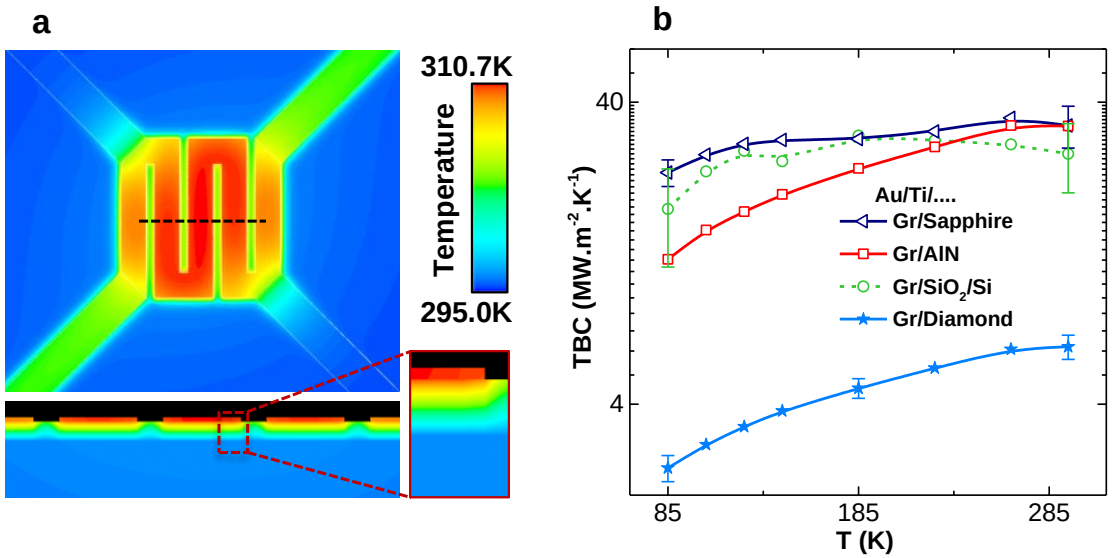

Figure 44. FE Analysis: (a) The top- and side-view of the temperature distribution of the Au/Ti/Gr/SiO_2/Si stack (270nm SiO_2 thickness) in the finite element (FE) model at 2mW applied power and at 295K base temperature. **(b)** Thermal boundary conductance (TBC) of the tested structures at different temperatures extracted from the FE analyses. The error bars represent the overall uncertainty of the measurements.

In Figure 44b, the error bars of the selected data points represent the overall uncertainty of the extracted TBCs, obtained through an analysis based on the partial derivative method[116], [172]. First, the sensitivities of the TBC to different input parameters were individually calculated by applying a small perturbation (∂x_i) to each of the parameters around its center value (x_i) and extracting the change in the TBC (∂TBC) by running the FE simulation:

$$s_i = \frac{x_i}{TBC}\frac{\partial TBC}{\partial x_i} \qquad (1)$$

Table 1. Uncertainty analysis for the TBC of the Au/Ti/Gr/SiO2/Si stack (270nm) at 85K.

Input	Units	x_i (values)	u_{xi} (errors)	u_{xi}/x_i (%)	s_i	$c_i = \lvert s_i \times u_{xi}/x_i \rvert$	$(c_i)^2 / \Sigma(c_i)^2$ (%)
R_{TH}	K/mW	15.55	0.20	1.31 %	6.64	0.00761	5.94
K_{Metal}	W/m/K	197.6	10	5.06 %	0.378	0.000366	0.28587
K_{SiO2}	W/m/K	0.56	0.03	5.36 %	5.654	0.09174	71.61
K_{Si}	W/m/K	1301	50	3.84 %	0.0122	2.198×10^{-7}	0.000172
R_B (Metal-SiO_2)	m^2.K/W	3.8×10^{-8}	2.5×10^{-8}	64.94%	0.0122	6.274×10^{-5}	0.049
δ_{Metal}	nm	55	2	3.64 %	0.3476	0.00016	0.125
δ_{SiO2}	nm	270	10	3.7 %	4.5316	0.02817	21.99
$W_{electrode}$	nm	950	20	2.11 %	Neglected	N.A.	N.A.
$L_{electrode}$	nm	6850	20	0.29 %	Neglected	N.A.	N.A.

This process has been done for all the thermal, geometrical, and experimental parameters involved in the TBC extraction process. The overall uncertainty (u_{TBC}) is obtained using the following equation:

$$\frac{u_{TBC}}{TBC} = \sqrt{\sum_i \left(s_i \times \frac{u_{x_i}}{x_i}\right)^2} \qquad (2)$$

where u_{x_i} is the uncertainty of the ith parameter around its typical value (x_i) and s_i is the sensitivity to that particular input. A representative set of uncertainty analysis for the Au/Ti/Gr/SiO_2/Si stack (270nm oxide thickness) at 85K is provided in Table 1, showing different input parameters and their individual errors and calculated sensitivities. The absolute and relative contributions of each parameter to the overall uncertainty of the TBC was also calculated and respectively shown in the last two columns of the table.

As shown in Figure 44b, the largest uncertainty ($\frac{u_{TBC}}{TBC}$) was found to be 35.79% for the Au/Ti/Gr/SiO_2/Si stack at 85K. However, in higher conductance substrates and at higher temperatures, the uncertainty becomes smaller, e.g., 9.16% for Au/Ti/Gr/Diamond and 15.85% for Au/Ti/Gr/Sapphire structures at 295K.

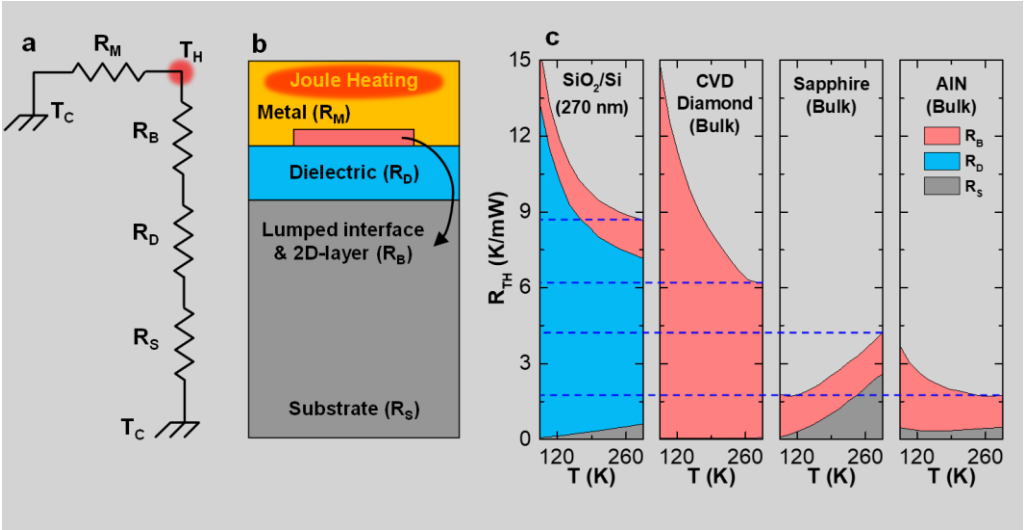

Figure 45.Thermal circuit analyses for the tested substrates: (a) The equivalent thermal circuit of the fabricated platform. The metal resistance (RM) is parallel to the through-plane resistance which consists of the TBR (RB), dielectric resistance (RD - if present), and substrate resistance (RS). **(b)** Schematic side-view of the test structure. **(c)** Accumulative plots of RTH for the tested structures. The dashed lines provide eye guidance for a comparison of RTH at 295K.

To better identify the bottlenecks of heat dissipation in these structures, we modeled the thermometry platform with an equivalent thermal circuit, as shown in Figure 45a along with the schematic side view of the device (Figure 45b). The structure is modeled as an in-plane resistance through the metal electrodes (R_M) acting in parallel to the through-plane overall dissipation resistance. In the through-plane direction, the TBR (here noted as R_B), the dielectric resistance (R_D - if present), and the substrate resistance (R_S) act in series. It is worth noting that the serpentine-shape thermometry platform is designed in such a way that the in-plane conduction through the voltage leads (low-power electrodes) accounts for <2% of the overall heat dissipation ($R_M >> R_B+R_D+R_S$). Thus, the generated heat in the electrode predominantly transfers across the interface and

through the substrate, and the in-plane dissipation through the electrodes can be neglected. Knowing the geometry and the bulk/interfacial thermal properties in the tested devices, the values of R_B, R_D, and R_S are calculated and shown in Figure 45c. For the Au/Ti/Gr/SiO_2/Si stack, the R_{TH} at 295K is comprised of 17% R_B, 76% R_D, and 7% R_S. At 85K, the values for R_B, R_D, and R_S are 14.5%, 85%, and 0.5%, respectively. For the Au/Ti/Gr/Diamond stack, the R_S is negligible and the R_{TH} is mainly contributed by the R_B (~99%). In the sapphire stack, the R_S at 295K is the largest among other stacks, but the R_{TH} remains relatively small owing to a decent interface conductance. The results for the AlN stack are remarkable, because it provides the lowest R_{TH} among the tested structures.

We note that the applicability of the AlN substrate is limited to devices that do not require a back-gate for operation. Moreover, the fabrication process on AlN substrate is more difficult (due to a poor metal adhesion) compared to the substrates with sub-nanometer roughness such as Si/SiO_2 and sapphire. Silicon substrate is also preferred in many industries due to its abundance, low cost, and availability of developed fabrication recipes. From a thermal transport perspective, Figure 45c shows that R_S for the silicon substrate (with K~150 $W.m^{-1}.K^{-1}$) is a tiny fraction of R_{TH}, while a major contribution comes from the R_D. A prospective approach to improve the overall heat dissipation is to reduce the thickness of SiO_2 or deposit dielectric thin films with higher thermal conductivity. There is a wide range of different dielectric materials that can be reliably deposited on silicon wafers to potentially deliver desirable thermal and electrical

properties[197]. Finding the best choice of the dielectrics for a given 2D material requires an extensive survey of materials, which lies beyond the scope of this work. Here, we investigate the possibility of reducing the R_{TH} by using thinner dielectrics of highest practicality. We chose the thermally-grown SiO_2 (thickness of 22 and 29nm) and atomic layer deposited (ALD) aluminum oxide (Al_2O_3) (thickness: 12 and 25nm) thin films. SiO_2 has proven to form an excellent insulator with a high quality interface with silicon[197], [198]. Al_2O_3 is also a widely used alternative to SiO_2 with higher permittivity[199].

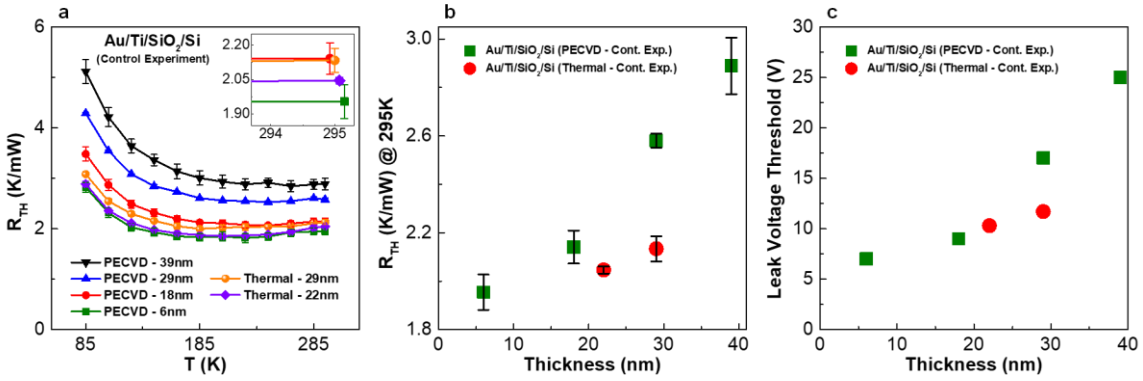

Figure 46. control experiments for thinner oxide layers: (a) R_{TH} for different Si/SiO_2 samples deposited by PECVD or grown by thermal dry oxidation with respect to temperature. **(b)** R_{TH} at 295K with respect to oxide thickness **(c)** The leakage voltage threshold for different Si/SiO_2 samples.

On these substrates, we performed thermometry measurements on bare substrates (control experiment) as well as graphene stacks. Figure 46a compares the R_{TH} of control experiments on Si/SiO_2 substrates in which the oxide is either deposited by plasma-enhanced CVD (PECVD) method or grown by dry oxidation. The PECVD SiO_2 samples

were initially examined to estimate the minimum required thickness to prevent the electrical leakage to the underlying silicon. The PECVD samples have oxide thicknesses of 6, 18, 29, and 39 nm. The dry oxidation samples have oxide thicknesses of 22 and 29 nm. We also tested the R_{TH} (control experiment) in these structures (Figure 46a). As shown in Figure 46b, the R_{TH} of the control experiments (Au/Ti/SiO_2/Si stack) almost linearly decreases as the SiO_2 thickness is reduced. It is clear that the thermally grown oxides have lower R_{TH}. Electrically, current-voltage (I-V) experiments across the deposited oxide layer show a negligible ($<10^{-10}$ nA) leakage current at applied voltages smaller than a certain threshold (herein called: leakage threshold voltage) followed by a sudden increase in the current at higher applied voltages (Figure 46c). These experiments show that even 6 nm of PECVD SiO_2 can effectively prevent leakage current up to ~7V which is sufficient to induce a large charge carrier density of $\sim 2.52\times10^{13}$ cm^{-2} in the gated 2D material (assuming zero threshold voltage).

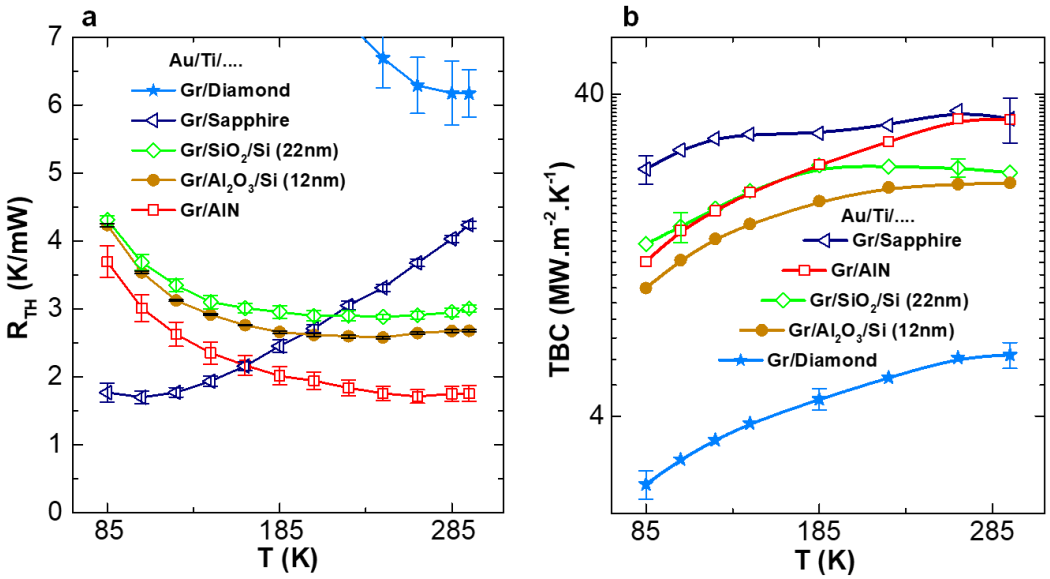

Figure 47. Thermometry measurements of graphene stacks on silicon substrate with different oxide thicknesses: (a) R_{TH} and **(b)** TBC versus Temperature results of Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) stacks along with the graphene stack results on sapphire, AlN, and diamond substrates. The error bars in (a) indicate the standard deviation of >3 experiments in identical conditions. The error bars in (b) shows the uncertainty of the extracted TBC values.

Figure 47 shows the R_{TH} measurements and TBC extractions for the Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) stacks at different temperatures along with the graphene-stack results on diamond, AlN, and sapphire. The R_{TH} of Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) structures at 295K are 3.00 K/mW and 2.68 K/mW, respectively (Figure 47). The values are still higher than those of AlN structure, but are far lower than the case of diamond and Si/SiO_2 (270nm). Figure 47b shows the extracted TBC values of the graphene stacks on silicon substrates. At 295K, the TBC for Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) structures

are respectively 22.8 and 21.2 $MW.m^{-2}.K^{-1}$, which reduce to 13.7 and 10 $MW.m^{-2}.K^{-1}$ at 85K. These values are also lower than the TBC on AlN and sapphire substrates. Overall, our results suggest that thin oxide substrates provide a competitive thermal dissipation performance for devices that require a back-gate. However, AlN shows the best through-plane heat dissipation performance near room temperature among the tested structures. The full datasets for the control experiments and graphene stacks on silicon substrates with thin oxides are displayed in Figure 48.

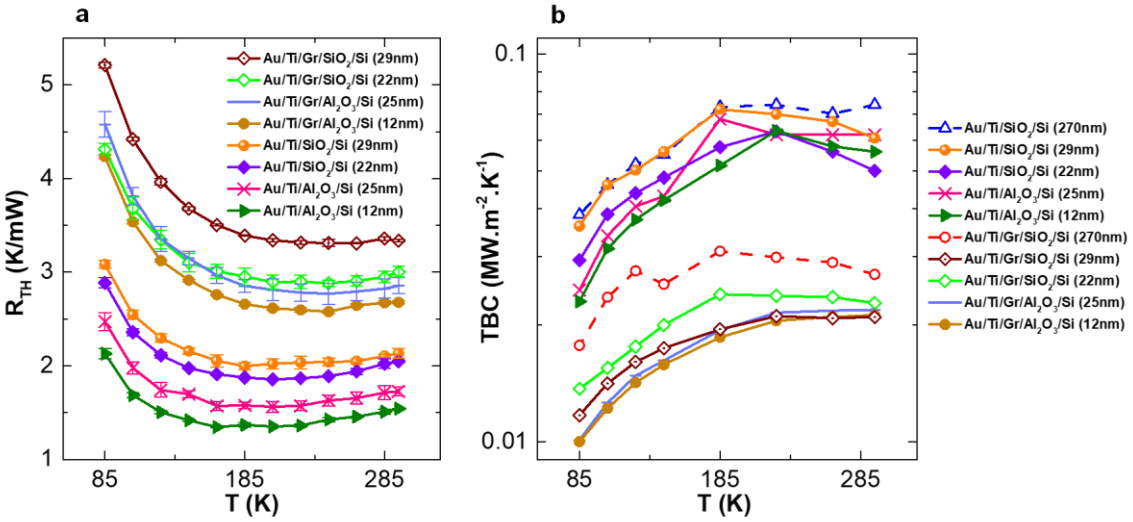

Figure 48. The full dataset for the thermometry measurements on silicon substrate with different oxide thicknesses. (a) R_{TH} and (b) TBC for different test structures on thin oxides at the temperature range of 85-295K. The TBC curves are plotted against the data for Si/SiO_2 (270nm) for comparison.

In a different presentation, Figure 49 demonstrates the R_{TH} values at 295K with respect to TBC. The solid lines show the trends predicted by the FE analyses and the symbols indicate the experimentally obtained data points. This figure demonstrates the

importance of substrate conductance and TBC on the R_{TH} in the tested structures. It is observed that for high-conductance substrates (i.e., thin oxides on silicon, AlN, and diamond), the TBC is the bottle-neck of dissipation. This implies that further improvement of the substrate thermal conductance would not lead to a significant reduction in the R_{TH}, unless the TBC is improved. For instance, the AlN substrate provides lower R_{TH} than diamond due to a superior TBC where the impact of substrate conductance is insignificant. This figure also visualizes the shift in the TBC upon incorporation of a graphene monolayer in the stack. For instance, although the control experiment TBC for AlN is lower than those of thin oxides, but the TBC after addition of a graphene is greater, leading to a lower R_{TH}.

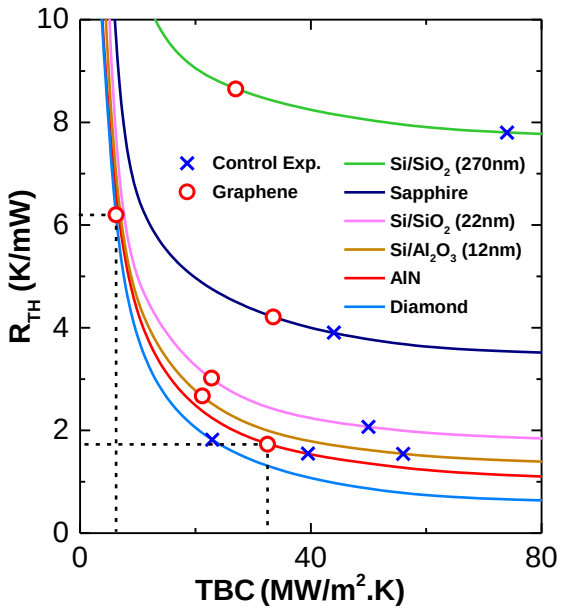

Figure 49. Dependence of the R_{TH} on the TBC for all the tested structures: The solid lines show the trends obtained from FE analyses and the symbols represent the experimental data. The dashed lines compare the R_{TH} and TBC between the Au/Ti/Gr/Diamond and Au/Ti/Gr/AlN stacks.

4.3. Details of Material Synthesis, Device Fabrication and FE Simulations

4.3.1. Graphene growth procedure

Monolayer graphene films were grown by CVD process, similar to our previous reports.[115], [132], [187] In this process, copper foils were initially cleaned in 10% hydrochloric acid, acetone, and isopropyl alcohol and then loaded in the CVD chamber after drying under nitrogen flow. The chamber is then evacuated and refilled with forming gas (5% hydrogen in argon) to atmospheric pressure. The growth takes place for ~90 minutes at 1050°C by introducing 20 ppm methane into the inlet flow using precise mass flow meters. The chamber is then cooled to room temperature using forced convection. The graphene films were transferred to the test substrates using the conventional polymer-assisted method.[200], [201] Combination of Raman spectroscopy and atomic force microscopy characterizations show that the graphene films are monolayer.

4.3.2. Device Fabrication

After the transfer processes, the substrates were cleaned and annealed at 300 in °C for 3 hours in presence of forming gas. A clean area was then selected by SEM for fabrication of the thermometry platform through standard electron beam lithography (EBL), oxygen plasma etching, and electron-beam metal evaporation deposition processes.

4.3.3. FE Simulation

The commercial software ANSYS was used for the FE analyses. The 3D model has a lateral size of 100x100 μm^2 with a thickness of ~50 μm and is comprised of ~$2x10^5$ elements (element: Solid70). The geometry exactly follows the fabricated devices (obtained from SEM images within 5% error). The mesh size is refined and the convergence of the results is tested. A constant temperature is applied to the back and side surfaces of the model and the top surface is isolated. The Joule heating is modeled as a volumetric heat generation in the high-current electrodes. The average nodal temperature rise of the electrode (between voltage leads) at different powers is obtained from the steady-state thermal solution. In several iterations, the TBC is found in such a way that the experimental and modeled temperature rise is matched within 0.5% error.

4.4. Summary and Conclusion

In summary, we studied the thermal dissipation across monolayer CVD graphene as a representative 2D materials on different technologically-viable substrates having a wide range of thermal conductances and interfacial properties. We systematically quantified the contributions of the interfaces and substrate resistances on the overall thermal dissipation resistance to the environment (R_{TH}), which is essential for the design of electronic circuitry from a thermal management perspective. Our results indicate that the overall thermal dissipation performance of monolayer graphene on AlN substrate can rival that of diamond and silicon substrate (even with thin oxides) as a result of a superior

TBC. This study reveals that the TBC of monolayer 2D materials on high-conductance substrates is the bottle-neck of power dissipation, while the role of substrate conductance is insignificant.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

This research has demonstrated the synthesis of some members of the 2D-materials and their in-plane heterostructures by the CVD method and has investigated their electrical and thermal properties.

One of the main goals in this thesis was to synthesize the lateral heterojunction of the graphene and MoS_2 through the CVD method for large-scale production and flexible electronic systems. Temperature-dependent electrical characterization of this heterostructure shows Ohmic behavior at back-gate voltages above 60 V, resulting in an order of magnitude higher extrinsic mobility for this in-plane heterostructure compared to conventional metal-contact MoS_2 devices. The 1/f noise measurement was also performed on this heterostructure for the first time, and it reveals that mobility fluctuation is the dominant mechanism of the noise in the accumulation region. Also, an order of magnitude lower noise amplitude is measured for this device as compared to MoS_2-metal devices fabricated under similar conditions. Furthermore, the electrostatic breakdown measurements for MoS_2-graphene and MoS_2-metal devices exhibit comparable current density and breakdown fields, and similar failure modes. The Kelvin Probe Force Microscope (KPFM) study was performed to map the surface potential distribution across the MoS_2-graphene interface under applied source-drain and gate voltages. The study visualizes the reduction of the MoS_2-graphene interface resistance at positive gate voltages. Also, DFT calculations reveal that the role of this interface

resistance is less than 1% of the overall device resistance at gate voltages above 60 V. In addition, these calculations show that both the barrier at the interface and the resulting interfacial resistance decrease as sheet charge is increased in response to the external gate voltage.

The discovered 2D-materials are very promising to be used for future nanotransistors due to their unique mechanical, physical, and chemical properties at their atomic thicknesses. The thermal management of these nanotransistors is going to be a formidable challenge which needs a comprehensive study. In this thesis, the power dissipation of the WSe_2 FET, as a representative of the 2D-materials, is investigated by the Raman thermometry method to determine the average temperature rise of this device under operation and the role of the interface resistance between WSe_2 material and its substrate. For this study, the WSe_2 FET is made from the mechanically exfoliated WSe_2 material transferred to the silicon substrate with 300 nm oxide thicknesses. A 20 nm Al_2O_3 layer is deposited on top of this device by using the ALD system to prevent from degrading the performance of the device because of the moisture absorption in the air environment. The creation of the uniform deposition of this layer on top of the WSe_2 flake was challenging due to lack of the dangling bonds in this material. Therefore, to achieve a uniform deposition of the AL_2O_3 layer on top of the WSe_2 flake, 1 nm SiO_x layer is deposited by the e-beam evaporation method prior to the deposition of this layer. Then, to perform the Raman thermometry measurements, the Raman peaks of WSe_2 and silicon materials are first calibrated versus different temperatures. These calibrations

reveal that the E_{2g}^1 and A_{1g} peaks of WSe_2 material cannot be used for this measurement due to their peak broadening at higher temperatures. As a result, the low-frequency E_{2g}^2 peak of the WSe_2 material is used to investigate the power dissipation of WSe_2 FET versus different applied electrical powers. The calculation of the thermal resistance at the interface of the WSe_2 material and SiO_2 substrate reveals that the thermal boundary conductance (TBC) is 16 MW/m^2K. This TBC is in the low range of the known solid-solid interfaces and it could limit the performance of the device significantly due to weak thermal dissipation across the interface [96]. Therefore, it is very important to fabricate 2D-material FETs on substrates that have high thermal conductances and better quality of the interfaces with 2D-materials.

Another goal of this dissertation was to shed light on the role of the different substrates on their thermal boundary conductances with 2D-materials. In this work, CVD graphene is used as representative of 2D materials and transferred to different technologically-viable substrates having a wide range of thermal conductances and interfacial properties. Investigation of the interface resistances between graphene and different tested substrates reveals that due to the superior TBC between graphene and AlN substrate, the overall thermal dissipation performance of this material on this substrate is better than diamond and silicon substrate (even with thin oxides). These results prove that the thermal conductance of the substrate is not the only key factor that is important for the thermal dissipation of the 2D-material devices and that the role of the boundary resistance between 2D-material and substrate is very critical.

The projects which were presented in this thesis provide a comprehensive understanding of the growth of in-plane MoS_2-graphene heterostructure, as well as its electrical characterization and the role of the interface resistance between 2D-materials and different substrates. However, there is still a lack of understanding about the heat dissipation at the junction of the MoS_2-graphene heterostructure, which can be investigated in the future. Also, scientists have shown that making vertical heterostructures of 2D-materials could significantly improve their performances [24], [202], but there is no further information about the thermal dissipation through these vertical heterostructures. Hence, study of the TBC between different 2D-materials could be another subject for future research in this field.

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Editor of portion(s)	N/A
Author of portion(s)	Poya Yasaei, Amirhossein Behranginia, Zahra Hemmat, Ahmed I El-Ghandour, Craig D Foster and Amin Salehi-Khojin
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- Development of 2D-material systems: Graphene, Transition Metal Dichalcogenides, Phosphorene
- Development of novel chemical, biological, and environmental sensors
- Electrical and Thermal transport in nanoscale systems
- Novel energy generation, conversion, and storage systems

Relevant Course Work:

- Micromachining & Sensors
- Nanoscale Semiconductor Structure
- Heat Transfer Micro Nano Scale
- NanoBio Technology
- Physics of Semiconductor Devices
- Microelecteronic Fabrication Techniques
- Nanoelectronics
- Introduction to Micro Fluids
- Intermediate Heat Transfer

Patent and Publications:

Patents:

1. A. Salehi-Khojin, **A. Behranginia**, M. Asadi, P. Yasaei, "Three-Dimensional Chemical Vapor Deposited Molybdenum Disulfide Catalyst for Hydrogen Evolution Reaction" U.S. Provisional Patent Application, Submitted

Published journal papers:

1. P. Yasaei, **A. Behranginia**, Z. Hemmat, A. I. El-Ghandour, C. D. Foster, and A. Salehi-Khojin, "Quantifying the limits of through-plane thermal dissipation in 2D-material-based systems," *2D Mater.*, vol. 4, no. 3, p. 35027, Aug. 2017.
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