Soft-Switched Hybrid-Modulation for an Isolated DC-Link-Capacitor-Less Pulsating-DC-Link Inverter

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THESIS

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This thesis is dedicated to my father “Houshang”, mother “Flour”, and my sister “Niloofar” who always provide me continuous love and support. I would also like to dedicate my thesis to my late grandpa “BabaAkhtari” who passed away during my doctoral study.

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AR

TABLE OF CONTENTS

CHAPTER PAGE

LIST OF TABLES

TABLE PAGE

LIST OF FIGURES

FIGURE PAGE

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF ABBREVIATIONS

DPDPWM	Discontinuous Pulse Density Pulse Width Modulation
HFPDCL	High Frequency Pulsating dc Link
HF	High Frequency
HM	Hybrid Modulation
LF	Line Frequency
PDCL	Pulsating DC Link
PDM	Pulse Density Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switchng

SUMMARY

The main goal of this dissertation is to increase the performance of the capacitor-less high-frequency pulsating dc-link (HFPDCL) inverters suitable for renewable energy sources. The HFPDCL inverters are compact, small foot-printed, modular, and reliable since they do not employ large dc-link capacitors and line-frequency transformers. However, they require additional power conversion stages which increases the losses of the converter. The dc-link capacitor of the conventional fixed dc-link inverters provides a buffer stages for the inverter and it decouples the power conversion stages of the converter. Therefore, Power conversion stages of the HFPDCL inverters are not decoupled. As a result, they need a modulation scheme to synchronize the operation of the conversion stages and reduce the switching losses of the converter.

Auxiliary circuits conventionally are used to provide a soft-switching condition for power converters to reduce the switching losses. This increases the efficiency and performance of the converter. However, they require additional passive and active components. The modulation-based soft-switching schemes are a better solution since they do not require any additional components. Not only can they provide soft-switching for the converter, but they can also reduce the switching requirement of the converter. They use the pulsating dc-link feature of the HFPDCL inverters to provide soft-switching condition. The modulation scheme also needs to synchronize the operation of the different conversion stages of the HFPDCL inverters.

This dissertation presents modulation-based, soft-switching schemes to increase the performance of the HFPDCL inverters without using any auxiliary circuits. It reduces the switching requirement and provides a soft-switching condition to reduce the switching losses of the HFPDCL inverters to increase the overall efficiency. They also generate high-quality output waveforms with low total harmonic distortion (THD). The presented soft-switching modulation scheme operates

based on the pulsating nature of the dc-link of the HFPDCL inverters. The three presented modulation schemes are as follows: 1) a discontinuous modulation scheme that synthesizes the fixed-width pulses on the pulsating-dc link (PDCL) waveform, 2) soft-switched hybrid modulation that reduces the switching requirement of the output inverter of the HFPDCL inverter and provides a soft-switching condition for it, and 3) a pulse-density pulse-width hybrid modulation (discontinuous modulation) to reduce the switching requirement of the conversion stages of the HFPDCL inverter and provide a soft-switching condition for it.

Finally, two experimental setups are implemented to validate the performance of the presented soft-switched modulation schemes: 1) a discrete design that uses discrete silicon switching devices, and 2) a compact and modular design that uses power modules to increase the power density of the implemented HFPDCL inverter. The experimental results validate the performance of the presented soft-switched modulation schemes.

I. Introduction

Renewable energy sources offer the promise of clean abundant energy gathered from resources such as sun, wind, earth, hydro power, geothermal, and biofuels. Renewable energy technologies show promising benefits compared to conventional energy sources [1]. Most renewable energy systems are modular and have the flexibility to match energy consumption growth [2]. Power electronic converters such as dc/ac converters (inverters) are the heart of renewable energy systems. They deliver power from a renewable energy source to a utility grid or a stand-alone load. The important aspects of the inverters are efficiency [3], cost [4], reliability [5], and power density [6]. Therefore, the inverters play a key role in harvesting power from renewable sources and delivering a proper AC power to consumers. The efficiency of the inverter is critical for the amount of power we can harvest from renewable energy sources and to maximize the power delivery to consumers [7]. The first step in the design procedure of the inverters is selecting a proper topology.

A. Topology

Transformer-less inverters show some advantages such as high efficiency, reliability, and a rather simple schematic [8], [9]. However, these topologies are not able to provide isolation for power electronic systems, which is a requirement in the USA and some parts of Europe. Additionally, ground current and noise issues make these topologies less attractive for distributed generation systems. Finally, transformer-less inverters cannot adapt the voltage level of the energy source to the voltage level of the load. Therefore, they are not suitable for energy sources with low output voltage such as photovoltaic and full-cell energy sources.

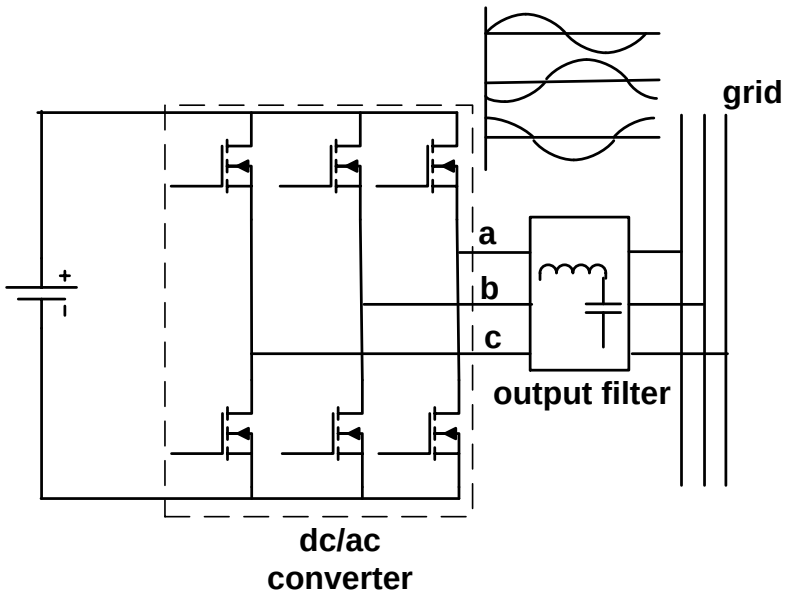


Fig. 1. A simplified Topology of a three-phase transformer-less inverter.

A simplified topology of a transformer-less grid-connected three-phase inverter is shown in Fig. 1. This topology only consists of one active stage. They usually are employed for low-power generation systems where galvanic isolation is not required. Consequently, it may lead to safety hazards in the case of any ground fault [10]. Park [11] presented a transformer-less topology for uninterruptible power supply (UPS) with relatively high efficiency and reliability. Lopez [12] and González [13] investigated a low-power, single-phase PV inverter to study the influence of the harmonics, injected by the inverter, on the ground current and investigate the leakage currents between the PV system and the ground. These issues show the troublesome performance of these inverters for high-power applications. As a result, this topology is suitable for low-power applications where galvanic isolation and ground currents can be neglected, such as small-distributed generation systems.

Line-frequency (LF) transformers are conventionally used to provide galvanic isolation and voltage scalability for power-electronic systems. They can be applied to applications such as UPS

[14], [15] and grid-connected inverters [16]. A simplified typical grid-connected three-phase inverter with a three-phase LF transformer is shown in Fig. 2. The LF transformer is connected after the output filters; therefore, it operates at LF. Krishnan [17] and Jain [18] investigated the performance of single-stage UPS inverters employing LF transformers. They reported reasonably good performance factors such as efficiency THD. However, LF transformers are bulky and heavy compared to high-frequency (HF) transformers. This not only decreases the power density of the system but also results in an increased cost of manufacturing and maintenance of the LF transformers.

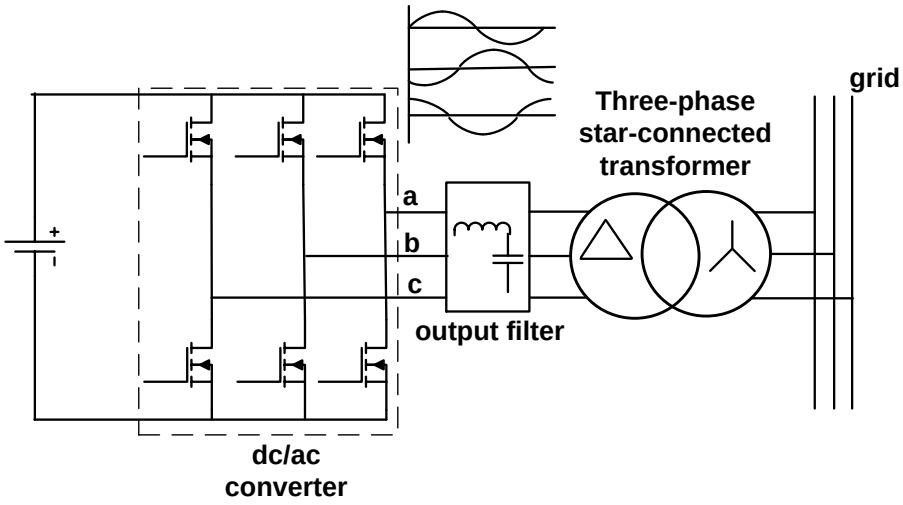


Fig. 2. The conventional LF isolated inverters.

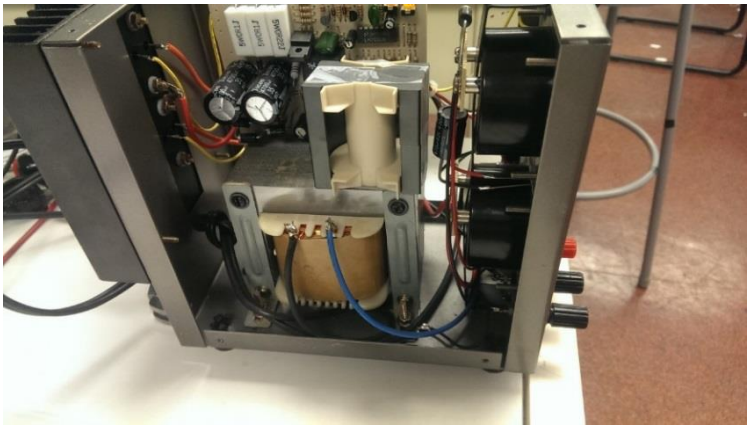


Fig. 3. The comparison between a 150 W LF transformer and a 1250 W HF transformer.

Fig. 3 shows a 150 W LF transformer and 1250 W HF (20 kHz) transformer. The shown HF transformer is much smaller than the LF transformer, even though its nominal power is almost 10 times higher than the LF transformer's. As a result, the LF transformers are the main obstacle to increasing the power density of the isolated power-electronic systems for distributed generation.

By developing high-frequency magnetic cores [19]-[21], high-frequency transformers can be used instead of the traditional LF transformers. Using HF transformers increases the power density of the high-frequency link (HFL) inverters. Therefore, HF transformers provide the required galvanic isolation and voltage scalability while dramatically decreasing the size of the transformers. The general configuration of the HFL inverters is shown in Fig. 4. The front-end dc/HF-ac converter generate bipolar pulses for HF operation of the HF transformers. A series of bipolar pulses are required to avoid saturation of the HF transformers. The output HF-ac/ac converter generates the desired output LF sinewave waveforms. The HF-ac/ac conversion stage can be a single stage or two stages.

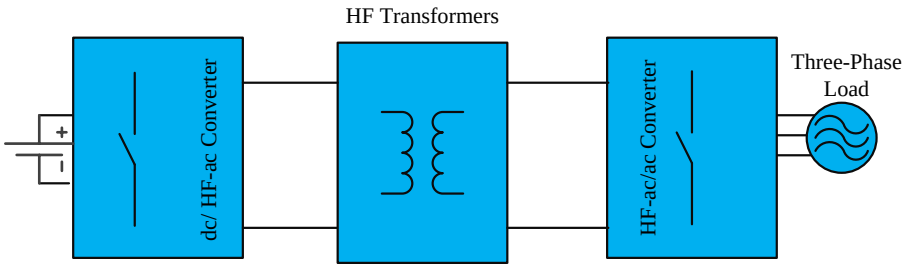


Fig. 4. The general configuration of the HFL inverters.

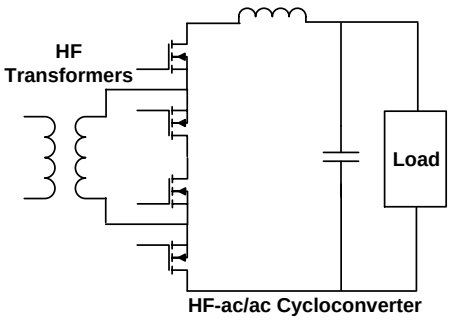


Fig. 5. A HF-ac/ac cycloconverter

The single stage HF-ac/ac converter consists of a three-phase cyclo-converter that requires bipolar voltage-block switching devices. Fig. 5 shows a single phase HFL inverter using a single-phase cycloconverter. Kan [22] presented a re-shaped single-phase HFL inverter using a HF-ac/ac cycloconverter to improve the performance of the cycloconverter-type HFL (CHFL) inverters. They developed a 500 W prototype to evaluate the performance of their proposed topology. They recorded an efficiency of 90% at a full output power condition. Rodrigues [23] proposed a soft-switched three-phase inverter using HF-ac/ac cycloconverter at the secondary side of the HF transformers. The presented soft-switching scheme is modulation based. It also reduces the switching requirement of the HF-ac/ac converter by 33%. Researchers [24]-[26] also presented modulation and soft-switching schemes to reduce the losses of the CHFL inverters. This topology does not require dc-link capacitors, which reduces the size of the inverter. However, there is no freewheeling path for the current in the secondary-side cycloconverter. The cycloconverter used at the secondary-side of the inverter requires 12 switching devices, despite having only one conversion stage. As a result, this topology does decrease the number of the switching devices of the inverter. More importantly, this topology is not modular. Meaning that it cannot be implemented using standard bridge power modules.

The two stage HF-ac/ac converters, as shown in Fig. 6, are conventionally comprised of a rectifier and a following dc/ac converter. The dc-link filter, comprised of an inductor and large dc-link capacitor, decouples the front-end conversion stages of the inverter from the output dc/ac converter. Therefore, the two front-end stages of the converter can independently operate as a dc/dc converter. The output dc/ac converter generates the desired LF output waveforms. The voltage of the dc-link capacitor is fixed. As a result, a large electrolytic capacitor is usually employed as the dc-link capacitor. This increases the size and decreases the reliability and power density of the

inverter. Electrolytic capacitors are the main cause of failure of power electronics systems because their lifetime is very sensitive to their operational temperature [27]-[29].

HFL inverters require more conversion stages than conventional inverters. This results in higher losses due to the higher number of switching devices. As a result, losses of the HFL inverters need to be decreased in order to increase the overall efficiency of the power electronic systems. HFPDCL inverters [30]-[37] have high-power density due to the elimination of the bulky dc-link capacitors and use of HF transformers. They do not need a faulty electrolytic capacitor, which results in a higher reliability than the fixed dc-link HFL inverters. Fig. 7 shows a simple schematic of a HFPDCL inverter that consists of two conversion stages: 1) a dc/pulsating-dc converter that comprises dc/ac converters, HF transformers, and an ac/pulsating-dc converter; and 2) a pulsating-dc/ac converter that generates the desired LF output waveforms.

Reference [30] used a small dc-link filter single-phase HFPDCL inverter to be able to synthesize the waveform of the dc-link. They generate a LF rectified sinewave voltage waveform at the dc-link of the inverter to reduce the switching requirement of the output dc/ac converter. They reported a maximum efficiency of 87% for an implemented 1 kW HFPDCL inverter. Chen [31] proposed a single-phase HFPDCL inverter using a forward converter as the front-end dc/ac converter. The front-end forward converter provides the HF isolation of the inverter. They reported a low THD output waveform, and an efficiency between 80-85%.

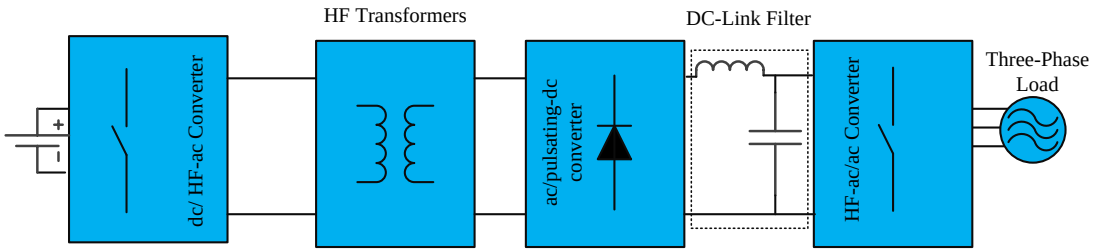


Fig. 6. Fixed-dc link HFL inverter.

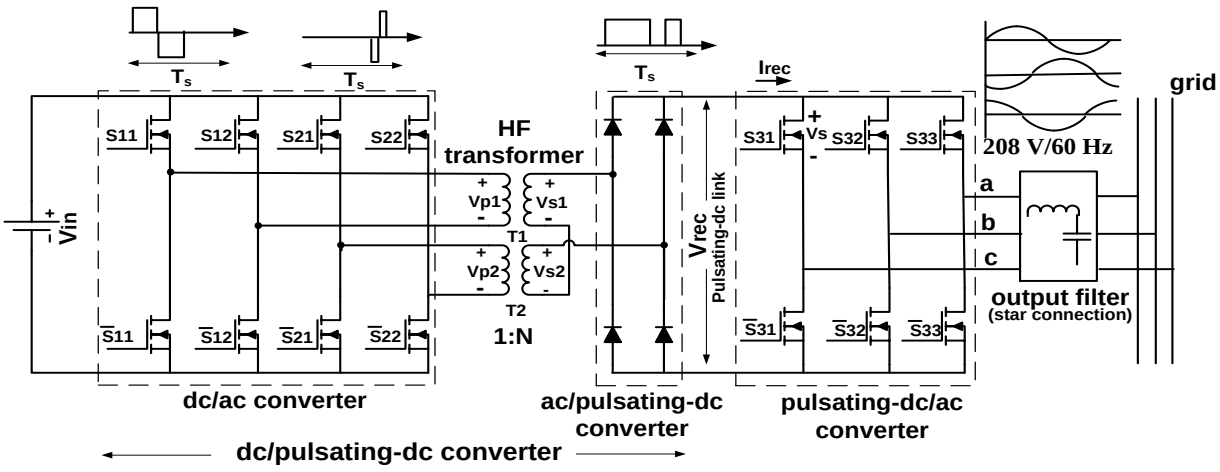


Fig. 7. Schematic of a three-phase HFPDCL inverter (©2014IEEE).

In [32], a multilevel HFPDCL inverter is proposed, which shows the proper performance of this topology for multilevel applications. Fujimoto [33] presented a novel single phase HFPDCL inverter using a fully-controlled synchronous ac/pulsating-dc converter. Their implemented 3 kW prototype showed an output THD below 5% and efficiency as high as 92%. Koutroulis [34] explained the design of a single-phase HFPDCL inverter. Their efficiency for 200 W prototype varies between 80% and 85%. Recent work by our group [35]-[37] has also shown the proper performance of the HFPDCL inverter for renewable energy sources.

B. Switching Scheme

HFL inverters have more conversion stages than the conventional LF isolated inverters. Therefore, the switching losses of the HFL inverters need to be addressed to increase the efficiency of the system. There are two soft-switching schemes available for HFL inverters: 1) soft-switching schemes using auxiliary circuits, and 2) modulation-based soft-switching schemes. Auxiliary circuits are conventionally used to provide soft-switching [38]-[41] conditions for isolated power converters. Yakushev and Han [38], [39] used an active clam, which consists of a switched-capacitor circuit, to provide a soft-switching condition for the switches of the full-bridge converter.

Tabias and Rivas [40], [41] used the concept of the resonant circuits to provide a soft-switching condition. All of these techniques require additional components. This results in a larger number of components and makes the topology of the HFL inverters more complicated. The passive and active components of the auxiliary circuits also result in some losses. More importantly, these approaches are load-dependent, and they are not usually effective for a wide range of operation conditions. Therefore, soft-switching schemes using no auxiliary circuits (modulation-based soft-switching schemes) are preferred over traditional soft-switching schemes using auxiliary circuits.

The PDCL feature of the HFPDCL can be used to decrease the switching requirement and switching losses of the HFPDCL inverters. It also eliminates the bulky filters of the fixed-dc link inverters. Therefore, the reliability and power density of the HFPDCL inverters are improved by elimination of the bulky electrolytic capacitors. However, multi-stage power conversion of the HFPDCL inverter requires a carefully designed switching scheme to reduce device losses and switching requirements of the inverter and to ensure the synthesis of the inverter output waveforms with acceptable harmonic distortion. As a result, a proper approach needs to be addressed to decrease the losses and increase the efficiency of the HFPDCL inverters.

Carrier based PWM modulation schemes [42], [43] have been developed based on the comparison of the modulation signals and a triangle carrier waveform. Discontinuous PWM schemes [44]-[48] reduce the switching requirement of the inverter compared to the conventional continuous PWM schemes. This decreases the switching losses and increases the efficiency of the inverter. This method of loss mitigation does not require any additional circuits in contrast to soft-switching methods using auxiliary circuits. In a cyclic manner, Discontinuous PWM clamps one predetermined leg of the pulsating-dc/ac converter to the dc-bus while the other legs of the converter operate at HF. Although different Discontinuous PWM schemes [49]-[53] are presented for the

fixed-dc link inverters, they are not optimized for HFPDCL inverters, where the nature of the dc link is pulsating instead of the conventional fixed dc. These presented discontinuous PWM schemes [49]-[53] decrease the switching requirement of the inverter. They can reduce the switching losses of the inverter by allowing no switching of one of the legs of the three-phase converter. Therefore, these schemes yield no commutation of a leg for a specific angular duration (e.g., 30^o or 60^o) of any line cycle. However, this still incurs HF switching of the remaining legs of the converter under hard-switching condition. They are developed based on the zero-sequence signal injection to the reference signals. They decrease the switching requirement of the inverter by 33%. These modulation schemes are designed for the fixed dc-link inverters.

The modulation scheme described in [54] uses a square-wave modulation scheme. It uses the square-wave modulation for the dc/ac converter. Using such a modulation, the dc/ac converter generates a stream of pulses with fixed on-time width on the PDCL waveform. As such, a sine-wave modulation technique must be applied to the pulsating-dc/ac converter to generate the LF output voltage waveforms. Therefore, all the legs of the pulsating-dc/ac converter operate at HF under the hard-switching condition.

The originally proposed HM scheme (referred to as the conventional HM in this dissertation), described in [55]-[58], can be applied to the pulsating-dc/ac converter to decrease the switching requirements of the converter. Unlike the discontinuous-modulation schemes, the conventional HM scheme requires no HF commutation on two of the legs of the pulsating-dc/ac converter. Therefore, only one of the three legs operates under HF hard-switching condition. This additional reduction in switching is achieved by recognizing that if the dc/ac converter switches are sinusoidally modulated (emulating the inverter output), the PDCL waveform, representing the maximum (dc/ac-converter) phase-to-phase voltage, is also encoded with this sinusoidal information. This information is

exploited by the HM to reduce the switching need for the pulsating-dc/ac converter. Because the maximum phase-to-phase voltage of the dc/ac converter changes every 60^o of the line cycle, the HM of the pulsating-dc/ac converter appropriately selects the two converter legs that are not switched in this 60^o interval. Notwithstanding, switching loss incurred in the remaining converter leg (that is hard-switched) needs to be addressed.

As such, in this dissertation, a soft-switched HM scheme [59] is developed to provide a soft-switching condition for the pulsating-dc/ac converter. A novel and fundamentally different modulation scheme must be applied to the dc/ac converter to enable soft-switched HM of the pulsating-dc/ac-converter switches. Using this scheme, the two predetermined legs of the pulsating-dc/ac converter are not switched in every 60^o of the line cycle while the other leg works at HF but under soft-switching condition. Therefore, soft-switched HM scheme proposes a unique modulation mechanism for the dc/ac and the pulsating-dc/ac converters. However, this modulation increases the switching requirement of the front-end dc/ac converter and the rectifier. Therefore, a dual discontinuous pulse-density pulse-width modulation (DPDPWM-hybrid modulation) scheme to reduce the switching requirement of the dc/ac converter, the rectifier, and pulsating-dc/ac converter.

C. Motivation and Objectives of Research

The switching losses of the HFPDCL inverters need to be decreased to increase the overall efficiency of the system. Although HFPDCL inverters consist of three active switching stages, they operate as a single stage power converter because the dc-link capacitors are eliminated from the power stage. The dc-link capacitor decouples the front-end and output converters of the HFL inverters. Therefore, the front-end dc/ac and the output dc/ac converters can be controlled

independently. As a result, the modulation scheme of the HFPDCL inverters needs to synchronize the operation of all the conversion stages due to the elimination of the dc-link capacitor.

HF transformers are used to provide galvanic isolation for the PDCL HF inverters. The power density of the HFL inverters is increased because of the high-frequency operation of the transformers in contrast to the inverters with line-frequency transformers. However, the leakage inductance of the HF transformers causes voltage spikes on the devices of the ac/pulsating-dc and pulsating-dc/ac converters. Therefore, a proper approach needs to be used to absorb the leaked energy of the HF transformers to limit the voltage spikes on the PDCL waveform. A carefully-designed and manufactured transformer can decrease the leakage inductance of the system. An RCD [60] clamp can also be used to absorb the leakage energy of the HF transformers and dissipate it to suppress the voltage spikes on the switching devices of the inverter. In addition, an active clamp [55] can also be used to recover the leakage energy and transfer it to the load or the input source.

Any random pulses can be synthesized on the PDCL waveform by the dc/ac converter because of the elimination of the dc-link capacitor. The synthesized pulses can be used by the pulsating-dc/ac converter to decrease the switching losses of the output stage of the HFPDCL inverter. There are two approaches to decrease the switching losses of the pulsating-dc/ac converter: 1) by decreasing the switching requirement and 2) by providing the soft-switching condition for the switching devices of the converter. The proposed approach in dissertation reduces the switching requirement of the HFPDCL inverter. Two predetermined legs of the pulsating-dc/ac converter clamp to the dc bus in 120^{o} of the line cycle. Therefore, the switching requirements of the pulsating-dc/ac converter are practically decreased by 66%. The remaining leg of the pulsating-dc/ac converter can operate under ZVS condition to decrease the switching losses. As a result, the switching losses of the pulsating-dc/ac converter are practically mitigated. Therefore, the presented

approach for mitigating the switching losses of the pulsating-dc/ac converter is provided without using any auxiliary circuit.

A unique switching scheme is required for the dc/ac converter to provide zero states on the PDCL waveform. The legs of the pulsating-dc/ac converter turn off/on during these provided zero states on the PDCL waveform. That provides zero-voltage switching condition for the remaining leg of the pulsating-dc/ac converter that operates at HF.

The ac/pulsating-dc converter consists of a single-phase diode-bridge module for unidirectional application. Additionally, it can be used for bidirectional applications by using a fully-controlled full-bridge module. Using a single-phase full-bridge module also provides zero-voltage switching condition for the ac/pulsating-dc converter. The switching requirement of the ac/pulsating-dc converter can be decreased by synthesizing a unique stream of pulses on the PDCL waveform and using pulse density modulation for the pulsating-dc/ac converter.

The soft-switched hybrid modulation [59] reduces the switching requirement of the pulsating-dc/ac converter by 66% and provides ZVS condition for the remaining leg of the converter operating at HF. However, it increases the switching requirement of the front-end dc/ac and the ac/pulsating dc converter. Therefore, a DPDPWM scheme is developed to not only decrease the switching requirement of the pulsating-dc/ac converter, but also decrease the switching requirement of the front-end dc/ac and the ac/pulsating-dc converters.

In Chapter II, a discontinuous PWM scheme, optimized for HFPDCL inverters, is developed to reduce the switching requirement of the pulsating-dc/ac converter without modulating the PDCL waveform. Therefore, the generated pulses on the PDCL waveform have a fixed duty cycle representing a dc value. Later in this chapter, the basic principal operation of the hard-switched HM

scheme is explained. Hard-switched HM scheme reduce the switching requirement of the pulsating-dc/ac converter by 66%.

In Chapter III, the soft-switched HM scheme is presented to reduce the switching requirement and switching losses of the pulsating-dc/ac converter. Therefore, two predetermined legs of the pulsating-dc/ac converter clamp to the dc rail while the other leg operates at HF under ZVS condition. The ZVS condition is provided for the pulsating-dc/ac converter by generating the zero states on the PDCL waveform. The zero states are generated on the PDCL waveform by a unique switching scheme for the dc/ac converter. Therefore, the switching losses of the pulsating-dc/ac converter are practically eliminated without using any auxiliary circuit.

In Chapter IV, the soft-switched HM scheme is validated by experimental results using a discrete 1 kW HFPDCL inverter. The results show that the soft switching condition is provided for the pulsating-dc/ac converter over a wide range of load conditions. The output current THD is well below 5% for a wide range of output powers and different load types. The efficiency of the pulsating-dc/ac converter is increased using soft-switched HM scheme in contrast to the existing modulation scheme for a PDCL HF inverter.

In Chapter V, a compact and modular design is developed for the HFPDCL inverter to decrease the leakage inductance of the board. It also increases the power density of the implemented HFPDCL inverter. The performance of the presented soft-switched modulation schemes are validated using the implemented 2 kW compact and modular HFPDCL inverter. In Chapter VI, a DPDPWM scheme is presented to reduce the switching requirement of the dc/ac converters. It also provides soft-switching condition for the pulsating-dc/ac and ac/pulsating-dc converters by generating the zero states on the PDCL waveform. The ZVS operation of the pulsating-dc/ac converter is validated using experimental results.

II. A Discontinuous Modulation Schemes optimized for HFPDCL inverters

A. DC-Modulated PDCL Waveform Discontinuous Modulation

(Parts of this section, including figures and text, are based on my paper [67], ©2015 IEEE)

The modulation signals divide the modulation schemes of the inverters into two groups: continuous PWM and discontinuous PWM. In the continuous PWM schemes, the modulation signals are always in the boundary of the triangle carrier. However, in the discontinuous PWM schemes at least one phase leg of the inverter clamps to the negative or the positive rail of the dc bus. Therefore, one predetermined phase leg of the inverter does not modulate during any given period of the line cycle

An isolated neutral star-connected load allows us to inject any zero sequence signals to the reference signals. It gives us freedom to vary the duty cycle of the switches of the output pulsating-dc/ac converter. This degree of freedom can be used to decrease the switching requirement of the converter and enhance the quality of the output waveforms. The conventional sine PWM (SPWM) is the simplest continuous modulation scheme and has gained wide application due to its simplicity. However, the dc-bus rail utilization of the SPWM scheme is low. PWM schemes such as third harmonic injection PWM (THIPWM) and space-vector PWM (SVPWM) inject a zero sequence signal to increase the dc-bus utilization of the inverter. Fig. 8 shows the modulation signals of the SPWM, THIPWM, and SVPWM. As we can see, although the THIPWM and SVPWM schemes increase the dc-bus utilization of the converter, they do not decrease the switching requirement of the inverter. As a result, the three leg phase of the output pulsating-dc/ac converter operate at HF using continuous modulation schemes.

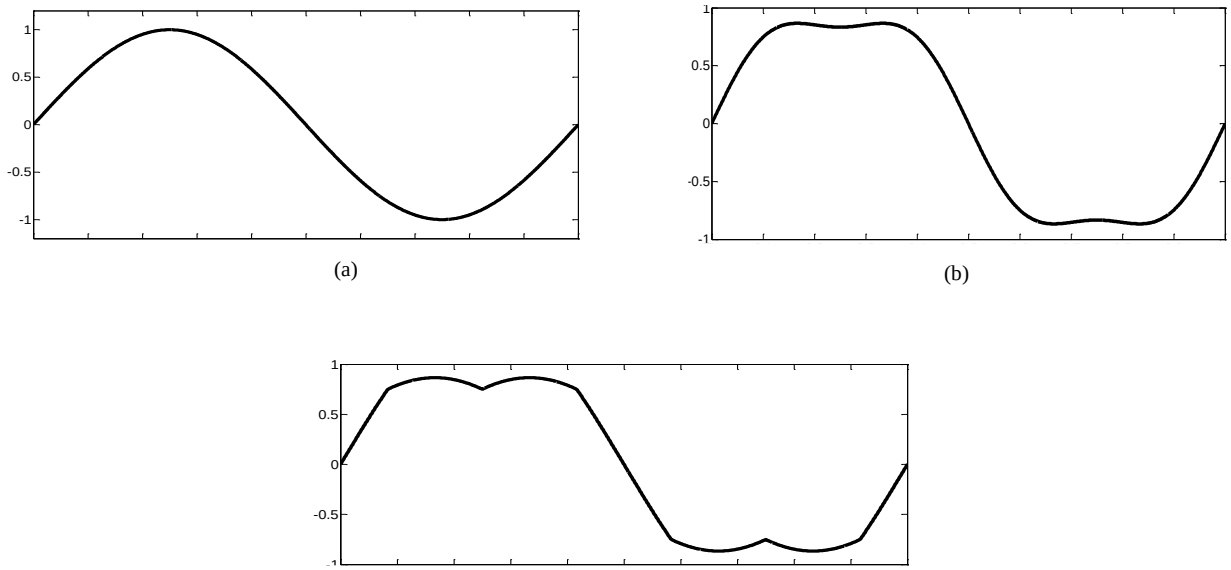


Fig. 8. The modulation signals of the SPWM, THIPWM, and SVPWM schemes: a) SPWM, b) THIPWM, and c) SVPWM, ©2015 IEEE.

The front-end dc/ac converter of the HFPDCL inverter, shown in Fig. 7, determines the width of the pulses on the dc-link waveform. As a result, the operation of the front-end dc/ac and pulsating-dc/ac converters needs to be synchronized to synthesize the output LF waveforms. The front-end dc/ac converter determines the maximum achievable modulation index and the position of the generated zero states on the dc-link waveform. The pulsating-dc/ac converter synthesizes the output waveforms based on the generated pulses on the dc-link waveform by the front-end dc/ac converter. The zero states on the dc link waveform are generated by shorting the primary of the HF transformers. The ac/pulsating-dc converter (rectifier) rectifies the bipolar pulses generated by the front-end dc/ac converter. Fig. 9 shows the pulse placement and the generation of the dc-link waveform. The duty cycle of the pulses on the dc-link waveform are fixed; therefore, they represent a dc value. This dc value is set by the modulator of the HFPDCL inverters which synchronize the operation of the front-end dc/ac converter and the pulsating-dc/ac converter.

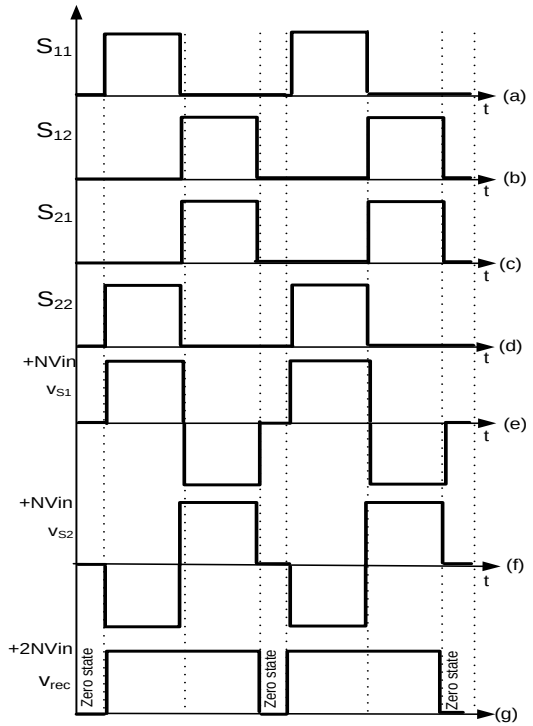


Fig. 9. Pulse placement and the generation of the dc-link waveform: (a)-(d) the synthesized gate signals of S11, S21, S21, and S22, (e)-(f) the secondary voltages of the HF transformer, and (g) the generated dc-link waveform, ©2015 IEEE.

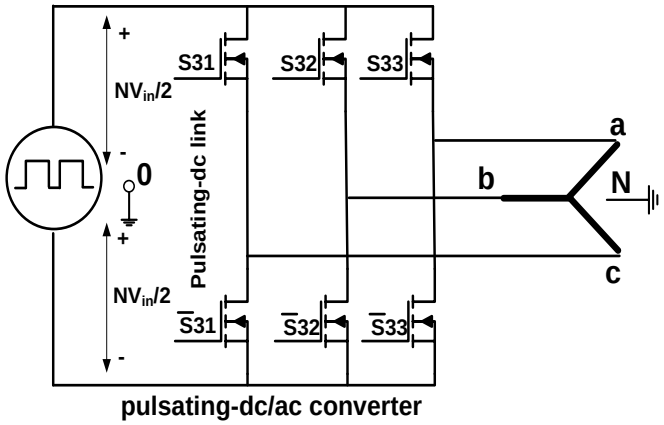


Fig. 10. The equivalent circuit of the pulsating-dc/ac converter and the HF pulsating-dc link, ©2015 IEEE.

The equivalent circuit of the pulsating-dc/ac converter and the HF pulsating-dc link of the HFPDCL inverter is shown in Fig. 10. The frond-end dc/ac, HF transformers, and the rectifier are replaced by a pulsating-voltage power supply. The neutral point of the Y-connected load is isolated. The balanced three-phase reference signals can be defined as below:

$$u_A(t) = m * \sin(\omega t)$$
$$u_B(t) = m * \sin\left(\omega t + \frac{2\pi}{3}\right) \quad (1)$$
$$u_C(t) = m * \sin\left(\omega t + \frac{4\pi}{3}\right)$$

where m is the modulation index and ω is the angular frequency of the output waveforms. It should be noted that the dc-link waveform is pulsating and is not fixed. Therefore, the value of the dc-link waveform is either $N*V_{in}$ or zero. The dc-link voltage is zero when the HF transformers are shorted by the front-end dc/ac converter. Thus, when switches S_{31}, S_{32}, and $\bar{S}_{33}$ are on and the dc-link value is $N*V_{in}$, the output phase voltage can be written as follows:

$$v_{aN} = v_{bN} = N \times \frac{V_{in}}{3} \quad (2)$$
$$v_{cN} = -N \times \frac{2V_{in}}{3}$$

A zero sequence signal can be injected to reference signals in (1) to generate the modulation signal of the inverter. The modulation signal can be represented as follows:

$$v_a(t) = u_a(t) + z(t)$$
$$v_b(t) = u_b(t) + z(t) \quad (3)$$
$$v_c(t) = u_c(t) + z(t)$$

where z is the injected zero-sequence signal. The zero-sequence signal is equal to $1/6m*\sin(3\omega t)$ for the THIPWM. It is equal to $1/2(1-\max(u_i))+1/2(-1-\min(u_i))$ for the SVPWM, where i is a, b, or c. These zero-sequence signals are injected to reference signals to increase the dc-link utilization of the inverter. The output phase voltages can be written as follows:

$$v_{aN}(t) = D_{PDCL} N \frac{V_{in}}{2} (m \times \sin(\omega t) + z(t))$$
$$v_{bN}(t) = D_{PDCL} N \frac{V_{in}}{2} (m \times \sin\left(\omega t + \frac{2\pi}{3}\right) + z(t)) \quad (4)$$
$$v_{cN}(t) = D_{PDCL} N \frac{V_{in}}{2} (m \times \sin\left(\omega t + \frac{4\pi}{3}\right) + z(t))$$

where D_{PDCL} is the width of the pulses on the dc-link waveform set by the front-end dc/ac converter. The resulting output line-to-line voltages do not contain the zero-sequence signal z(t) and they can be written as follows:

$$v_{ab}(t) = D_{PDCL} N \frac{\sqrt{3} V_{in}}{2} \times m \times \sin\left(\omega t + \frac{5\pi}{6}\right)$$

$$v_{bc}(t) = D_{PDCL} N \frac{\sqrt{3} V_{in}}{2} \times m \times \sin\left(\omega t + \frac{5\pi}{6}\right) \quad (5)$$

$$v_{ca}(t) = D_{PDCL} N \frac{\sqrt{3} V_{in}}{2} \times m \times \sin\left(\omega t + \frac{3\pi}{2}\right)$$

The maximum output voltage is equal to the dc-link average voltage which is equal to $D_{PDCL} N V_{in}$ when the modulation index is equal to $\frac{\sqrt{3}}{2}$. Therefore, the modulation signal is linear and in continuous mode when we have:

$$-1 + \frac{1-D_{PDCL}}{2} - u_{min} < z(t) < 1 - \frac{1-D_{PDCL}}{2} - u_{max} \quad (6)$$

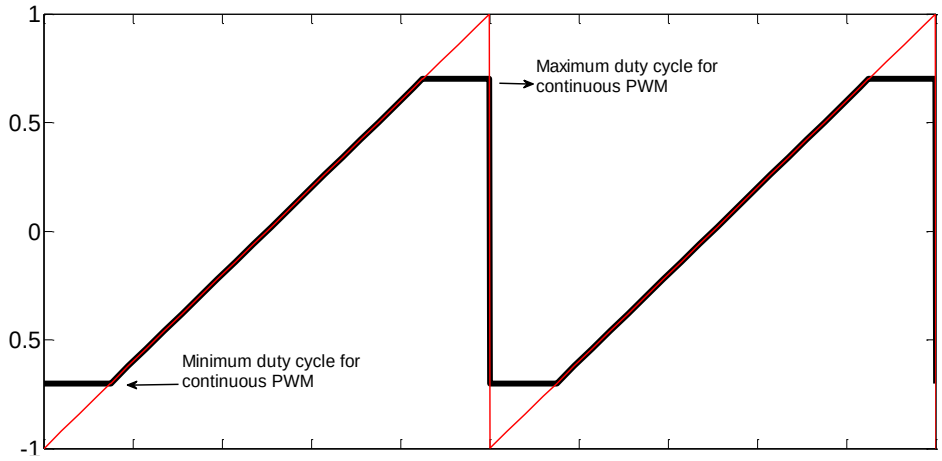


Fig. 11. The modified carrier signal for HFPDCL inverters, ©2015 IEEE.

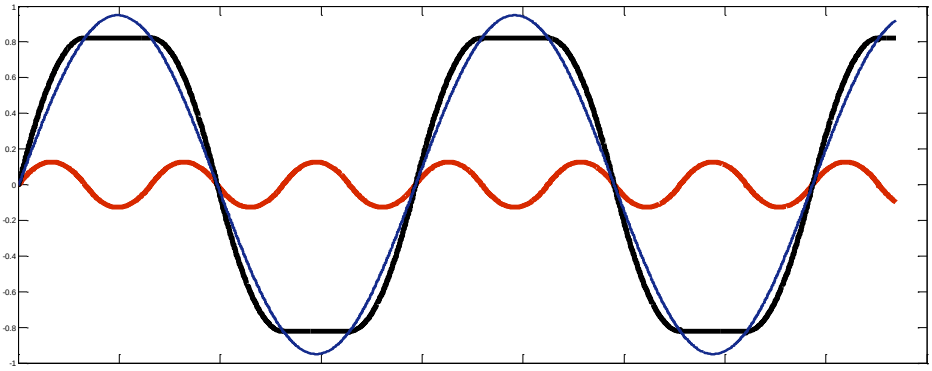


Fig. 12. The modulation signal after injecting the zero sequence signal, ©2015 IEEE.

where u_{min} and u_{max} are respectively the minimum and the maximum value of the defined reference signals in equation (1). For linear region, equation (6) means that the minimum duty cycle of the output pulsating-dc/ac converter is $-1+\frac{1-D_{PDCL}}{2}$ and the maximum duty cycle is $1-\frac{1-D_{PDCL}}{2}$ when the dc-link is HF pulsating. This is in contrast to the conventional fixed-dc link inverters where the maximum and the minimum duty cycles are respectively 1 and 0. The triangle carrier of the modulator of the HFPDCL inverters can be modified as shown in Fig. 11. This can be used to provide a high performance DPWM scheme for HFPDCL inverters. A zero sequence signal defined can be injected as follows:

$$Z(t) = \text{sgn}[\sin(3 \times \omega t)] \times \left[\max|u_A, u_B, u_C| - m \times \frac{\sqrt{3}}{2}\right] \quad (7)$$

where sgn(x) is the sign function and sin(3ωt) is the third harmonic function of the reference signals. The final modulation signal after injecting the zero-sequence signal and the sequence signal are shown in Fig. 6.

Therefore, the width of the pulses (DPDCL) on the dc-link waveform must be equal to $\frac{\sqrt{3}}{2} * \text{m}$. As a result; using the modified triangle carrier shown in Fig. 5 and the obtained modulation signal shown in Fig. 12, the desired output waveforms can be achieved. The resulting modulation scheme

is discontinuous. Therefore, one phase leg of the pulsating-dc/ac converter clamps to the dc-link at any given time. Each phase leg of the inverter does not commutate at 120o of the line cycle. This decreases the switching losses of the converter to increase the overall efficiency of the HFPDCL inverter.

B. Hybrid Modulation

(Parts of this section, including figures and text, are based on my paper [66], ©2014 IEEE)

The HM scheme [55]-[57] unlike discontinues PWM schemes [49]-[53] decreases the switching requirement of the two predetermined legs of the pulsating-dc/ac converter in every 60^o of the output line cycle. Therefore, every line cycle is divided in six different sectors; that is Pi-PVI. However, discontinues PWM schemes reduce the switching requirement of the pulsating-dc/ac converter by allowing no switching of one of the legs of the pulsating-dc/ac converter in every 30^o or 60^o of the line cycle.

The additional decrease in switching requirement of the pulsating-dc/ac converter is achieved by generating a unique PDCL waveform that represents the maximum of the output reference signals. The maximum of the output reference signals changes in every 60^o of the output line cycle. Fig. 13 shows the achieved PDCL waveform that consists of six distinct operating sectors, PI-PVI. Therefore, two predetermined legs of the pulsating-dc/ac converter do not need to commutate in Sectors, PI-PVI.

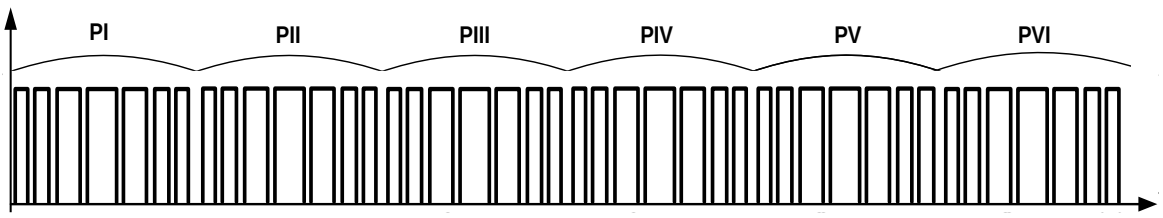


Fig. 13. The sinusoidal encoded information on the pulsating dc-link waveform for the HM scheme, ©2014 IEEE.

1. Front-End DC/AC Converter Modulation

As mentioned in the previous section, the HM scheme needs a PDCL waveform representing the maximum of the output reference signals. Therefore, the dc/ac converter generates a pattern that represents the maximum of the output reference signals. The generated bipolar pulses are, then, rectified to achieve the required PDCL waveform. The three-phase output reference signals are defined as (1). The PDCL waveform is generated to represent the maximum of the output reference signals u_{AB}, u_{BC}, and u_{CA}. Therefore, the modulation signal for dc/ac converter is defined as:

$$1 - \max((|u_{AB}|, |u_{BC}|, |u_{CA}|) \tag{8}$$

where $|u_{AB}|$, $|u_{BC}|$, and $|u_{CA}|$ are respectively the absolute value of the output reference signals u_{AB}, u_{BC}, and u_{CA}. The modulation signal for the dc/ac converter is shown in Fig. 14. As a result, the modulation function of the dc/ac converter is equal to $|v_{CA}|$ in PI. The full-bridge modules of the dc/ac converter operate complementary. Therefore, the gate signal of the high-side switch S_{11} is identical to the gate signal of the high-side switch S_{22}. Accordingly, the gate signal of the high-side switch S_{12} is identical to the gate signal of the high-side switch S_{21}. The peak-to-peak value of the obtained PDCL waveform, v_{rec}, is calculated as follows:

$$v_{rec(pk-pk)} = 2 \times N \times V_{in} \tag{9}$$

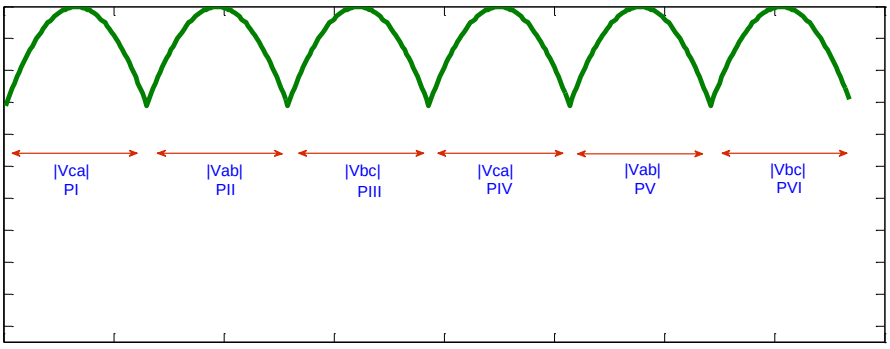
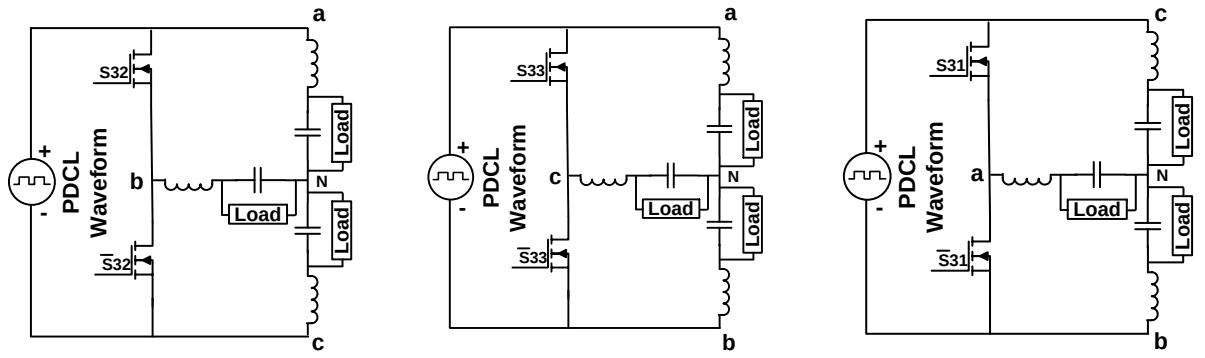


Fig. 14. The modulation function of the dc/ac converter, ©2014 IEEE.



(a): Sector PI (b): Sector PII (c): Sector PIII

Fig. 15. The equivalent circuit of the PDCL and the pulsating-dc/ac converter, ©2014 IEEE.

2. Pulsating-dc/ac Converter

Fig. 15 shows the equivalent circuit of the PDCL and pulsating-dc/ac converter during different operating sectors. The pulsating supply represents the PDCL waveform that is generated by the dc/ac and ac/pulsating-dc converters. The generated PDCL waveform represents the maximum of the output reference signals. Therefore, two predetermined legs of the pulsating-dc/ac converter do not commutate in and Sectors, PI-PVI. Sectors PI, PII, and PIII are respectively are complementary with respect to Sectors PIV, PV, and PVI. Therefore, the gate signals of the switches of the pulsating-dc/ac converter are inverted in the complementary Sectors. In the following section, only Sectors PI, PII, and PIII are, as a result, explained.

Sector PI:

In this sector, u_{CA} is negative and its absolute value is the maximum of the output reference signals. Both of u_{AB} and u_{BC} are positive. Therefore, switches S_{31} and $\bar{S}_{33}$ are always ON in Sector PI. The second leg of the pulsating-dc/ac converter operates at HF to generate other output reference signals. The equivalent circuit of the pulsating-dc/ac converter is shown in Fig. 15a. Nodes “a” and “c” are permanently connected to the PDCL, which represents the output reference signal u_{CA}. The

output reference signal u_{BC} is the modulation signal of the high-side switch of the second leg of the pulsating-dc/ac converter, S_{32}. Therefore, three-phase output voltages are calculated as:

$$\begin{aligned} v_{ca} &= v_{rec} = 2 \times N \times V_{in} \times m \times \sin\left(\omega t + \frac{4\pi}{3}\right) \\ v_{ab} &= 2 \times N \times V_{in} \times (v_{rec} - u_{BC}) = 2 \times N \times V_{in} \times m \times \sin(\omega t) \\ v_{bc} &= 2 \times N \times V_{in} \times m \times \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad (10)$$

Sector PII:

In Sector PII, u_{AB} is positive and it is the maximum of the output reference signals while u_{BC} and u_{CA} are negative. Therefore, node "a" and "b" need to be connected to the PDCL in Sector PII. The equivalent circuit of the pulsating-dc/ac converter is shown in Fig. 15b. The third legs of the pulsating-dc/ac converter operates at HF while S_{31} and $\bar{S}_{32}$ are always ON. The high-side switch of the third leg of the pulsating-dc/ac converter, S_{33}, is modulated by the output reference signal u_{BC}. The three-phase output voltages are calculated as:

$$\begin{aligned} v_{ab} &= v_{rec} = 2 \times N \times V_{in} \times m * \sin(\omega t) \\ v_{ca} &= -2 \times N \times V_{in} \times (v_{rec} - |u_{BC}|) = 2 \times N \times V_{in} \times m \times \sin\left(\omega t + \frac{4\pi}{3}\right) \\ v_{bc} &= 2 \times N \times V_{in} \times m \times \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad (11)$$

In equation (10), the absolute value of the u_{BC} is used because it is negative in Sector PII.

Sector PIII:

The output reference signal u_{BC} becomes the maximum of the output reference signals in Sector PIII. The output reference signal u_{BC} is negative while u_{CA} and u_{AB} are positive. Therefore, the

second and third legs of the pulsating-dc/ac converter do not commutate as shown in Fig. 15c. The first leg of the pulsating-dc/ac converter operates at HF to generate phase-to-phase output voltages u_{ab} and u_{ca}. The high-side switch of the first leg of the pulsating-dc/ac converter is modulated by the output reference signal u_{AB}. As a result, the output reference signal u_{BC} is already modulated on the PDCL waveform by the dc/ac converter and two other output reference signals are generated by the first leg of the pulsating-dc/ac converter. The three-phase output voltage are calculated as follows:

$$\begin{aligned} v_{bc} &= v_{rec} = 2 \times N \times V_{in} \times m \times \sin\left(\omega t + \frac{2\pi}{3}\right) \\ v_{ca} &= 2 \times N \times V_{in} * m \times (v_{rec} - u_{AB}) = 2 \times N \times V_{in} \times m \times \sin(\omega t) \\ v_{ab} &= 2 \times N \times V_{in} \times m \times \sin(\omega t) \end{aligned} \tag{12}$$

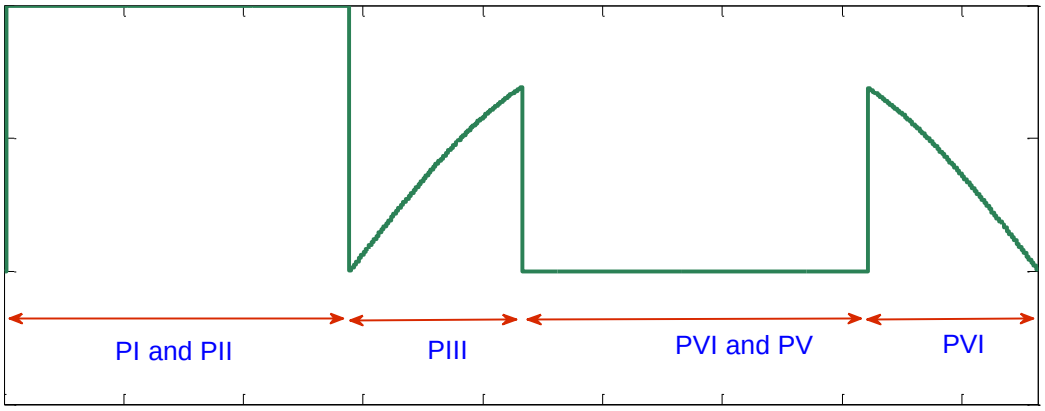


Fig. 16. The modulation signal of the first leg of the pulsating-dc/ac converter, ©2014 IEEE.

Therefore, all three-phase output voltages are generated by the pulsating-dc/ac converter while two predetermined legs of the converter do not commutate. This decreases the switching requirement of the pulsating-dc/ac converter by 66%. The overall modulation signal of the pulsating-dc/ac converter is shown in Fig. 16. As a result, each leg of the pulsating-dc/ac converter

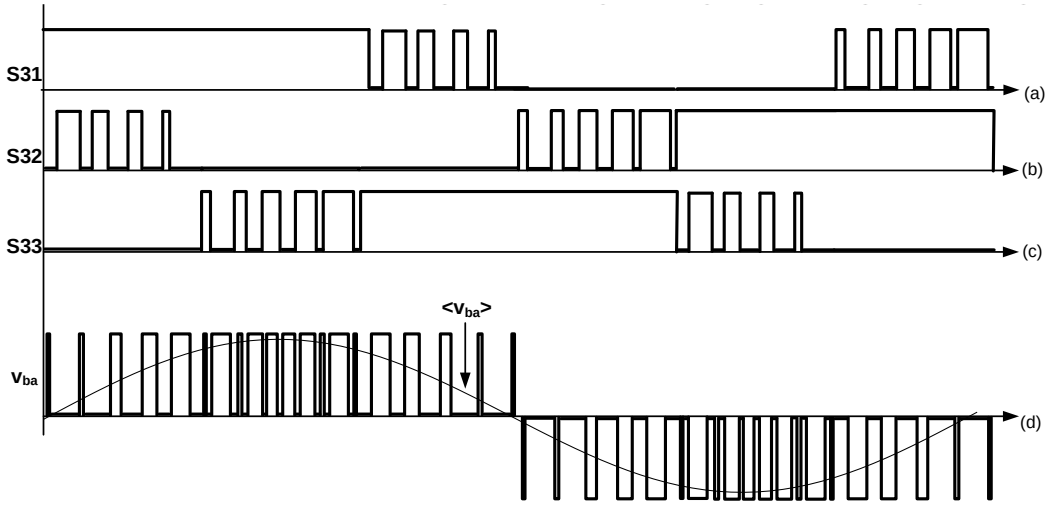


Fig. 17. The switching signals of the pulsating-dc/ac converter using the HM scheme. a) Gate signal of S_{31}, b) Gate signal of S_{32}, c) Gate signal of S_{33}, and d) The achieved output voltage waveform $v_{ba.}$, ©2014 IEEE

do not commutate during 240^o of the output LF. The next section explores the operation of the dc-link-capacitor less HFL inverter using the HM scheme. The resulting gate signals for all three legs of the pulsating-dc/ac converter to generate the output voltage waveforms are shown in Fig. 17. Therefore, only one leg of the pulsating-dc/ac converter operates at HF in each Sector. TABLE I summarizes the HF operation of the three legs of the pulsating-dc/ac converter in any Sectors. In the next section, the operation of the dc-link-capacitor less HFL inverter using hybrid modulation is verified by the experimental results.

TABLE I**:** Switching signals for the pulsating-dc/ac converter.

Gate signal	PI	PII	PIII	PIV	PV	PVI
S_{31}	HF	1	1	HF	0	0
S_{32}	0	0	HF	1	1	HF
S_{33}	0	HF	0	0	HF	1

C. Conclusion

A discontinuous PWM scheme optimized for HFPDCL inverters with HF pulsating dc-link waveform has been developed to decrease the switching requirement of the inverter and generate

high-quality output waveforms. The presented discontinuous PWM decreases the switching requirement of the output three-phase inverter (pulsating-dc/ac converter) by 33%. One phase leg of the output inverter is clamped to the dc-rail in 120^{o} of the line cycle. It does not need to modulate the PDCL waveform. Therefore, the PDCL waveform presents a dc value. This modulation scheme clamps two legs of the pulsating-dc/ac converter to the dc rail at any given time. Therefore, it decreases the switching requirement of the pulsating-dc/ac converter by 66%. However, the remaining leg of the pulsating-dc/ac converter still operates under hard-switching condition.

III. Soft-Switched Hybrid Modulation

(Parts of this chapter, including figures and text, are based on my journal paper [59], ©2014 IEEE)

HFPDCL inverters consist of three active stages, which are the front-end dc/ac, rectifier, and pulsating-dc/ac converters. The dc/ac converter generates width modulated bipolar pulses for HF transformers. The modulated voltage pulses across the secondary sides of the HF transformers are rectified by the ac/pulsating-dc converter to generate the PDCL waveform. An RCD snubber [60] can be used to limit the voltage spikes on the PDCL waveform due to the leakage inductances of the HF transformers and parasitic output capacitors of the ac/pulsating-dc converter. Finally, the pulsating-dc/ac converter generates the LF output sine waveforms using the pulses on the PDCL waveform.

Therefore, the PDCL waveform is synthesized by the dc/ac converter and the pulsating-dc/ac converter uses the synthesized pulses on the PDCL waveform to generate LF output sine waveforms. The soft-switched HM scheme decreases the switching losses of the pulsating-dc/ac converter by decreasing the switching requirement and ZVS operation of the pulsating–dc/ac converter. This section explains the modulation scheme to synthesize the PDCL waveform.

A. Synthesis of the PDCL waveform

The dc/ac converter generates two sets of bipolar pulses for the HF transformers to avoid core saturation. The HFPDCL inverter has two full-bridge modules operating as a dc/ac converter. The first full-bridge module includes S_{11}, $\bar{S}_{11}$, S_{12}, and $\bar{S}_{12}$. The second full-bridge module (using modulator II) includes S_{21}, $\bar{S}_{21}$, S_{22}, and $\bar{S}_{22}$. Each full-bridge module generates a set of bipolar pulses for a HF transformer. Two switches of each leg operate complementary and a proper dead-

time is considered to avoid short-circuit of the input dc bus. Fig. 18 shows the modulation scheme for switching signal generation of the dc/ac converter. A set of normalized three-phase sine-wave references are defined as (1).

$$\begin{aligned} v_{AB} &= m * \sin(\omega t) \\ v_{BC} &= m * \sin\left(\omega t + \frac{2\pi}{3}\right) \\ v_{CA} &= m * \sin\left(\omega t + \frac{4\pi}{3}\right) \end{aligned} \tag{1}$$

where m is modulation index and ω is output line angular frequency of the LF output sine-waves. We also obtain the following relationships for a balanced system:

$$\begin{aligned} v_{ij} + v_{jk} + v_{ki} &= 0 \\ v_{ij} &= -(v_{jk} + v_{ki}) \end{aligned} \tag{2}$$

where $i, j, k \underbrace{\in}_{i \neq j \neq k} \{A, B, C\}$. One can conclude:

$$v_{ij} = |v_{jk} + v_{ki}| \tag{3}$$

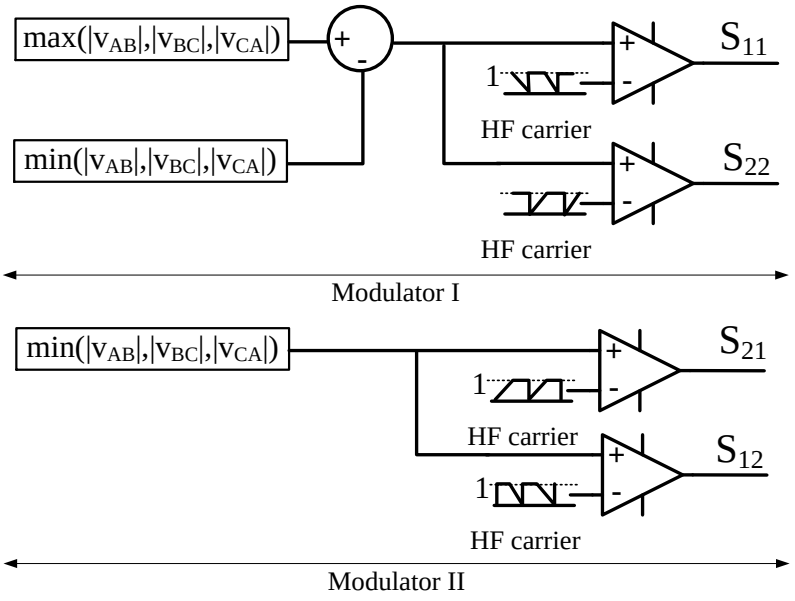


Fig. 18. Switching signal generation for the dc/ac converter (dc/ac modulator), ©2014 IEEE.

Then, following equation are obtained for different 60^o sectors of the output line cycle:

$$|v_{CA}| = |v_{AB}| + |v_{BC}| \qquad 0 < \omega t < \frac{\pi}{3} \text{ or for } \pi < \omega t < \frac{4\pi}{3}. \tag{4}$$

$$|v_{AB}| = |v_{BC}| + |v_{CA}| \qquad \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \text{ or for } \frac{4\pi}{3} < \omega t < \frac{5\pi}{3}. \tag{5}$$

$$|v_{BC}| = |v_{CA}| + |v_{AB}| \qquad \frac{2\pi}{3} < \omega t < \pi \text{ or for } \frac{5\pi}{3} < \omega t < 2\pi. \tag{6}$$

Therefore, the PDCL waveform is required to be compartmentalized in six distinct sectors; that is PI: 0-60^o, PII: 60^o-120^o, PIII: 120^o-180^o, PIV: 180^o-240^o, PV: 240^o-300^o, and PVI: 300^o-360^o. During each sector, the dc/ac converter generates two sets of pulses representing rectified signals v_{AB}, v_{BC}, and v_{CA}. In each sector, the non-maximum voltage reference signal is synthesized by two pulses representing two other non-maximum reference signals as shown in equations (4)-(6). Therefore, the voltage reference signals of the dc/ac modulator change in every 60^o of the line cycle. In sectors PI and PIV, $|v_{CA}|$ is synthesized on the PDCL waveform using two sets of pulses synthesized by $|v_{AB}|$ and $|v_{BC}|$ as the voltage reference signals. These two sets of pulses are generated by the two-full-bridge modules of the dc/ac converter. In sectors PII and PV, $|v_{AB}|$ is synthesized on the PDCL waveform using $|v_{BC}|$ and $|v_{CA}|$ as the voltage reference signals of the full-bridge modules of the dc/ac converter. Finally, in sectors PIII and PVI, $|v_{BC}|$ is synthesized using two sets of pulses synthesized by $|v_{AB}|$ and $|v_{CA}|$ as the voltage reference signals of the full-bridge modules of the dc/ac converter.

Equations (4)-(6) can be rewritten as:

$$|v_{BC}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \qquad 0 < \omega t < \frac{\pi}{6} \text{ or for } \frac{\pi}{2} < \omega t < \frac{2\pi}{3} \tag{7}$$

$$|v_{CA}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \qquad \frac{\pi}{3} < \omega t < \frac{\pi}{2} \text{ or for } \frac{5\pi}{6} < \omega t < \pi \tag{8}$$

$$|v_{AB}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \qquad \frac{\pi}{6} < \omega t < \frac{\pi}{3} \text{ or for } \frac{2\pi}{3} < \omega t < \frac{5\pi}{6} \tag{9}$$

Using equations (7)-(9), Modulator I of the dc/ac modulator can be implemented using the maximum and minimum signals of $|v_{AB}|$, $|v_{BC}|$, and $|v_{CA}|$. This approach makes the implementation of the dc/ac modulator just based on the maximum and minimum function of the voltage reference signals.

For example, when ωt is between 0 and π/6, $|v_{CA}|$ is the maximum of the rectified signals v_{AB}, v_{BC}, and v_{CA} and $|v_{AB}|$ is the minimum of the rectified signals v_{AB}, v_{BC}, and v_{CA}. Therefore, the voltage reference signal of Modulator I is $|v_{CA}|$ minus $|v_{AB}|$, which is equal to $|v_{BC}|$. Modulator II uses $|v_{AB}|$ (the minimum reference signal) as its voltage reference signal. Therefore, a set of pulses are synthesized by $|v_{AB}|$ and the other set of the pulses are synthesized by $|v_{BC}|$ on the PDCL waveform. Then, the average of two resulting consecutive pulses on the PDCL waveform over the switching cycle is equal to $|v_{CA}|$ (the maximum reference signal). The duration of the synthesized zero states between these two sets of pulses on the PDCL waveform are calculated as follows:

$$z(t) = 1\text{-}\max(|v_{AB}|,|v_{BC}|,|v_{CA}|) \tag{10}$$

These zero states on the PDCL waveform are used to achieve ZVS operation for the switches of the pulsating-dc/ac converter. Therefore, $|v_{AB}|$ and $|v_{BC}|$ are directly synthesized on the PDCL waveform by two full-bridge modules of the dc/ac converter. Also, $|v_{CA}|$ is indirectly synthesized on the PDCL waveform as two consecutive pulses. Therefore, all the required voltage reference signals are synthesized on the PDCL waveform. As a result, two legs of the pulsating-dc/ac converter do not switch while the other leg switches at middle of the provided zero states on the PDCL waveform to achieve ZVS condition. The soft-switched HM scheme for the pulsating-dc/ac converter is explained in the following section.

As shown in Fig. 18, the HF carrier of Modulator I has 180^o phase shift with respect to the HF carrier of Modulator II of the dc/ac converter. Therefore, the dc/ac converter generates a set of bipolar pulses at the end and beginning of the switching cycle. But, it also generates a set of bipolar pulses at the middle of the switching cycle. Consequently, two sets of the generated pulses by the full-bridge modules of the dc/ac converter have 180^o phase shift with respect to each other.

Fig. 19 shows the HF carriers, references, signal-waveforms of Modulator I and Modulator II of the dc/ac converter, bipolar pulses for the HF transformers, and the resulting PDCL voltage waveform. As shown in Fig. 19, two sets of pulses with 180^o phase shift are generated on the PDCL waveform with enough zero states to enable ZVS condition for the pulsating-dc/ac converter. As a result, the average of two consecutive pulses on the PDCL waveform over the switching cycle is equal to the maximum of the rectified signals v_{AB}, v_{BC}, and v_{CA}.

B. Soft-switched hybrid modulation for the pulsating-dc/ac converter

The modulation scheme to generate the required PDCL waveform for pulsating-dc/ac converter is described in the previous section. The two sets of generated pulses by the full-bridge modules of the dc/ac converter are used to decrease the switching requirement of the pulsating-dc/ac converter. Also, the zero states on the PDCL waveform are used to provide ZVS condition for the pulsating-dc/ac converter. The modulation scheme to generate switching signals for three legs of the pulsating-dc/ac converter is shown in Fig. 20. The sign of v_{AB} (as represented by sgn(v_{AB})) is used to generate the complementary pulses for the second half of the line cycle. Each leg of the pulsating-dc/ac converter does not switch for two-thirds of the line cycle. For instance, the first leg of the pulsating-dc/ac converter operates only at HF when $|v_{BC}|$ is greater than $|v_{AB}|$ and $|v_{CA}|$. The available zero states on the PDCL waveform are calculated using (10). Therefore, the term z(t)/2 is

added to the reference signals of the comparators to operate at middle of the zeros states on the PDCL waveform. As a results, the switches of the pulsating-dc/ac converter turn off/on when the voltage across the PDCL waveform is zero. Fig. 21 shows a simplified operation overview of the soft-switched HM. The dc/ac and pulsating-dc/ac modulators are respectively described in Fig. 19 and Fig. 20. A sine-wave rectifier is used to provide rectified sine-wave voltage reference signals (v_{AB}, v_{BC}, and v_{CA}) for the dc/ac and pulsating-dc/ac modulators. These modulators have synchronous carriers to achieve ZVS condition for the pulsating-dc/ac converter. The generated pulses for the pulsating-dc/ac converter are inverted when the sign of signal v_{AB} changes. Therefore, the sign of v_{AB} is provided for the pulsating-dc/ac modulator. The signals v_{AB}, v_{BC}, and v_{CA} are the output of the controller for close loop of the HFPDCL inverter. Fig. 22 illustrates the switching scheme of the pulsating-dc/ac converter and the zero states on the PDCL over a line cycle. Figs. 6b-6d show the required gate signals to extract the desired phase-to-phase output voltages using the soft-switched HM. The resulting output voltage, v_{ba}, is depicted in Fig. 6e before and after the output filter stage. Topological modes of operation are thoroughly presented in the next section. In order to study the topological modes of operation of the HFPDCL inverter using the soft-switch HM, an equivalent circuit is derived as shown in Fig. 23. It is obtained by eliminating the HF transformers and simplifying the dc/ac converter to analyze the soft-switching operation of the soft-switched HM. The voltage supplies (v_{1s} and $v_{2s)}$ represent the secondary reflected voltages of transformers T_1 and T_2, while the inductors are the secondary-side leakage inductances. The capacitors across the switches of the pulsating-dc/ac converter represent the parasitic capacitors of the switches.

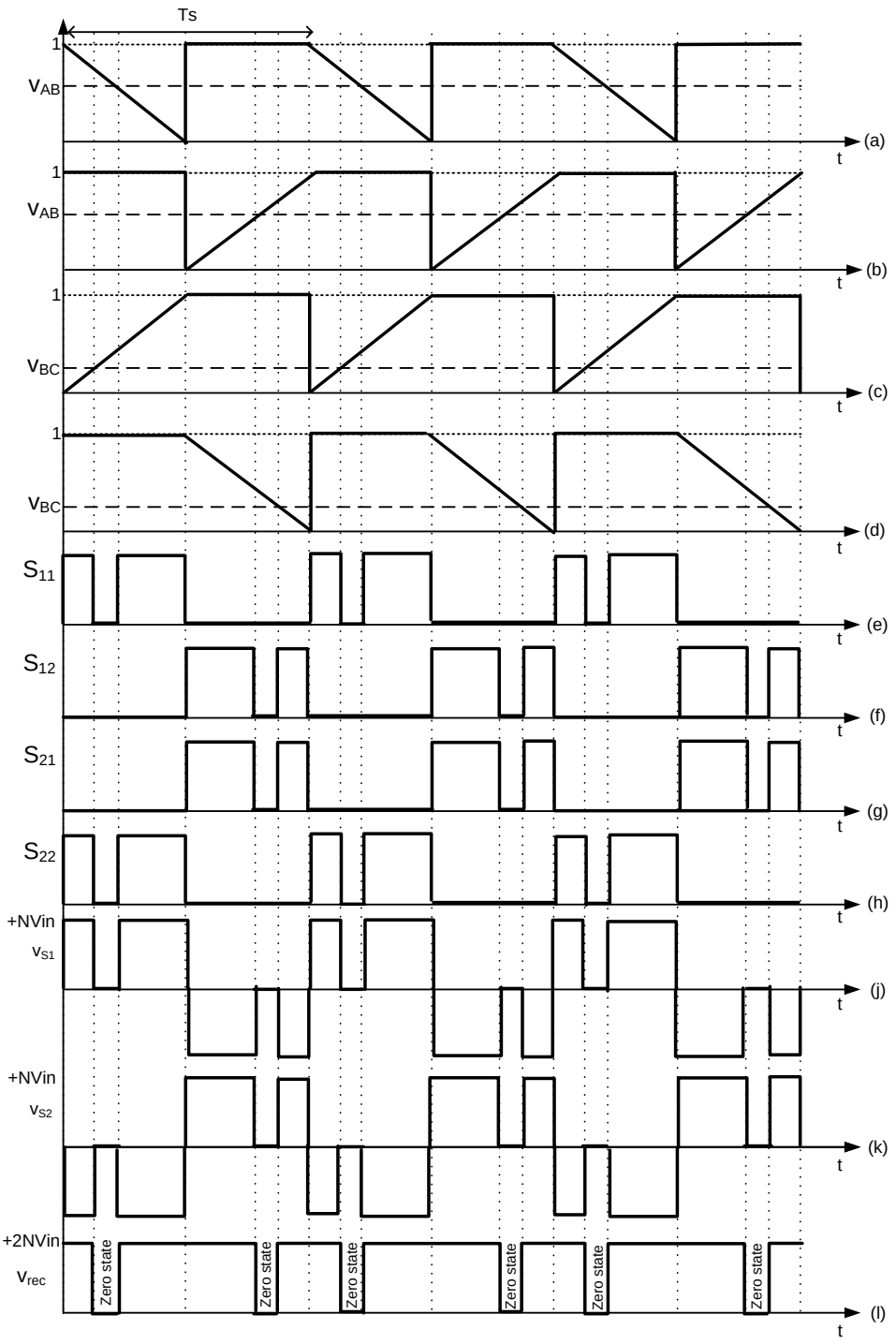


Fig. 19. Pulse placement on the PDCL using the dc/ac converter to provide zero states: (a)-(d) the HF carriers and references of the full-bridge modules of the dc/ac converter to generate bipolar pulses for HF transformers, (e)-(h) the synthesized gate signals of S_{11}, S_{21}, S_{21}, and S_{22}, (j)-(k) the secondary voltages of the HF transformer, and (l) the generated PDCL waveform, ©2014 IEEE.

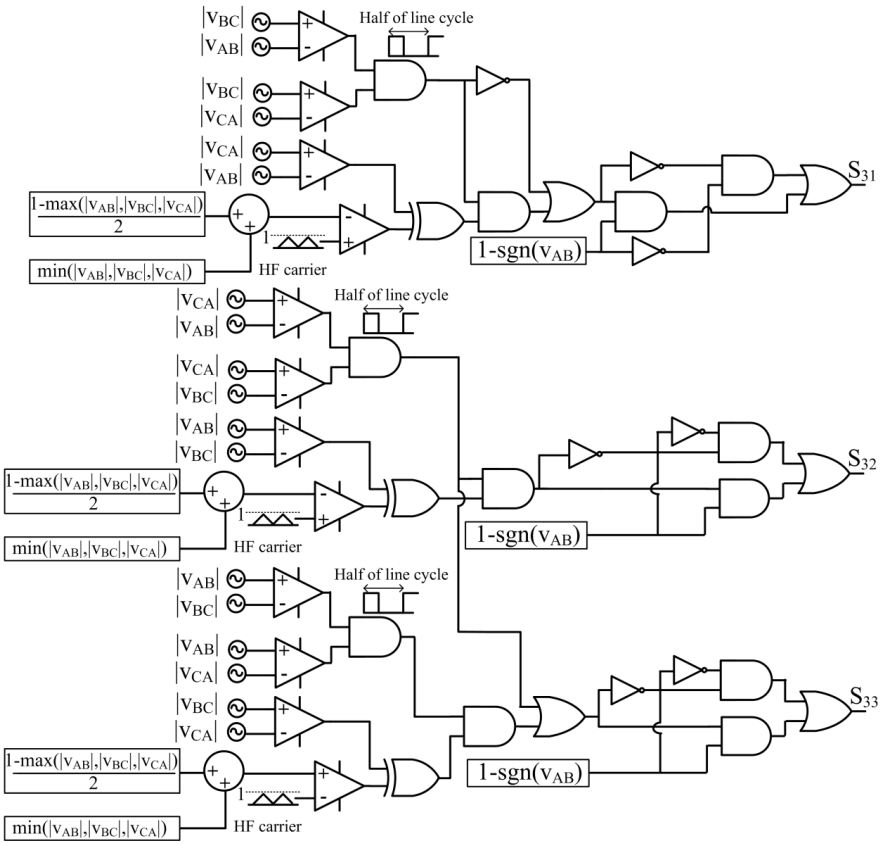


Fig. 20. Switching signals generation for the pulsating-dc/ac converter, ©2014 IEEE.

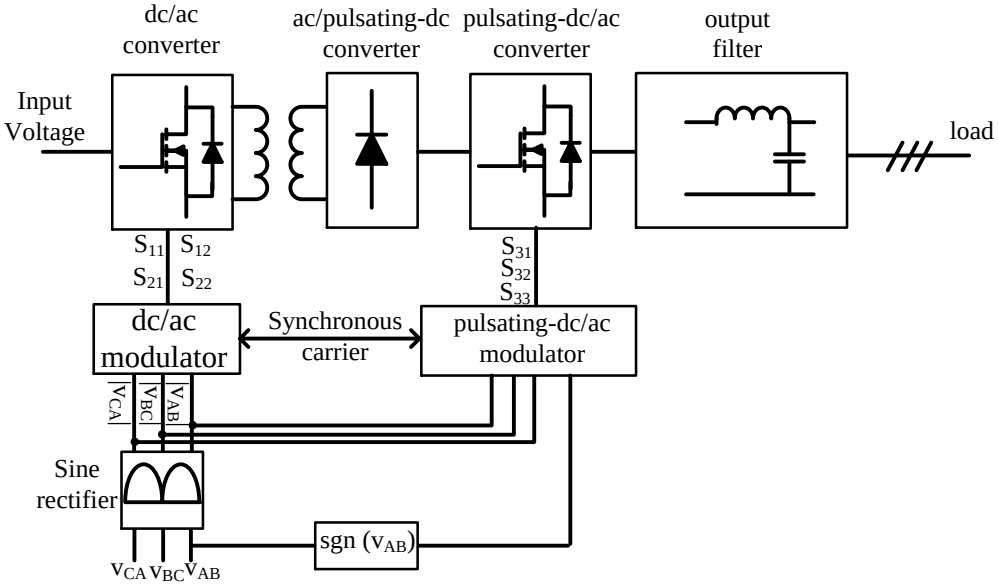


Fig. 21. A simplified operation overview of the HFPDCL inverter using the soft-switched HM, ©2014 IEEE.

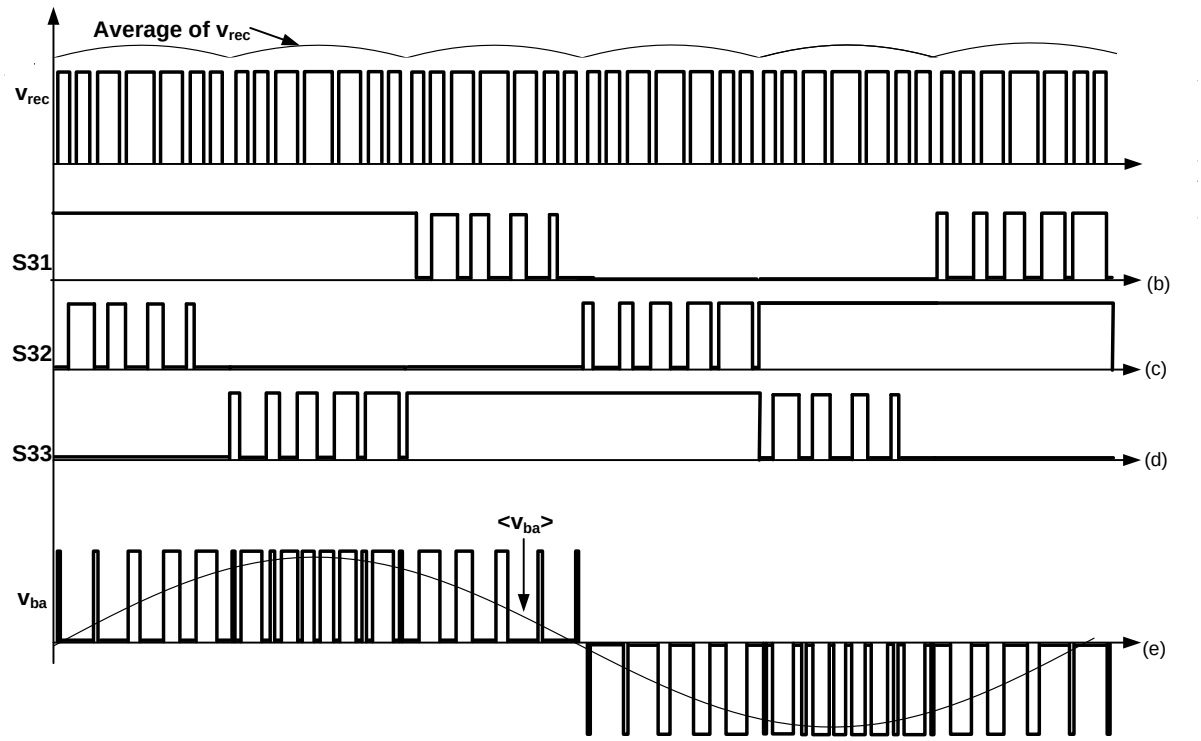


Fig. 22. Switching functions and waveforms of the soft-switched HM: (a) PDCL, (b)-(d) gate signals of pulsating-dc/ac converter switches, and (e) resulting phase-to-phase voltage before and after the output filters, ©2014 IEEE.

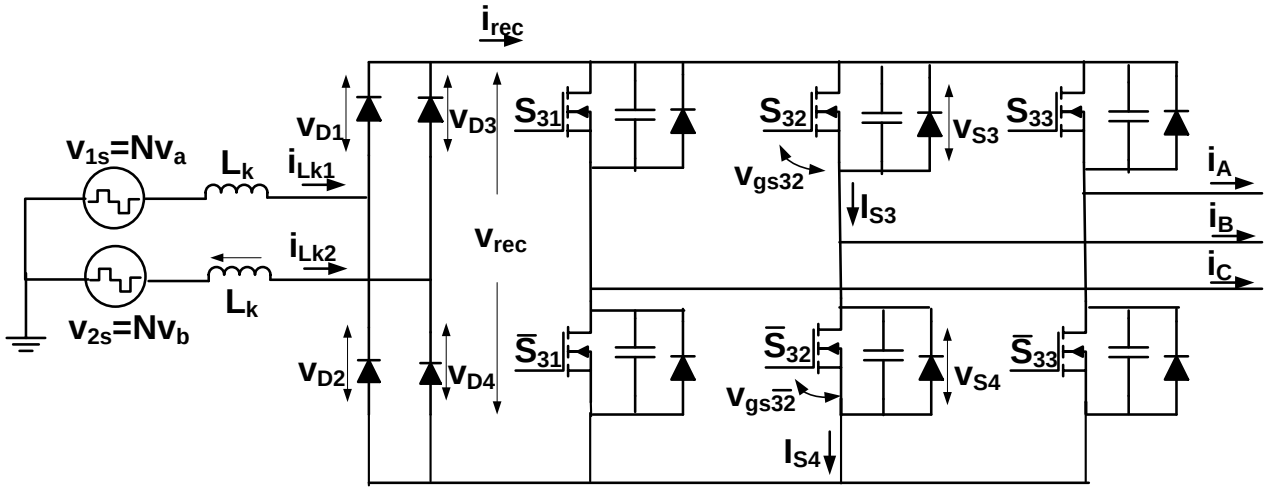


Fig. 23. Equivalent circuit of the ac/pulsating-dc converter, HF transformers, and the front-end pulsating-dc/ac converter to study topological modes of operation, ©2014 IEEE.

C. Modes of Operation

To analyze the modes of operation, the following assumptions are made:

- The voltage drops of the diodes and conduction losses of the switches are neglected;
- The dead time considered for the complementary switches of the pulsating-dc/ac converter is disregarded (it should be noted that switches of the pulsating-dc/ac converter operate at zero states, therefore; no dead time is necessary for complementary switches of the converter);
- The currents are considered to be constant during switching cycle.
- The currents and voltages are assumed to be balanced three-phase sinusoidal waveforms; that is,

$$\begin{aligned} i_A &= I_m \sin(\omega t + \gamma) \\ i_B &= I_m \sin\left(\omega t + \gamma + \tfrac{2\pi}{3}\right) \\ i_C &= I_m \sin\left(\omega t + \gamma + \tfrac{4\pi}{3}\right) \end{aligned} \tag{11}$$

where I_m is the peak value of the line output currents and γ represents the power factor of the output load, which is negative for inductive load. A HFPDCL inverter with diode rectifier supports a power factor up to 30^o according to [55]-[57]. Due to symmetry, the soft-switching operation of a leg of the pulsating-dc/ac converter is analyzed, which operates at HF.

In this section, $|v_{CA}|$ is greater than $|v_{AB}|$ and $|v_{BC}|$ and the sign of v_{AB} is negative. Therefore, switches S_{31}, $\bar{S}_{31}$, S_{33}, and $\bar{S}_{33}$ do not switch. However, the second leg of the pulsating-dc/ac converter consisting of S_{32} and $\bar{S}_{32}$ operates at HF. Currents i_A and i_C are positive, but i_B is negative.

The topological modes of operation and the key waveforms are respectively shown in Figs. 24 and 25.

Mode 1 ($t_0 < t < t_1$): Before t_0, S_{32} is off and i_B is shared between $\bar{S}_{32}$ and the body diode of S_{32}. Therefore, all the diodes of the ac/pulsating-dc converter are off and the currents freewheel in the legs of the pulsating-dc/ac converter. Therefore, the PDCL voltage (v_{rec}) and current (i_{rec}) are zero. Hence, the second leg (S_{32} and $\bar{S}_{32}$) is switched under ZVS turn-on/off condition. This mode ends when v_{rec} starts to rise from zero.

Mode 2 ($t_1 < t < t_2$): At $t = t_1$, the voltage of the PDCL waveform starts to rise from zero. Before this instant, the voltage across parasitic capacitors of the switches is zero. Thus, D_1 and D_4 start to conduct to supply the required current for charging the parasitic capacitors of $\bar{S}_{31}$, $\bar{S}_{32}$, and S_{33}.

Voltage supplies v_{1S} and v_{2S} are respectively equal to $-NV_{in}$ and $+NV_{in}$. The current i_A is positive and S_{31} is on. Consequently, the required current to charge the parasitic capacitor of $\bar{S}_{31}$ is supplied by a path through S_{31}. The voltage across the parasitic capacitors is calculated as follows:

$$\begin{aligned} v_{s2} &= v_{s4} = v_{s5} = v_c \\ 2NV_{in} &= 2L_k \frac{di_{Lk2}}{dt} + v_c \\ i_{c2} &= i_{c4} = i_{c5} = C\frac{dv_c}{dt} \end{aligned} \tag{12}$$

We can rewrite (10) as follows:

$$2NV_{in} = 2L_kC\frac{d^2v_c}{dt^2} + v_c \tag{13}$$

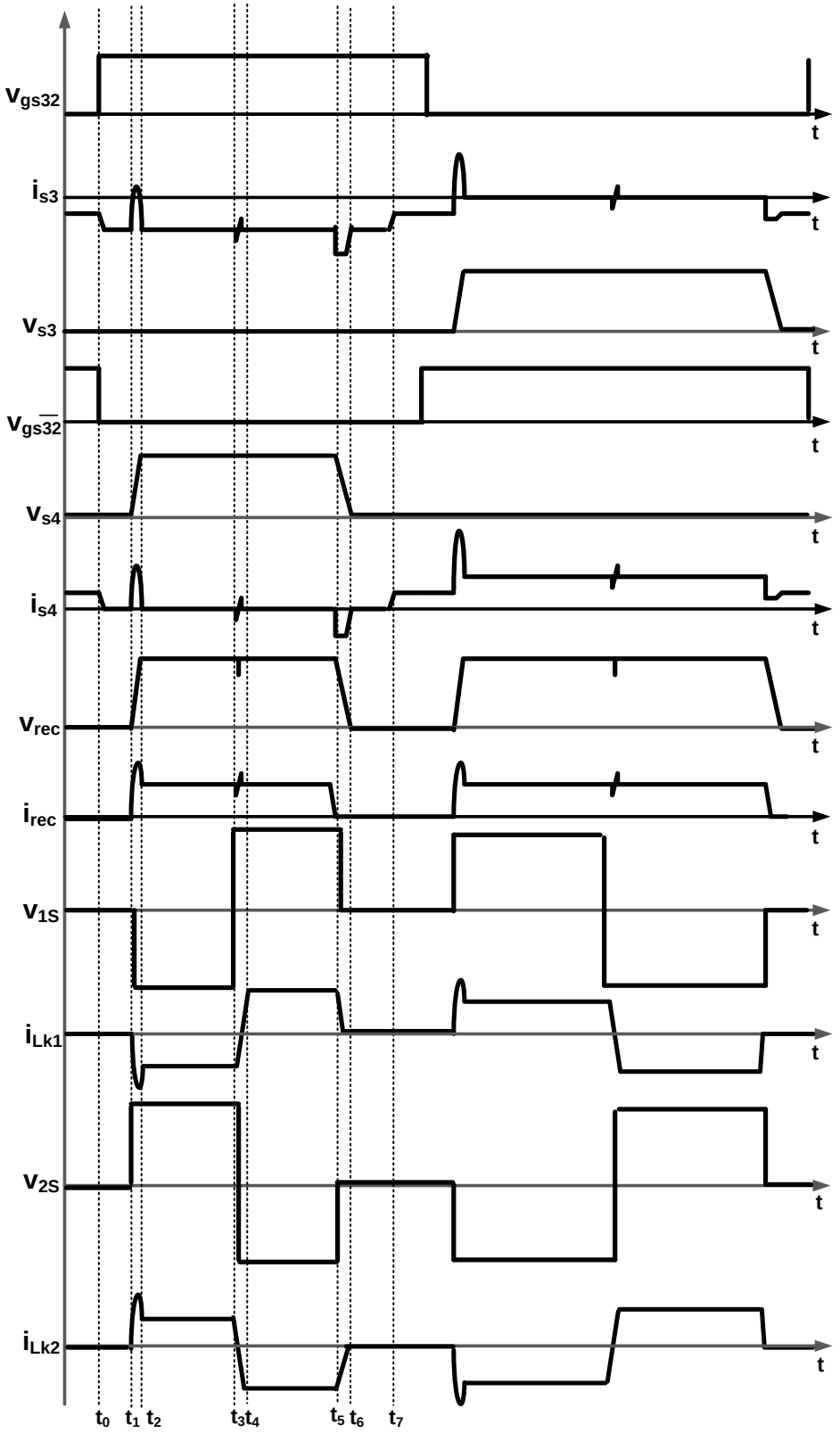
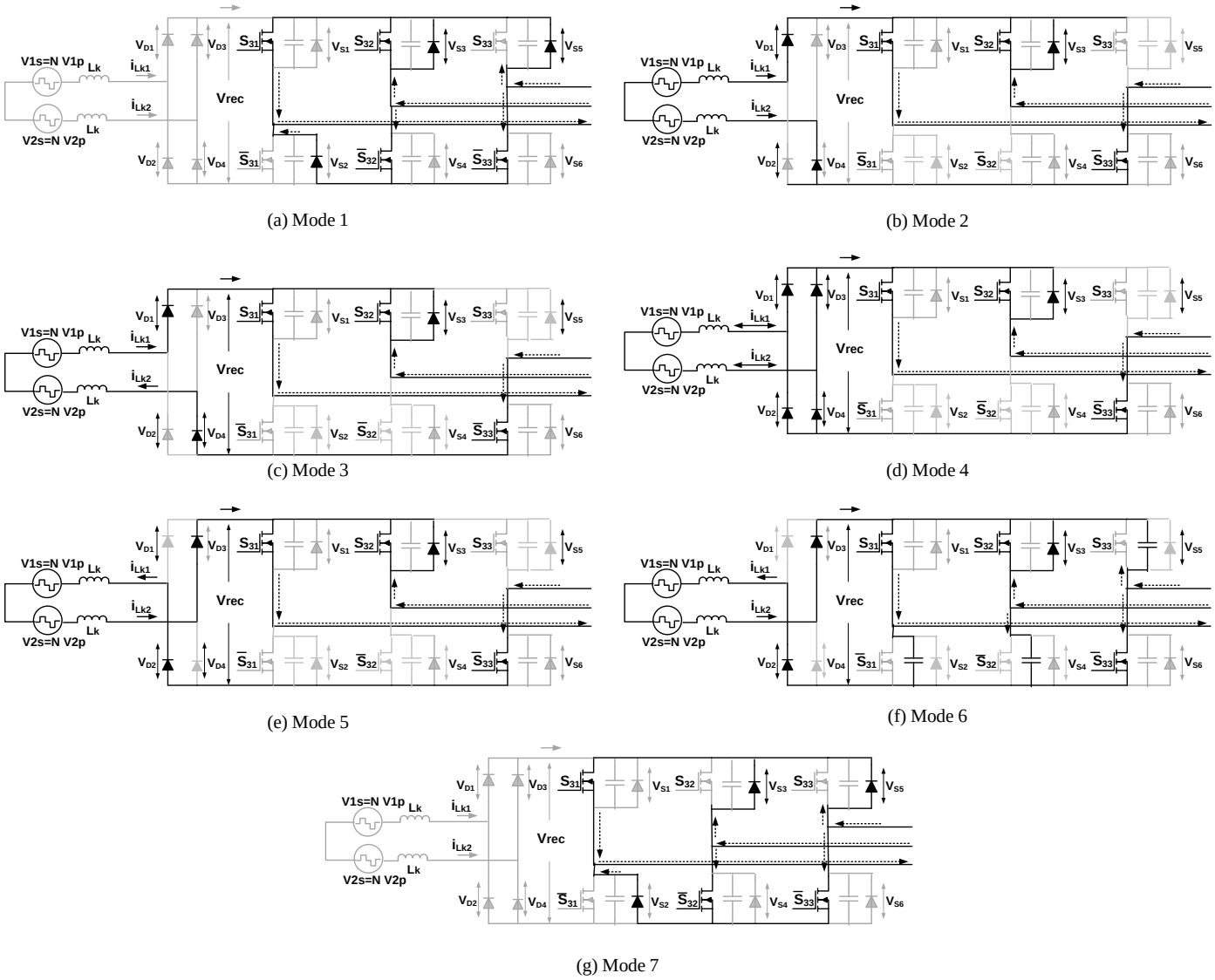


Fig. 24. Key waveforms of the equivalent circuit shown in Fig. 23 to study the soft-switching operation of the pulsating-dc/ac converter, ©2014 IEEE.



(a) Mode 1

(b) Mode 2

(c) Mode 3

(d) Mode 4

(e) Mode 5

(f) Mode 6

(g) Mode 7

Fig. 25. Topological modes of the equivalent circuit shown in Fig. 23 to study the soft-switching operation of the pulsating-dc/ac converter, ©2014 IEEE.

According to (12), the resonant paths between the parasitic capacitors and the leakage inductances of the HF transformers build up the voltage of $\bar{S}_{31}$, $\bar{S}_{32}$, and S_{33}. This mode ends at t = t_2 when the voltage of the parasitic capacitors reaches their final value, which is equal to $2NV_{in}$.

Mode 3 ($t_2 < t < t_3$): At the beginning of this mode, the PDCL voltage waveform reached its final value. The currents are supplied by the PDCL. The current of the leakage inductances remains constant because their voltages are zero. At the end of this mode, v_{1S} and v_{2S} change their polarity.

Mode 4 ($t_3 < t < t_4$): In this mode, v_{1S} and v_{2S} are constant and respectively equal to NV_{in} and -NV_{in}. There are two commutations in the ac/pulsating-dc converter to change the current directions of the leakage inductances. As a result, D_1 commutes with D_2 and D_3 takes over the current of D_4. The commutation times of the diodes are neglected here. Therefore, all the diodes conduct in this mode of operation. The leakage currents are taken over by D_3 and D_2 at the end of this mode. Therefore, the leakage inductance currents are equal and calculated as:

$$2L_k \frac{di_{Lk1}}{dt} = +2NV_{in} \tag{14}$$

$$i_{Lk1}(t) = i_{Lk1(t_3)} + \frac{NV_{in}}{L_k}(t - t_3)$$

Finally, the currents of leakage inductance are equal to the PDCL current.

Mode 5 ($t_4 < t < t_5$): This mode of operation starts when the currents of leakage inductances reached their final value to support the balanced output currents. Similar to Mode 3, the voltages across the leakage inductances are zero, consequently; the leakage currents are constant. At the end of this mode, v_{1S} and v_{2S} become zero and the leakage currents start to decrease.

Mode 6 ($t_5 < t < t_6$): The PDCL voltage waveform tends to decrease, because the secondary winding voltages are zero. As a result, the body capacitors of $\overline{S}_{31}$, $\overline{S}_{32}$, and S_{33} are being discharged by output load currents.. This mode ends when the leakage currents become zero and load currents start to freewheel again in the pulsating-dc/ac converter. In this mode of operation, S_{32} turns off under zero voltage turn-off condition because the voltage of the PDCL waveform is zero.

Mode 7 ($t_6 < t < t_7$): $\overline{S}_{32}$ is off and i_B must pass through the S_{32} and its body diode. $\overline{S}_{32}$ turns on under zero-voltage turn on condition. Similar to Mode 1, the load current shares between S_{32} and $\overline{S}_{32}$. Therefore, the load currents again freewheel in the pulsating-dc/ac converter. The ZVS

operation of the other switches has the same principle of operation during other operation conditions.

D. Conclusion

The dc-link capacitors are eliminated from the inverter topology to increase the power density and reliability of the inverter. Different pulses can be generated on the pulsating-dc link (PDCL) waveform by eliminating the dc-link capacitors. Two streams of pulses are synthesized on the PDCL waveform to provide soft-switching condition for the pulsating-dc/ac converter. Each stream of pulse is synthesized by a different reference signal during different operating sectors. Therefore, the PDCL waveform is compartmentalized in six different operating sectors during each line cycle. As a result, two legs of the pulsating-dc/ac converter do not commutate during each operating sector. The remaining leg of the pulsating-dc/ac converter operates at high frequency under zero-voltage switching condition. Therefore, the switching losses of the pulsating-dc/ac converter are practically mitigated up to 100%. The next chapter verifies the operation of the soft-switched hybrid modulation for a 1 kW HFPDCL inverter. The soft-switched HM scheme decreases the switching requirement of the pulsating-dc/ac converter and provide ZVS condition. However, it increases the switching requirement of the front-end dc/ac and the ac/pulsating-dc converters.

IV. Experimental Results for Validating the Soft-Switched Hybrid Modulation

(Parts of this chapter, including figures and text, are based on my journal paper [59], ©2014 IEEE)

Chapter III discussed the analysis and implementation of the soft-switched HM for a HFPDCL inverter. Chapter three presents experimental results to verify the performance of the soft-switched HM. A 1 kW HFPDCL inverter is implemented to compare the performance of the different present modulation schemes and the soft-switched HM. Therefore, the efficiencies, THD, and different aspects of these modulation schemes are provided to comment on the advantages and disadvantages of the soft-switched HM. As mentioned in Chapter two, the HFPDCL inverter has two conversion stages: The first stage is comprised of the dc/ac converter, HF transformers and the ac/pulsating-dc converter; the second stage is comprised of the pulsating-dc/ac converter to generate the output sinewaves based on the provided pulses on the PDCL waveform. The dc/ac converter operates at low voltage and high current condition. Therefore, conduction loss is dominant for the dc/ac converter. As a result, low-voltage MosFETs are used, which have lower on-resistance to decrease the conduction losses.

Nano-crystalline cores are used as the magnetics of the HF transformers to decrease the size and core losses of the transformers. The leakage inductances of the HF transformers are minimized to limit the voltage stress on the diodes of the ac/pulsating-dc converter. At the secondary side of the HF transformer, the voltage is higher and current is lower. Therefore, the switching loss is dominant for the ac/pulsating-dc and pulsating-dc/ac converter. The specifications and main components of the implemented HFPDCL inverter for validating the operation of the soft-switched HM scheme are summarized in TABLE II. Fig. 26 shows the implemented prototype of the HFPDCL inverter to validate the soft-switched HM. The output filter capacitors and inductors are respectively 5 μF

and 1 mH. The secondary-side voltage and current of a HF transformer of the HFPDCL inverter are shown in Fig. 27. The secondary-side voltage waveforms of the HF transformers are rectified by the ac/pulsating-dc converter to generate the PDCL waveform. The Fig. 28 shows the resulting PDCL waveform using the explained modulation scheme in Section II for the dc/ac converter. The resulting zero states on the PDCL waveform provide ZVS turn-on/off condition for the pulsating-dc/ac converter. These two pulses with different widths are related to different output sine-wave reference voltage signals.

TABLE II. THE SPECIFICATIONS AND MAIN COMPONENTS OF THE HFPDCL INVERTER.

Frequency	**Input voltage**	**Output phase-to-phase voltage**	**Output power**	**Transformer turns ratio**
21.6 kHz	40 V	208 V	1 kW	1:4.2
Name	**Components**			
dc/ac converter	IRF3808; MOSFET, 75 V, 140 A, 7 mΩ			
ac/pulsating-dc converter	D06S60; 600 V, 6A			
pulsating-dc/ac converter	IPW60R045CP; 650V, 60A, 45 mΩ			
transformers	Nano-crystalline core			

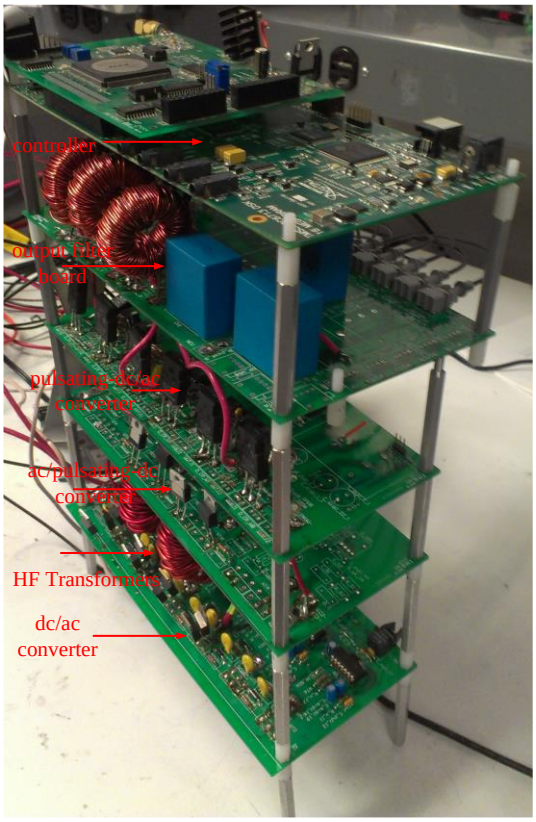


Fig. 26. The implemented prototype to validate the soft-switched hybrid modulation.

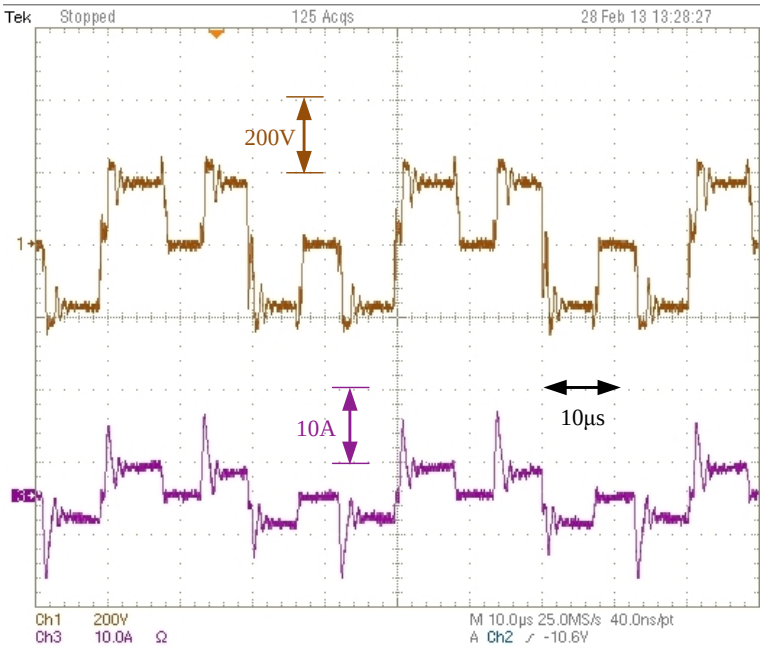


Fig. 27. The secondary-side voltage and current of a HF transformer of the inverter.

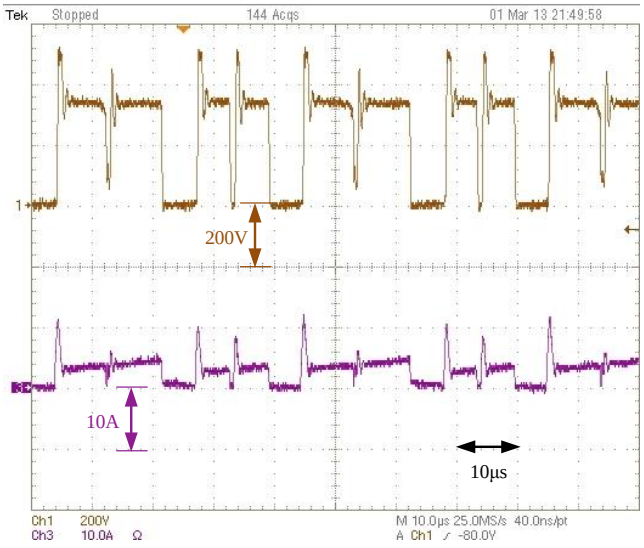


Fig. 28. PDCL voltage and current waveform of the HFPDCL inverter using the soft-switched HM. Each switching cycle contains two pulses that represent different output sine-wave reference voltage signals as explained in Section II.

A. Output waveforms

Fig. 29a shows the three-phase output sine-wave voltages using soft-switched HM modulation for a 1 kW resistive load. The respective output phase voltages and currents of the HFPDCL inverter

are shown in Figs. 29b-29d. The THD of the HFPDCL inverter for the soft-switched HM, the conventional HM, and square-wave modulation is shown in Fig. 30. The soft-switched HM shows a more promising THD because of soft-switching of the pulsating-dc/ac converter. The resulting THD of the HFPDCL inverter is well below 5% for a wide range of the output powers for the soft-switched HM.

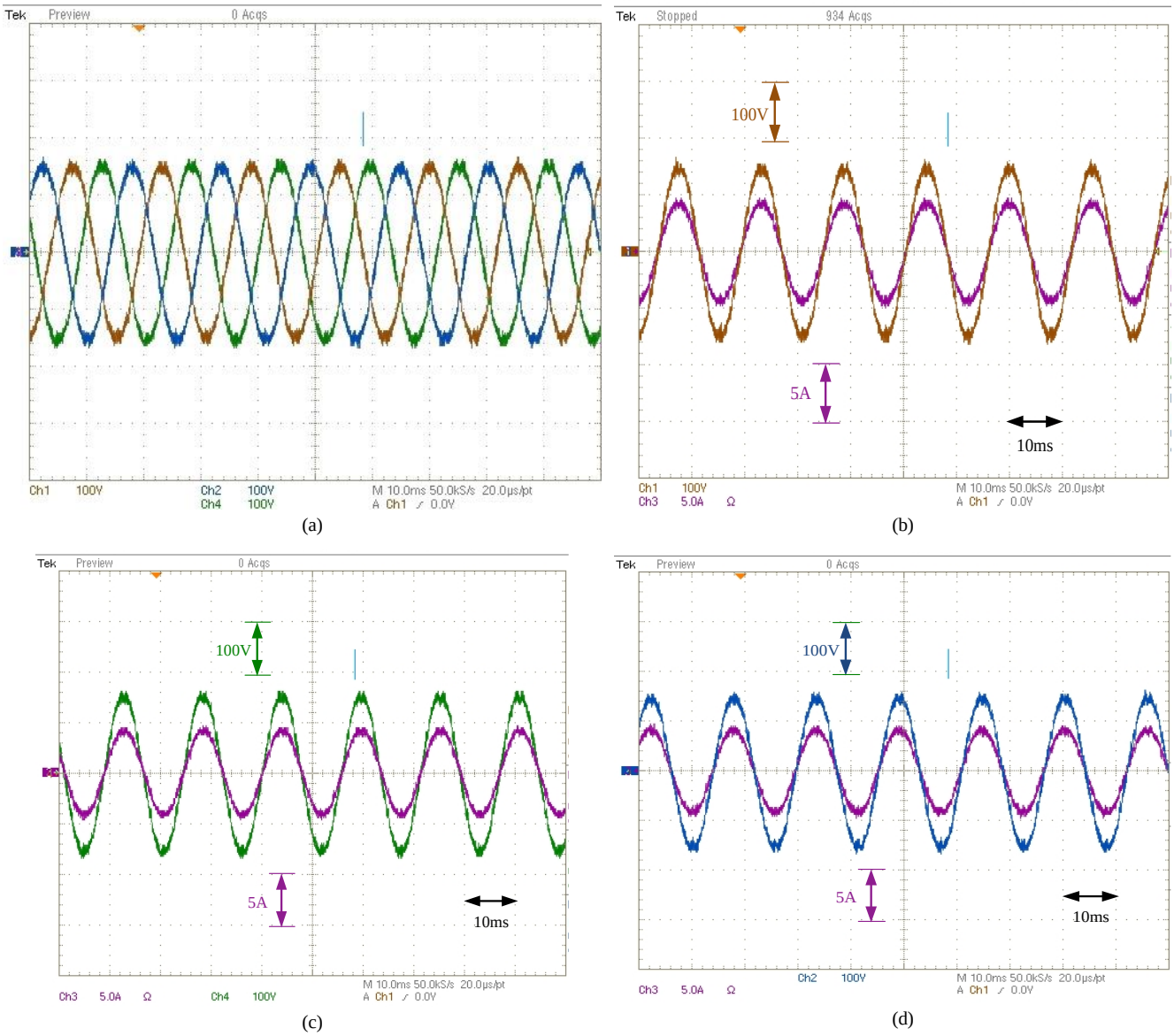


Fig. 29. Output phase voltages and currents for a 1-kW resistive load: (a) three phase output voltage, (b) voltage and current of phase A, (c) voltage and current of phase B, and (d) voltage and current of phase C.

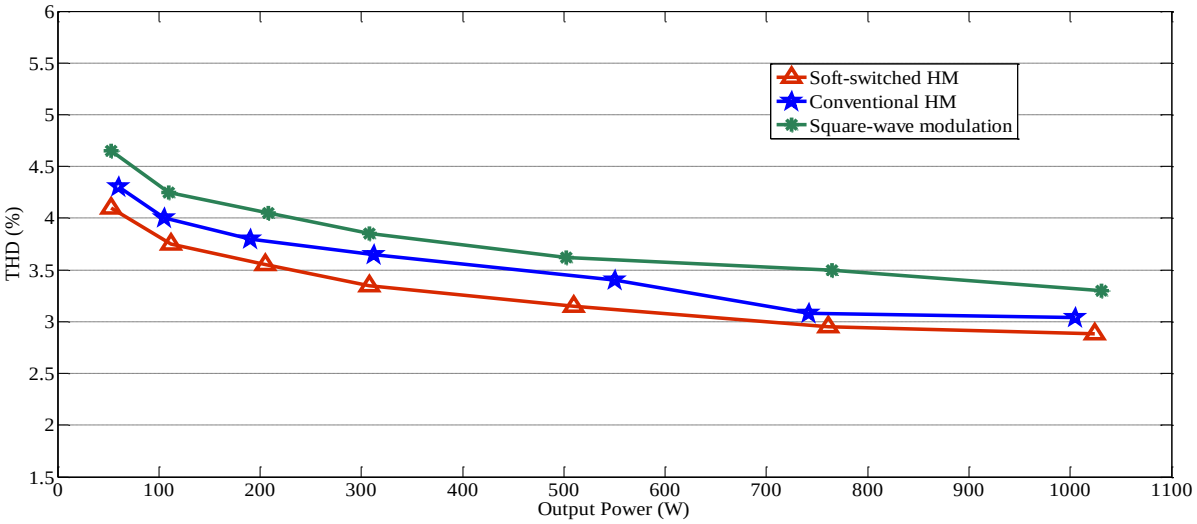


Fig. 30. Output current THD vs. output power of the inverter, ©2014 IEEE.

B. ZVS Operation of the Soft-Switched HM Scheme

The ZVS soft-switching operation of the pulsating-dc/ac converter is shown in Fig. 31. All of the switches turn-on/off in the zero states available on the PDCL voltage waveform. The ZVS operation and performance of the HFPDCL inverter using soft-switched HM scheme is evaluated when the inverter supplies an induction motor. The power factor of the motor is about 30º. The obtained output voltage and current of a phase of the HFPDCL inverter is shown in Fig. 32. The THD of the output voltage of the inverter is 4.7% for this inductive load. Fig. 33 shows the ZVS operation of the HFPDCL inverter for the first leg of the pulsating-dc/ac converter when the HFPDCL inverter supplies the induction motor. A three-phase diode rectifier is used as a nonlinear load for the implemented HFPDCL inverter. Fig. 34 shows the output voltage and current waveforms of the inverter when it supplies a nonlinear load. The THD of the output voltage is 4.85% when the output power is 1kW. The soft-switching operation of the inverter for the first leg of the inverter is shown in Fig. 35.

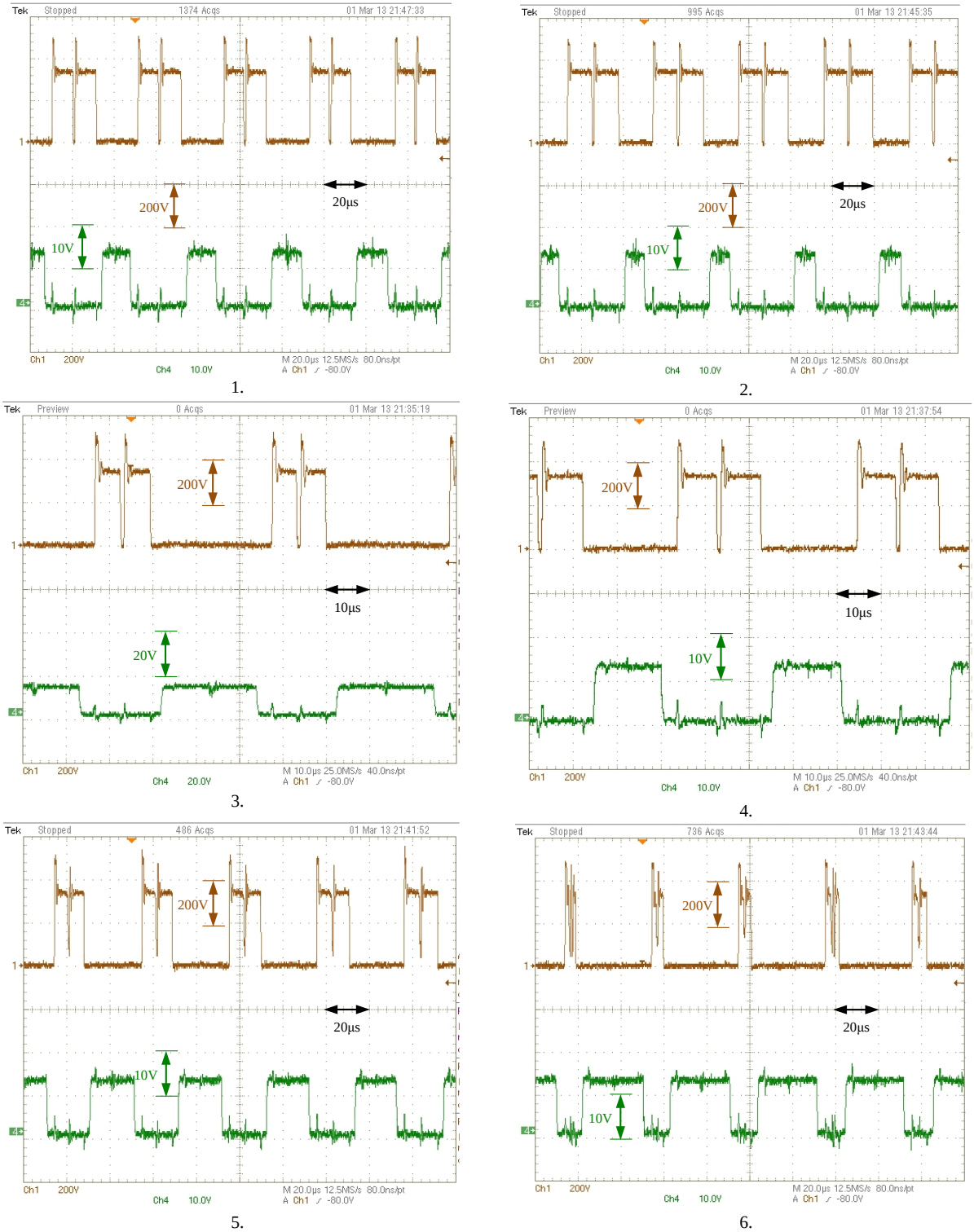


Fig. 31. Soft-switching operation of all switches of the pulsating-dc/ac converter: (a) S_{31}, b) $\bar{S}_{31}$,(c) S_{32}, (d) $\overline{S}_{32}$, (e) S_{33}, and (f) $\bar{S}_{33}$ (Ch1: drain to source voltage, and CH4: gate voltage).

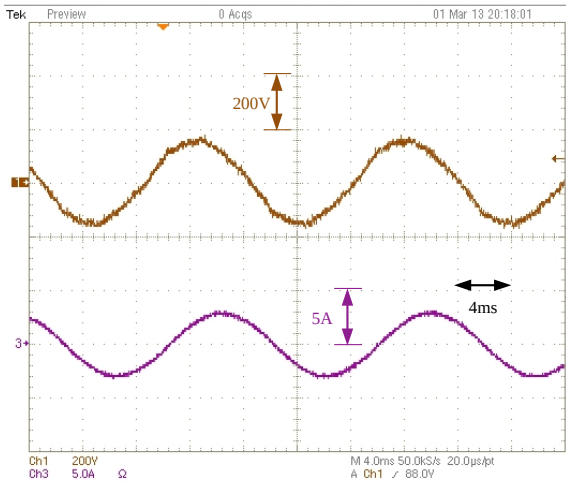
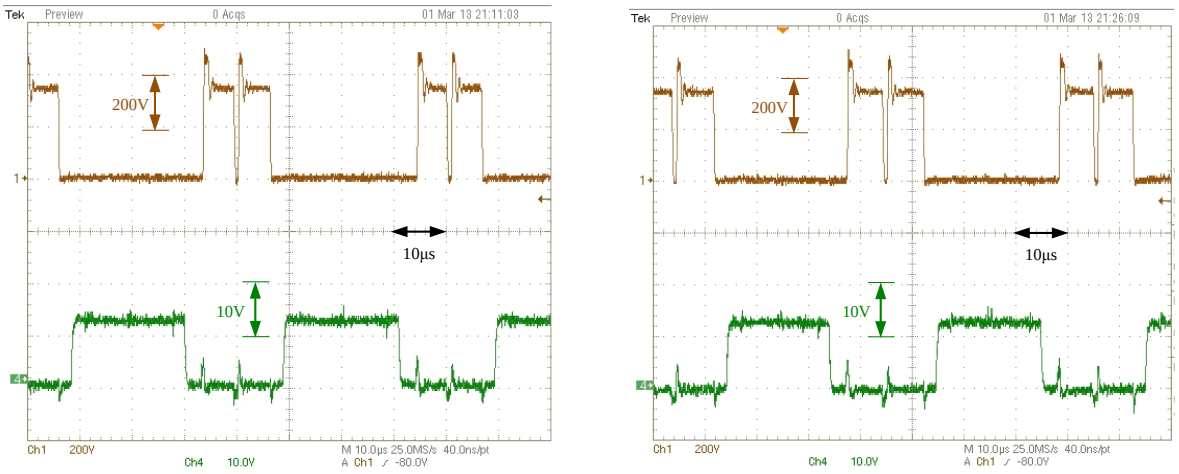


Fig. 32. The output phase voltage and current of a phase of the HFPDCL inverter when it supplies an induction motor.



(a) (b)

Fig. 33. Soft-switching operation of the first leg of the pulsating-dc/ac converter when it supplies an induction load: (a) S_{31}, b) $\bar{S}_{31}$ (Ch1: drain to source voltage, and CH4: gate voltage).

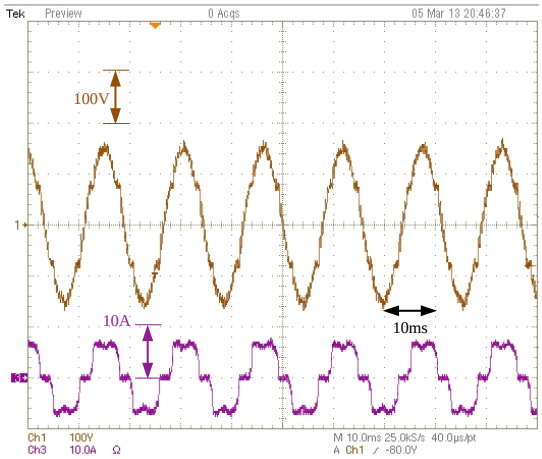
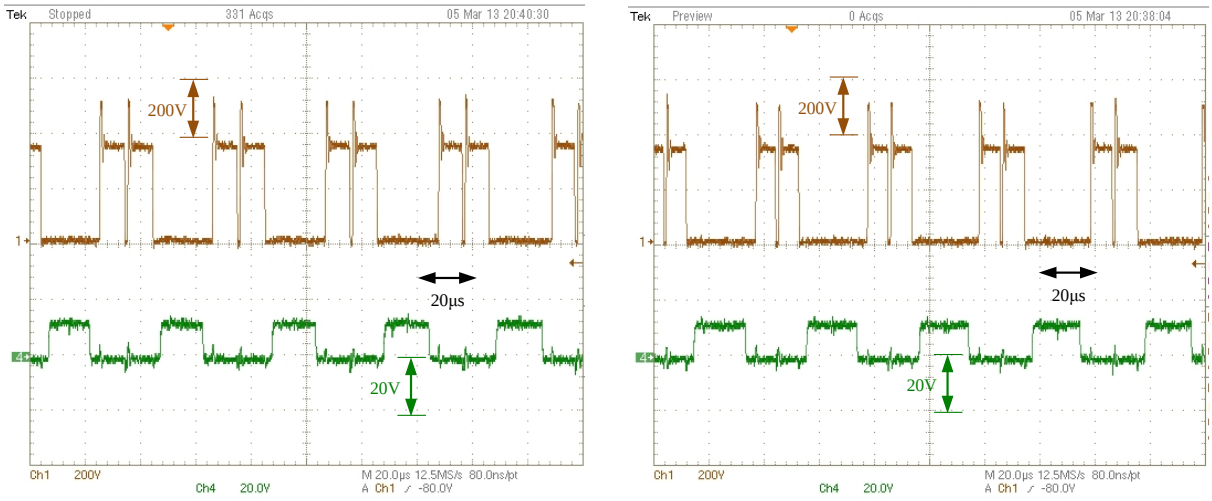


Fig. 34. The output voltage and current of a phase of the HFPDCL inverter when it supplies a nonlinear load.



(a) (b)

Fig. 35. Soft-switching operation of the first leg of the pulsating-dc/ac converter when it supplies a nonlinear load: (a) S_{31}, b) $\bar{S}_{31}$ (Ch1: drain to source voltage, and CH4: gate voltage).

C. Efficiency and THD

The efficiency of the soft-switched HM scheme, the conventional HM and the square-wave modulation scheme in [54] for HFPDCL inverters are compared using the implemented inverter. The achieved efficiencies for the HFPDCL inverter using the mentioned schemes are shown in Fig. 36. The efficiency of the pulsating-dc/ac converter is increased using the soft-switched HM compared to other modulation schemes. The efficiency of the three stage of the HFPDCL inverter is depicted in Fig. 37. The conduction loss of the dc/ac converter is dominant because of high current rating of the front-end stage. However, the ac/pulsating-dc and pulsating-dc/ac converters have considerably lower conduction loss. Therefore, switching loss is dominant at the stages after the secondary-side of the HF transformers. European weighted efficiency (EU) and The California Energy Commission (CEC) weighted efficiencies are calculated and recorded in Fig. 37 and Fig. 38.

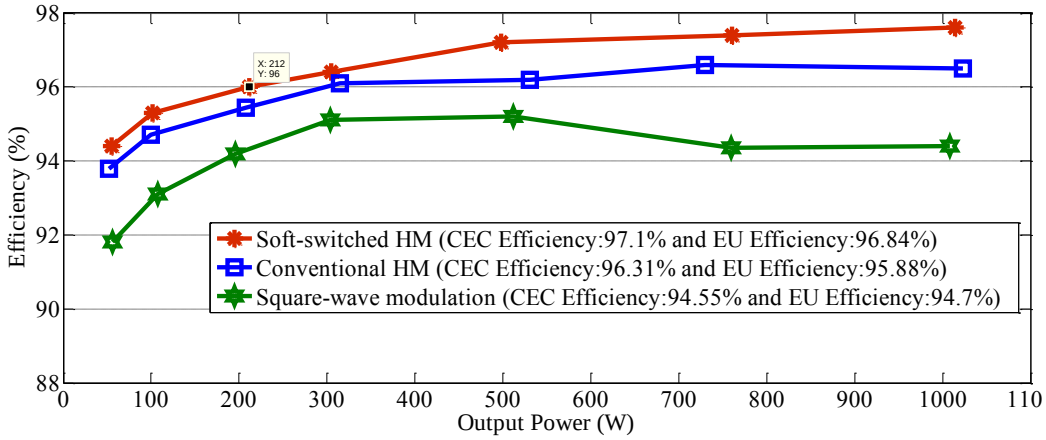


Fig. 36. The efficiency of the pulsating-dc/ac converter, ©2014 IEEE.

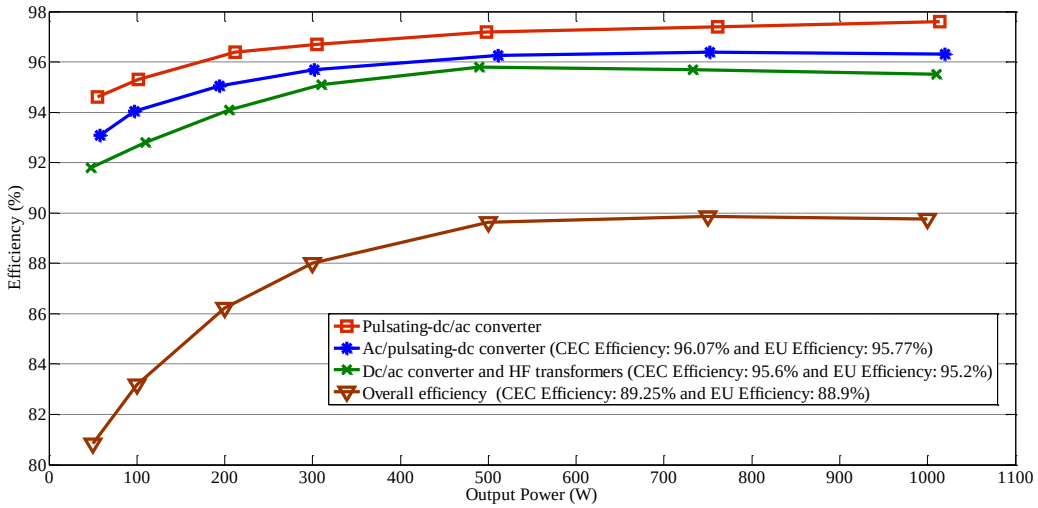


Fig. 37. The efficiency of the different stages of the HFPDCL inverter, ©2014 IEEE.

The operation of the soft-switched HM is reviewed for the light load conditions. As explained in Section III, load currents charge and discharge the parasitic capacitors of the switches of the pulsating-dc/ac converter. Therefore, enough load currents is required to provide the zero states for the ZVS operation of the pulsating-dc/ac converter. Fig. 38 shows the soft-switching operation of switch S_{31} when the output power is 50W. Because parasitic capacitors of the switches are typically small (320 pF for IPW60R045CP MosFets), enough zero states are generated on the PDCL waveform. Therefore, the soft switching is achieved for light load although it takes more time to discharge the parasitic capacitors. The Fig. 39 shows the drain-source voltage and the gate signal

of switch S_{31} when the output power is 40W. The ZVS operation is lost due to lack of enough load currents. But, the switch still commutate at lower voltages compared to the conventional HM.

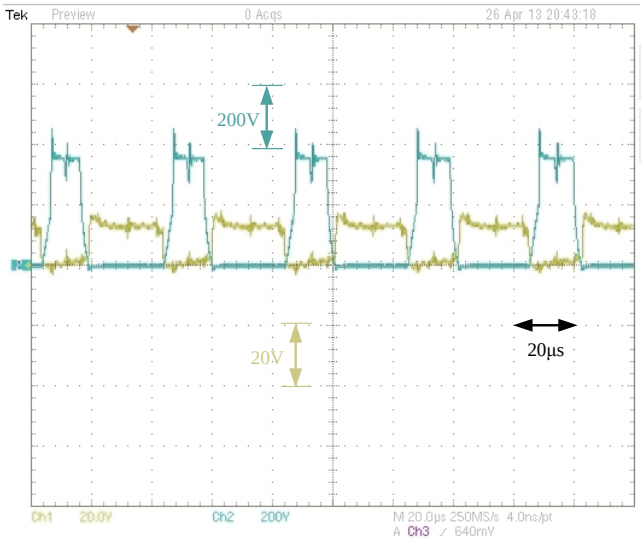


Fig. 38. The soft-switching operation of S_{31}.

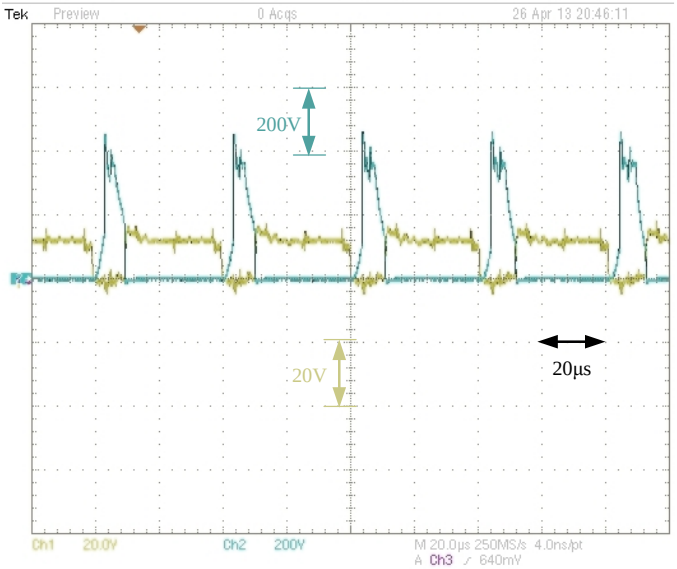


Fig. 39. The operation of the S_{31} when the output power is 40W.

D. Conclusion

A 1 kW HFPDCL inverter is implemented to validate the performance of the soft-switched HM. An RCD snubber is used for pulsating-dc link to minimize the voltages spikes on diode and devices of the ac/pulsating-dc and pulsating-dc/ac converters. Two predetermined legs of the pulsating-dc/ac converter do not switch while the remaining leg operates at HF under ZVS condition. The efficiency and THD of the HFPDCL inverter are improved using soft-switched HM. The inverter achieves a wide range of ZVS operation using soft-switched HM for loads up to 50W. The soft-switched HM needs a synchronized operation between dc/ac converter and the pulsating-dc/ac converter. Therefore, the zero states are generated by the dc/ac converter and the pulsating-dc/ac converter operates at the middle of the provided zero states to achieve ZVS operation for the pulsating-dc/ac converter.

V. Experimental Results using Compact and Modular HFPDCL Inverter

A. Low-Input Voltage Design

(Parts of this section, including figures and text, are based on my paper [66], ©2014 IEEE)

A compact and modular design is implemented to increase the power density of the HFPDCL inverter and decrease the leakage inductance of the board. The HFPDCL inverters do not have any bulky dc-link capacitor that makes its topology suitable for a modular and compact design. The pulsating-dc link waveform is modulated to reduce the switching requirement of the pulsating-dc/ac converter. The input dc voltage is 60 V under nominal condition. Therefore, HF transformers with turn ratios equal to 3.2 are utilized to boost the input voltage to the desired output voltage level. Infineon three-phase IGBT power modules are used as active and passive devices of the dc-link-capacitor less HFL inverter. The operation frequency of the converters, i.e. the dc/ac, ac/pulsating-dc, and pulsating-dc/ac converters, of the inverter is 20 kHz. The nominal output power is 2 kW. TABLE III summarizes the specifications of the implemented HFPDCL inverter.

TABLE III. THE SPECIFICATIONS AND MAIN COMPONENTS OF THE HFLDC INVERTER.

Frequency	**Input voltage**	**Output phase-to-phase voltage**	**Output power**	**Transformer turns ratio**
20 kHz	76 V	208 V	2 kW	1:3.2
Name	**Components**			
Switches	IFS75S12N3T4, 1200 V, 75 A			
HF transformers	PQ 5050 Ferrite Core			

The implemented HFPDCL inverter is shown in Fig. 40. Three HF transformers are used to increase the redundancy of the inverter. Therefore, the converter continues its operation when one of the full-bridge modules of the dc/ac converter fails [58]. A Field-Programmable Gate Array (FPGA) board is employed to generate the gate signals of the switches of the inverter. Optic fibers are used to send out the gate signals from the FPGA board to the drivers of the switches. Toroid

cores are used as the inductors of the output filters. Each inductor is 1 mH and each output filter capacitor is 2 μF. The winding of the HF transformers are interleaved to minimize the leakage inductance of the windings. The overall primary-side inductance of each transformer is equal to 3.2 μH.

The experimental results are obtained for 2 kW resistive loads. Fig. 41 shows the primary-side voltages of the two HF transformers of the inverter. The pulses are placed to achieve a PDCL voltage waveform with a frequency of 20 kHz. Therefore, the operation frequencies of the different stages of the inverter are equal to each other. The implemented modulation schemes of the converter is hard-switched HM scheme to evaluate the performance of the compact and modular board.

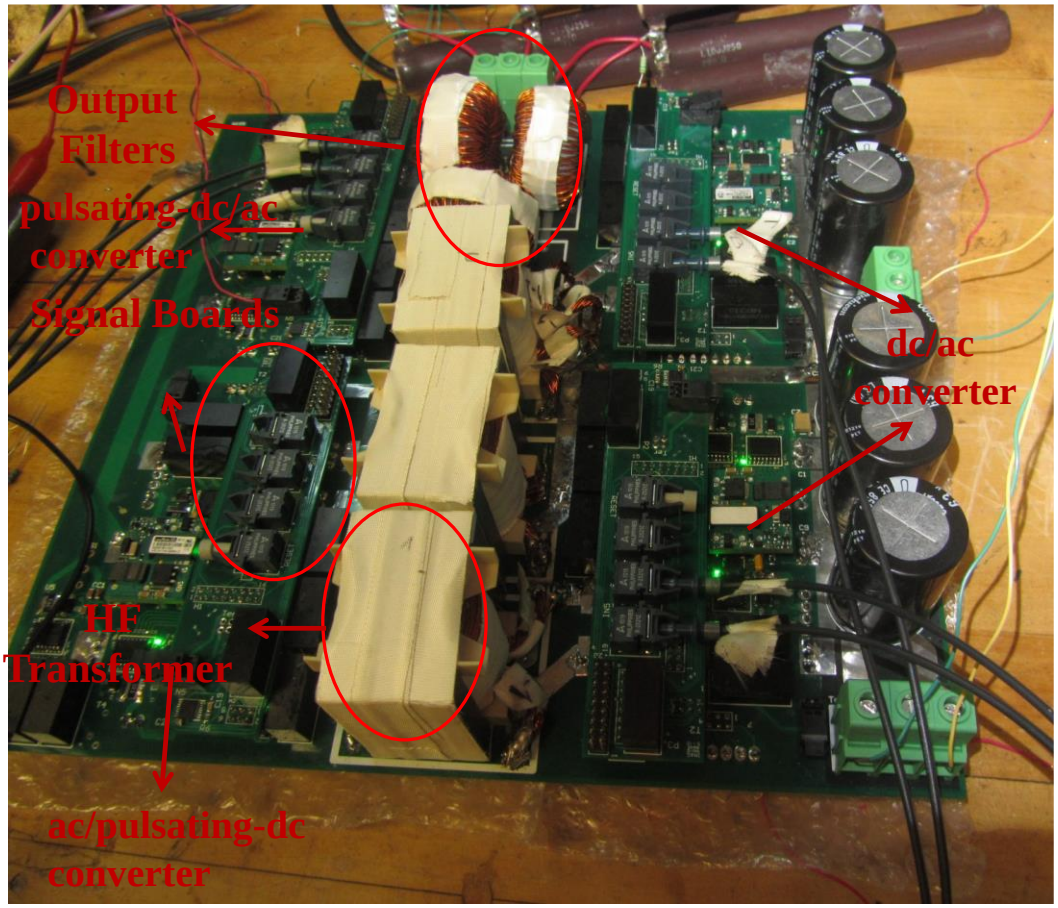


Fig. 40. The implemented dc-link capacitor less HFL inverter.

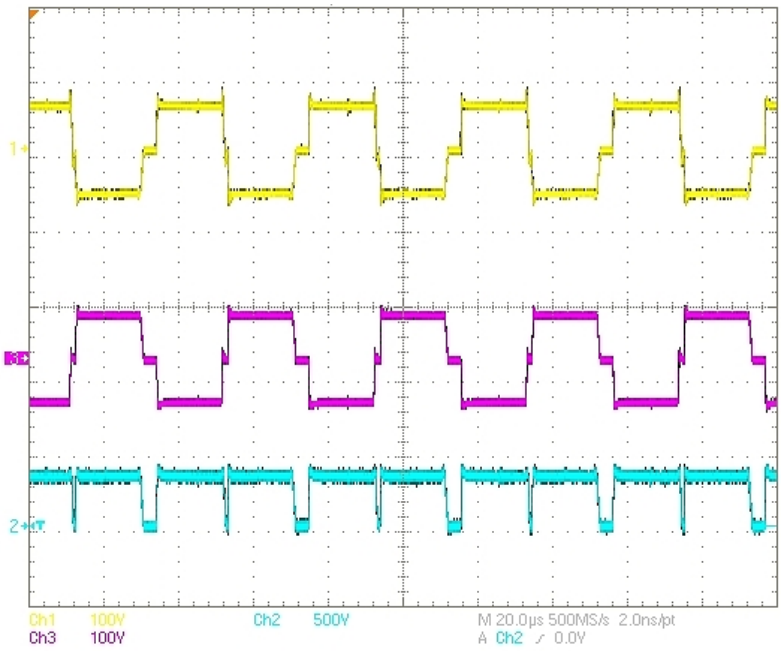


Fig. 41. The primary-side voltages of transformers and the PDCL waveform. Ch1: Primary-side voltage of the HF transformer T1, Ch2: The PDCL voltage waveform, and Ch3: Primary-side voltage of the HF transformer T2.

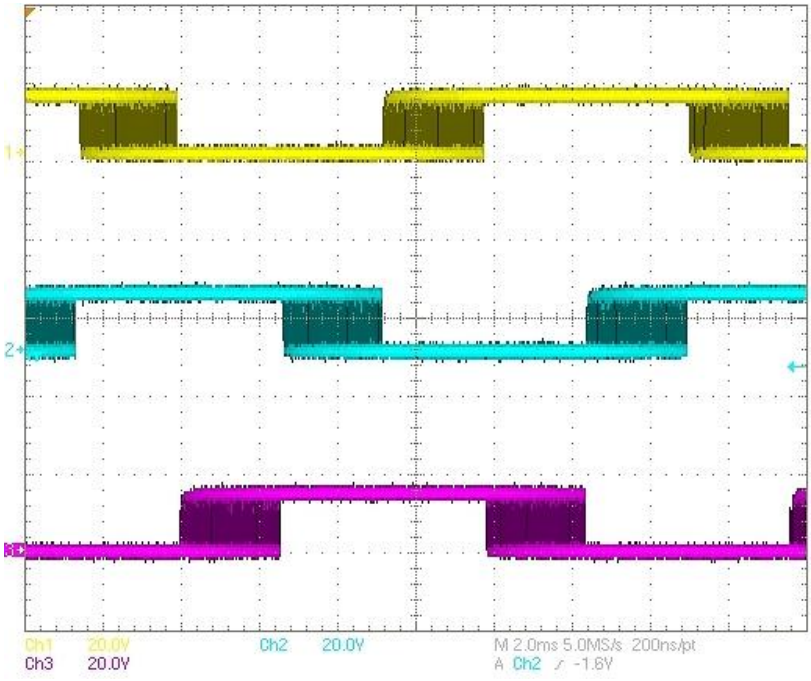


Fig. 42. The generated gate signals of the pulsating-dc/ac converter using the HM scheme. Ch1: Gate signal of S_{31}, Ch2: Gate signal of S_{32}, and Ch3: Gate signal of S_{33}.

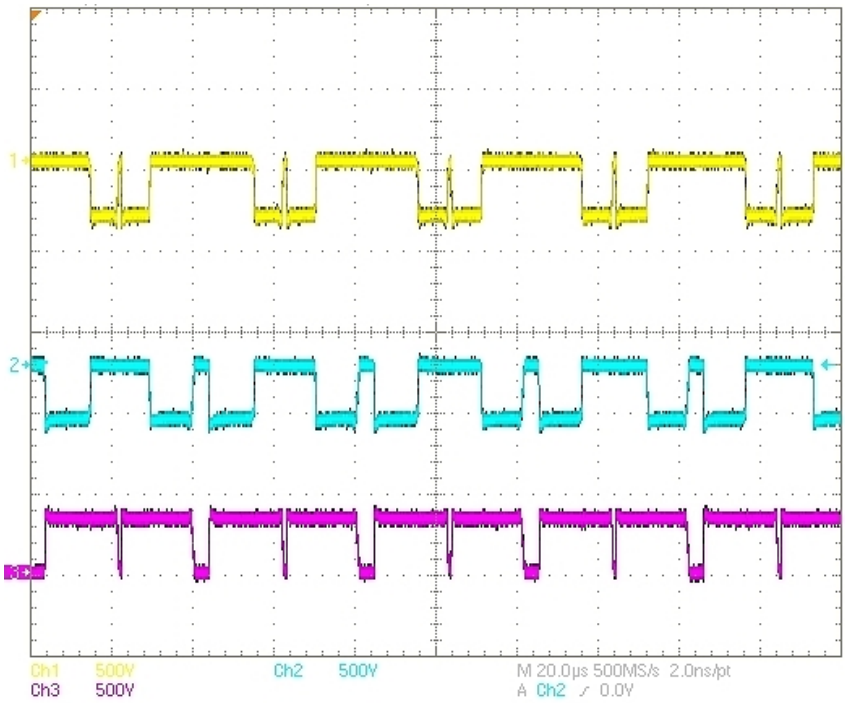


Fig. 43. The output voltage waveforms of the pulsating-dc/ac converter before the output filter. Ch1: Output voltage v_{ab}, Ch2: Output voltage v_{bc}, and Ch3: Output voltage v_{ca}.

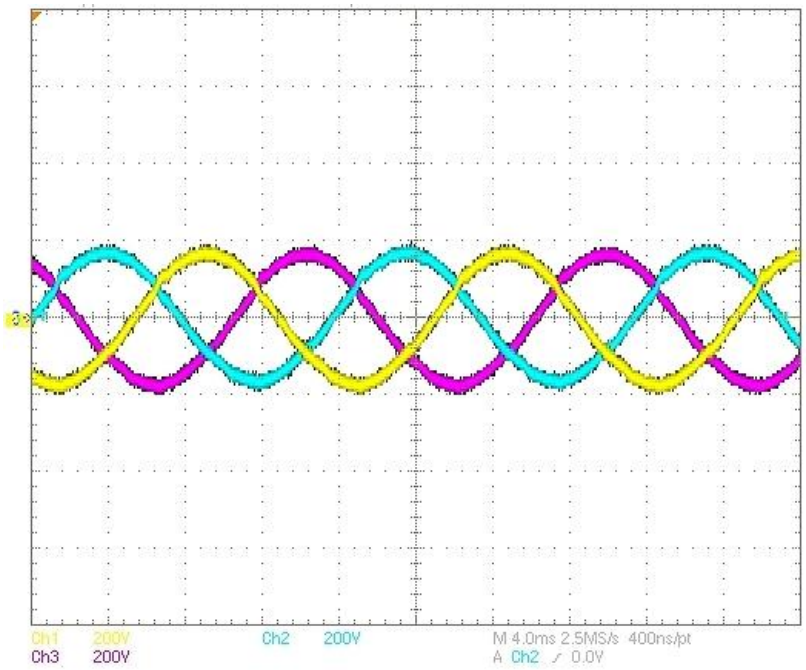


Fig. 44. The three-phase sine-wave voltage waveforms using the HM scheme.

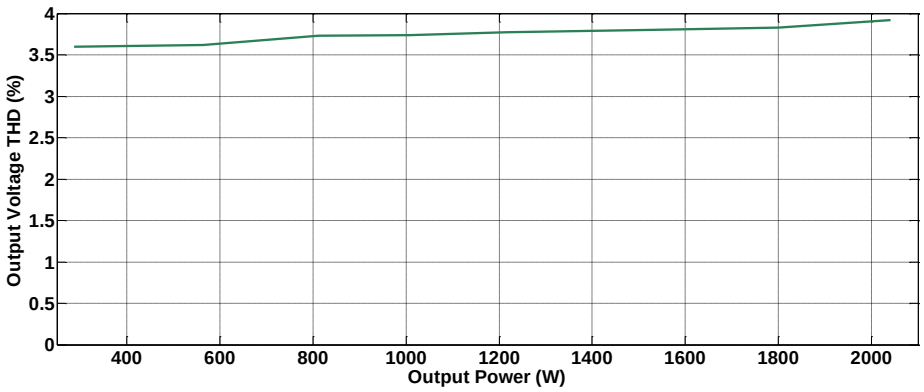


Fig. 45. The THD of the output voltage waveforms for different output powers.

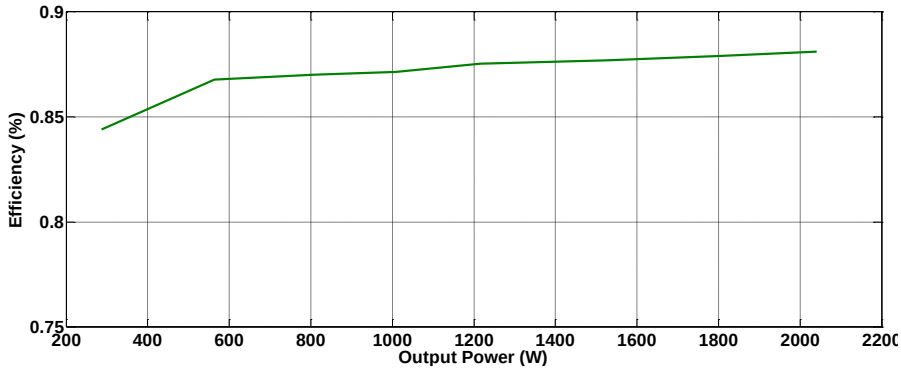


Fig. 46. The efficiency of the HFPDCL inverter for different output powers, ©2014 IEEE.

A. Hard Switched HM Scheme

The generated gate signals using the hard-switched HM scheme are shown in Fig. 42. Two legs of the pulsating-dc/ac converter do not commutate in any Sectors, PI–PVI. Therefore, switching requirement of the pulsating-dc/ac converter is decreased by 66%. As a result, the pulsating-dc/ac converter connects the two phases of the output load to the PDCL, which represents the maximum of the output reference signals. The other leg of the pulsating-dc/ac converter, which operates at HF, generates two other reference signals.

Fig. 43 shows the output voltage waveforms of the pulsating-dc/ac converter before the output filter stage when the inverter operates in Sector PIV. Therefore, the output reference signal v_{CA} is the maximum of the output reference signals. The output voltage waveform v_{ca} is identical to the

PDCL voltage waveform. The other two output voltage waveforms are generated by the leg of the pulsating-dc/ac converter that operates at HF. Fig. 44 shows the three-phase output sine-waves using the HM scheme for a 2 kW resistive load. The total harmonic distortion (THD) of the output voltage waveforms is measured and shown in Fig. 45 for different output powers. The HM scheme for the dc-link capacitor less HFL inverter shows a proper THD under all range of the output powers. The nominal efficiency for a 2 kW resistive load is 88% as shown in Fig. 46.

In this section, a modular and compact design of the HFPDCL inverter is presented using IGBT power modules to increase the power density of the inverter. The bulky dc-link capacitors are eliminated from the power stage of the HFL inverter as well to increases the power density of the inverter. The PDCL waveform is also manipulated to decrease the switching requirement of the pulsating-dc/ac converter. The switching requirement of the pulsating-dc/ac converter is decreased by 66% using the HM scheme. The dc-link-capacitor less inverter shows a proper THD of the output sine-wave voltage waveforms. Fig. 46 shows that the efficiency of the HFPDCL inverter is not well improved although the modular and compact design is used. Therefore, it was concluded that the IGBT modules do not operate very well at low-voltage high-current condition. The reason for this is IGBT has a constant voltage drop that causes significant conduction loss in the front-end dc/ac converter. The estimate of the conduction loss of the front-end dc/ac converter is almost 8% of the output power, which is significant. As a result, the input voltage is increased to make suitable for the IGBT modules. New transformers and other modifications have been done to increase the int voltage.

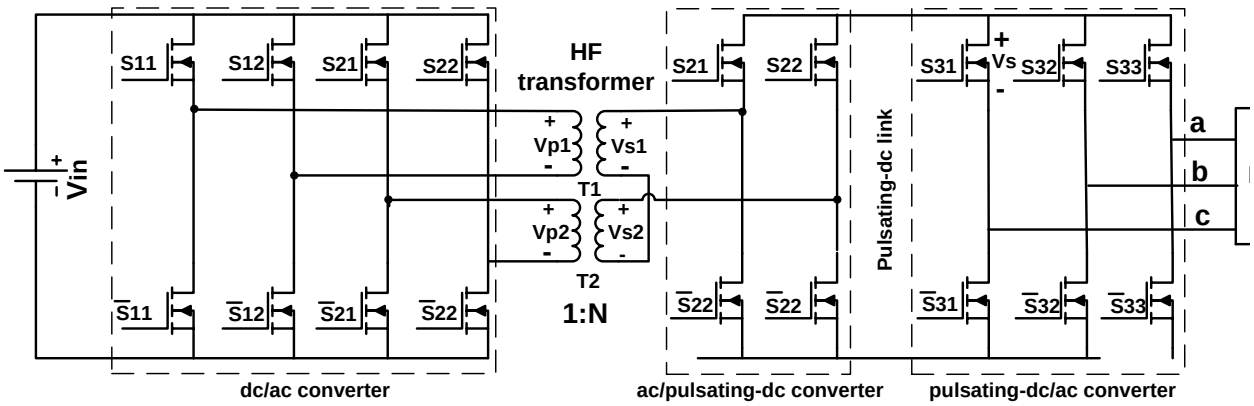


Fig. 47. The simplified schematic of a HFPDCL inverter using fully-controlled ac/pulsating-dc converter, ©2015 IEEE.

B. High-Input Voltage Design

(Parts of this chapter, including figures and text, are based on my paper [67], ©2015 IEEE)

The input voltage is increased to make the design suitable for IGBT modules. The specifications of the high-input voltage implemented inverter are summarized in TABLE IV. New HF transformers are designed to increase the input voltage of the implemented HFPDCL inverter. The new turn ratio of the HF transformers is 1:1.2 to achieve the desired output voltage level, which is 208 V_{ac}. The input capacitors of the HFPDCL inverter were replaced to make it compatible with higher input voltage.

TABLE IV. THE SPECIFICATIONS AND MAIN COMPONENTS OF THE HFLDC INVERTER.

Frequency	**Input voltage**	**Output phase-to-phase voltage**	**Output power**	**Transformer turns ratio**
20 kHz	200 V	208 V	2 kW	1:1.2
Name	**Components**			
Switches	IFS75S12N3T4, 1200 V, 75 A			
HF transformers	PQ 5050 Ferrite Core			

Also, the new design uses fully-controlled ac/pulsating-dc converter to provide ZVS condition for its switching devices. The simple schematic of the HFPDCL inverter with fully controlled ac/pulsating-dc converter is shown in Fig. 47. The switching devices of the ac/pulsating-dc converter are synchronized with the switching signals of the dc/ac converter. It only rectifies the

bipolar pulses at the secondary winding of the HF transformers. Therefore, it does not contribute in the modulation scheme of the HFPDCL inverter. The gate signals of the ac/pulsating-dc converter operate at a fixed duty cycle equal to 50%. This results in ZVS operation of the ac/pulsating dc-converter.

In this section, the performance of the presented dc-modulated discontinuous PWM scheme is verified using high input-voltage HFPDCL inverter. Fig. 48 shows the obtained output waveforms using the presented discontinuous PWM optimized for HFPDCL inverters. Fig. 49 shows the gate signals of the one phase of the pulsating-dc/ac converter using the modulation signal achieved using the presented discontinuous PWM scheme for the HFPDCL inverters with HF pulsating dc-link waveform. It shows that each leg phase of the pulsating-dc/ac converter is clamped to the dc-bus rail for 120^{o} of the line cycle. This practically decreases the switching losses of the pulsating-dc/ac converter by 33%. The overall efficiency of the HFPDCL inverter is shown in Fig. 50. The output current THD of the HFPDCL inverter using the presented discontinuous PWM is shown in Fig. 51. Figs. 50 and 51 verify the proper performance of the HFPDCL inverter using the presented modulation scheme. The THD is well below 3% for all range of the output loads. The achieved efficiency is over 90% for a wide range of the output loads. The soft-switching ZVS operation of the switches of the fully-controlled ac/pulsating-dc converter is shown in Fig. 52 It shows that the duty cycle of the gate signals of the ac/pulsating-dc converter is fixed equal to 50%. The switches device of the converter turn on/off when the voltage over the PDCL waveform is zero. Therefore, they operate under ZVS condition, which practically eliminates the switching losses of the ac/pulsating-dc converter. The new high input-voltage design increased the efficiency of the implemented HFPDCL inverter although dc-modulated discontinuous PWM scheme decreases the switching requirement of the pulsating-dc/ac converter by 33%.

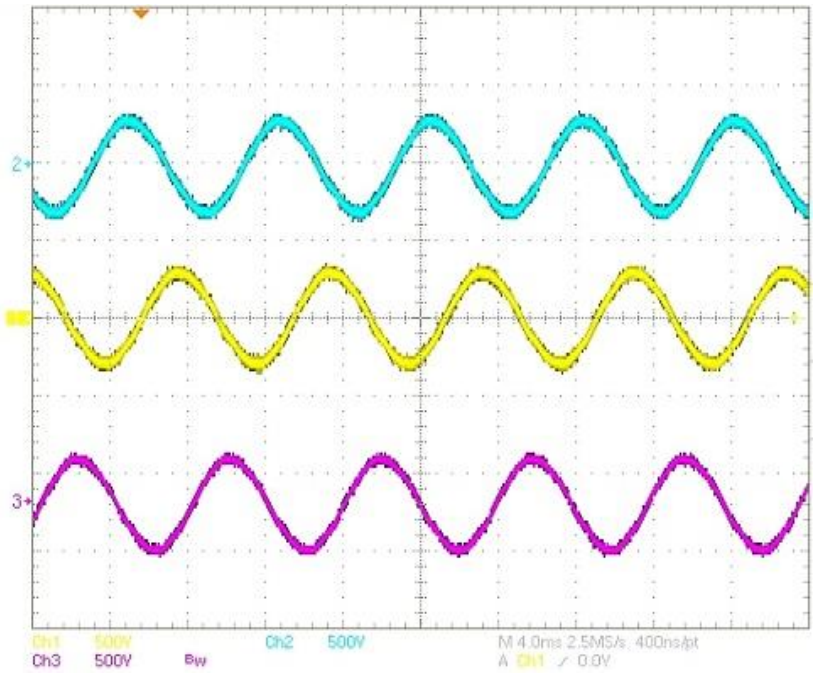


Fig. 48. The output voltage waveform of the HFPDCL inverter using the presented discontinuous PWM scheme.

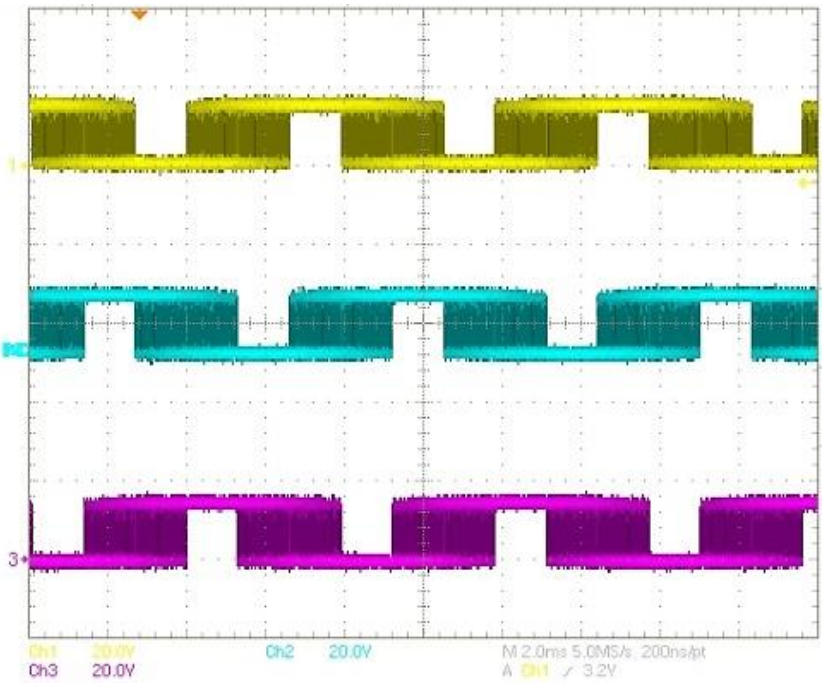


Fig. 49. The gate signals of the pulsating-dc/ac converter using the presented discontinuous PWM scheme.

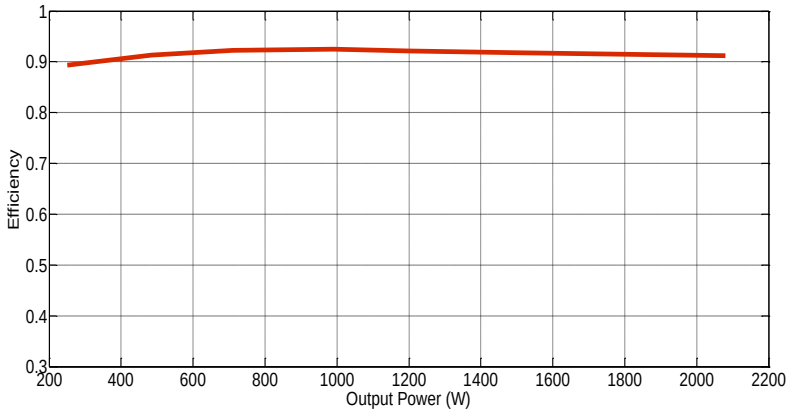


Fig. 50. The overall efficiency of the HFPDCL inverter versus the output power, ©2015 IEEE.

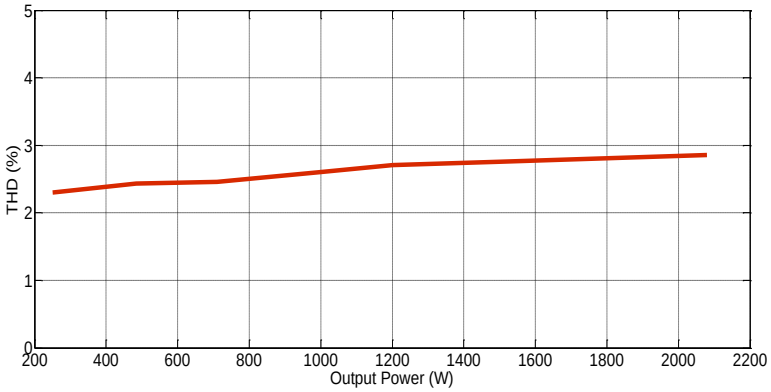
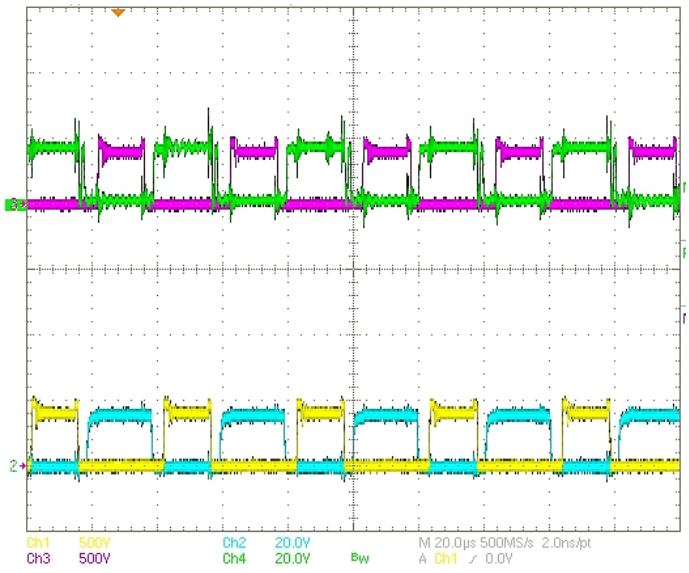
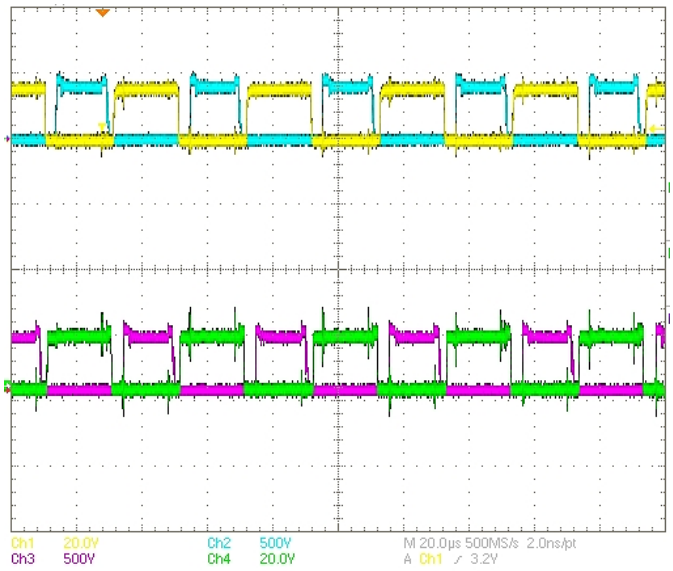


Fig. 51 The current THD of the HFPDCL inverter versus the output power, ©2015 IEEE.



(a)



(b)

Fig. 52. Soft-switching operation of all switches of the pulsating-dc/ac converter: (a) S_{21} and $\bar{S}_{21}$, and (b) S_{22}, and $\overline{S}_{22}$.

C. Conclusion

A compact and modular design of the HFPDCL inverter is implemented to validate the performance of the dc-modulated discontinuous modulation and hard-switched HM schemes. IGBT modules are not suitable for low-voltage high-current applications since the conduction loss of the front-end dc/ac converter significantly decrease the efficiency of the system. The input voltage is increased to decrease the conduction loss of the front-end dc/ac converter. New HF transformers are designed and implemented to increase the input voltage of the inverter. The performance of the dc-modulated discontinuous PWM scheme is verified using the new modular and compact design. The dc-modulated discontinuous PWM scheme decrease the switching requirement of the pulsating-dc/ac converter by 33%.

VI. Soft-Switched Discontinuous Pulse Density Pulse Width Modulation Scheme

Discontinuous modulation scheme reduces the switching requirement of the HFPDCL inverters by clamping one or two legs of the pulsating-dc/ac converter to the dc rail for a fraction of the line period. Therefore, the switching requirement can be decreased by 33% [49]-[53] or up to 66% [55]-[59]. The switching requirement can be decreased up to 33% without modulating the pulses on the PDCL waveform. Therefore, the generated pulses on the PDCL waveform represent a dc value. The switching requirement can be decreased up to 66% with modulation of the PDCL waveform. As a result, the PDCL waveform represents the maximum output reference signal. However, other legs of the converter still operate under hard-switching condition. These losses associated with the legs operating under hard-switching condition need to be mitigated to increase the overall efficiency of the inverter.

Soft-switched HM scheme provides ZVS condition for the remaining leg of the pulsating-dc/ac converter while two other legs are clamped to the dc bus. Therefore, the switching losses of the pulsating-dc/ac converter is practically mitigated. However, the soft-switched HM scheme generates two streams of pulses on the PDCL voltage waveform. As a result, the switching requirement of the front-end dc/ac and ac/pulsating-dc converters are increased since two stream of pulses are required. Therefore, the dc/ac converter synthesizes v_{AB} and v_{BC} in Sectors PI and PIV, v_{BC} and v_{CA} in Sectors PII and PV, and v_{CA} and v_{AB} in Sectors PIII and PVI. As shown in Fig. 19, the switching requirement of the dc/ac and ac/pulsating-dc/ac converters is double of the switching requirement of the pulsating-dc/ac converter.

In this Chapter, a discontinuous modulation scheme is presented to decrease the switching requirement of the dc/ac and ac/pulsating-dc converters to decrease their switching losses. It also clamps two predetermined legs of the pulsating-dc/ac converter to the dc bus. It provides ZVS condition for the remaining leg of the pulsating-dc/ac converter. Therefore, it practically mitigates the switching losses of the pulsating-dc/ac converter. However, in contrast to the soft-switched HM scheme, it does not increase the switching requirement of the dc/ac and ac/pulsating-dc converters. As a result, it decreases the switching losses of the front-end converters.

The presented discontinuous pulse-density pulse-width modulation (DPDPWM) scheme takes advantage of the pulsating nature of the PDCL waveform. It employs pulse-density modulation (PDM) [61]-[65] and pulse-width modulation (PWM) schemes. It is only possible due to the pulsating nature of the PDCL waveform. PDM schemes decrease the switching requirement of the inverters by varying the frequency operation of the converter. It synthesizes the output sine waveforms by varying the density of the pulses instead of varying the width of the pulses. References [61], [62] presented a single phase to three-phase matrix converter using PDM scheme. They reported a THD of over 5%. Reference [63] presented a fixed dc-link three-phase inverter using PDM scheme to synthesize the output sine waveforms. An output THD of over 5% is also reported. Reference [64], [65] presented single phase inverter using PDM scheme to decrease the switching requirement and losses of the inverter. Therefore, they only employed PDM scheme, which decreases the switching losses and increases the THD of the inverter. But, DPDPWM scheme employ both PDM and PWM schemes.

The frond-end dc/ac converter synthesizes the PDCL waveform using PWM scheme. It synthesizes a series of pulses on the PDCL waveform representing the maximum output reference signal. The generated PDCL voltage waveform is shows in Fig. 53. The maximum reference voltage

signal changes every 60^o of the output line cycle. Therefore, v_{CA} is the maximum reference voltage signal in PI and PIV, v_{AB} is the maximum reference signal in PII and PV, and v_{BC} is the maximum reference voltage signal in PIII and PVI. Therefore, the dc/ac converter generates a stream of pulses based on the maximum reference voltage signal during each operating sector. Then, two predetermined legs of the pulsating-dc/ac converter are clamped to the dc-rail. However, in contrast to the hard-switched HM scheme, zero states are used to provide ZVS condition for the pulsating-dc/ac converter.

Therefore, the zero-states need to be placed and adjusted on the PDCL waveform to turn on/off the switches of the pulsating-dc/ac converter during the generated zero states. The zero-states are generated on the PDCL waveform by the front-end dc/ac converter. Fig. 9 shows the PDCL waveform generation of the presented dc-modulated discontinuous PWM scheme. The width of the generated zero-states is constant for the dc-modulated discontinuous PWM scheme. Fig. 54 shows the generated PDCL waveform using the maximum reference signal as the modulation signal of the dc/ac converter. It shows that the switches of the pulsating-dc/ac converter turn on/off during zero states of the PDCL waveform. It also shows that two legs of the pulsating-dc/ac converter are clamped to the dc bus. The third leg turns on/off during the zero states of the PDCL waveform. The pulses are placed in the middle of the switching cycles to turn on/off the switches of the pulsating-dc/ac converter at the beginning and end of each switching cycle. It makes the modulation of the dc/ac and the pulsating-dc/ac converter symmetric.

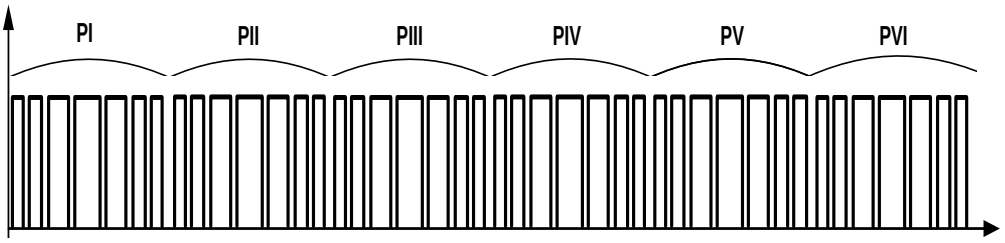


Fig. 53. The PDCL waveform when the dc/ac converter generates a stream of the pulses, ©2014 IEEE.

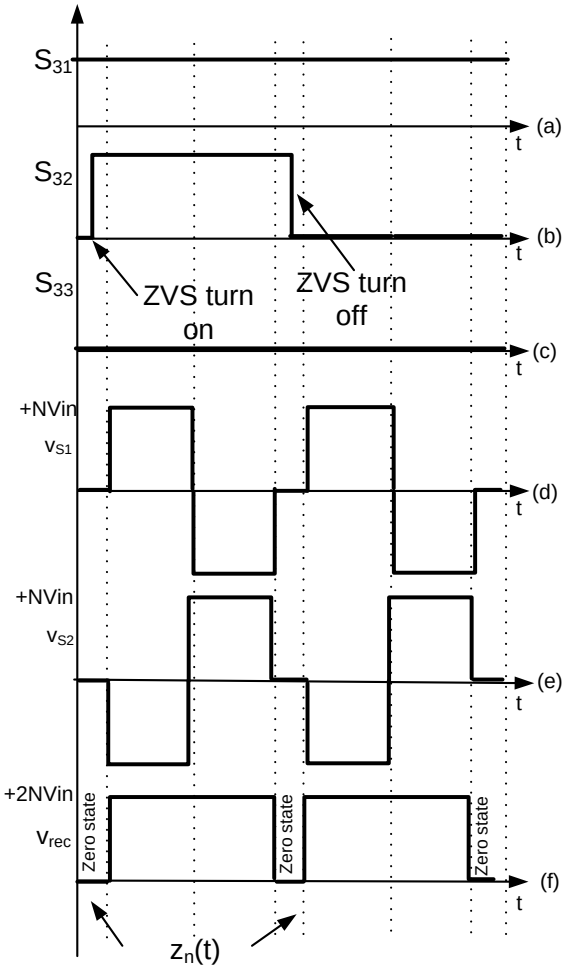


Fig. 54. The dc-link waveform generation and ZVS of the pulsating-dc/ac converter: (a)-(c) the synthesized gate signals of S_{31}, S_{32}, and S_{33}, (e)-(f) the secondary voltages of the HF transformer, and (g) the generated dc-link waveform.

The duration of the generated zero state on the PDCL waveform can calculated as follows:

$$z(n) = 1-\max(|v_{AB}(n)|,|v_{BC}(n)|,|v_{CA}(n)|) \quad (15)$$

where z(n) is the sampled value of the z(t) in n^{th} switching cycle of a line cycle. Therefore, enough zero states are available on the PDCL waveform to provide ZVS condition for the pulsating-dc/ac and ac/pulsating-dc converters. Fig. 55 shows the synthesized signals of the pulsating-dc/ac converter over a line cycle. It shows that the generated output pulses of the inverter are a mix of PDM and PWM schemes. Therefore, two predetermined legs of the pulsating-dc/ac converter are

clamped to dc bus. And the remaining legs, is modulated by PDM scheme, operates under ZVS condition. The operation frequency of the remaining leg is varying and its duty cycle is always 50%

In summary, the DPDPWM scheme uses the advantages of both PWM and PDM schemes. The PWM of the PDCL waveform decreases the THD of the output sine waveforms. This is possible due to pulsating nature of the PDCL waveform in contrast to the fixed-dc link inverter. Next section describes the implementation of the DPDPWM scheme using sigma-delta controllers. Each line cycle is divided into six operation sectors: PI-PVI. Sectors PI and PIV, Sectors PII and PV, and PIII and PVI are complementary. Therefore, gate signals of S_{31}, S_{32}, and S_{33} are inverted in Sectors PI and PIV, Sectors PII and PV, and Sectors PIII and PVI. As a result, DPDPWM scheme divides in three distinctive operating sectors:

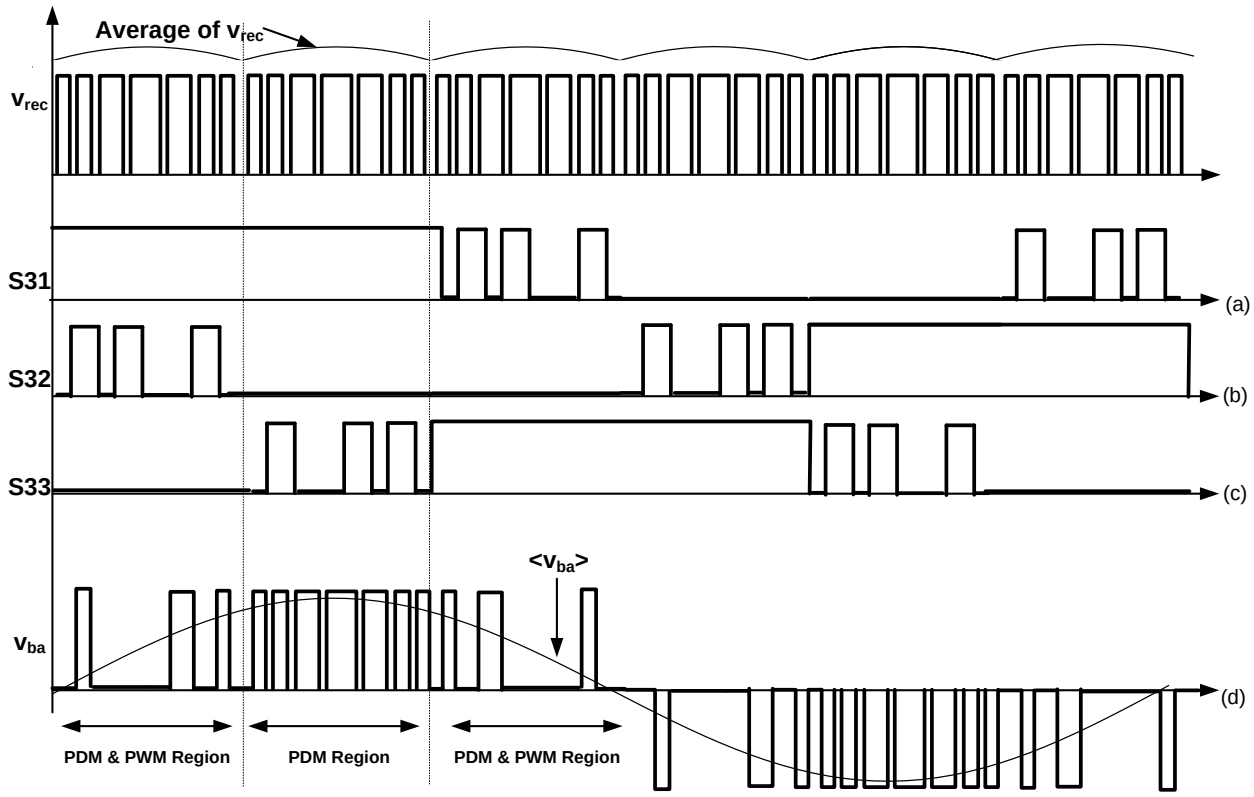


Fig. 55. The switching signals of the pulsating-dc/ac converter using the HM scheme. a) Gate signal of S_{31}, b) Gate signal of $S_{32,}$ c) Gate signal of S_{33}, and d) The achieved output voltage waveform v_{ba}.

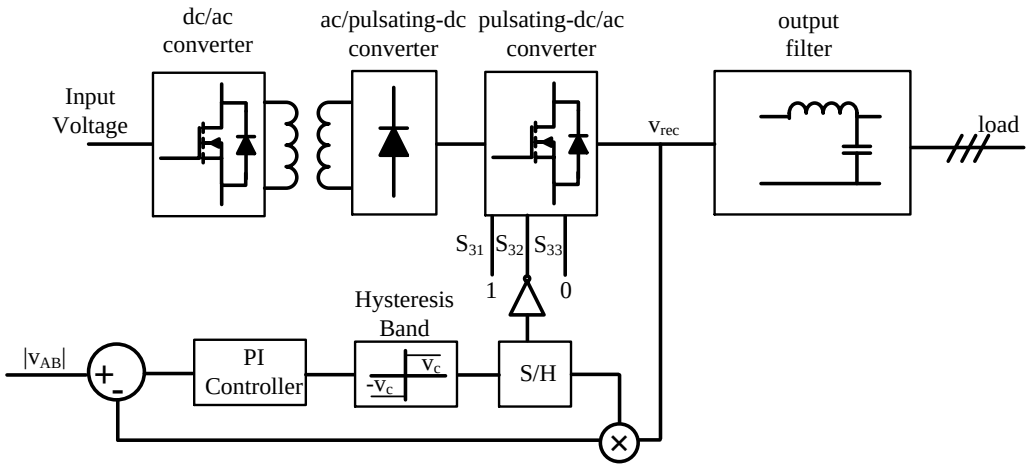


Fig. 56. The DPDPWM modulator of the pulsating-dc/ac converter during PI and PIV.

Sectors PI and PIV:

Reference signal v_{CA} is the maximum reference during these operating sectors. Therefore, the PDCL waveform is synthesized based on the v_{CA}. Then, the first leg and the third leg of the pulsating-dc/ac converter are clamped to the dc bus in PI and PVI. Fig. 56 shows the controller for Sectors PI and PIV. Variable v_C is the upper and lower limits of the hysteresis band.

The second leg of the pulsating-dc/ac converter is switched with a variable frequency. The PDM modulator is implemented using a sigma-delta controller. The base frequency of the hysteresis block is the frequency of the PDCL waveform. A feedback from PDCL voltage waveform is required to generate the output voltage waveforms. Signal v_{AB} is used as the reference of the sigma-delta controller. As a result, the v_{CA} is synthesized directly on the PDCL waveform and v_{AB} and v_{BC} are generated using the PDM of the second leg of the pulsating-dc/ac converter.

Sectors PII and PV:

Reference signal v_{AB} is the maximum reference voltage signal in PII and PV. Therefore, the PDCL waveform is synthesized based on the v_{AB}. Then, S_{31} and S_{32} do not commutate in these

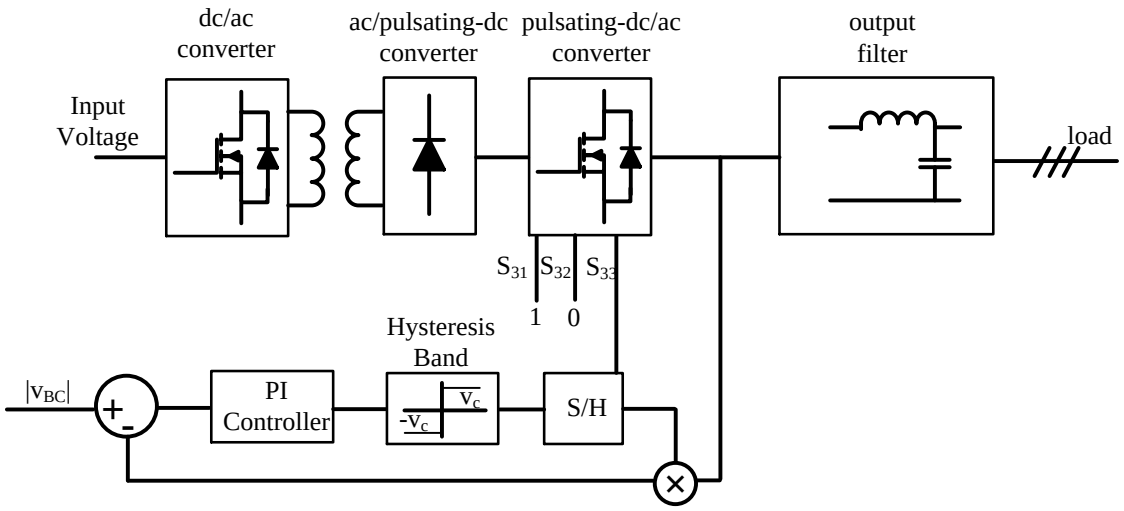


Fig. 57. The DPDPWM modulator of the pulsating-dc/ac converter during PII and PV.

sectors. Fig. 57 shows the controller for Sectors PII and PV. The third leg of the pulsating-dc/ac converter is switched with a variable frequency. The other features of the controller are same as the controller in Fig. 56. Signal v_{BC} is used as the reference of the sigma-delta controller. Hence, the v_{AB} is synthesized directly on the PDCL waveform and v_{BC} and v_{CA} are generated using the PDM of the third leg of the pulsating-dc/ac converter.

Sectors PIII and PVI:

Reference voltage signal v_{BC} is the maximum signal in PIII and PVI. Therefore, the PDCL waveform is synthesized based on the v_{BC}. Then, the second leg and the third leg of the pulsating-dc/ac converter do not commutate in these sectors. Fig. 58 shows the controller for Sectors PIII and PVI. The first leg of the pulsating-dc/ac converter is switched with a variable frequency. Reference signal v_{BC} is used as the reference of the sigma-delta controller. As a result, the v_{BC} is synthesized

directly on the PDCL waveform and v_{AB} and v_{BC} are generated using the PDM of the first leg of the pulsating-dc/ac converter.

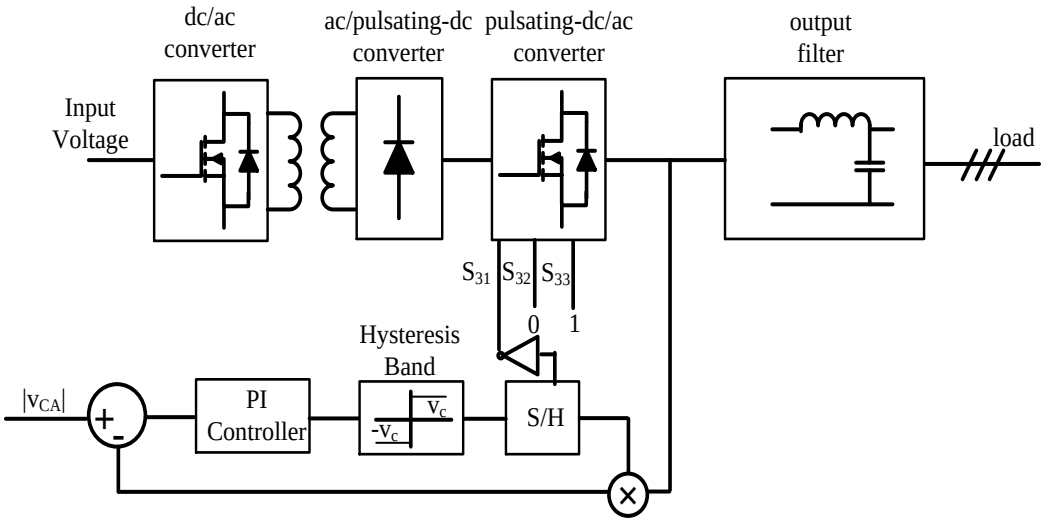


Fig. 58. DPDPWM of the pulsating-dc/ac converter during PIII and PVI.

A. Experimental Results

The performance of the presented DPDPWM scheme is evaluated by the implemented modular and compact HFPDCL inverter. The specifications of the implemented HFPDCL inverter are summarized in Table IV. The ac/pulsating-dc converter is a fully-controlled converter to provide ZVS condition for its switches. The switches of the ac/pulsating-dc converter turn on/off during zero states of the PDCL waveform. Their gate signals need to be synchronized with the gate signals of the dc/ac converter. A simple schematic of the implemented HFPDCL inverter is shown in Fig. 47. The output voltage waveforms of the inverter before output filters are shown in Fig. 59. It shows the PDM operation of the pulsating-dc/ac converter. The output pulses are modulated by both PWM and PDM schemes. The front-end dc/ac converter indirectly participates in the PWM modulation of the output waveforms.

The resulting output sine waveforms of the HFPDCL inverter using DPDPWM scheme is shown in Fig. 60, which shows high-quality output waveforms. The soft-switching operation of the ac/pulsating- converter is shown in Fig. 61. It shows that the switches of the ac/pulsating-dc converter turn on/off during the zero states of the PDCL waveform. Therefore, they operate under ZVS condition. As a result, the switching loss of this converter is practically mitigated.

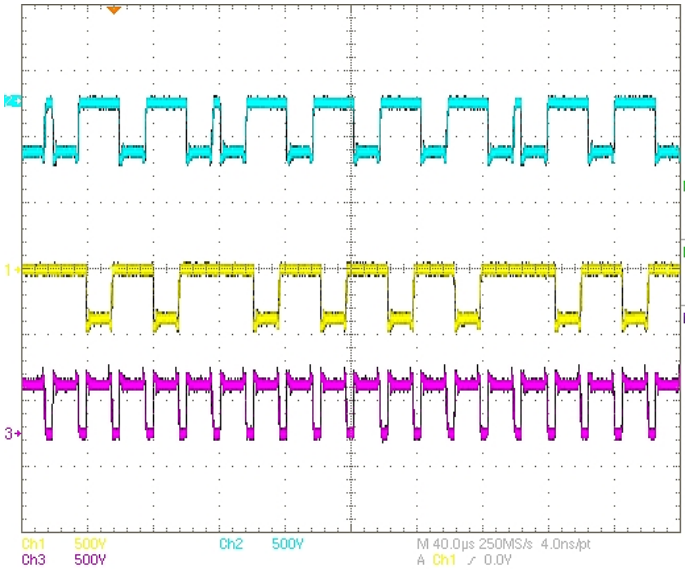


Fig. 59 . The output voltage phase to phase waveforms before output filters.

.

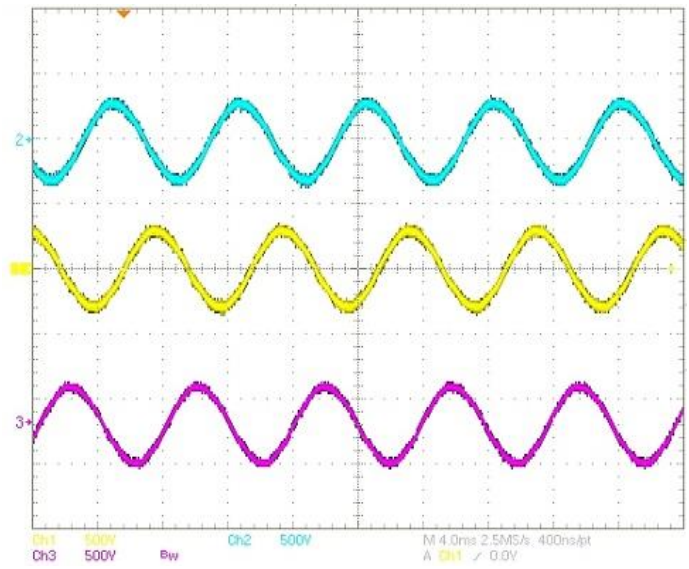
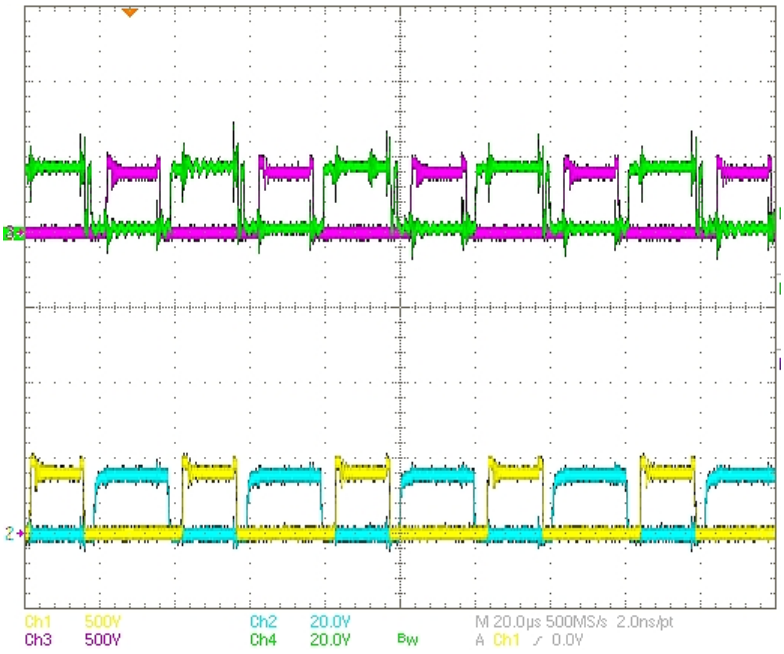
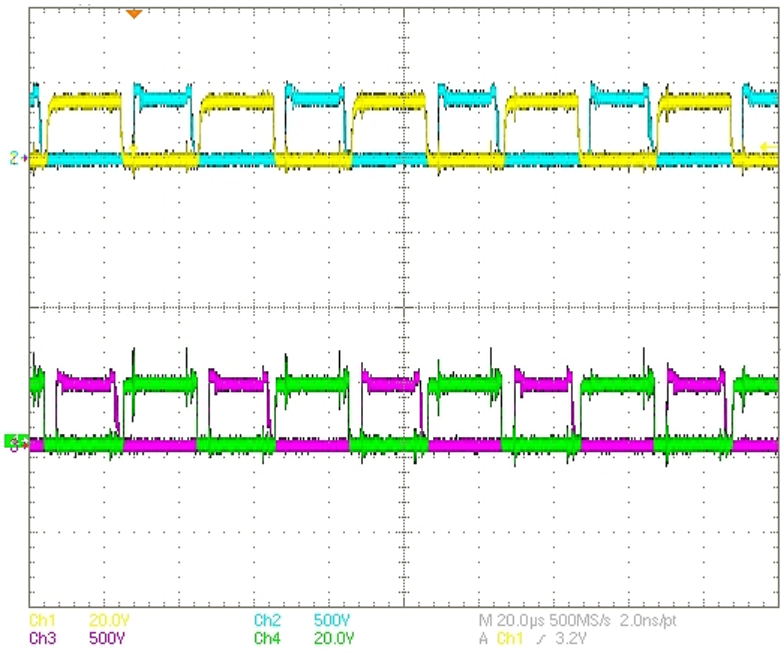


Fig. 60. The output sine waveforms of the HFPDCL inverter using DPDPWM scheme.



(a)



(b)

Fig. 61. Soft-switching operation of the pulsating-dc/ac converter using DPDPWM: (a) S_{21} and $\bar{S}_{21}$, and (b) S_{22}, and $\bar{S}_{22}$.

The soft-switching operation of the switches of the pulsating-dc/ac converter using DPDPWM is shown in Fig. 62. The switches turn off/on when the voltage across the PDCL is zero. Therefore, they can operate under ZVS condition. Therefore, two legs of the pulsating-dc/ac converter are

clamped to the dc bus, and the remaining leg operates under ZVS condition. Using DPDPWM, the duty cycle of the switches of the pulsating-dc/ac converter is fixed and equal to 50%. The operation frequency of the converter varies due to the PDM modulation of the pulsating-dc/ac converter. Fig. 63 shows the output THD of the HFPDCL inverter using DPDPWM scheme. The THD is well below 5% for all range of output power.

The modulation scheme of the front-end dc/ac converter is PWM, and it operates at fixed frequency. It generates and synthesizes the pulses of the PDCL waveform. Therefore, its operating frequency is fixed and independent from the modulation index and load. The modulation index changes the width of the pulses on the PDCL waveform generated by the front-end dc/ac converter. However, it does not affect the operating frequency of the front-end dc/ac converter. The maximum operating frequency of the pulsating-dc/ac converter is limited to the frequency of the PDCL waveform, which is 20 kHz for the implemented converter. The minimum frequency of the pulsating-dc/ac converter can be set by the controller. Which is 3 kHz for the implemented converter. Therefore, the minimum and maximum operating frequency of the converter is set by the controller and it is independent from the modulation index and load.

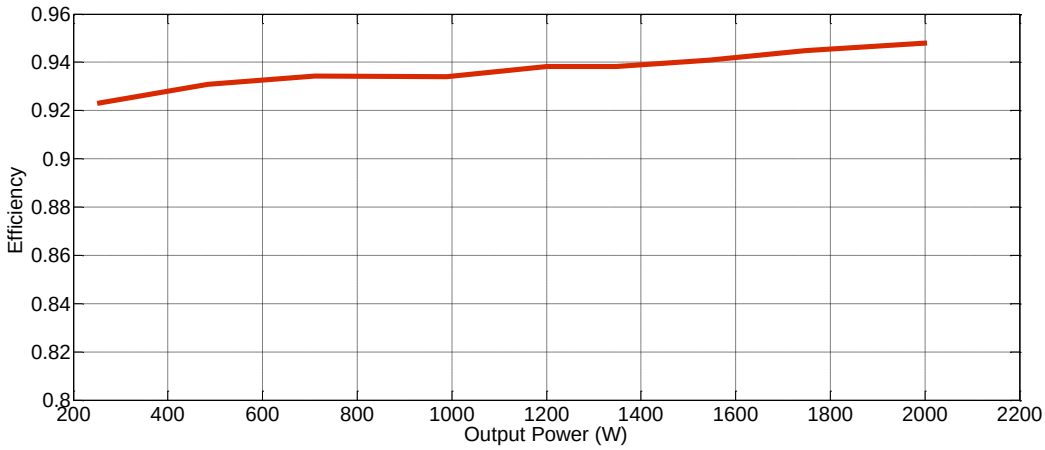


Fig. 62. The overall efficiency of the HFPDCL inverter using DPDPWM scheme.

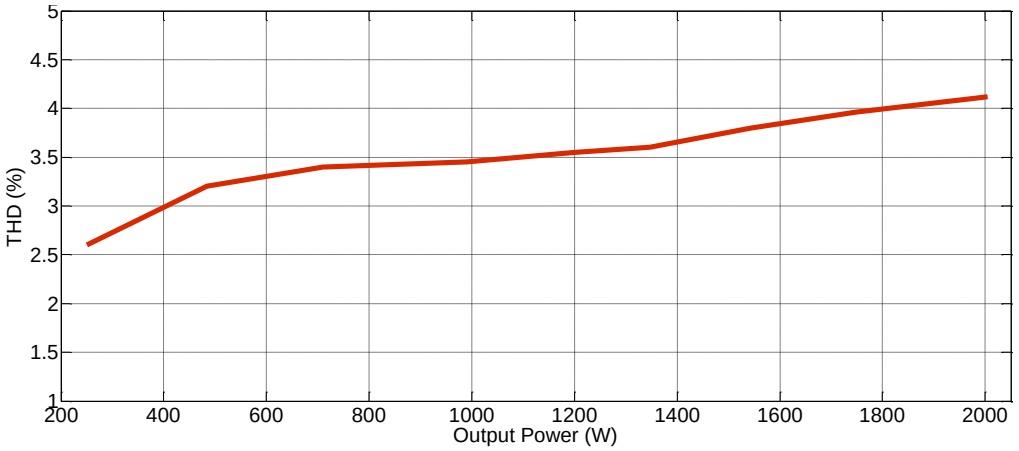
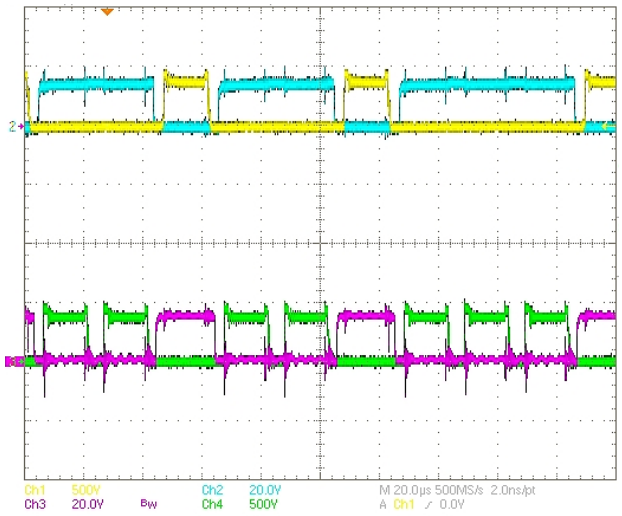
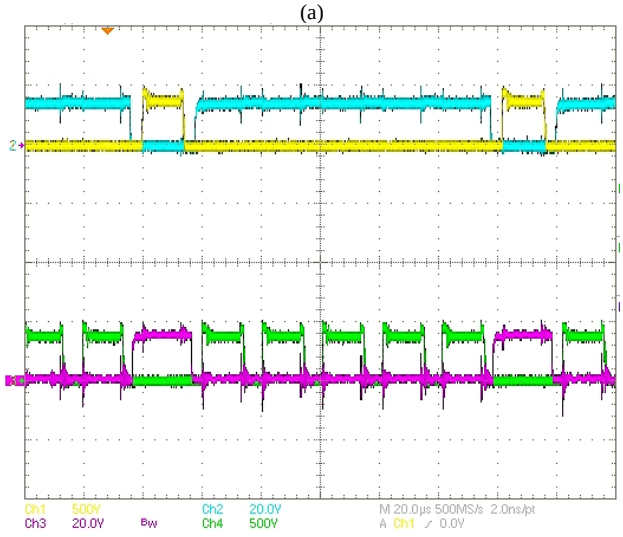


Fig. 63. The output THD of the HFPDCL inverter using DPDPWM scheme.



(a)



(b)

(c)

Fig. 64. Soft-switching operation of the pulsating-dc/ac converter using DPDPWM: (a) S_{31} & $\bar{S}_{31}$,(b) S_{32}, $\overline{S}_{32}$, and (c) $S_{33,}$ $\bar{S}_{33}$.

B. Conclusion

The THD of the HFPDCL inverter using DPDPWM scheme is comparable with the THD of the hard-switched HM and dc-modulated discontinuous PWM schemes. Because the pulsating-dc/ac converter operates under ZVS converter. However, the pulsating-dc/ac converter operate under hard-switched condition using hard switched HM and dc-modulated discontinuous PWM schemes. This results in an increase in the THD of these schemes. Fig. 64 shows the efficiency of the HFPDCL inverter. As we can see, the peak efficiency of the inverter is about 95%. This proves the promising performance of the HFPDCL inverter using DPDPWM scheme. The ac/pulsating-dc converter operate under ZVS condition, which practically mitigates its switching loss. The switching requirement of the pulsating-dc/ac converter is also decreased. The pulsating-dc/ac converter operate under ZVS condition. This soft-switching condition is achieved without increasing the switching requirement of the dc/ac and ac/pulsating-dc converters.

VII. Conclusion and Future Work

A. Conclusion

In this dissertation, a high-frequency pulsating-dc link (HFPDCL) inverter is considered as suitable option for renewable energy sources. They operate as interference between the renewable energy sources and the grid or stand-alone loads. The HFPDCL inverter provides galvanic isolation using high-frequency (HF) transformers in contrast to the conventional inverters. The conventional inverters provide galvanic isolation using line-frequency (LF) transformers. The HF transformers are way smaller than the LF transformers, which increase the power density of the inverter. The HFPDCL inverter do not require any bulky electrolytic capacitor as the dc-link capacitor unlike the fixed dc-link high-frequency link (HFL) inverters. The electrolytic capacitors are bulky and they are one of failure causes of the inverters. However there are two issues regarding HFPDCL inverters.

1. HFPDCL inverters have three conversion stages. It increases the switching requirement and losses of the inverter. It can decrease the efficiency of the HFPDCL inverters.
2. The dc-link capacitors decouples the converters before the dc-link capacitor from the output dc/ac converter. Therefore, the control and modulation schemes of the converters before and after the dc-link capacitor can be independent from each other. As a result, the HFPDCL inverters operate as a single stage inverter despite having three conversion stage. The modulation scheme of the inverter needs to synchronize these conversion stages.

Therefore, the switching losses of the HFPDCL inverters need to be addressed. The soft-switching schemes reduces the switching losses of the power converters by reducing the

switching requirement and providing zero-voltage or zero-current condition. Soft-switching schemes are divided into two general groups: 1) soft-switching schemes using auxiliary circuits, and 2) modulation-based soft-switching schemes. Auxiliary circuits can be employed to provide zero-voltage switching (ZVS) or zero-current switching (ZCS) condition for the power converter. However, they require additional passive and active components. This decreases the modularity of the converter. It also makes the topology more complicated. The additional components can increase the conduction losses of the converter. The modulation-based soft-switching scheme do not require any additional components. They decrease the switching requirement of the converter, which decrease the switching losses. They can also provide ZVS or ZCS condition for the switches of the power converter.

The modulation signals of the inverters divide the modulation schemes into two groups: 1) continuous PWM schemes, and 2) discontinuous PWM schemes. In continuous PWM scheme, the modulation signals is always in the boundary of the carrier signal. Therefore, the legs of the inverter always operate at HF. However, the modulation signals of the discontinuous PWM schemes can be out of the boundary of the carrier signal for a fraction of the line cycle. As a result, one or two legs of the inverter clamp to the dc rail. This decreases the switching requirement of the inverter by 33% or 66%. A decrease in switching requirement decreases the switching losses of the inverter.

A dc-modulated discontinuous modulation scheme is presented to reduce the switching requirement of the pulsating-dc/ac (inverter) converter by 33%. One predetermined leg of the pulsating-dc/ac converter is clamped to the dc bus. This modulation scheme does not need to modulate the pulses on the pulsating dc-link (PDCL) waveform. Therefore, the generated pulses on the PDCL waveform have a fixed duty cycle representing a dc value. The carrier and

modulation signals are optimized based on the pulsating nature of the PDCL waveform. However, two legs of the pulsating-dc/ac converter still operate under hard-switching condition.

A soft-switched hybrid modulation (HM) scheme is presented to reduce the switching requirement of the pulsating-dc/ac converter by 66%. Therefore, two predetermined legs of the pulsating-dc/ac converter are clamped to the dc bus. There remaining leg of the converter still operates at HF. However, this legs turn on/off under ZVS condition using soft-switched HM scheme. The front-end dc/ac converter generates two streams of pulses on the PDCL waveform to provide ZVS condition for the pulsating-dc/ac converter. The switches of the pulsating-dc/ac converter turn on/off in the middle of the generated zero state on the PDCL waveform. As a result, the switching losses of the pulsating-dc/ac converter is practically eliminated. This modulation scheme doubles the switching requirement of the dc/ac and ac/pulsating-dc converter.

A discontinuous pulse-density pulse-modulation (DPDPWM) scheme is proposed to decrease the switching requirement of the pulsating-dc/ac converter by 66%. Therefore, it clamps two predetermined legs of the pulsating-dc/ac converter to the dc bus. The remaining leg operate under ZVS condition. The zero states are generated and placed on the PDCL waveform by the dc/ac converter to provide ZVS condition for the pulsating-dc/ac converter. This modulation uses the advantages of both pulse-density modulation (PDM) and PWM schemes. The front-end dc/ac converter indirectly modulates the output waveform using PWM scheme. However, the pulsating-dc/ac converter uses the PDM scheme to synthesize the output waveform. Therefore, the output signals are a mix PDM and PWM schemes.

Two experimental prototypes were developed to verify the performance of the proposed modulation schemes. The first prototype were implemented using discrete switching devices.

The performance of the soft-switched HM scheme is verified using this prototype. However, a modular and compact design is designed and developed to increase the power density and decrease the leakage inductances of the board. The performance of the dc-modulated discontinuous PWM, hard-switched HM, and DPDPWM schemes are verified using this prototype. The DPDPWM scheme shows a promising performance with high-quality output waveforms and high overall efficiency.

B. Future Work

As a future work beyond dissertation, a multi-level HFPDCL inverter can be developed to increase the output voltage level of the inverter to the distribution level. The proposed modulation schemes in this research are designed and optimized for three-level HFPDCL inverters. However they can be extended to multi-level HFPDCL inverters. A new design needs to be developed to increase the voltage level of the output waveforms. The HFPDCL topology is modular that makes this topology suitable for multi-level application. The proposed modulation-based soft-switching schemes do not require any auxiliary circuit, which increases the modularity of the topology.

Soft-switching schemes using auxiliary circuits can be developed to compare their performance with the performance of the proposed modulation-based soft-switching schemes. Lossless snubbers, active clamps, and resonant schemes are well-known soft-switching schemes, which can be applied for HFPDCL inverters. However, these schemes can increase the current or voltage stress of the switching devices. They can also increase the conduction losses of the HFPDCL inverters.

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