A Unified Controller for a High-Frequency-Link (HFL) Inverter

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THESIS

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This thesis is dedicated to the sprit of my father, (MohammadReza) who helped me and showed me the right way of dealing with challenges in the journey of life till the day he passed away, to my mother, (Manijeh) who taught me love and sacrificed her youth for us, and to my lovely wife, (Nakissa) without whom it would never have been accomplished, and also my beautiful and kind sister, (Mehrnaz) who has been always supported me without even being asked.

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LIST OF ABBREVIATIONS

FTSS	Fault-tolerant Switching Scheme
HFL	High-Frequency Link
HM	Hybrid Modulation
MPPT	Maximum Power-Point Tracking
OSBC	Optimal Sequence-Based Control
PI	Proportional Integral
P&O	Perturb and Observe
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse-Width Modulation
SLR	Switching-Loss Reduction
SPWM	Sine Pulse-Width Modulation
VR	Voltage Regulation
VSI	Voltage-Source inverter

SUMMARY

High-frequency-link (HFL) inverter topologies featuring dc-link-capacitor-less solution have gained tremendous significance due to their higher power density and modular design yielding a superior solution to several conventional inverter approaches for renewable energy systems. Among the HFL inverters, those with pulsating-dc links eliminate the need for bulky dc-link capacitors in contrast to the HFL fixed-dc-link inverters. However in isolated topologies, operating without a buffer stage, performing different control actions such as voltage regulation, MPPT, and loss mitigation in different stages of the inverter independently leads to degraded overall performance. In addition, stiffness of the HFL inverter is reduced against source / load transients because there is no intermediate energy storage.

To address the first issue, a most feasible solution is to perform all of the control actions in a single stage using an optimization-oriented algorithm. Regarding the second issue, a high-bandwidth power conversion is required to provide fast enough dynamic response for the power stage. However, this requires a high switching frequency, which enhances the switching loss of the inverter. Yet another approach is to control the switching sequences of the inverter in such a way so that an optimal dynamic response is achieved without degrading the efficiency.

In this Dissertation a unified controller is proposed, which simultaneously meets different control-performance requirements at disparate time scales (i.e., slow- and fast-time scales) under wide operating conditions. The key advantage of the proposed control over conventional model-predictive and sliding-mode controls is the ability of the proposed control to restrict the control search space to only reachable switching sequences, which are obtained using a composite-Lyapunov function. This feature enables the proposed controller to dynamically change the

switching sequences of the inverter under stability bound. Further, a reduction in the search space for control sequences reduces the time to execute the optimal switching-sequence-based controller. Finally, the feasibility of the inverter when subjected to device fault is also demonstrated using a modulation based switching-sequence control.

I. INTRODUCTION

Renewable energy systems are non-stiff in nature requiring energy storage to provide a stiff interface to the grid in grid-connected mode or to the load in standalone mode of operation. However, the intermittency of renewable energy sources (drop in wind speed, or reduction of sunlight intensity) requires that for certain applications transient energy storage be available for fast-scale reliability and stability. It is also desirable to reduce the effect of these transients in several applications. Achieving such fast dynamic responses require higher operating frequency of the converter which leads to higher switching loss. Yet, another approach is to control the time-evolution of switching states of a converter in an optimal way so that the fast enough dynamic response is achieved in a switching cycle. Fast dynamic control algorithms are prone to instability. As such, they need to be designed and executed under a predefined stability margin to ensure that fast dynamic response is not achieved at the cost of instability or significantly reduced stability margin. Again, this is of more concern in non-stiff energy sources.

High-frequency-link (HFL) inverter topologies featuring dc-link-capacitor-less solution have gained tremendous significance in recent years due to their higher power density and modular design yielding a superior solution to several conventional inverter approaches for renewable energy systems. Recent work [1]-[6] by our group and those [7]-[11] by several reputed researchers world-wide on HFL inverters for photovoltaic, wind, fuel-cell, storage, and electrical-vehicular energy systems have clearly demonstrated the potential of these power-conversion systems with regard to a) power density, b) cost, c) efficiency, d) and fault tolerance. Among the HFL inverters, which significantly reduce the size of the galvanic-isolation

transformer due to HF operation, those with pulsating-dc links eliminate the need for bulky dc-link filters in contrast to the HFL fixed-dc-link inverters [1], [2], [6]. Thanks to the patented hybrid modulation switching scheme [6] this particular topology features an efficiency improvement of 66% as compared with conventional fixed-dc-link voltage-source-inverter (VSI) approach. Capacitor-less design enables retaining of the maximum line information in the pulsating-dc link voltage (V_{REC}), leading to line-frequency switching of the two relevant legs in Ac/Ac converter (Fig. 1).

In isolated and multi-stage converter topologies, comprising a buffer stage (such as a dc-link capacitor), different control objectives can be set for different power-conversion stages without control overlap. Typical control goals in a multi-stage isolated-converter are output voltage regulation, flux balance of the HF transformer, fault-tolerant-switching, noise reduction, loss mitigation, and maximum power point tracking (MPPT). However, in isolated topologies without a buffer stage, performing different control actions in different stages independently leads to degraded overall performance. In other words, the consequence of individual control actions in each stage will propagate to other stages causing control overlap. Therefore, a most feasible solution is to perform all of the control actions in one stage (such as the front-end Dc/Ac converter).

The goal of this Dissertation is to develop a unified controller which simultaneously meets different control performance requirements at disparate time scales (slow and fast time scales) under wide operating conditions. The operation of the controller is desired to be stability bound meaning that the fast dynamic response should not lead to instabilities. Such a controller should also have the capability to prioritize different terms of a multi-objective cost function based on the mode of the operation.

In this chapter, we first outline the motivations of our research in Section 2. Subsequently, in Section 3, we provide a review of the state of the art in related areas. Finally, we provide a brief outline of the subsequent chapters of this Dissertation and describe our key research goals in Section 4.

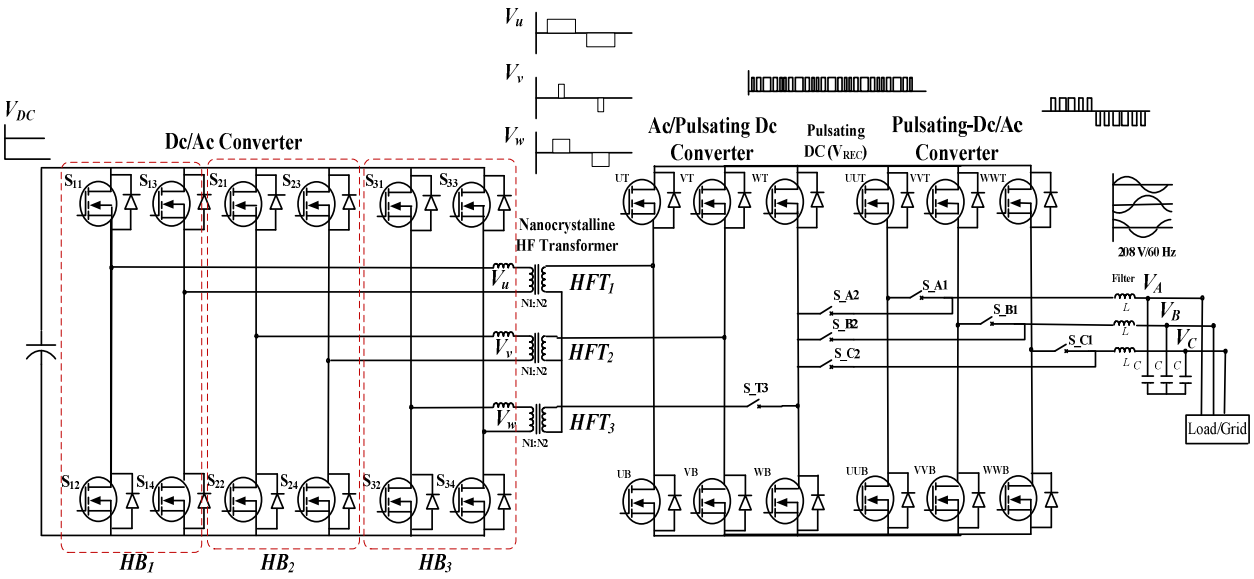


Fig. 1. A multi-stage isolated three phase HFL inverter.

A. Motivations and Objectives of Research

In order to operate a HFL inverter in the most efficient way, a unified control scheme is desired satisfying different control objectives at different time scales and under normal and fault modes. Unification of the individual performance requirements such as voltage regulation, MPPT, loss mitigation, active and/or reactive power injection, flux-balance control of HF transformer, and fault-tolerant operation using a single controller apart from achieving fast dynamic response requires an optimal approach.

In general, inclusion of various performance goals requires some degree of compromise to be made among them depending on the operating conditions. For instance, if the HFL inverter is

connected to a non-ideal dc source with a low-frequency envelope, increasing the switching frequency somewhat reduces the flux imbalance in the HF isolating transformers but increases the switching loss leading to a reduced efficiency. Therefore, if for some reason (e.g., a fault in an active rectifier feeding the Dc/Ac Converter) the frequency of the ac component of V_{DC} (Fig. 1) decreases, the flux imbalance in the HF transformers increases which can be compensated by increasing the switching frequency resulting in a higher switching loss. In other words, under the above condition, the flux balance may attain a higher priority as compared to loss mitigation. Hence, to prevent core saturation of the HF transformer, a compromise has to be made on the loss mitigation by increasing the switching frequency.

As another example, a compromise can be made between switching loss and voltage regulation in standalone as well as in grid-connected modes of operation. More specifically, if we consider a set of reachable switching sequences for a typical boost converter, it is found that some of the switching sequences lead to less number of commutations and hence yield reduced switching loss (Fig. 2). Also note that, this reduced switching loss is obtained at the cost of higher voltage ripple (Fig. 3). This statement can be generalized to a HFL inverter as well as shown in Fig. 1.

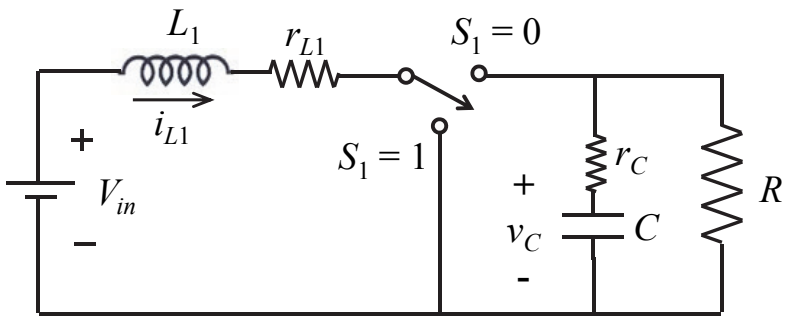
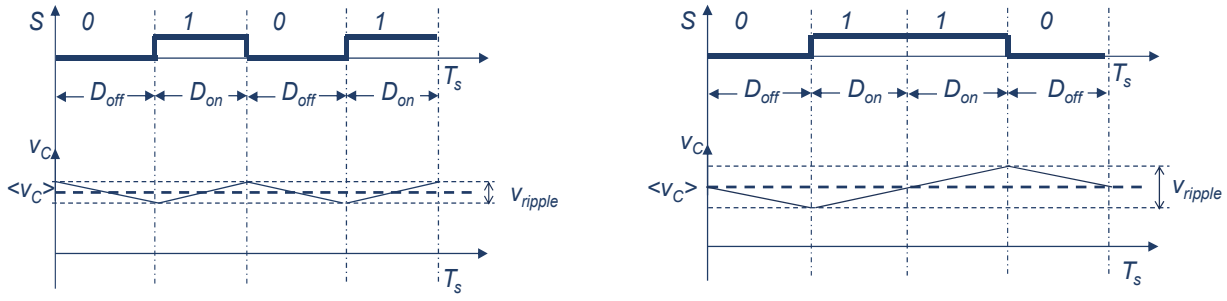


Fig. 2. A boost dc-dc converter.



(a) (b)

Fig. 3. Compromise between the number of commutations and output voltage ripple. (a) Using a switching sequence of (01) a total number of 2 commutations in a switching cycle (T_s/2) is achieved with a lower output voltage ripple compared to (b) which using switching sequence of (0110) yields a total of two commutation in the switching cycle (with a period of T_s) but for a cost of higher ripple.

As another example (Fig. 4), consider a grid-connected HFL inverter operating with two independent control schemes to address MPPT as well as switching-loss-mitigation. According to the I-V characteristics of the photovoltaic (PV) cells and based on an optimization algorithm, a certain amount of power, corresponding to the maximum operating efficiency of the PV panel, is injected into the grid. Loss-mitigation scheme is based on a soft-switching open-loop control algorithm. However, because the loss mitigation mechanism is not included in the overall control scheme, there is no guarantee that the overall efficiency of the whole system (comprising the PV panel and the HFL inverter) is optimized at the operating point dictated by the MPPT algorithm. For instance, assume that according to the MPPT algorithm, if a certain current I_{MPPT} is injected

into the grid, the PV panel operates at the highest efficiency. However, there is a current I_2 ($I_2 < I_{MPPT}$) at which the efficiency of the HFL inverter increases 1% compared to I_{MPPT} (due to lower conduction loss) while the efficiency of the PV reduces by 0.5%. Therefore, the overall efficiency of the whole system will increase by 0.5% if it operates at I_2. However, if there is no compromise between MPPT and loss mitigation, I_{MPPT} will be dictated by MPPT which is not necessarily the global optimum operating point.

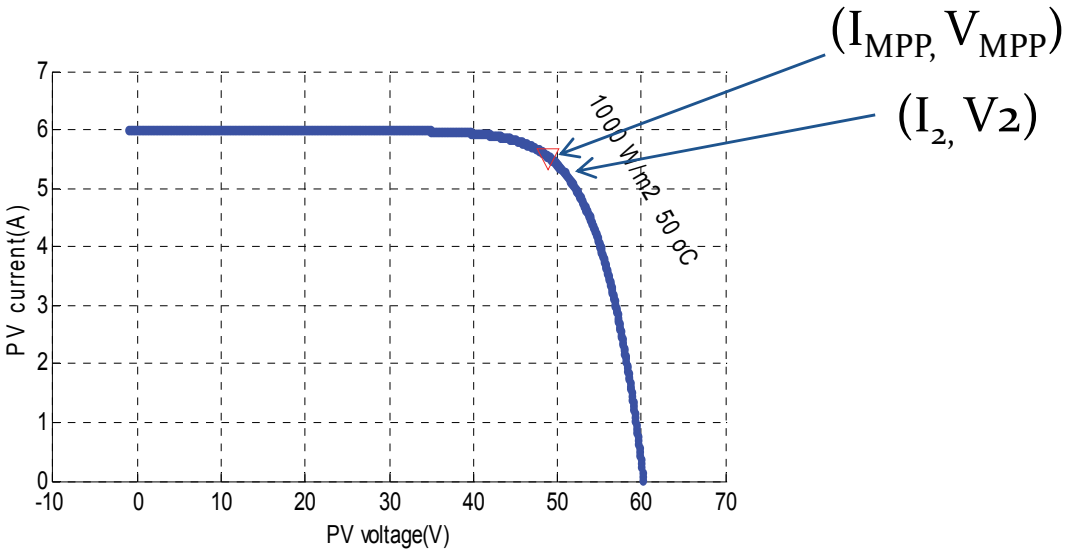


Fig. 4. Joint optimization of MPPT and loss mitigation.

Regarding fast dynamic response, one approach would be to increase the switching frequency so that a higher bandwidth is achieved for the controller. However, the drawback of this solution is higher switching losses. A more sophisticated approach is to control the time evolution of the switching states (switching sequences) by solving an optimal control problem.

Based on the above statements and reasoning, a mechanism is desirable which can adaptively adjust the priority of various control objectives at disparate scales depending on the different operating conditions. Moreover, as stated earlier, in a buffer-less topology such as the HFL

inverter of Fig. 1, the consequence of individual control actions in each stage will propagate to other stages causing control overlap. Therefore, a most feasible solution is to perform all of the control actions in one stage. This is another reason for unifying all of the control goals.

On the other hand, in order to develop solutions for any of the individual control goals, such as fault-tolerant control and soft switching, a significant effort is needed to come up with a proper scheme intuitively. However, use of an optimal approach simplifies this procedure in that by inclusion of a new term (defining the relevant performance criterion) into a cost function an all-encompassing solution is generated and applied to the system without relying on intuition.

Our research is an attempt to address some of the issues mentioned in this section and to synthesize a unified control scheme for a HFL inverter. Thus, the key objectives of our research are as follows:

- Synthesize a unified controller which simultaneously meets different control requirements at disparate time scales with capability of prioritizing different control objectives under various operating conditions;
- Design algorithms for fast and robust execution of the synthesized control scheme;
- Validate the proposed control scheme using application scenarios.

B. Literature Review

In this section, a review of the literature on the control objectives for HFL inverters is conducted. In the context of HFL inverters, output-voltage regulation is widely discussed in the literature [12]-[20]. In reference [12], a soft-switched single-stage bidirectional HFL inverter topology is discussed with the bipolar combined phase-shifted SPWM control schemes. A

double loop control scheme is used with an outer loop for output voltage regulation and an inner loop for inductor current control. A proportional-integral (PI) controller is used for the outer loop and a one-cycle controller is used for the inner loop.

In [13], a control strategy with double closed-loop feedback for the output voltage is proposed for a bidirectional quasi-single-stage push-pull forward HFL inverter. This control scheme is based on sensing the transient output load voltage as an inner feedback loop to ensure that the load voltage is sinusoidal and well regulated. An average outer voltage feedback loop is also incorporated in the proposed control system.

Reference [14], presents the analysis and design of a dual-loop controller based on pole-assignment for a HF link inverter. The dual-loop controller consists of an inner current loop and an outer voltage loop. The inner current loop adopts a control method combined the instantaneous inductance current control with the forward compensation control of the disturbing loads. In [15], a new control scheme in the design of HFL inverters is suggested which lowers the switching frequency in the cycloconverter stage. Again a PI controller is exploited for the output voltage control loop. In [16], a novel control method for a high-frequency link inverter using cycloconverter techniques is suggested and a surge reduction circuit is presented for the inverter. In [17], a two-degree-of-freedom proportional-integral-derivative (PID) digital controller is applied to achieve high performance in both the command tracking and the load-disturbance regulation for a bidirectional quasi-single-stage push-pull forward HFL inverter.

Reference [18] proposes a double closed-loop controller with load current feed-forward for an active-clamp bi-directional voltage mode HFL inverter. Based on the current inner loop within the voltage outer loop, a load current feed-forward controller is introduced which can be used to improve the dynamic response of the inverter system. In [19], a proportional-resonant (PR)

controller is designed for a full-bridge full-wave HFL inverter with an active clamper. In [20], a PID digital controller is applied to achieve high performance in both the command tracking and the load disturbance regulation for a photovoltaic HFL inverter.

In [21], a deadbeat controller for a bidirectional HFL inverter is described. The proposed controller consists of an inner current loop, an outer voltage loop and a feedforward controller. Additional disturbance decoupling networks are employed to improve the robustness of the system towards load variations. References [22] and [23] also present a deadbeat controller for output voltage regulation and disturbance rejection for a bidirectional HFL inverter. Reference [24] uses a sliding-mode control scheme for voltage regulation of a HFL matrix inverter. In [25], a resonant power-conversion technique is applied to HFL inverters. Reference [26] presents a HFL inverter system using a resonant tank applied to a photovoltaic AC module and discusses the relevant grid regulation scheme.

In [27], a proportional and multi-resonant controller is suggested for a three-phase four-wire HFL inverter in order to achieve voltage regulation while supplying unbalanced and nonlinear loads. Reference [28] proposes a control scheme for a standalone HFL inverter topology based on a quasi-square modulation in the primary side Dc/Ac converter. The main goal of the control scheme proposed in this paper is output voltage regulation and load disturbance rejection. However, the topology itself does not provide any redundancy in the primary side of the HF transformer and switching of the Ac/Ac converter is not lossless.

MPPT is one of the other control goals which is an essential part of every PV power-conversion system. Reference [29] suggests a simple control strategy for MPPT and grid power injection control verified on a multi-stage isolated single-phase grid-connected HFL inverter with dc-link low-pass filter. However, because the PV-side and the grid-side inverter stages

(transferring power from dc-link to the grid) are all hard-switched, the efficiency of the overall power-conditioning unit is low, which is more severe in higher-power applications. References [30] and [31] outline a PI controller to realize MPPT for a multi-stage isolated single-phase grid-connected HFL inverter with dc-link low-pass filter. The front-end Dc/Ac converter is hard-switched and the overall efficiency is not optimized. Effects of fault and other disturbances are not considered and the proposed system is not robust against parameter changes. Reference [32] proposes a resonant HFL inverter for interfacing a PV to the utility grid and considers application of MPPT to the PV.

Reference [33] suggests a grid-control and a MPPT scheme for a multi-stage isolated single-phase grid-connected HFL inverter with dc-link low-pass filter. Therefore, the secondary-side inverter only unfolds the dc-link voltage to generate the ac current at the output port. A feedforward scheme is used to remove the loop gain dependence on the utility grid and keeps the maximum power extraction from the PV during variable grid voltage. Reference [34] discusses application of a proportional-integral-resonant (PIR) controller with MPPT for a cycloconverter type HFL conversion system for grid interfacing of PV.

Majority of the papers referred to above discuss only the MPPT and grid-current regulation. They focus on different multi-stage topologies including isolated HFL inverters with dc-link filters, resonant converter based HFL inverter, and cycloconverters with HFL. It seems that limited work has been carried out with focus on capacitor-less HFL inverter interfacing a PV to the grid. Besides, none of the previous works has considered the combination of the PV and the power-conversion system as a whole unit for which an optimized scheme is needed. On the other hand, many of these papers do not include any loss-mitigation scheme for the power-conditioning system. Even if one or more than one stage is soft-switched, there is no weighted

optimization among MPPT and loss mitigation schemes to increase the efficiency of the whole system at different operating conditions.

Generally, in the surveyed literature on different control goals for HFL inverters such as voltage regulation, current injection into the grid, and MPPT, limited work has been done on control of capacitor-less multi-stage isolated HFL inverter. Different control approaches like PI, PR, deadbeat control, and sliding-mode control are applied to various HFL topologies such as isolated HFL inverters with dc-link filters, resonant converter based HFL inverter, and cycloconverters with HFL.

On the other hand, developing some control schemes (such as loss mitigation) usually takes a lot of efforts and is done intuitively. This issue is more reasonable when the power-conversion topology is more complex and has inter-related stages such as a capacitor-less HFL inverter [35], and [11]). Using OSBC helps to synthesis different control schemes such as MPPT, voltage regulation, grid-current regulation, loss mitigation, flux-balance control, fault-tolerant control, and noise reduction without too much of effort and even makes it possible to do a joint-optimization of two or more control objectives. Using this approach even makes it possible to change the weightage of various control functions based on the operating conditions and new system requirements.

C. Research Outline

The main emphasis of this Dissertation is to develop a unified controller for a HFL inverter optimally meeting various control objectives at disparate time scales. This controller is also capable of changing the weightage of different control goals based on the operating condition.

Using an optimal sequence-based control (OSBC) technique to directly control the switching of the HFL inverter ensures a superior dynamic performance since the controller design is based on a discontinuous model of the power stage rather than on an average model which is used in conventional controller design.

In this Dissertation, we address the above-mentioned issues and outline our proposed approach to achieve the objectives that were presented in Section 2. We believe that the new approaches for unified control of HFL inverters that are outlined in this Dissertation will lead to improved overall performance of HFL inverters in particular and switching power converters (SPCs) in general.

In Chapter 2, an OSBC scheme is developed to regulate the output voltage of the HFL inverter in standalone mode of operation and control the injected current into the grid. First of all, a discontinuous model for the HFL inverter is derived in stationary frame for both standalone and grid-connected modes of operation and then transformed to a synchronous-rotating frame (*dq0*). Then, a composite Lyapunov function is used to determine a reachable subset of the total number of feasible switching sequences. Superior dynamic response of the HFL inverter in both operating modes is compared with that of a conventional linear controller designed based on an average model of the HFL inverter.

Further, other control objectives such as switching loss-reduction and MPPT (which are fast-scale and slow-scale parameters) are integrated into the optimization frame.

In Chapter 3, a novel fault-tolerant switching scheme (FTSS) is proposed for all of the three stages in a multi-stage isolated HFL inverter. The proposed FTSS is designed based on the inherent redundancy of one phase in the primary side Dc/Ac Converter and Ac/Pulsating-Dc Converter and is based on changing the PWM references for the remaining full-bridge converters

upon detection of the fault using a proposed fault diagnosis system. The new switching scheme provides the continuity of service of the inverter while maintaining acceptable dc-link and output voltages when one or even two phases of the Dc/Ac Converter ceases to generate any output, or when one phase in Ac/Pulsating-Dc Converter or Pulsating-Dc/Ac Converter fails. Effect of the time (or phase angle) at which a fault happens was discussed and based on a comprehensive analysis of the latter a fault diagnosis algorithm is proposed. In the diagnosis step, the distortion pattern of the three line voltages V_{AB}, V_{BC}, and V_{CA} are diagnosed. As explained in Section III of this chapter, by analyzing the pattern of distortion in each of the three line voltages with regard to phase angle, one can determine the lost phase and the faulty stage.

In the next step, based on the type of lost phase(s) and faulty stage, the PWM reference for the remaining phase(s) is changed so as to restore the output line voltages of the inverter. The effectiveness of the FTSS under various fault scenarios was investigated through experimental results on a 1-kW prototype and found to be satisfactory. The results of this chapter verify that the unified controller can be exploited not only under normal operation mode, but also when a fault has happened in any of the stages of the HFL Inverter of Fig. 1.

In Chapter 4 an OSBC-based switching loss reduction scheme is proposed for the HFL inverter of Fig. 1 which is based on the joint optimization of voltage regulation / grid control primary control goals and switching loss mitigation. The main contribution of this loss-mitigation scheme is first of all, the automated nature of the developed switching sequences as compared with the heuristically developed hybrid modulation scheme and secondly its capability to be generalized for other HFL Inverter topologies.

Finally, in Chapter 5 we draw conclusions based on the work outlined in this Dissertation. Further, potential future work is outlined as an extension to this Dissertation.

II. SEQUENCE-BASED MODELING, STABILITY ANALYSIS, AND CONTROL OF AN ISOLATED MULTI-PHASE HIGH-FREQUENCY-LINK (HFL) INVERTER FOR RENEWABLE-ENERGY SYSTEMS

Abstract—**This chapter describes the control of an isolated multi-phase HFL inverter by controlling the time evolution of its switching states (or, switching sequences). It is referred to as the optimal-switching-sequence-based control (OSBC). Unlike several conventional control schemes, where, typically the control is based on averaged model of the inverter and the modulation scheme sets a pre-determined switching sequence, OSBC synthesizes the fundamental switching sequence depending on the control needs on the fly. For instance, OSBC can seamlessly play with the inverter switching sequences if the input voltage of the inverter changes as evident in solar or wind-based energy systems. This necessitates that OSBC use a switching-sequence-based discontinuous (instead of averaged) modeling approach. Further, the stability of the closed-loop inverter is determined in OSBC using an advanced composite Lyapunov-function based approach, which also enables one to predetermine the reachability of the inverter dynamics for a given switching sequence. Thus, optimal control in OSBC is ensured under stability bound of the switching sequence. This provides a fundamental difference between OSBC and model predictive control for inverters. This also implies that in a multi-objective OSBC, one can shift the weights of the individual cost functions to yield better inverter performance without compromising stability.**

Index Terms—**Inverter, modeling, stability, control, three phase, switching sequence, Lyapunov function, map, optimal**

A. Introduction

High-frequency-link (HFL) power conversion systems (PCSs) have been widely studied recently as a popular interface between renewable energy sources and loads/utility grid. Among

various proposed topologies, capacitor-less HFL inverter has gained tremendous significance in recent years due to its superior benefits of cost, modular design and scalability, high power density, efficiency and fault-tolerant operability [1]-[6], [11], [35], [36]. However, removal of a bulky dc-link capacitor leads to the following challenges:

1- Lack of an intermediate buffer stage between different power stages of the HFL inverter results in interference between control actions implemented in different stages.

2- Stiffness of the HFL inverter is reduced against source / load transients since there is no temporary power storage such as a bulky dc-link capacitor.

Hence, in order to take the full advantage of this perfect topology for renewable energy applications, the above issues need to be addressed properly. Regarding the first issue, the potential solution to implement different control objectives effectively and without interference in such a buffer-less multi-stage topology seems to be an optimization-oriented algorithm. To address the second issue, one possible solution is to design a high-bandwidth power conversion to yield fast enough dynamic response for the power stage. However, this requires a high switching frequency which also increases the switching losses and degrades the efficiency of the HFL inverter [1]. Yet another approach is to control the time evolution of the switching states (i.e. the switching sequence) of the inverter in such a way so that optimal dynamic response is achieved for a given switching frequency. Traditional control of the inverter in synchronous or stationary frame implement the basic control scheme without the modulator under consideration and then use a predetermined modulation scheme to transform the continuous output of the controller to a discontinuous one that after level shifting can be used to activate the devices of the inverter [37]. The reason behind such a two-step implementation is that, typically the

averaged output of the inverter evolves on a slow scale (e.g. 60/50 Hz scale) and the fast scale is essentially filtered.

Recently, our research group has demonstrated (using non-isolated converters) that by directly controlling the sequence of a power converter, control and modulation can be integrated, as illustrated in Fig. 5 [38]. Such a closed-loop controller does not need a predefined modulation scheme and hence the switching sequence can be generated on the fly simply based on a single or multi-objective cost function. The HFL inverter shown in Fig. 7 is used to show the effectiveness of the proposed controller. We will demonstrate in Section III, the superior transient performance of this optimal-sequence-based control (OSBC). What is unique about this OSBC, as described in this chapter, the control is achieved under stability bound. That is even though the inverter has multiple but finite switching sequences, a unique composite Lyapunov function [39] based stability approach (as outlined in Section II) determines which of these switching sequence ensures reachability and these feasible sequences are used for OSBC under stability bound. Thus OSBC is different from traditional model predictive control [40] and sliding mode control [41]. Moreover, since OSBC is implemented by solving an optimal problem, joint-optimization of various control objectives (which could happen at different scales) such as voltage regulation in standalone mode of operation, grid control in grid-connected mode of operation, switching-loss mitigation and maximum power point tracking (MPPT) can be individually or jointly realized. Joint-optimization of such multi-scale parameters are also developed and verified through several results in this chapter.

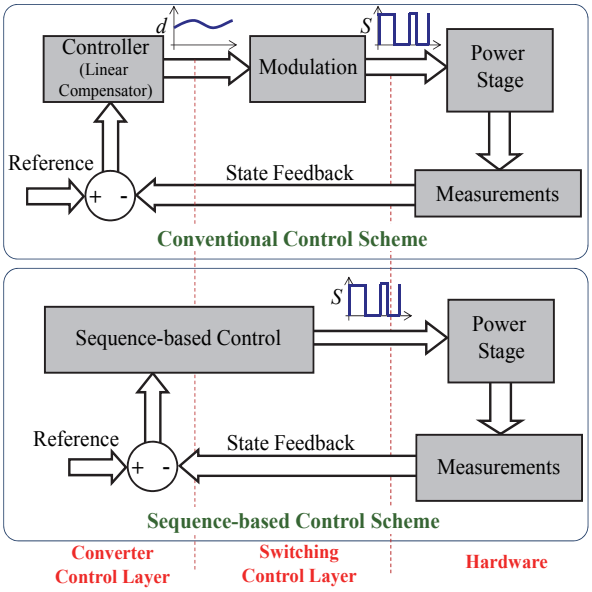


Fig. 5. Block diagram illustrating a comparison between a conventional control scheme for power electronic converters and a sequence-based control scheme.

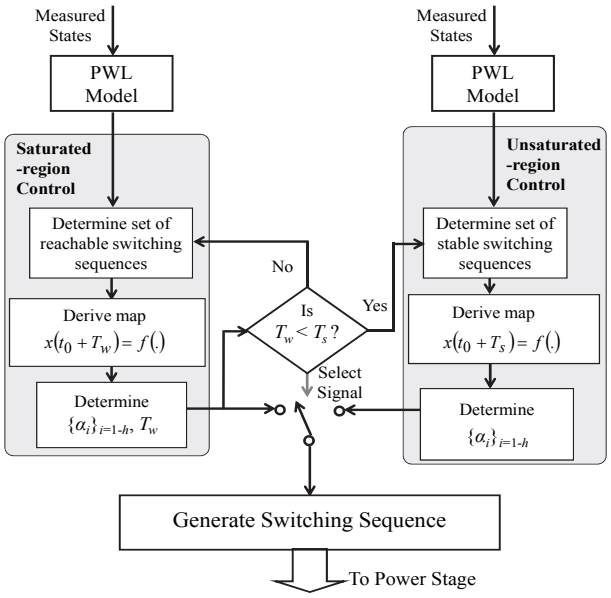


Fig. 6. Schematic illustrating the operation of OSBC. The "Select Signal" is used to switch from SROC to USROC when $T_w < T_s$.

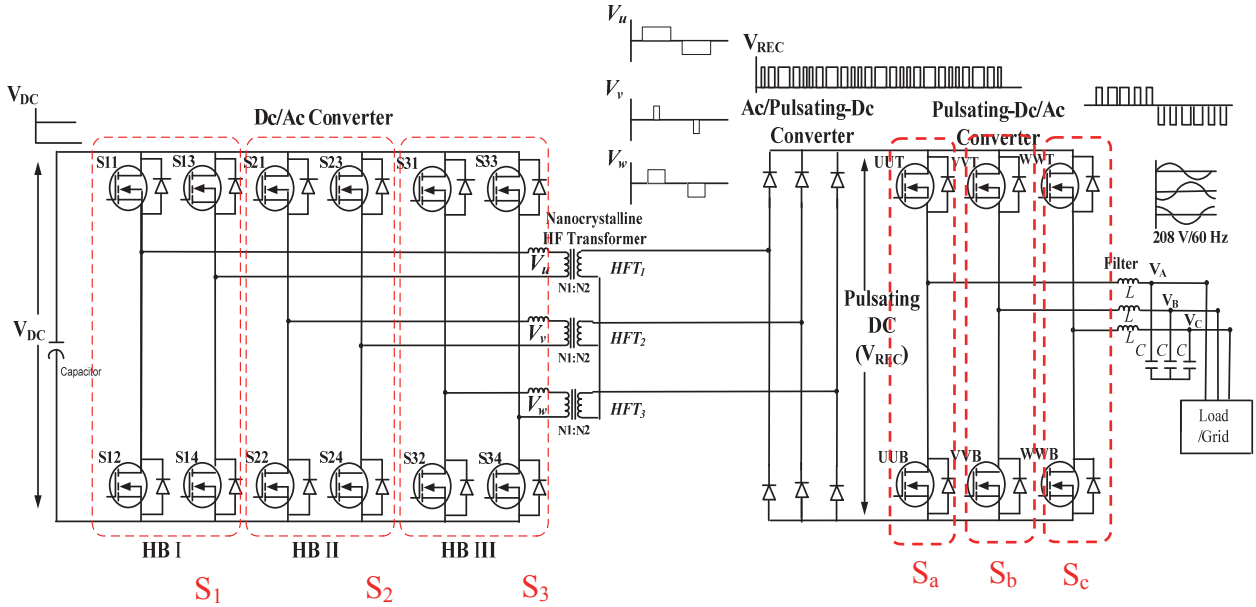


Fig. 7. Topology and definition of switching functions (S_1, S_2, S_3, S_a, S_b, and S_c) of HFL inverter.

B. Optimal Sequence-Based Control (OSBC)

OSBC is an advanced model predictive control which directly controls the evolution of switching states (switching sequences) of devices (such as MOSFETs) of a power converter through minimization of a predefined cost function. As a result, the optimal switching sequences and also the relevant time horizon for which the HFL inverter stays in each switching state are determined. A flowchart for OSBC is shown in Fig. 6 which shows that the overall control comprises two key elements: "(a) a saturated-region optimal control (SROC) that controls the converter dynamics from an arbitrary initial condition to the steady-state (or orbit)" [38] and "(b) an unsaturated-region optimal control (USROC) that controls the steady-state dynamics of the converter" [38]. In this section, the necessary steps for development of the OSBC scheme for a three-phase HFL inverter are described in detail. The first step is to derive a piecewise-linear (PWL) model for the HFL inverter in terms of switching functions defined according to the number of switching devices and their modes of operation in the HFL inverter. Having set the PWL model, firstly the total number of possible switching sequences is determined and subsequently, a set of reachable or feasible switching sequences is selected based on a reaching criterion. The final step is to design an OSBC scheme which is a constrained optimization problem aimed to minimize a predetermined cost function under system constraints.

1. General PWL Modeling of an Isolated Three-Phase HFL inverter (Standalone Operation)

With respect to Fig. 7, showing the topology of a HFL inverter, three switching functions are defined respectively for three legs of the Pulsating-Dc/Ac Converter as S_a, S_b, and S_c such that

S_a, S_b, $S_c \in \{0,1\}$ (top and bottom switches in each leg switch complementarily to prevent a short circuit of the input dc source). Also, for each H- bridge of the front-end Dc/Ac Converter (marked as HBI, HBII, and HBIII) a switching function is assigned such that S_1, S_2, $S_3 \in \{-1,0,1\}$; the value of the switching function depends on whether the polarity of the bipolar and tri-state pulse train generated is negative, zero, or positive . However, because the Ac/Pulsating-Dc Converter rectifies the pulse train outputs of three HF transformers, the values of 1 and -1 could be treated the same while tabulating the switching state table.

The state vector for this HFL inverter is defined as $x = (i_a, i_b, i_c, v_a, v_b, v_c)^T$ consisting of the HFL inverter three-phase currents and voltages. A PWL state-space model is derived for the HFL inverter which is of the form:

$$\dot{x} = Ax + B_{i,j} \tag{1}$$

where i represents the switching sequence of the HFL inverter, j determines the switching states of the i^{th} switching sequence, x represents the converter states, and A and $B_{i,j}$ are matrices and vectors of appropriate dimensions that model the converter in each switching state. First, a set of differential equations in terms of states and switching functions are written for the HFL inverter using Kirchoff's voltage and current laws (i.e., KVL and KCL) as follows:

$$\begin{cases} L\dot{i}_{abc} = \frac{1}{3}B' S_{abc} V_{REC} - V_{abc} \\ C\dot{V}_{abc} = i_{abc} - \frac{1}{R}V_{abc} \end{cases} \tag{2}$$

where $i_{abc} = (i_a, i_b, i_c)^T$, $V_{abc} = (v_a, v_b, v_c)^T$, $S_{abc} = (S_a, S_b, S_c)^T$, $V_{REC} = \frac{N_2}{N_1} V_{DC} \max(S_1 - S_2, S_1 - S_3, S_2 - S_3)$ and B' is defined in Appendix A. Based on the above set of differential equations, a PWL model for the HFL inverter in terms of switching functions and in the stationary abc frame is derived as follows:

$$\dot{X}_{abc} = A_{abc}X_{abc} + B_{abc} \tag{3}$$

where $X_{abc} = (i_a, i_b, i_c, v_a, v_b, v_c)^T$. However, in order to make the controller design more straightforward and to deal with dc variables instead of ac ones, the PWL model in (3) is mapped into *dqz* synchronous frame using Park's transformation as follows:

$$\dot{\bar{X}}_{dq} = A_{dq}\bar{X}_{dq} + B_{dq} \tag{4}$$

where $X_{dq} = \left(i_d, i_q, v_d, v_q\right)^T$, ω is the line (slow scale) angular frequency, and S_d and S_q are the switching functions in dq frame. Matrices A and B in abc and dq frame are given in Appendix A. Note that B_{abc} and B_{dq} are functions of switching sequences as stated in the general form (1). Also note that, here a symmetrical system is assumed and as a result, the *z*-axis parameters are neglected and removed from the derived model. The total number of switching states base on the

TABLE I. POSSIBLE SWITCHING STATES FOR HFL INVERTER

i	S_d	S_q	S_{d1}	S_{q1}
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

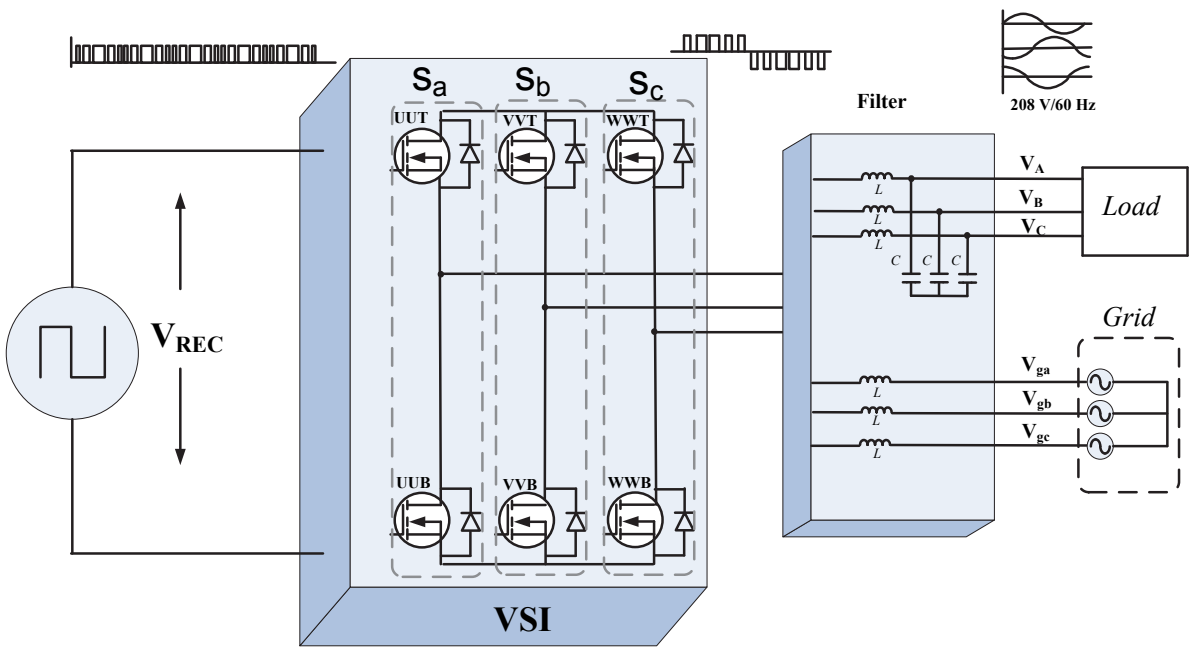


Fig. 8. Simplified topology of HFL inverter used for PWL modeling with reduced number of switching functions.

mapped switching functions S_d and S_q as well as S_{d1} and S_{q1} (equivalents of S_1, S_2, and S_3 in dq reference frame) are provided in Table I. Based on the possible switching states mentioned in Table I, the total number of feasible combinations of switching sequences is obtained as follows [39]:

$$M = \sum_{l=1}^{(2^N - W)} \left(\frac{(2^N - W)!}{l!(2^N - W - l)!} \right) = \sum_{l=1}^{(2^4)} \left(\frac{(2^4)!}{l!(2^4 - l)!} \right) = 65535 \tag{5}$$

where N is the total number of non-complementary switching functions and W is the number of redundant switching states (switching states for which the state-space equations of the switching system are identical). With a search space of this size, the optimization process will take so long because the OSBC algorithm needs to search for the optimal switching sequence amongst a total

number of 65,535 feasible candidates. Therefore, in order to reduce the search space and increase the rate of optimization, a different modeling approach is chosen which will be explained in detail in the next section.

2. Simplified PWL Modeling of an Isolated Three-Phase HFL inverter (Standalone Operation)

In order to reduce the search space and to speed up the optimization process, a simplified model of the HFL inverter will be derived and used. The HFL inverter of Fig. 7 could be considered as a standard voltage-source inverter (VSI) connected to a Pulsating-Dc voltage source input, V_{REC} (Fig. 8). As shown in the Appendix A, in (4), V_{REC} is embedded in B_{dq}. In order to develop the PWL model of the HFL inverter, initially a Fourier series representation of V_{REC} is described as follows:

$$V_{REC} = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}\{a_n cos\omega_n t + b_n sin\omega_n t\} \tag{6}$$

where $a_0 =< V_{REC} >$, $a_n = \frac{\sin(2n\pi D)}{n\pi}V_{REC}$, $b_n = \frac{V_{REC}}{n\pi}\{1 - \cos(2n\pi D)\}$, $\omega_n = 2n\pi/T_p$, represents the frequency of the n^{th} order harmonic component of V_{REC} (T_p is the period of the fundamental component of V_{REC}), and D is the duty cycle of pulses in V_{REC}. Using (6) and (4), an augmented PWL model of the HFL inverter can be derived. To do so, each harmonic component of V_{REC} is described by two additional states called y_{n1} and y_{n2} that are defined as follows:

$$y_{n1} = a_n cos\omega_n t + b_n sin\omega_n t \tag{7a}$$

$$\frac{dy_{n1}}{dt} = -\omega_n a_n cos\omega_n t + \omega_n b_n sin\omega_n t = y_{n2} \tag{7b}$$

$$\frac{dy_{n2}}{dt} = -\omega_n^2 a_n cos\omega_n t - \omega_n^2 b_n sin\omega_n t = -\omega_n^2 y_{n1} \quad (7c)$$

An augmented PWL model for the HFL inverter using the simplified model in Fig. 8 is provided in Appendix A.

3. Simplified PWL Modeling of an Isolated Three-Phase HFL inverter (Grid-Connected Operation)

So far a discontinuous model in terms of switching functions was derived for standalone operation. For grid-connected operation, the state vector in abc synchronous reference frame and dq stationary reference frame would be $X_{abc} = (i_a, i_b, i_c, V_{DC})^T$ and $X_{dq} = \left(i_d, i_q, V_{DC}\right)^T$, respectively. Input vector U in the general form of $\dot{x}(t) = Ax(t) + BU$ is described by $U = [-V_{gd}, -V_{gq}, i_{pv}]^T$. According to KVL and assuming a symmetrical three phase system, we have the following set of differential equations:

$$\bar{V}_g = -R\bar{\imath}_{abc} - L\dot{\bar{\imath}}_{abc} + \frac{1}{3}B' \times \bar{S}_{abc}.V_{REC} \quad (8)$$

$$C\dot{V}_{DC} + \bar{S}_{abc}.\bar{\imath}_{abc} \times Max(|S_1 - S_2|, |S_1 - S_3|, |S_2 - S_3|) = i_{pv} \quad (9)$$

As stated before, different terms included in the above equations are $\bar{\imath}_{abc} = (i_a, i_b, i_c)^T$, $\bar{v}_{abc} = (v_a, v_b, v_c)^T$, $\bar{S}_{abc} = (S_a, S_b, S_c)^T$, $V_{REC} = \frac{N_2}{N_1} \times V_{DC} \times MAX\{(S_1 - S_2), (S_1 - S_3), (S_2 - S_3)\}$ and B' are defined in Appendix A. In order to simplify (8) and (9), we assume that in the front-end Dc/Ac converter only two full bridges operate (those with switching functions S_1 and S_2) and the third one is a redundant phase for fault-tolerant operation. This leads to

$$C\dot{V}_{DC} + \bar{S}_{abc}.\bar{\imath}_{abc} \times (|S_1 - S_2|) = i_{pv} \quad (10)$$

$$V_{REC} = \frac{N_2}{N_1} \times V_{DC} \times (S_1 - S_2) \tag{11}$$

Using (1), (8), (10), and (11), matrices A_{abc} and B_{abc} for PWL model of the HFL inverter in grid-connected operation is derived in abc stationary reference frame and is included in Appendix A.

Using the Park transformation matrix, mathematical model of HFL inverter in $dq0$ rotating frame can be derived as follows:

$$L\dot{\bar{\imath}}_{dq} + R\bar{\imath}_{dq} + f(\omega).L.\bar{\imath}_{dq} = (S_1 - S_2).N.V_{DC}.\bar{S}_{dq} - \bar{V}_{gdq} \tag{12}$$

$$C\dot{V}_{DC} = -\frac{3}{2}\bar{\imath}_{dq}.\bar{S}_{dq}(S_1 - S_2) + i_{pv} \tag{13}$$

where $f(\omega) = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$. Equations (12) and (13) yield matrices A_{dq} and B_{dq} that are needed to describe (under grid-connected operation) the PWL model of the HFL inverter as captured in Appendix A.

Matrices for the discontinuous model derived for grid-connected mode of operation can also be derived in a way similar to that adopted for the standalone mode (i.e., using a model of the VSI with a Pulsating-Dc input source represented by a Fourier series). Such a model is provided in Appendix A.

For standalone or grid-connected modes of operation, there exists only three switching functions (i.e., S_a, S_b, and S_c) for the HFL-Inverter model when it is described in the abc stationary reference frame. When the HFL-Inverter model is described in the dq frame, the corresponding switching functions are described by S_d and S_q. Based on this definition, the possible switching states are tabulated in Table II while the total number of feasible combinations of switching sequences, obtained using the following relation are tabulated in Table III:

$$M = \sum_{l=1}^{(2^N - W)} \left(\frac{(2^N - W)!}{l!(2^N - W - l)!} \right) = \sum_{l=1}^{(2^2)} \left(\frac{(2^2)!}{l!(2^2 - l)!} \right) = 15 \quad (14)$$

TABLE II. POSSIBLE SWITCHING STATES FOR HFL INVERTER USING SIMPLIFIED PWL MODEL.

i	S_d	S_q
1	0	0
2	0	1
3	1	0
4	1	1

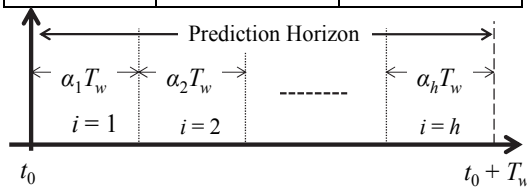


Fig. 9. Illustration of the prediction horizon for computation of the optimal control law.

TABLE III: POSSIBLE FEASIBLE COMBINATIONS OF SWITCHING SEQUENCES BASED ON TABLE II.

M	Switching sequences				Total number of combinations
	first SS*	second SS	third SS	fourth SS	
1	i = 1				4
2	i = 2				
3	i = 3				
4	i = 4				
5	i = 1	i = 2			6
6	i = 1	i = 3			
7	i = 1	i = 4			
8	i = 2	i = 3			
9	i = 2	i = 4			
10	i = 3	i = 4			
11	i = 1	i = 2	i = 3		4
12	i = 1	i = 2	i = 4		
13	i = 1	i = 3	i = 4		
14	i = 2	i = 3	i = 4		
15	i = 1	i = 2	i = 3	i = 4	1

***SS = switching state**

In contrast to the other optimal control methods such as model-predictive control (MPC), which has been applied for controlling switching power converters (SPCs), in the OSBC, only a set of reachable switching sequences are used to perform the optimal control of a SPC in general. This ensures that if control requires any jump between switching sequences, this transition should be stable. Hence, among the total feasible switching sequences given in Table III, a reachable set is calculated using a composite-Lyapunov-function (CLF) based criteria [39] as outlined in the next section.

4. Stability Analysis of an Isolated Three Phase HFL Inverter

In order to determine a set of reachable switching sequences from among all of the fundamental switching sequences provided in Table III, the following linear matrix inequality is solved using the simplified PWL model of the HFL inverter shown in Fig. 8:

$$\sum_{i=1}^{h} \propto_{ki} \begin{bmatrix} A^T P_{ki} + P_{ki} A & P_{ki} \bar{B}_i \\ \bar{B}_i^T P_{ki} & 0 \end{bmatrix} < 0 \qquad (15)$$

where $k = 1,2, \ldots, M$, h is the number of switching states in a given switching sequence, $\propto_{ki}$ are the weights of the composite Lyapunov functions in each switching state such that $0 \leq \propto_{ki} \leq 1$, $\sum_{i=1}^{h} \propto_{ki} = 1$, $P_{ki} = P_{ki}^T > 0$, and $\bar{B}_i = -B_i - AX^*$. The results of reaching analysis for all of the switching sequences in Table III are shown in Fig. 10. The reaching criterion is assessed for standalone and grid-connected modes of operation. For the standalone mode of operation of the HFL inverter the simplified PWL, as derived in Section B and presented in Appendix A, is used for a range of a_0 between 200 V and 500 V and a resistive load (P_L) varying between 2.5 kW and 10 kW. It is demonstrated that, the switching sequences M = 13, 14 are not reachable for any input-voltage dc component (a_0) and any load in the above range. Fig. 10a shows the result of this analysis for standalone mode of operation.

For grid-connected mode of operation the PWL model, as derived in Section C and presented in Appendix A, is used for a range of a_0 between 200 V and 500 V and a range of injected active power into the grid (P_G) varying between 2.5 kW and 10 kW. It is determined that, the switching sequences M = 13, 14 are not reachable for any input-voltage dc component (a_0) and any load in the above range. Fig. 10b shows the result of this analysis for grid-connected mode of operation.

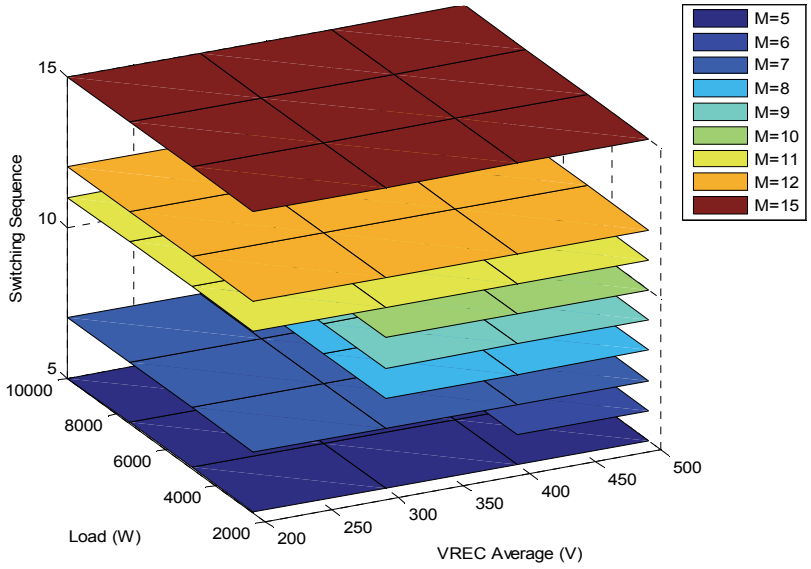


Fig. 10a. Plot showing the stability / reachability of switching sequences in Table III for the HFL inverter vs. the input voltage dc component (a_0) and load power. Existence of a plain (associated with a specific switching sequence according to the legend) shows reachability of that specific switching sequence whereas the extents of the plain show the range of load power and input voltage dc component for which the switching sequence is reachable. It is shown that the switching sequences M = 13 and 14 are not reachable for any range of a_0 and P_L.

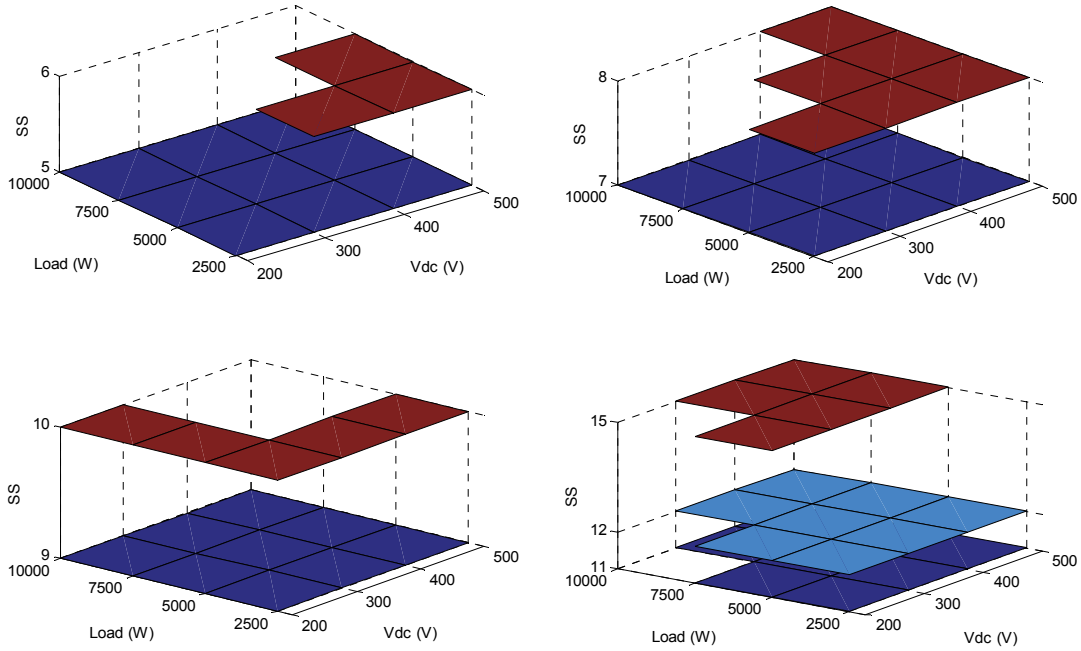


Fig. 10b. Plot showing the stability / reachability of switching sequences in Table III for the HFL inverter vs. the input voltage dc component (a_0) and injected power into the grid. Existence of a plain (associated with a specific switching sequence according to the z-axis) shows reachability of that specific switching sequence whereas the extents of the plain show the range of injected power into the grid and input voltage dc component for which the switching sequence is reachable. It is shown that the switching sequences M = 13 and 14 are not reachable for any range of a_0 and P_G.

5. Synthesizing an Optimal Sequence-Based Controller for a HFL Inverter

"Having determined the set of reachable switching sequences, the next step is to derive a discrete map for the states of the HFL inverter over a time horizon T_w such as $(t_0 + T_w)$, given initial values of the states $X_0 = X(t_0)$" [47]. Fig. 9 shows such a map which can be derived using a switching sequence consisting of *h* switching states. "For USROC, the time horizon T_w is equal to the switching period. The overall map can be obtained by patching together the individual maps corresponding to each switching state, as follows" [47]:

$$X(t_0 + T_w) = f(X(t_0), \propto_i, T_w, A, \{B_i\}_{i=1,\dots,h}) \quad (16)$$

where the function $f(.)$ depends on the dynamics of the HFL inverter over the time horizon T_w. The last step is to determine the optimal time horizon (T_w), the optimal switching sequence and the optimal duration of time VSI spends in each switching state of that optimal sequence ($\{\propto_i\}_{i=1,\dots,h}$).Choice of the cost function is user dependent and may also vary with applications and operating conditions. In this chapter, cost function will include the output voltage regulation or grid control in the single-objective optimization and voltage regulation or grid control and switching-loss reduction in the multi-objective optimization problem.

"The constraints for the optimal control problem include the map (16) and the maximum values that each state can attain (X_{max}). The SROC optimization problem can be summarized as to determine $\{\propto_i\}_{i=1,\dots,h}$ and T_w that minimizes the cost function $J(.)$" [47]

$$J(\{\propto_i\}_{i=1-h}, T_w) = (x^* - x(t_0 + T_w))^T P (x^* - x(t_0 + T_w))$$

given the constraints

$$x(t_0 + T_w) = f(.)$$

$$x(t_0 + T_w) \leq X_{max}$$

$$\sum_{i=1}^{h} \propto_i = 1 \text{ and } 0 < \propto_i < 1 \qquad (17)$$

In (17), P is a positive-definite diagonal matrix and x^* represents the reference values for all of the HFL inverter states. Note that (17) is a quadratic programming problem that can be solved numerically using conventional algorithms. When $T_w < T_s$ control transitions to the USROC in which $T_w = T_s$ and only $\{\alpha_i\}_{i=1,\ldots,h}$ need to be computed.

Fig. 11 shows a flowchart as used for implementation of OSBC in a digital processor. Note that J_0 is the initial value of the cost function and T_s is the switching period. In order to implement the OSBC algorithm, many parameters should be taken into consideration such as the processor speed, the total number of parameters to be sensed, the maximum allowable limit for the time horizon, the size of the search space, and the maximum number of iterations to achieve the optimal/suboptimal response.

For the hardware prototyping of the controller, a TMS320F28335 DSP from Texas Instrument (TI) with a 150-MHz clock can be used. The microinstruction cycle of this chip is about 6.77 ns. With a 40 kHz switching frequency (switching period of 25 μs), a total number of 3730 instructions are available to calculate the optimal control. In order to be conservative 3700 instructions can be assumed which is 24.7 μs. This includes the time duration required for sensing the output voltages, analog to digital conversion (ADC) process, digital filtering and signal conditioning / buffering, and implementation of the optimal control as stated in the flowchart of Fig. 11. With a total number of 15 fundamental switching sequences (Table III), the loop in Fig. 11 should be repeated 15 times. The other two inner loops consist of 100 iterations

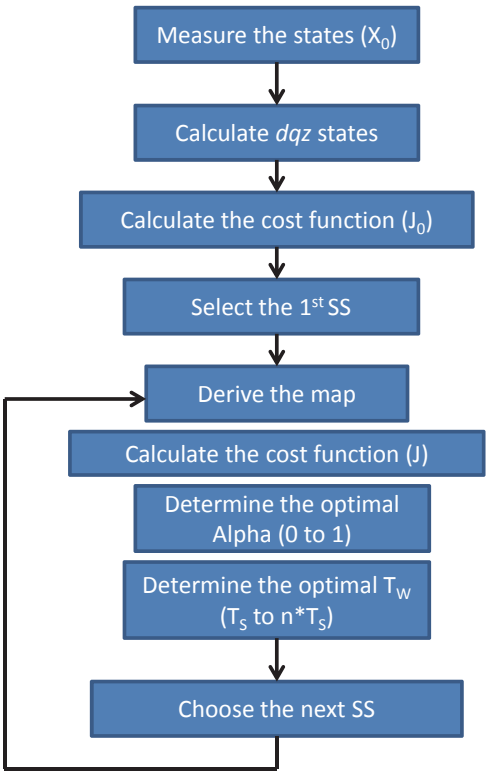


Fig. 11. Flowchart of implementation of OSBC in DSP.

for α and n iterations for T_w (time horizon). If we assume n = 10, for each switching sequence, a total number of 1,000 iterations is required in the worst case of finding the optimal values for α and T_w. If we consider all of the fundamental switching sequence to do the optimization, this leads to a total number of 15,000 iterations. If for each iteration a typical number of 10 instruction is assigned, the total time for execution of the optimal control in each switching cycle would be 150,000 × 6.77 ns = 1.0155 ms which is totally out of the range of a switching period. So, in order to reduce the execution time of the OSBC algorithm, some of the above parameters need to be reduced without too much of compromising on the optimal solution. For instance, instead of sequentially surfing the whole range of $\alpha = (0, 1)$ bisection method can be employed. This will reduce the search time by a factor of 7% if a resolution of 0.01 is desired. This is

justified by the fact that in order to search the whole interval of α linearly, 100 iterations are required while using the bisection-search method, the global optimal point can be found (with a resolution of 0.01) using n iterations so that $(\frac{1}{2^n} < 0.01)$ for which n = 7. Consequently, the total execution time for OSBC would be equal to 1.0155 ms × 0.07 = 71.085 µs.

However, the main advantage of OSBC over MPC can be explained here having provided the above discussion. In essence, the main difference between OSBC and MPC is that, in MPC, all of the feasible switching sequences are involved in optimization process. In contrast to MPC, OSBC algorithm initially performs a reachability analysis to reduce the search space to only those switching sequences which lead to a reachable operation. For instance, if for the HFL inverter of Fig. 7, a_0 (the average of V_{REC}) varies between 200 V and 500 V, the search space is limited to a set of reachable switching sequences for this range as $M \in \{5,7,11,12,15\}$. Therefore, the execution time of OSBC algorithm would be reduced to 71.085 µs / 3 = 23.7 µs which is less than a switching cycle of 25 µs. This typically occurs for cases in which the set of reachable switching sequences is smaller than the fundamental search space (including all of the fundamental switching sequences).

C. Results and Analysis

In this section initially a single-objective optimization problem is considered for voltage regulation and grid control using the HFL inverter operating in standalone and grid-connected modes, respectively. Results are compared with those obtained using conventional linear controller. Subsequently, a dual-objective optimization problem is presented which

simultaneously addresses regulation of the output voltage or current injection of the HFL inverter and mitigation of the switching losses.

1. Single-Objective OSBC: Standalone Operation

A 6-kW three-phase resistive load is considered and the nominal switching frequency of the HFL inverter is assumed to be 40 kHz. Input Pulsating-Dc voltage source is assumed to have a value of a_0 = 480 V and a fundamental frequency of $\omega_0 = 2\pi \times 4 \times 10^4$. The cost function for the single-objective control of HFL inverter contains weighted terms for $v_d^e = v_d^* - v_d$, $v_q^e = v_q^* - v_q$, and $i_q^e = i_q^* - i_q$ which are d-axis and q-axis voltage error and q-axis current error, respectively. Therefore, the goal of OSBC is to regulate the output voltage of the HFL inverter. Fig. 12 shows that the d-axis voltage is controlled on the reference value of $v_d^* = 154V$ in almost 50 µs.

Fig. 13 shows the same results for v_d and i_d using a linear PI controller. It is shown that the settling time is about 1.6 ms even at a high d-axis proportional gain (K_{pd}) of 2800 which also results in an overshoot of 174 V (about 13%).

Fig. 14 shows a parametric plot of settling time vs. K_{pd} for the PI controller. It is obvious that a compromise has to be made between settling time and overshoot. Even at high gains, still the transient response of the linear controller is a lot slower as compared with the same dynamics obtained using OSBC. Furthermore, the fast transient response of the OSBC is not achieved for the price of an increase in the overshoot. Moreover, OSBC results in almost no overshoot.

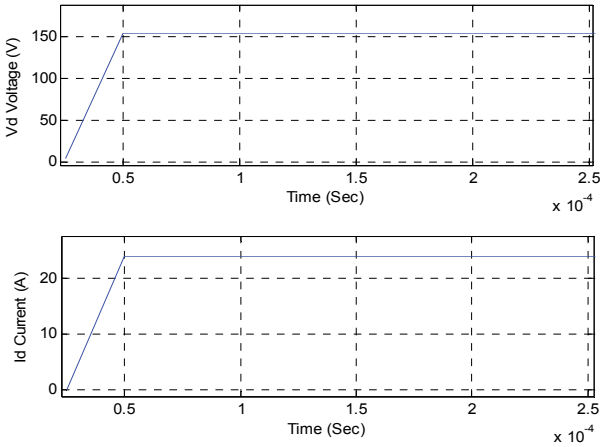


Fig. 12. Single-objective control in standalone operation: Voltage Regulation (VR). Transient response of v_d (top) and i_d (bottom) in a HFL inverter using OSBC. The settling time is found to be 50 µs and no overshoot is observed.

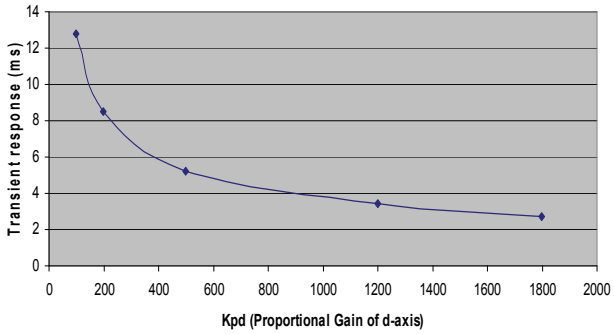


Fig. 14. Parametric plot showing the relationship between the d-axis proportional gain in a linear controller and the settling time of v_d.

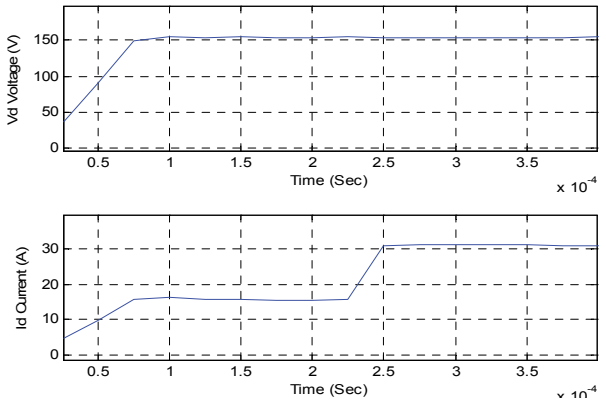


Fig. 16. Dynamic response of OSBC in a sudden load change at t = 225µs from 3.5 kW to 7 kW in terms of (a) v_d and (b) i_d. Almost no voltage dip is observed and it takes only 25 µs for the controller to adjust voltage and current to the set points.

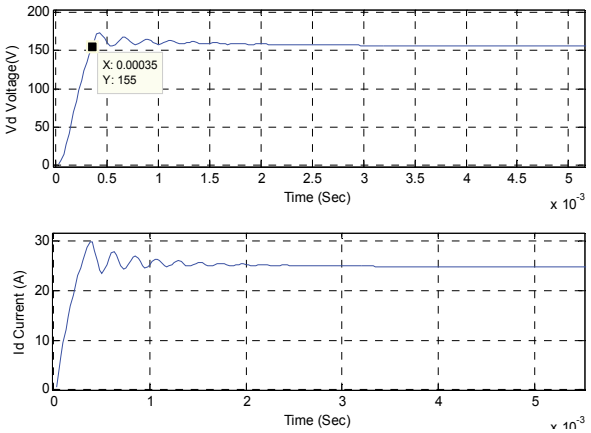


Fig. 13. Transient response of v_d (top) and i_d (bottom) in a HFL inverter using a PI controller for voltage regulation ($K_{Pd} = 2800$). The settling time is found to be 1.6 ms and an overshoot of 174 V (12.25%) is observed for v_d.

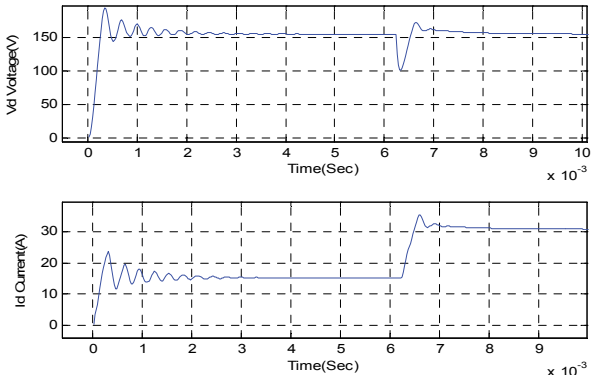


Fig. 15. Dynamic response of the linear controller in a sudden load change at t = 6.3 ms from 3.5 kW to 7 kW in terms of (a) v_d and (b) i_d. A 33% voltage dip is observed and it takes about 2 ms for the controller to adjust voltage and current to the set points.

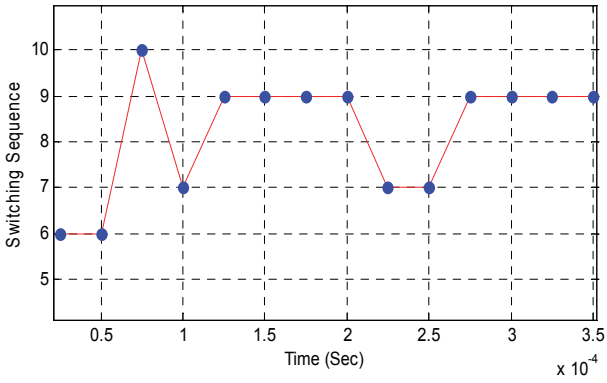


Fig. 17. Evolution of switching sequences corresponding to the startup and load change transients. It is observed that at startup, switching sequences 6,10,7, and 9 are chosen by OSBC and in 125µs, steady state is reached through SS = 9 . At t = 225µs again switching sequence 7 is chosen to remove the transient and adjust the load level to the new set point.

Fig. 15 shows the dynamic response of the linear controller to a sudden load change as demanded by the standalone load from the HFL inverter. The pre-transient load is supposed to be 3 kW and the post-transient demand is assumed to be 7 kW. A 33% voltage drop is observed and it takes about 2 ms for the controller to adjust voltage and current to the set points. However, in Fig. 16, it is shown that, the OSBC can almost seamlessly respond to this load demand in about 25 μs and almost no voltage dip is observed.

Fig. 17 shows the evolution of switching sequences corresponding to the startup and load transients (refer to Table III for interpretation of switching sequences). It is observed that, at startup, switching sequences (SS) 6,10,7, and 9 are chosen by OSBC and after an elapsed time of 125 μs, the steady state is reached through SS = 9. At $t = 225$ μs, again switching sequence 7 is chosen to remove the transient and adjust the load level to the new set point.

Superior dynamic response of OSBC as compared with a linear controller can be demonstrated using a sudden change in the dc component of V_{REC} (a_0) as well. Fig. 18 shows the Transient response of a linear controller (PI) to a sudden change in a_0 while Fig. 19 shows the same using OSBC. It can be observed that in contrary with the PI controller, OSBC leads to almost no voltage dip as the dc component of V_{REC} suddenly falls from 600 V to 350 V in this case study. Note that the post transient value of a_0 is in the range of reachability according to Fig. 10. Otherwise, none of the two controllers could stabilize the output voltage of the HFL inverter.

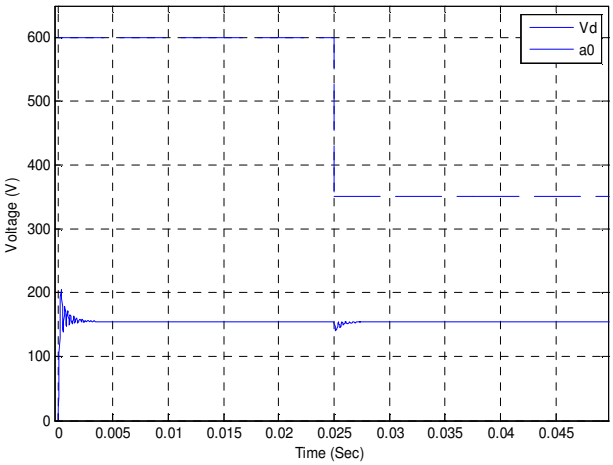


Fig. 18. Transient response of a linear controller (PI) to a sudden change in the dc component of V_{REC} (a_0) in standalone operation.

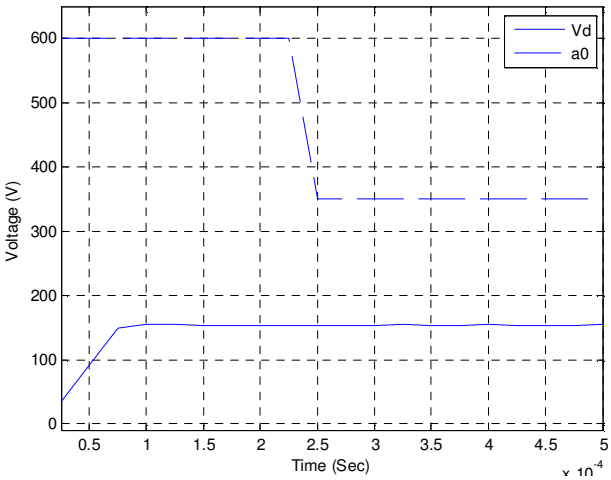


Fig. 19. Transient response of OSBC to a sudden change in the dc component of V_{REC} in standalone operation.

2. Single-Objective OSBC: Grid-Connected Operation

In this section, cost function includes the regulation of the PV voltage (V_{DC}) and the injected grid current according to a predetermined MPPT algorithm (Perturb & observe – P&O method [31]). In order to perform grid current regulation and MPPT simultaneously, a cost function is needed with the two terms for regulation of the HFL inverter states in synchronous reference frame (I_d and I_q) as well as the output voltage of the PV array determined by MPPT (V_{DC}) as follows:

$$J = w_1.(I_d^* - I_d)^2 + w_2.(I_q^* - I_q)^2 + w_3.(V_{DC}^* - V_{DC})^2 \quad (18)$$

where I_d^*, and I_q^* are reference values for the active and reactive currents to be injected to the utility grid and V_{DC}^* is the PV array output voltage determined by the P&O MPPT algorithm, I_d, I_q, and V_{DC} are the measured values for the same and w_1, w_2, and w_3 are weighting factors. In order to extract the maximum power from the PV panels (MPPT), P&O algorithm is

incorporated into the optimization process. Fig. 20 shows the flowchart of P&O. Fig. 21 shows I-V and P-V characteristics of the PV array under study. Switching frequency in the unsaturated region is limited to 40 kHz. Output filters are 2 mH per phase and the turns ratio of the HF transformers are set at 2.

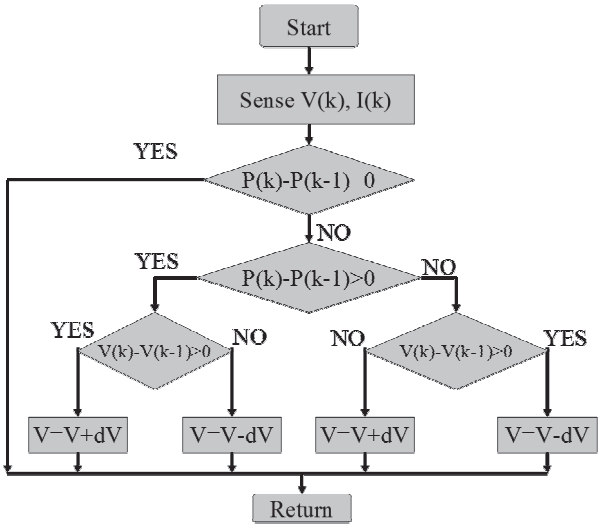


Fig. 20. Sequence of P&O MPPT method.

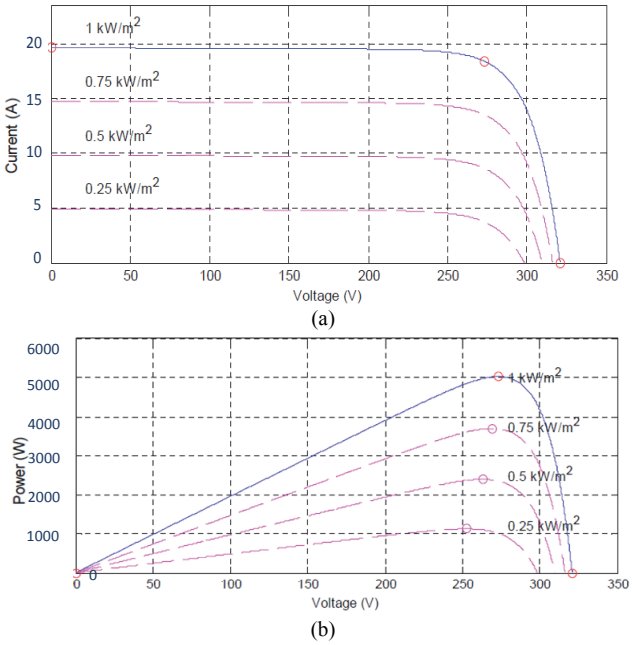


Fig. 21. (a). I-V and (b).P-V characteristics of the PV array.

For scenario 1, the irradiance level is assumed to be 1 kW/m^2 and MPPT suggests i_{pv} = 18 A (Fig. 21a). Consequently, a value of 277 V for V_{DC}^{*} is suggested in order to draw the maximum power form PV array. This turns into a value of 4200 W active power to be injected into the grid. Fig. 22 shows the three-phase injected current into the grid in abc as well as $\alpha\beta\gamma$ reference frames. Fig. 23 represents the regulation of input dc voltage V_{DC} as a result of inclusion of the third term into the cost function in (18). Fig. 24 demonstrates evolution of the optimal switching sequences from transient to the steady state.

In scenario 2, firstly the irradiance level is 0.5 kW/m^2 and MPPT suggests a value of 260 V for V_{DC}^*. The optimal value reactive power drawn from the PV array is 2350 W and I_d^* is 10 A. At t = 19 ms, the irradiance level changes to 0.25 kW/m^2 due to a cloud. Consequently, the reference value for array output voltage (V_{DC}^*) is changed to 250 V leading to optimal active power of 1250W to be drawn from PV array. The new value for I_d^* is set at 5 A. Fig. 25 shows the regulation of three phase injected current into the grid in abc as well as αβγ reference frames in response to a sudden change in irradiance level leading to a change in injected active power to maintain the MPPT.

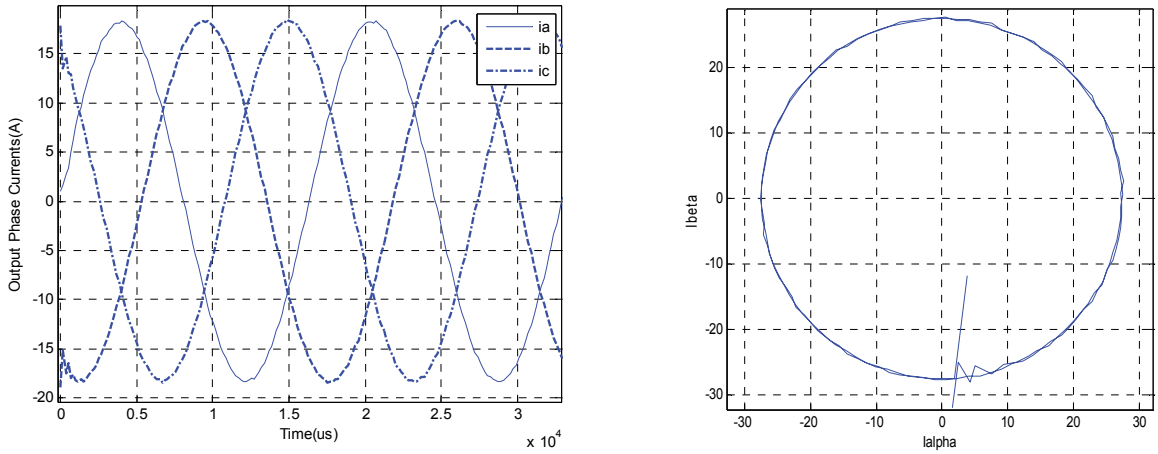


Fig. 22. Control of output injected currents into the grid (a) in abc and (b) in αβγ reference frames using OSBC.

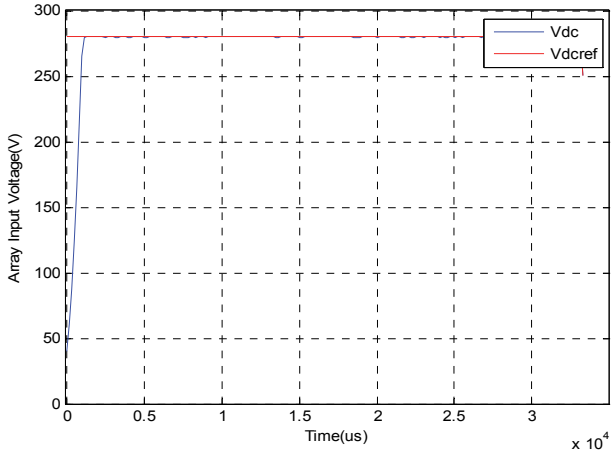


Fig. 23. Regulation of V_{DC} (PV-array voltage) according to MPPT algorithm.

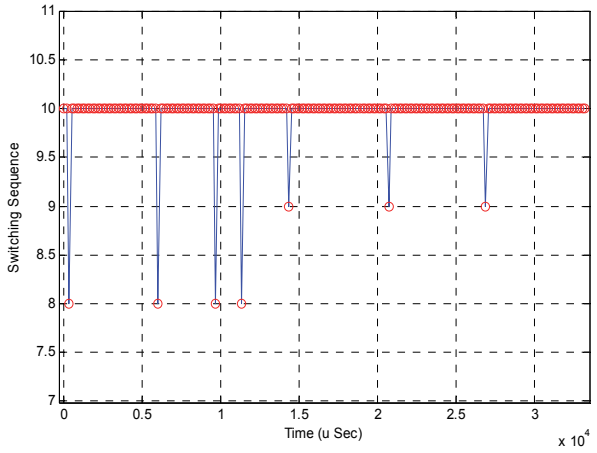


Fig. 24. Evolution of the optimal switching sequences from transient to the steady state.

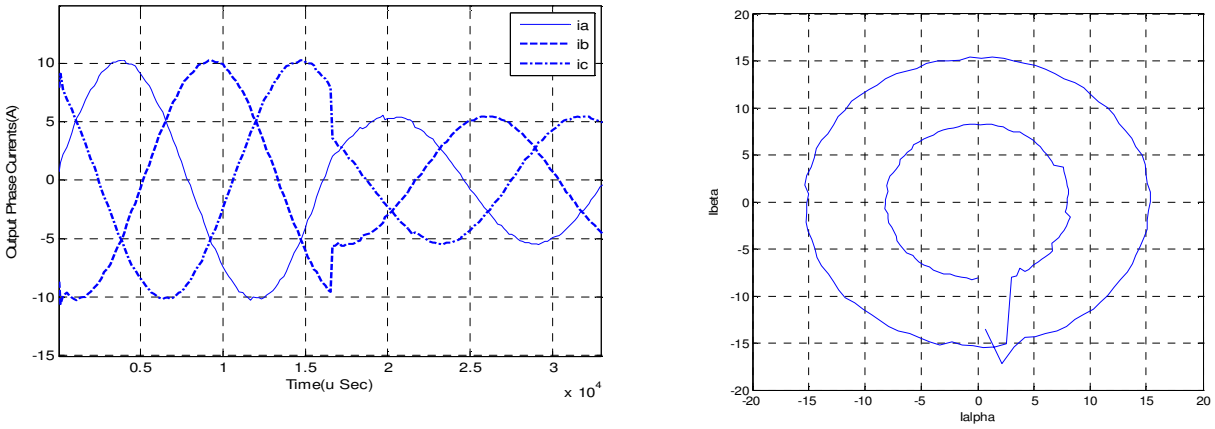


Fig. 25. Control of output injected currents into the grid (a) in abc and (b) in αβγ reference frames using OSBC. Dynamic response to a sudden irradiance level change at t = 16 ms.

3. Dual-Objective OSBC: Standalone Operation

In this section, a dual-objective cost function is considered in order to optimize both of the voltage regulation (VR) and switching-loss reduction (SLR) goals simultaneously. The cost function for such a multi-objective OSBC is of the form:

$$J = J_{VR} + J_{SLR} \quad \text{where } J_{VR} = w_1(v_d^* - v_d)^2 + w_2(v_q^* - v_q)^2 \quad \text{and } J_{SLR} = w_3 \times \hat{L}oss_{SW} \qquad (18)$$

where w_1, w_2 and w_3 are the weighting factors, the first and the second terms represent VR objective while the third term represents SLR. $\hat{L}oss_{SW}$ is an estimation of switching losses in the Ac/Ac Converter. Generally, in a switching power converter (SPC), the switching loss for each switching device (such as a MOSFET) depends on the overlap of the waveforms for the voltage across the drain and the source terminals v_{DS} and the current through the device i_{DS} during the turn-on and turn-off transitions (Fig. 26) as well as the switching frequency of SPC.

In the HFL inverter of Fig. 5, the total switching loss for the Ac/Ac converter in one switching cycle can be estimated considering the switching frequency and the area under the $v_{DS} \times i_{DS}$ waveform during the switching transients. The latter depends on the specifications of the

semiconductor switch chosen for the SPC as well as the voltage and current ratings for which the SPC is designed. The former, however, inversely depends on the time horizon T_w. In spite of fact that switching frequency somehow is predetermined in the design stage of the HFL inverter filters, isolating HF transformers and in the device selection phase, it can be adjusted in a joint-optimization of $\hat{L}oss_{SW}$ along with other cost function terms such as voltage regulation in standalone operation as well as current control in grid-connected operation. Regarding what was explained above and Fig. 26, we have that:

$$\hat{L}oss_{SW} = 0.5 \times I_D \times V_D \times (t_{SW(ON)} + t_{SW(OFF)}) \times (\frac{1}{T_W}) \tag{19}$$

where T_w is the prediction time horizon for OSBC. Fig. 27 shows the d-axis components of output voltage and load current in a dual objective control (VR & SLR) of a HFL inverter operating in standalone mode.

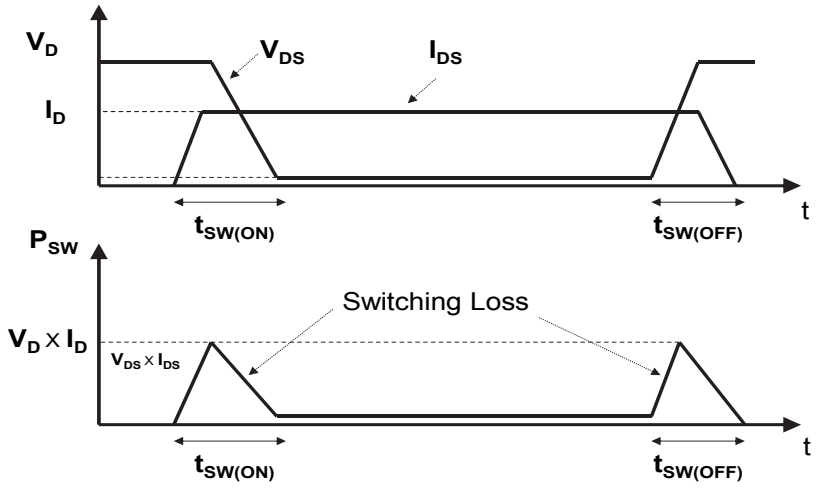


Fig. 26. Illustration of switching loss for a switching device such as a MOSFET.

Fig. 28 demonstrates the different terms of the cost function associated with the voltage regulation (VR) at the top (J_{VR}), the switching-loss reduction (SLR) goal in the middle (J_{SLR}),

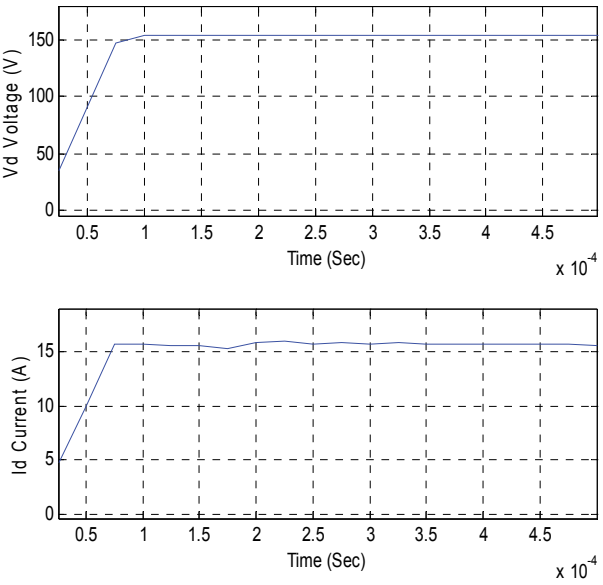


Fig. 27. v_d and I_d in Dual-objective (VR and SLR) OSBC for standalone operation.

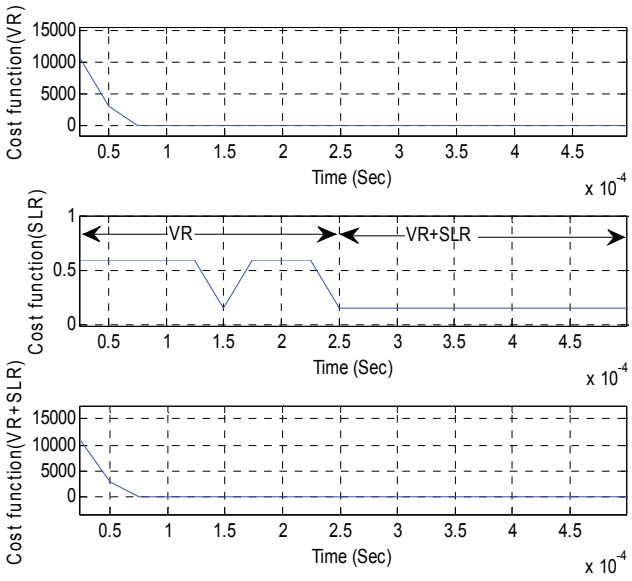


Fig. 28. Cost functions in Dual-objective OSBC for standalone operation. Top: cost function of VR (J_{VR}), middle: cost function of SLR (J_{SLR}), and bottom: total cost function (J_{VR}+J_{SLR}).

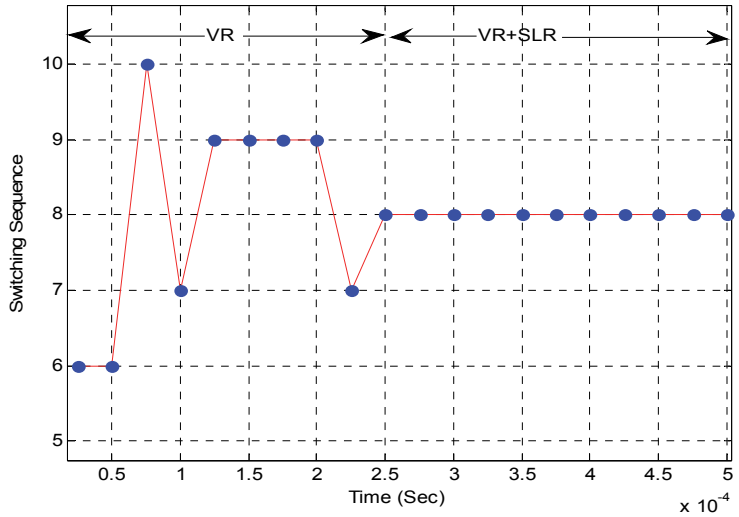


Fig. 29. Evolution of switching sequences in dual-objective control (VR & SLR) of a HFL inverter operating in standalone mode.

and the total cost function at the bottom (J). Note that at t = 250μs, the weight of the cost function term for SLR (w_3) is changed from zero to 0.1 leading to an increase in the switching time period which reduces the SLR cost function. Also note that the inclusion of the SLR term does not have any adverse effect on VR (Fig. 27).

Fig. 29 shows the evolution of switching sequences during the VR period and the period in which both the VR and SLR goals are included in the cost function to be minimized.

If for a typical MOSFET in the design range of our case study (IXFH 26N60Q) we consider $t_{SW(ON)}$ = 60ns and $t_{SW(OFF)}$ = 96 ns, then for the case illustration shown in Fig. 27 and 28, the amount of switching-loss reduction per each MOSFET in Ac/Ac Converter due to dual-objective OSBC would be about 9.75 W (table IV).

TABLE IV. SWITCHING LOSS REDUCTION DUE TO DUAL-OBJECTIVE OSBC.

Objective function	Weighting factors	Switching frequency	Switching loss per MOSFET
VR	$w_1 = 0.6$, $w_2 = 0.4$, $w_3 = 0$	40 kHz	$\hat{L}oss_{SW_1} = 0.5 \times 600V \times 16A \times 156ns \times 40kHz = 30W$
VR + SLR	$w_1 = 0.5$, $w_2 = 0.4$, $w_3 = 0.1$	27 kHz	$\hat{L}oss_{SW_1} = 0.5 \times 600V \times 16A \times 156ns \times 27kHz = 20.25W$

4. Dual-Objective OSBC: Grid-Connected Operation

In the grid-connected mode of operation, in a similar way as performed in the standalone mode, HFL inverter can be controlled using multi-objective OSBC. For instance, the injected power to the grid and switching loss reduction could be optimized simultaneously by minimizing the following cost function:

$$J = J_{GC} + J_{SLR}$$

where

$$J_{GC} = w_1.(I_d^* - I_d)^2 + w_2.(I_q^* - I_q)^2 + w_3.(V_{DC}^* - V_{DC})^2 \text{ and } J_{SLR} = w_4 \times \hat{L}oss_{SW} \qquad (20)$$

Fig. 30 shows the value of individual cost functions (J_{GC} and J_{SLR}) as well as the total cost function versus time. Note that at t = 25 ms, the weight of the cost function term for SLR (w_4) is

changed from zero to 0.1 leading to an increase in the switching time period (reduction in the switching frequency from 40 kHz to 27 kHz) which reduces the SLR cost function (reduction of switching losses from 30 W to about 20 W per MOSFET). Also note that the inclusion of the SLR term does not have a considerable adverse effect on GC but a little bit of more ripples in injected currents (Fig. 31).

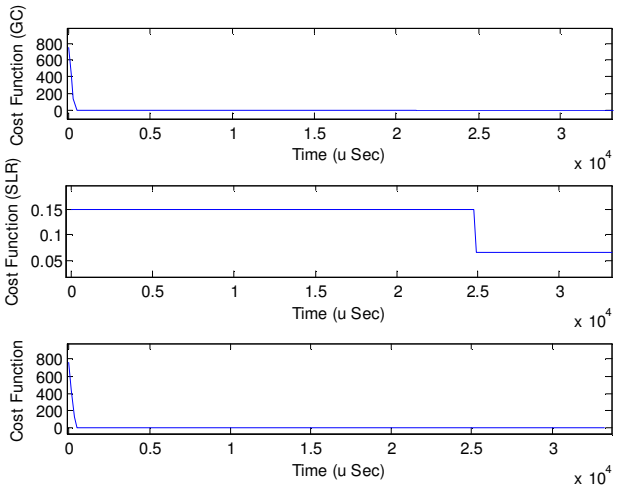


Fig. 30. Cost functions in Dual-objective OSBC for grid-connected operation. Top: cost function of GC (J_{GC}), middle: cost function of SLR (J_{SLR}), and bottom: total cost function (J_{GC}+J_{SLR}).

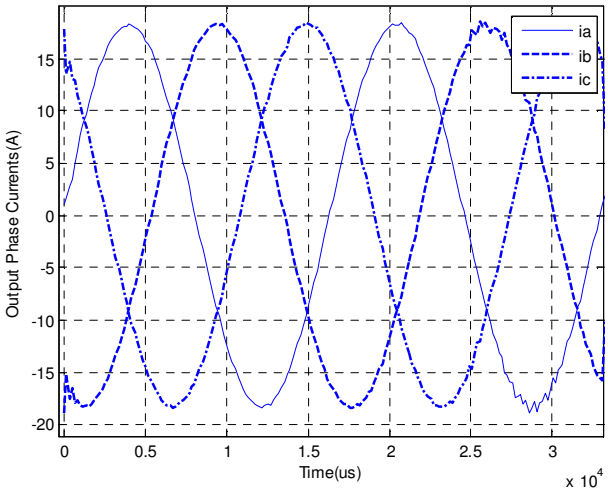


Fig. 31. Control of output injected currents into the grid. Note that inclusion of the SLR term (at t = 25 ms) does not have a considerable adverse effect on GC but a little bit of more ripples in injected currents

D. Conclusions

A comprehensive study on the proposed OSBC algorithm for a HFL inverter under standalone and grid-connected mode of operation was given which was based on a PWL model of the power stage. In essence, the discontinuous modeling which is a part of OSBC retains both the fast scale as well as the slow scale dynamics which in turn makes it possible to control multi-scale parameters at the same time through a predefined optimization algorithm. This, as was demonstrated in this chapter, leads to superior dynamic response of the OSBC controller as compared to that obtained the traditional control approaches that are based on average model of

the power stage. This is because average modeling ignores the fast-scale dynamics of the power converter.

Another inherent feature of the OSBC is its capability to support multi-objective control. Even though this feature is found in MPC algorithm as well, the key advantage of OSBC over MPC (and even sliding-mode control) is to ensure performance under stability bound by only using reachable switching sequences of the power converter. Further, this feature enables the OSBC controller to change the switching sequences with varying operating mode of the converter on the fly under stability bound. Moreover, the reduction in the search space leads to a reduced execution time for synthesizing the optimal control.

E. Appendix A

Matrices for the general PWL model of the HFL inverter in abc and dq reference frames (Standalone mode of operation):

$$A_{abc} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix}, \; B_{abc} = \frac{V_{REC}}{3L} \times B' \times \bar{S}_{abc}, \quad B' = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

where $\bar{S}_{abc} = [S_a, S_b, S_c]^T$

$$\begin{cases} A_{dq} = \begin{bmatrix} T & 0_{3\times3} \\ 0_{3\times3} & T \end{bmatrix} \times A_{abc} = \begin{bmatrix} 0 & \omega & -1/L & 0 \\ -\omega & 0 & 0 & -1/L \\ 1/C & 0 & -1/RC & \omega \\ 0 & 1/C & -\omega & -1/RC \end{bmatrix} \\ B_{dq} = \begin{bmatrix} T & 0_{3\times3} \\ 0_{3\times3} & T \end{bmatrix} \times B_{abc} = \begin{bmatrix} S_d \\ S_q \\ 0 \\ 0 \end{bmatrix} \times \frac{V_{REC}}{L} \end{cases}$$

where *T* is the Park's transformation matrix.

An augmented PWL model for the HFL inverter using the simplified model in Fig. 8 (standalone mode of operation):

$$\frac{d}{dt}\begin{bmatrix} X^{dqz} \\ y_{11} \\ y_{12} \\ \vdots \\ y_{n1} \\ y_{n2} \end{bmatrix} = \begin{bmatrix} A_{4\times4}^{dqz} & B_{4\times1}^{dqz} & 0_{4\times1} & \cdots & B_{4\times1}^{dqz} & 0_{4\times1} \\ 0_{1\times4} & 0 & 1 & \cdots & 0 & 0 \\ 0_{1\times4} & -\omega_1^2 & 0 & & 0 & 0 \\ & \vdots & & \ddots & \vdots & \\ 0_{1\times4} & 0 & 0 & & 0 & 1 \\ 0_{1\times4} & 0 & 0 & \cdots & -\omega_n^2 & 0 \end{bmatrix} \times \begin{bmatrix} X^{dqz} \\ y_{11} \\ y_{12} \\ \vdots \\ y_{n1} \\ y_{n2} \end{bmatrix} + \begin{bmatrix} B_{4\times1}^{dqz} \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \times \frac{a_0}{2}$$

Matrices for the general PWL model of the HFL inverter in abc and dq reference frames (grid-connected mode of operation):

$$A_{abc} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}, B_{abc} = \frac{1}{3L} \times B' \times \bar{S}_{abc} - \overline{V_g}_{abc}$$

where $\bar{S}_{abc} = [S_a, S_b, S_c]^T$ and $\overline{V_g}_{abc} = [\, v_{g_a}, v_{g_b}, v_{g_c}]^T$

$$\begin{cases} A_{dq} = \begin{bmatrix} -R/L & -\omega \\ \omega & R/L \end{bmatrix} \\ B_{dq} = \begin{bmatrix} S_d \\ S_q \end{bmatrix} \times \frac{V_{REC}}{L} \times \frac{3}{2} \end{cases}$$

An augmented PWL model for the HFL inverter using the simplified model in Fig. 8 (grid-connected mode of operation):

$$\frac{d}{dt}\begin{bmatrix} X^{dqz} \\ y_{11} \\ y_{12} \\ \vdots \\ y_{n1} \\ y_{n2} \end{bmatrix} = \begin{bmatrix} A_{2\times2}^{dqz} & B_{2\times1}^{dqz} & 0_{2\times1} & \cdots & B_{2\times1}^{dqz} & 0_{2\times1} \\ 0_{1\times2} & 0 & 1 & & 0 & 0 \\ 0_{1\times2} & -\omega_1^2 & 0 & & 0 & 0 \\ & \vdots & & \ddots & \vdots & \\ & 0_{1\times2} & 0 & 0 & 0 & 1 \\ & 0_{1\times2} & 0 & 0 & -\omega_n^2 & 0 \end{bmatrix} \times \begin{bmatrix} X^{dqz} \\ y_{11} \\ y_{12} \\ \vdots \\ y_{n1} \\ y_{n2} \end{bmatrix} + \begin{bmatrix} B_{2\times1}^{dqz} \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \times \frac{a_0}{2}$$

A_{abc}

$$= \begin{bmatrix} -R/L & 0 & 0 & (N/L)(S_1 - S_2).(S_a - (S_a + S_b + S_c)/3) \\ 0 & -R/L & 0 & (N/L)(S_1 - S_2).(S_b - (S_a + S_b + S_c)/3) \\ 0 & 0 & -R/L & (N/L)(S_1 - S_2).(S_c - (S_a + S_b + S_c)/3) \\ -(S_1 - S_2)S_a/C & -(S_1 - S_2)S_b/C & -(S_1 - S_2)S_c/C & 0 \end{bmatrix}$$

$$B_{abc} = \begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 \\ 0 & 0 & 1/L & 0 \\ 0 & 0 & 0 & 1/C \end{bmatrix}$$

$$A_{dq} = \begin{bmatrix} -R/L & \omega & N.(S_1 - S_2).S_d \\ -\omega & -R/L & N.(S_1 - S_2).S_q \\ (-3/2).(S_1 - S_2).S_d/C & (-3/2).(S_1 - S_2).S_q/C & 0 \end{bmatrix}$$

$$B_{dq} = \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/C \end{bmatrix}$$

III. A FAULT-TOLERANT SWITCHING SCHEME FOR A HIGH-FREQUENCY-LINK INVERTER

Abstract— **In this chapter, a fault-tolerant scheme is proposed for a multi-stage isolated three phase HFL inverter. It comprises a front-end Dc/Ac Converter connected to an Ac/Pulsating-Dc Converter followed by a Pulsating-Dc/Ac Converter. The fault-tolerant scheme ensures a consistent operation under different type of fault conditions in any of the three stages mentioned in above. A fault diagnosis scheme is outlined which identifies which H-Bridge in Dc/Ac Converter or which leg in Ac/Pulsating-Dc Converter or in Pulsating-Dc/Ac Converter has failed. Also an analysis is provided in this chapter to show the effect of the fault angle on the stability margin. Detailed results on the switching scheme as well as experimental validation using a fabricated prototype are presented.**

A. Introduction

Although a superior dynamic response and multi-objective control algorithm was developed for the HFL inverter and effectiveness of the OSBC was verified through various scenarios in chapter two, but all of these achievements are attainable only if a reliable operating condition is provided for the power conversion system. There is no need to note that at high power or for mission-critical or cost-sensitive applications, where the operational continuity of the inverter is vitally important, reliability of the HFL inverter attains significant importance. As such, the need for fault-tolerant operation, which has become almost a mandatory requirement in power converters for military and aeronautical applications, is gaining traction for commercial applications as well. While there have been some recent publications in the area of HFL inverters from the standpoints of power-stage and control performances, such analyses are often based on the nominal operation of the HFL inverters.

In recent years, many papers have focused on the development of fault-tolerant systems [48], [49], [50], [51], [52], [53]. Many of these fault-tolerant power conditioning systems are based on a multi-leg converter design. References [54] and [55], discuss about the reconfiguration of the power converters using isolating and connecting devices. In [56], a number of possible topologies based on redundancy of designs are considered which are all based on the fixed-dc-link configuration. Among the references [48]-[56] and other surveyed literature, limited work has been reported on fault-tolerant operation and continuity of the service of HFL converters. In addition, in majority of the previous research work, the key mechanism for power converter fault tolerance appears to be to incorporate redundant switches.

In contrast, this chapter provides a mechanism for fault-tolerance of a multi-stage pulsating-dc-link HFL inverter (i.e., an inverter operating without a dc-link capacitor) without using redundant switches for all of the stages. Instead, depending on the stage in which fault happens, it either takes advantage of the encoded phase information in the resultant pulsating-dc-link waveform of the HFL inverter or incorporates the switches in other stages (leading to less number of redundant switches) to restore the output voltages. The isolated HFL inverter, as shown in Fig. 32, comprises a front-end Dc/Ac Converter, followed by an Ac/Pulsating Dc Converter and a Pulsating-Dc/Ac Converter. S_xx switches are low frequency switching devices / relays for reconfiguration of the topology in case of a fault. The fault-tolerant switching scheme (FTSS), as outlined in this chapter, includes a number of steps. Firstly, the faulty stage and switching devices are identified using a fault diagnosis algorithm. Next, depending on the faulty stage, relevant restoration algorithm is employed to sustain the output voltages of the HFL inverter as follows:

1- If the fault happens in the Dc/Ac Converter, faulty circuit is isolated and also based on the type of the lost phase, the pulse-width-modulation (PWM) reference for the remaining phases in the Dc/Ac Converter is changed so as to restore the output line voltages.
2- If the fault happens in the Ac/Pulsating-Dc Converter, the faulty leg and the corresponding full bridge in the Dc/Ac Converter are isolated and the PWM reference for the remaining phases in the Dc/Ac Converter and the Ac/Pulsating-Dc Converter is changed so as to restore the output line voltages.
3- If the fault happens in the Pulsating-Dc / Ac Converter, the faulty leg is isolated from load, Dc/Ac Converter and Ac/Pulsating-Dc Converters will operate with two full bridges and two legs respectively provided that the PWM references for them are changed, and the third leg of Ac/Pulsating-Dc substitutes the faulty leg of Pulsating-Dc/Ac Converter.

Section II describes the HFL inverter topology and its fault-free operating principle. In Section III, a detailed analysis of different fault scenarios and their effects on the inverter output is given. Based on the results of this analysis, relevant fault-diagnosis algorithms are then discussed. The next step, i.e. the restoration from a fault and detailed explanations about the proposed algorithms are given in Section IV. Effectiveness of the proposed fault-tolerant scheme is experimentally verified in Section V using a 1-kW laboratory prototype. Finally, in Section VI some relevant conclusions are drawn.

B. Fault-Free Operation of the HFL Inverter

Fig. 32 demonstrates the topology of the isolated HFL inverter. The front-end Dc/Ac Converter comprises three full-bridge converters generating bipolar and tri-state HF voltage

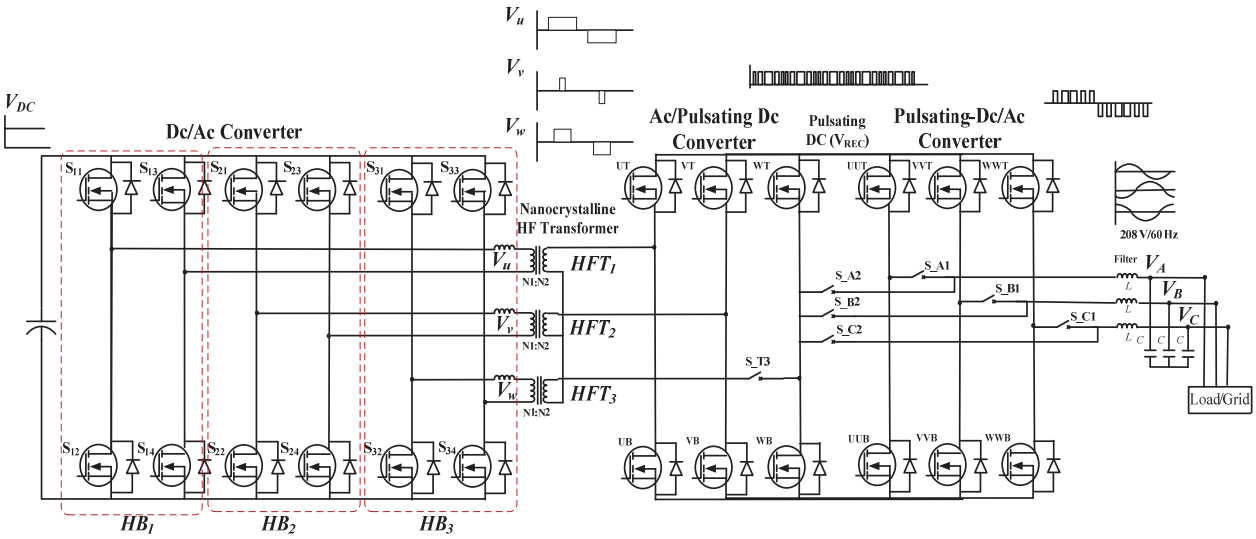


Fig. 32. Isolated three-phase HFL inverter with fault-tolerant front-end Dc/Ac Converter.

pulses, which are fed to the HF transformers. The secondary outputs of these HF transformers are then fed to the Ac/Pulsating-Dc Converter, which rectifies the bipolar voltage pulses and creates the resultant Pulsating-Dc voltage (V_{REC}). Using this Pulsating-Dc voltage and a specific modulation scheme [6], the Pulsating-Dc/Ac Converter generates the desired sinusoidal inverter outputs.

For the fault-free operation, first, the overall 360-degree period of a line cycle is divided into six sectors marked in Fig. 33 as P1 through P6. In a given switching cycle, three sets of instantaneous bipolar and tri-state HF pulses representing three phases are generated using the front-end Dc/Ac Converter (Fig. 34). These pulse trains are fed to the Ac/Pulsating-Dc Converter which generates a unipolar HF pulse train (V_{REC}). Note that the gate pulses for each of the legs in the Ac/Pulsating-Dc Converter are synchronized with those of the full bridge converters in Dc/Ac Converter generating the same phase. This pulse train (V_{REC}) contains information of the maximum line voltage at any instant which is encoded in the area under the pulse voltages.

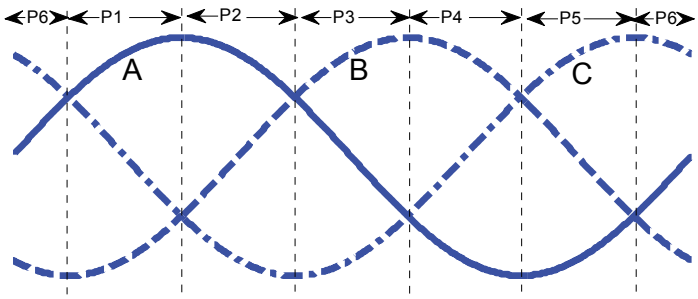


Fig. 33. Sectors P1 to P6.

As such, there is no need for HF switching of those two legs in the Pulsating-Dc/Ac Converter generating the maximum line voltage in each sector P1-P6.

We explain the generation of V_{REC} using an illustration. Suppose, the voltage reference vector is in sector P1, then, as per the fault-free switching algorithm, three instantaneous bipolar pulse sequences representing V_A, V_B, and V_C are generated. The Ac/Pulsating-Dc Converter output (V_{REC}) is defined by the following equation:

$$V_{REC} = \max \frac{N_2}{N_1} \{|V_u - V_v|, |V_v - V_w|, |V_v - V_w|\} \tag{21}$$

Since in the sector P1, V_A and V_B are the highest and the lowest phases respectively, based on (21), V_{REC} contains the information of V_A-V_B = V_{AB}, which is encoded in the area under the voltage pulses in every switching period. This is illustrated in Fig. 34 with a switching period of T_S. Therefore, UUT is permanently on and VVT is permanently off to pass the rectified pulses representing V_{AB}. The other line voltages are generated by HF switching of the third leg. So, the PWM reference of line cb is used for switching WWT. Therefore, and as shown in Fig. 34, V_{REC} is chopped so as to generate V_{BC} and V_{CA}. Table V shows the PWM references for the Pulsating-Dc/Ac-Converter switches for sectors P1 to P6. In Table V ab, bc, and ca represent PWM references for the line voltages V_{AB}, V_{BC}, and V_{CA} respectively. This switching scheme leads to

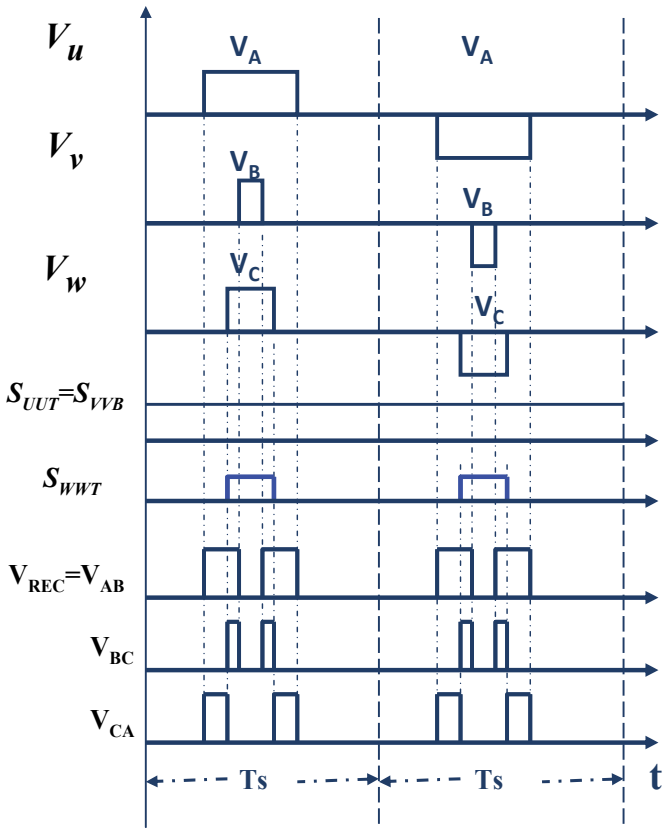


Fig. 34. Illustrating a fault-free operation of the HFL inverter in sector P1.

67% improvement of the efficiency compared with the conventional VSI. The detail of this switching scheme, which is referred to as hybrid modulation, is provided in [58], [11],[57],[59], [60],[61].

TABLE V. PWM REFERENCES FOR PULSATING-DC/AC CONVERTER. SYMBOLS AB, BC, AND CA ARE PWM REFERENCES FOR LINE VOLTAGES.

Sector / Signal	P1	P2	P3	P4	P5	P6
UUT	1	1	ac	0	0	ab
VVT	0	bc	1	1	ba	0
WWT	cb	0	0	ca	1	1

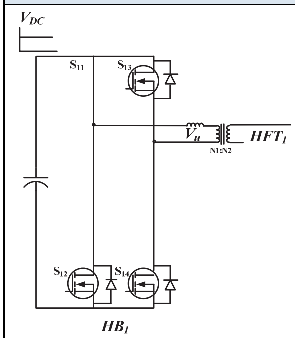
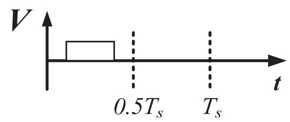
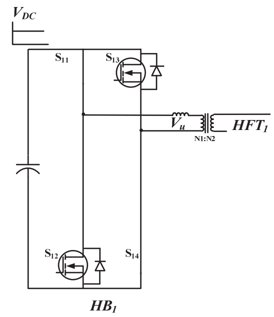
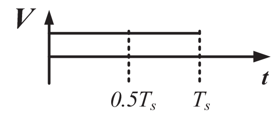
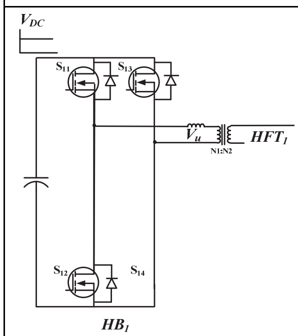
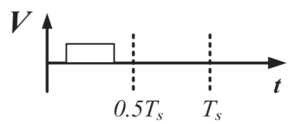
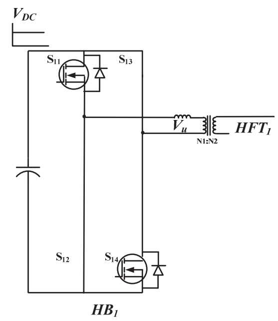
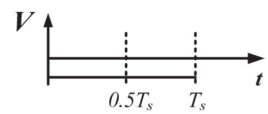
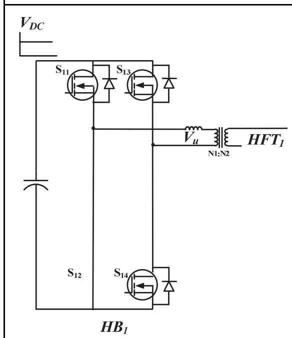
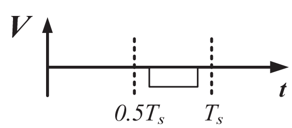
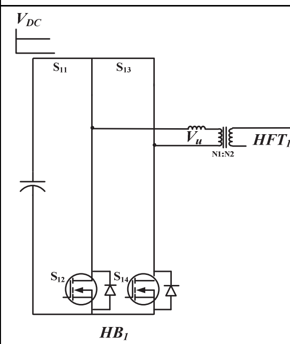
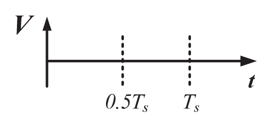
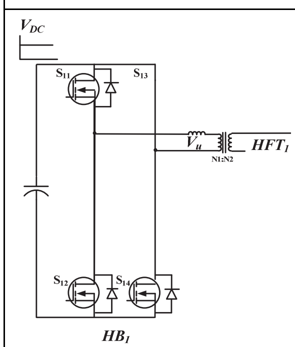
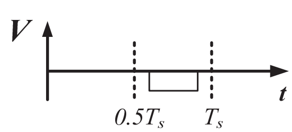
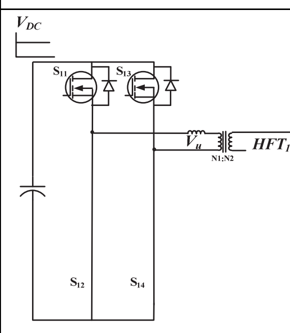
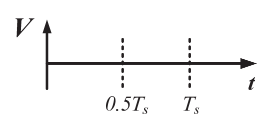
C. Possible Fault Types and Fault Diagnosis Algorithm

In the previous section we considered normal (fault-free) mode of operation of the HFL inverter of Fig. 32. In this section, possible fault scenarios are outlined and it will be shown that since each type of fault generates a specific distortion pattern in the output line voltages, a comprehensive fault diagnosis algorithm can be developed.

1. Failure in the Dc/Ac Converter

The term "phase loss" in this chapter is typically used for any kind of failure in full bridge switching devices that disrupts the generation of bipolar HF pulses trains or distorts the output line voltages. Table VI shows different types of device failure (leading to a short circuit between drain and source of the MOSFETs which is a very common type of failure) and the resultant distorted full bridge output. Failures listed in the left column lead to a flux imbalance in the HF transformers though encoding the phase information. Failures in the right column however, interrupt the process of encoding the phase data. No matter what type of fault happens, protection circuits such as V_{DS_Sat} monitoring (which are industrial standard and not discussed in this chapter) isolate faulty circuit from the whole converter topology thanks to the modular design of this HFL inverter. Yet, the output voltages of the Inverter have to be restored using the remained full bridges.

TABLE.VI. POSSIBLE TYPES OF FAULT IN FULL BRIDGES OF DC / AC CONVERTER (T_S: SWITCHING PERIOD).

Faulty circuit	Full Bridge Output	Faulty circuit	Full Bridge Output
			
			
			
			

1) Loss of One Phase in the Dc/Ac Converter

Consider the scenario in which one full-bridge converter of the Dc/Ac Converter fails. For instance, if phase w fails and the other two full-bridge converters continue to generate V_u and V_v, the output line voltages of the HFL inverter will be distorted. The obvious reason is that, due to the failure of HFT_3 output and based on (21), the information of phase c is no longer available in V_{REC}. Fig. 35 shows such a distortion in line voltages V_{AB} and V_{CA}. Note that, the distortion in V_{CA} is worse than V_{AB}. This is because for generating V_{AB}, the Pulsating-Dc/Ac Converter does not require the encoded information of phase c in V_{REC} no matter such information exist (fault-free operation) or not (faulty operation). However this is not the case for V_{BC} and V_{CA}. Note that the only sectors in which V_{CA} is not distorted despite lack of information of phase c are P1 and P4 as only in these two sectors c is the intermediate phase. This implies that in P1 and P4 (following (1)) information of phase c is not encoded in V_{REC} by Ac/Pulsating-Dc Converter even under fault-free operating conditions (generally, information of the intermediate phase in each sector is not encode in V_{REC}). Therefore, the effect of failure of V_w does not appear in these sectors and consequently no distortion in V_{CA} is observed in P1 and P4 (Fig. 35). Under this fault condition, the only way to restore the output line-voltages of the HFL inverter is to change the PWM references of the remaining full-bridge converters so as to encode the information of the lost phase in V_{REC} [62]. In case of a failure of two full-bridge converters in the Dc/Ac Converter, a proper change of the PWM reference for the remaining full-bridge converter can also restore the output voltages though with a lower voltage level.

Based on the case illustration stated in above, the lost phase in the Dc/Ac Converter can be diagnosed based on the sector in which fault happens and the type of distorted output line voltages (V_{AB}, V_{BC}, and V_{CA}). For instance, if the magnitude of the two line voltages V_{AB} and

V_{CA} suddenly fall below the reference values (dictated by load in standalone operation mode and the utility grid in grid connected mode) in any of the two sectors P1 or P2, it is an indication for failure of phase u.

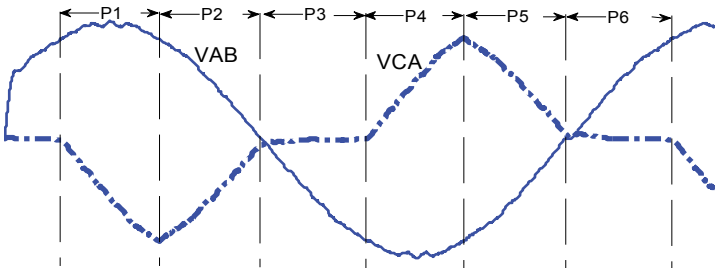


Fig. 35. Effect of a single phase outage (phase w) on the output line-voltages V_{AB} and V_{CA} of the HFL inverter in Fig. 32. It is shown that failure of phase w causes a severer distortion in V_{CA} rather than in V_{AB}. Note that V_{CA} is not distorted in P1 and P4.

In general, assume that the HFL inverter of Fig. 32 is operating under fault-free condition. Then after a few cycles, two of the line voltages abruptly get distorted. The phase which is common between the two line voltages is the lost phase in the primary-side Dc/Ac Converter provided that these distortions happen in the sectors in which this common phase has either the maximum or the minimum magnitude. Table VII shows distortion patterns associated with failure of each of the three phases. These distortion patterns are used to diagnose the lost phase in Dc/Ac Converter and Ac/Pulsating-Dc Converter.

TABLE. VII. DISTORTION PATTERNS OF THE OUTPUT LINE VOLTAGES IN CASE OF A FAILURE IN A PHASE OF DC/AC AND AC/PULSATING-DC CONVERTER.

Sector / Failed Phase	P1	P2	P3	P4	P5	P6
Phase u {S1x | x=1,…,4}	Distortion in VAB, VCA	Distortion in VAB, VCA	No Distortion	Distortion in VAB, VCA	Distortion in VAB, VCA	No Distortion
Phase v {S2x | x=1,…,4}	Distortion in VAB, VBC	No Distortion	Distortion in VAB, VBC	Distortion in VAB, VBC	No Distortion	Distortion in VAB, VBC
Phase w {S3x | x=1,…,4}	No Distortion	Distortion in VCA, VBC	Distortion in VCA, VBC	No Distortion	Distortion in VCA, VBC	Distortion in VCA, VBC

Fig. 36 shows an illustration of the fault diagnosis algorithm in case of a failure of one full-bridge converter in the Dc/Ac Converter based on the above explanations. P1 to P6 are the six sectors as shown in Fig. 33. V_{AB_Ref}, V_{BC_Ref}, and V_{CA_Ref} are the reference values for the three phase line voltages while V_{AB}, V_{BC}, and V_{CA} are the sensed values for the same. S_{1X_fail}, S_{2X_fail}, and S_{3X_fail} are flags, each indicating a failure of a full-bridge converter in Dc/Ac Converter. For instance, S_{1X_fail} indicates the loss of S_{11}, S_{12}, S_{13}, and S_{14}. As an illustrative example of this scheme, if in any of the sectors P1, P2, P4, or P5, the differences of V_{AB} and V_{CA} with their references are higher than a threshold, S_{1X_fail} is set.

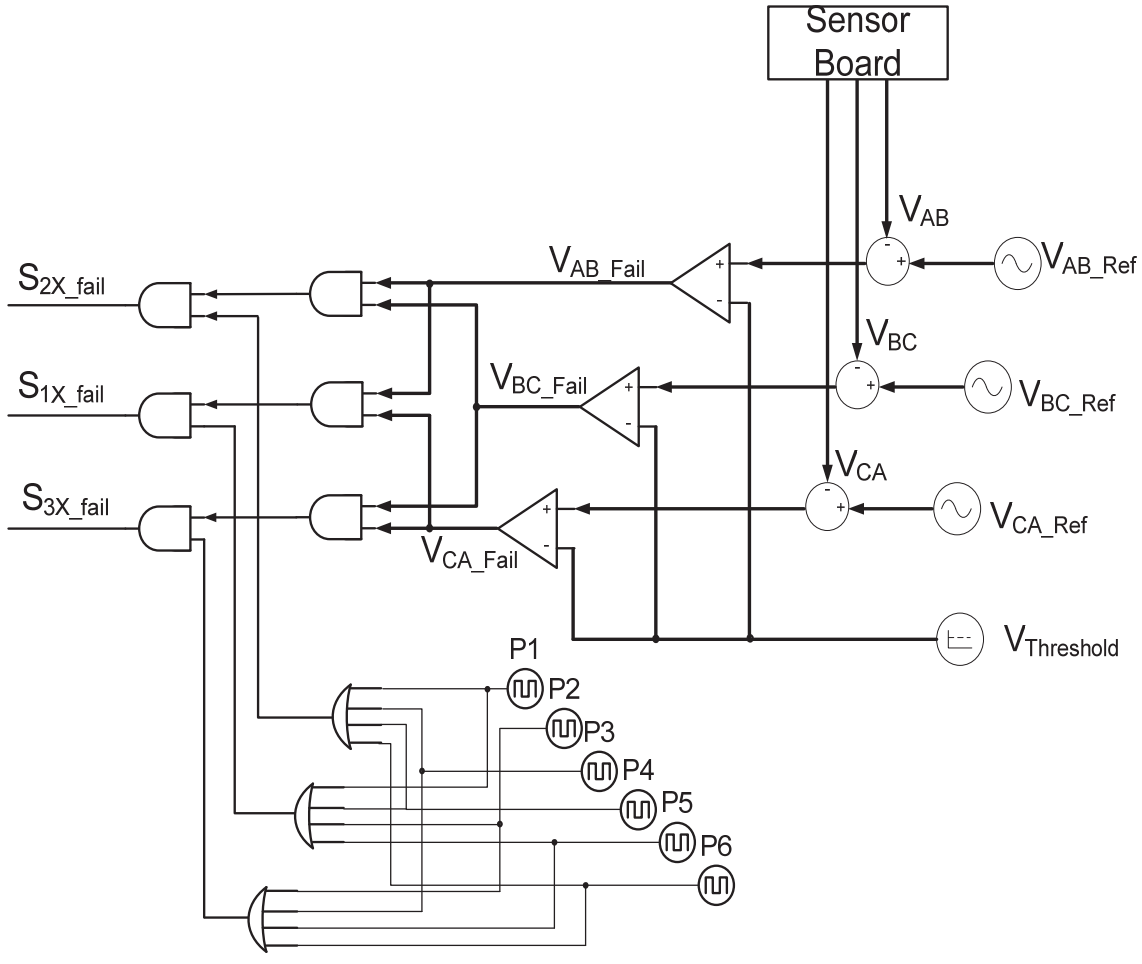


Fig. 36. The proposed fault diagnosis algorithm for transition from three to two active full-bridge converters

2) Loss of Two Phases in the Dc/Ac Converter

Fig. 36 also demonstrates the fault diagnosis scheme in case of transition from three to one active full-bridge converter in the Dc/Ac Converter. It is based on the fact that in such a fault (failure of two full-bridge converters in the Dc/Ac Converter), V_{REC} will become almost zero. Consequently, all of the output line voltages cease to zero as soon as the output filter capacitors get discharged.

Fig. 37 shows a case illustration in which HB1 fails at 32.7 msec. Fig. 37a shows that at t = 32.7 ms, $V_{AB\_error} = V_{AB}\_Ref - V_{AB}$ exceeds a threshold set in the fault diagnosis program (5%) and S_{1X_fail} is activated. It is shown that in less than 1 msec FTC can restore the output line voltage V_{AB}. Same scenario is repeated in Fig. 37b in which FTC is not activated intentionally in order to show the effect of HB1 loss on V_{AB}.

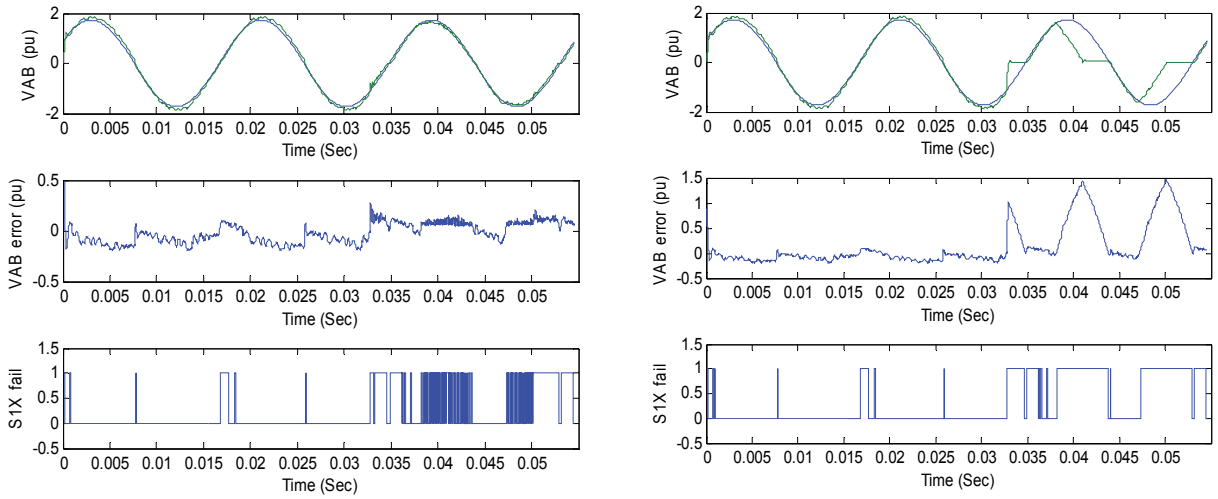


Fig. 37. (a). *Top*: V_{AB}_Ref (in blue) and V_{AB} (in green); both normalized to phase voltage, *middle*: error signal (V_{AB}_Ref-V_{AB}), and *bottom*: S_{1X_fail} . At t = 32.7 msec HB1 in Dc/Ac Converter fails and fault diagnosis logic in Fig. 36 activates S_{1X_fail}. Note that fault is removed in less than 1 msec. (b). The same scenario is repeated despite the fact that here, the fault is detected (see the jump in the error signal – middle curve) but fault is not restored intentionally in order to show the effect of HB1 loss on V_{AB}.

2. Failure in the Ac/Pulsating-Dc Converter

If a switching device in a leg of Ac/Pulsating-Dc Converter fails, the distortion in the output line voltages is exactly similar to what happens if the corresponding full bridge (for the same phase) in the Dc/Ac Converter fails. As such, the fault diagnosis algorithm of Fig. 36 disables gate pulses to the MOSFETs of the leg associated with the diagnosed faulty phase in the Ac/Pulsating-Dc as well. For instance, if the fault diagnosis algorithm tracks a failure in phase u, gate pulses to UT and UB in the Ac/Pulsating-Dc converter will be disabled upon diagnosis and PWM references for HB2 and HB3 will be changed as will be explained in section IV.

3. Failure in the Pulsating-Dc/Ac Converter

In order to facilitate our analysis, the content of V_{REC} at different sectors P_1 to P_6 is firstly given in Table VIII. For instance, it shows that in sector P1, the pulse area of V_{REC} at every switching period is equivalent to V_{uv}. The effect of a MOSFET failure in Dc/Ac Converter on the output line voltages is analyzed through a case illustration in order to develop the fault diagnosis concept for such failures. Consider that while the HFL inverter of Fig. 32 is in fault-free operation, suddenly UUT fails (a short circuit between 2 of the three MOSFET terminals [63]). As a typical example, the effect of a short circuit failure between drain and source terminals of MOSFETs on V_{REC} as well as on the output line voltages of HFL inverter is shown in Fig. 38. This fault occurs at t = 2 m sec which falls in sector P_1. It is shown that before sector P_3, no

distortion appears in the output line voltages. The reason is as Table VIII shows, in sectors P_1 and P_2, the information of line voltages V_{uv} and V_{uw} is encoded in V_{REC} and as shown previously in Table V, UUT is supposed to remain on in these sectors. However, it is observed that in P_3 since VVT turns on (according to Hybrid modulation algorithm - Table. V), V_{AB} is zero and $V_{BC} = -V_{CA}$. Note that in P_6, V_{CA} is zero and $V_{AB} = -V_{BC}$. In P_3 and P_6 there are voltage spikes in V_{REC} due to the fact that in these two sectors UUB starts HF switching while UUT is shorted due to the fault.

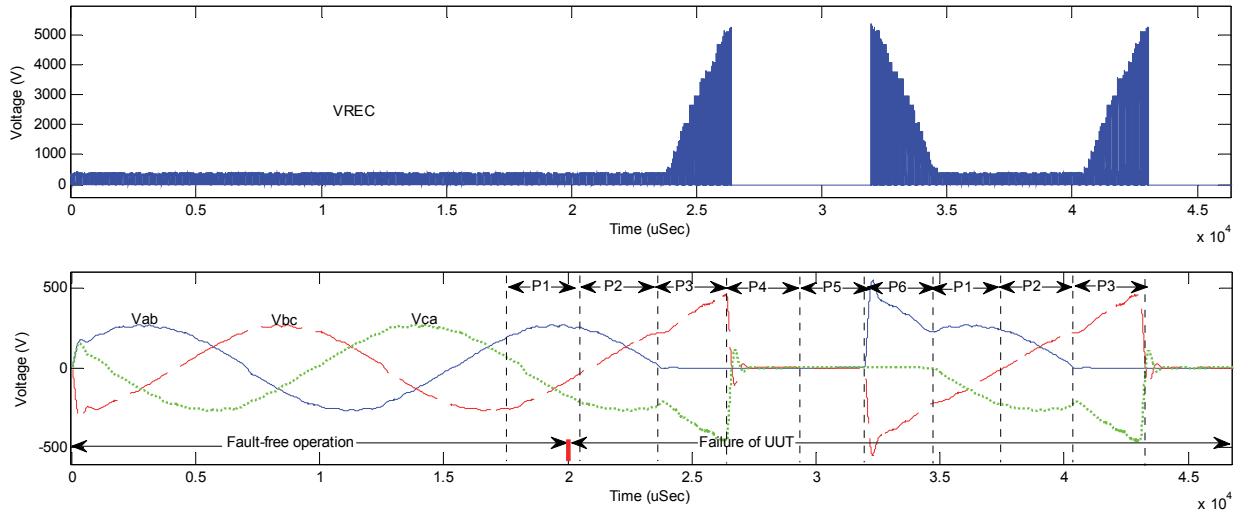


Fig. 38. The effect of UUT failure on V_{REC} and output line voltages of HFL inverter of Fig. 32.

TABLE VIII. THE CONTENT OF PULSATING-DC (V_{REC}) AT SIX SECTORS.

Sector / Signal	P1	P2	P3	P4	P5	P6
VREC	Vuv	Vuw	Vvw	Vvu	Vwu	Vwv

By generalizing this analysis to other switching devices, a fault diagnosis algorithm for Pulsating-Dc/Ac Converter can be developed as shown in Table IX. Having analyzed all types of faults in three stages of the HFL inverter and proposed relevant fault diagnosis algorithms, next section illustrates the FTSS for this topology in details.

TABLE IX. FAULT DIAGNOSIS FOR PULSATING-DC/AC CONVERTER.

Sector / Failed MOSFET	P1	P2	P3	P4	P5	P6
UUT	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC} = -V_{CA}$	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB} = -V_{BC}$
UUB	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB} = -V_{BC}$	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC} = -V_{CA}$
VVT	No Distortion	$V_{AB}=0$ $V_{BC} = -V_{CA}$	No Distortion	No Distortion	$V_{BC}=0$ $V_{AB} = -V_{CA}$	No Distortion
VVB	No Distortion	$V_{BC}=0$ $V_{AB} = -V_{CA}$	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC} = -V_{CA}$	No Distortion
WWT	$V_{CA}=0$ $V_{AB} = -V_{BC}$	No Distortion	No Distortion	$V_{BC}=0$ $V_{AB} = -V_{CA}$	No Distortion	No Distortion
WWB	$V_{BC}=0$ $V_{AB} = -V_{CA}$	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB} = -V_{BC}$	No Distortion	No Distortion

D. FTSS for the HFL Inverter

Using the backdrop of the fault-free switching scheme, as explained in Section II, and possible fault scenarios and diagnosis algorithms in section III, we now describe the FTSS for potential switching device failure in all of the three stages.

For Dc/Ac Converter, the proposed FTSS restores three phase output line voltages when one or even two phases of the Dc/Ac Converter are lost. In essence, the fault-tolerant operation of the Dc/Ac Converter ensures the synthesis of the same encoded pulsating-Dc voltage (obtained during the fault-free operation) when one or even two phases of the Dc/Ac Converter are lost.

In order to give an analytical insight into the FTSS, at first we consider the equations for the output line-voltages of the HFL inverter under fault-free operation condition. For the HFL inverter of Fig. 32, the following sets of equations are valid for the output line voltages:

$$V_{AB} = (S_{UUT} - S_{VVT}) \times V_{REC} \tag{22}$$

$$V_{BC} = (S_{VVT} - S_{WWT}) \times V_{REC} \tag{23}$$

$$V_{CA} = (S_{WWT} - S_{VVT}) \times V_{REC} \tag{24}$$

in which S_{UUT}, S_{VVT}, and S_{WWT} are the switching functions of the Pulsating-Dc/Ac Converter.

However, we know that

$$V_{REC} = \frac{N_2}{N_1} \times V_{DC} \times (MAX\{|S_{11} - S_{21}|, |S_{11} - S_{31}|, |S_{21} - S_{31}|\} + MAX\{|S_{13} - S_{23}|, |S_{13} - S_{33}|, |S_{23} - S_{33}|\}) \tag{25}$$

where S_{ij} (i,j=1,2,3) is the switching functions of the Dc/Ac Converter, V_{DC} is the input dc voltage, and N_1 and N_2 are the primary and the secondary turns ratio of the HF transformers respectively. As mentioned earlier, if any one of the three full-bridge converters of Dc/Ac Converter fails, the encoded information of the relevant phase in V_{REC} is lost. For instance, if the full-bridge converter consisting of S_{31}, S_{32}, S_{33}, and S_{34} fails, the information of phase c will no longer be encoded in V_{REC} in sectors P2, P3, P5, and P6. Consequently, V_{REC} will be expressed as follows:

$$V_{REC} = \frac{N_2}{N_1} \times V_{DC} \times (\{|S_{11} - S_{21}|\} + \{|S_{13} - S_{23}|\}) \tag{26}$$

This in turn leads to a severe distortion in V_{BC} and V_{CA} and a slightly more moderate distortion in V_{AB}. Fig. 35 shows the effect of loss of the full-bridge converter generating the information of phase c on V_{AB} and V_{CA} (Note that a generalized analysis of loss of phases u, v, and w are given in Table VII in context of the fault diagnosis). So, in order to restore the

information of the lost phase, PWM references for the remaining full-bridge converters should be modified. In the subsequent sections, it will be shown that this PWM reference modification is required for output line voltage restoration no matter in which stage a failure is occurred. The following parts discuss these modifications under different fault scenarios.

1. Case 1: FTSS under Single Phase Outage in Dc/Ac Converter

If one of the phase outputs of the Dc/Ac Converter is lost, the signature of the V_{REC} changes, which in turn affects the output phase voltages. To generate the pulsating-Dc voltage that has the same characteristic (or information content) as that obtained under fault-free operation, one of the remaining Dc/Ac Converter full-bridge converters has to generate a bipolar pulse train for the highest phase while the other full-bridge converter has to generate a bipolar pulse train for the lowest phase. “PWM1” and “PWM2” are two sets of four PWM signals which contain the information of the highest and the lowest phases in each sector if any one of S_{1X_fail}, S_{2X_fail}, or S_{3X_fail} signals is 1 (Fig. 39). Based on the diagnosed faulty phase in the Dc/Ac Converter, they are applied to the remaining full-bridge converters via a set of two demultiplexers “PWM DEMUX1” and “PWM DEMUX2”. For instance, if in any of the four sectors P1, P2, P4, or P5 the differences of V_{AB} and V_{CA} with their references are higher than a threshold, S_{1X_fail} is set (refer to Fig. 36). Hence, PWM1 is connected to the second full-bridge converter (S2X switches) via PWM DEMUX1 and PWM2 is connected to the third one (S3X switches) via PWM DEMUX2. The result will be generation of the information of the highest phase by the second full-bridge converter and of the lowest phase by the third one in every sector.

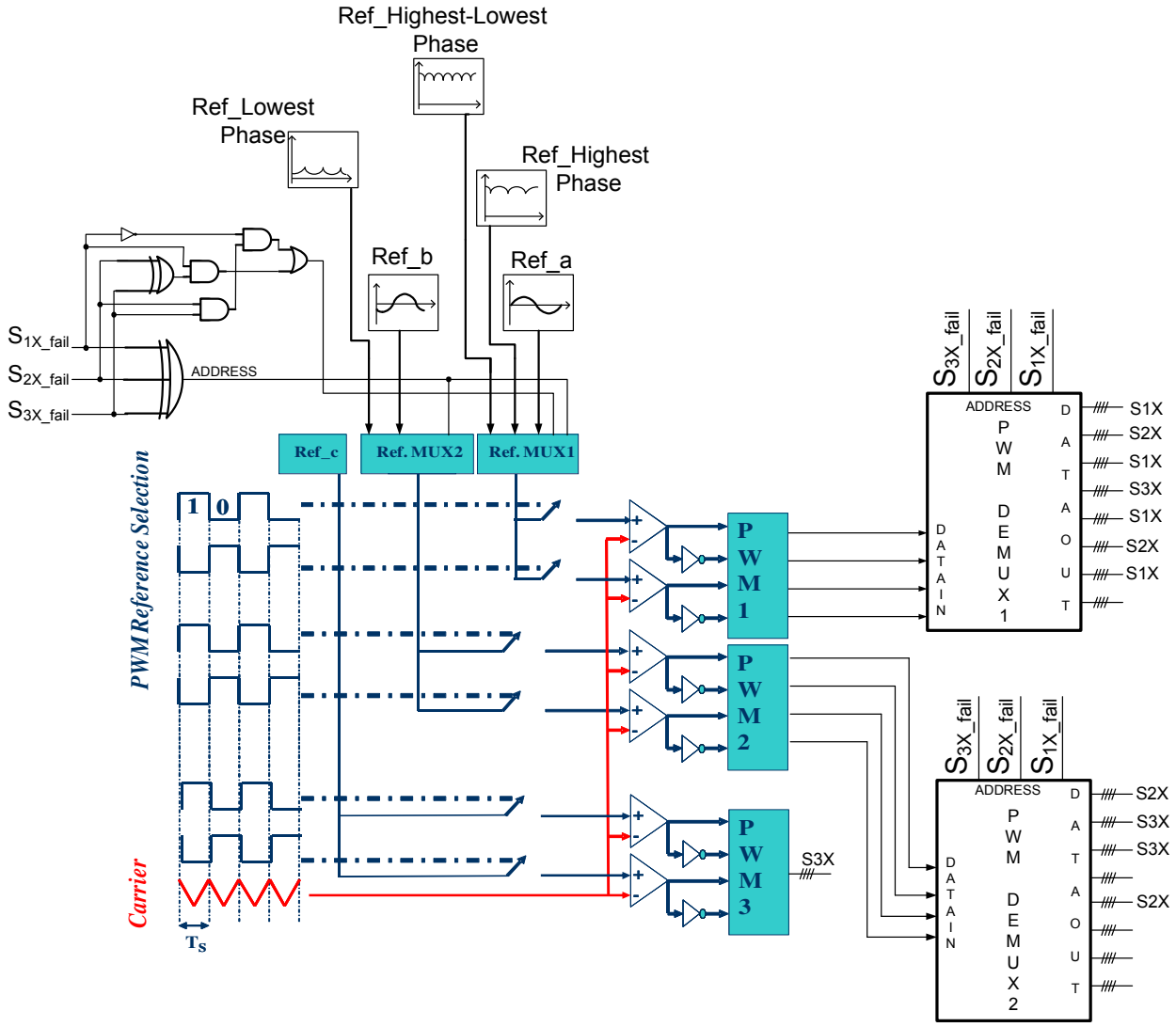


Fig. 39. A PWM technique to retain the nominal operation in case of a single phase or a double-phase outage. (If for instance phase w is lost, one of the remained full-bridge converters of the Dc/Ac Converter generates a bipolar pulse train containing the information of the highest phase in every sector from P1-P6 while the other one does the same for the lowest phase.

2. Case 2: FTSS under Double Phase Outage in Dc/Ac Converter

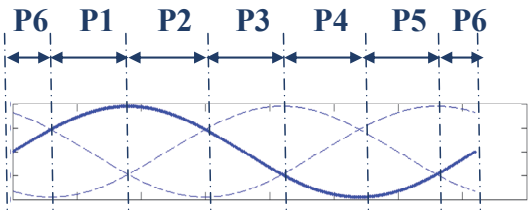
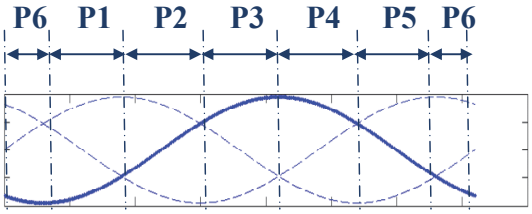
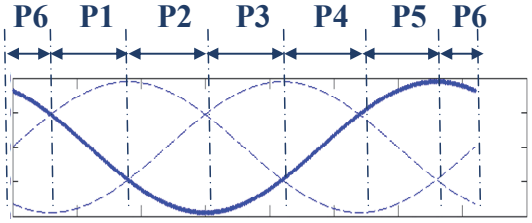
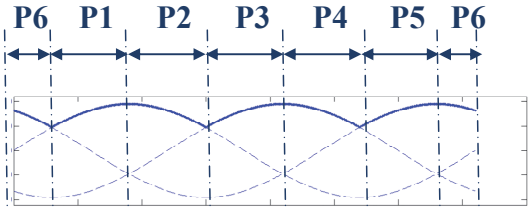
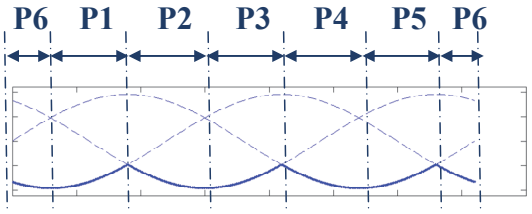
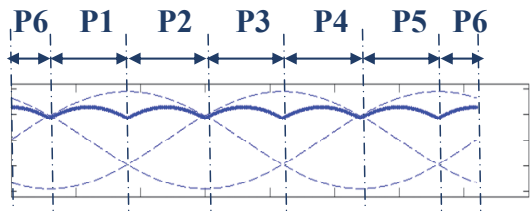
If two phases of the Dc/Ac Converter are lost, the modulating reference of the remaining full-bridge converter has to be modified so as to encode the same information in the Pulsating-Dc

voltage (V_{REC}) as in fault-free operation. This information is nothing but the highest line voltage at each time. The mechanism to realize this FTSS is shown in Fig. 39. It shows that the required PWM reference in each of the sectors P1 to P6 is generated using the PWM reference for the highest line voltage in that sector. Based on the diagnosed faulty phases in the Dc/Ac Converter, the modified PWM is applied to the remaining full-bridge converter via demultiplexer PWM DEMUX1. For instance, consider that both of the S_{1X_fail} and S_{3X_fail} signals are set indicating that the only remained full-bridge converter in the Dc/Ac Converter is the one consisting S_{21}, S_{22}, S_{23}, and S_{24}. Hence, the modified PWM is connected to the second full-bridge converter via PWM DEMUX1. The result will be generation of the information of the highest line voltage by the second full-bridge converter in every sector. Table X summarizes the PWM references for nominal operation, single- phase outage and double phase outage.

3. Case 3: FTSS for Fault in Ac/Pulsating-Dc Converter

As explained in section III part B, if a leg of the Ac/ Pulsating –Dc Converter suddenly fails, it causes the same distortion pattern in the output line voltages as resulted from a failure of the same phase in the Dc/Ac Converter. It was also shown that for the same reason, the fault diagnosis algorithm for these two converters are equivalent and upon detection of a certain distortion pattern in the output line voltages, a certain phase in both Dc/Ac Converter and Ac/Pulsating-Dc Converter would be considered faulty. As an example, assume that during fault-free operation, suddenly a MOSFET in the phase c fails. Since the protection circuits of the module prevents firing of WT and WB (upon detection of a short circuit in the leg consisting these switching devices), V_{REC} will include only the information of phase a and phase b. As a

TABLE X. PWM REFERENCES FOR THE DC/AC CONVERTER UNDER FAULT-FREE AND FAULT CONDITIONS.

Operational mode	Switches	PWM Reference for sectors P1 – P6
Fault free	S_{11}, S_{12}, S_{13}, and S_{14}	
	S_{21}, S_{22}, S_{23}, and S_{24}	
	S_{31}, S_{32}, S_{33}, and S_{34}	
Singe-phase outage (Loss of S_{31}, S_{32}, S_{33}, and S_{34})	S_{11}, S_{12}, S_{13}, and S_{14}	
	S_{21}, S_{22}, S_{23}, and S_{24}	
Double-phase outage (Loss of S_{31}, S_{32}, S_{33}, S_{34}, S_{21}, S_{22}, S_{23}, and S_{24})	S_{11}, S_{12}, S_{13}, and S_{14}	

result, output line voltages of HFL inverter will be distorted according to the last row of Table VII. This fault scenario is shown in Fig. 40. This specific distortion pattern in the output line voltages is interpreted using the fault diagnosis algorithm of Fig. 36 as a failure of phase c in either Dc/Ac Converter or Ac/Pulsating-Dc Converter. The restoration steps are listed as follows:

1. Inactivation of the gate pulses for S31, S32, S33, and S34 in Dc/Ac Converter and WT and WB in Ac/Pulsating-Dc Converter.
2. Modifying the PWM references for S11, S12, S13, S14 and S21, S22, S23, S24 switches according to restoration methodology of Fig. 39 and waveforms of Table X.

In case of a failure in other phases, the above steps will be adjusted accordingly (Refer to Fig. 39)

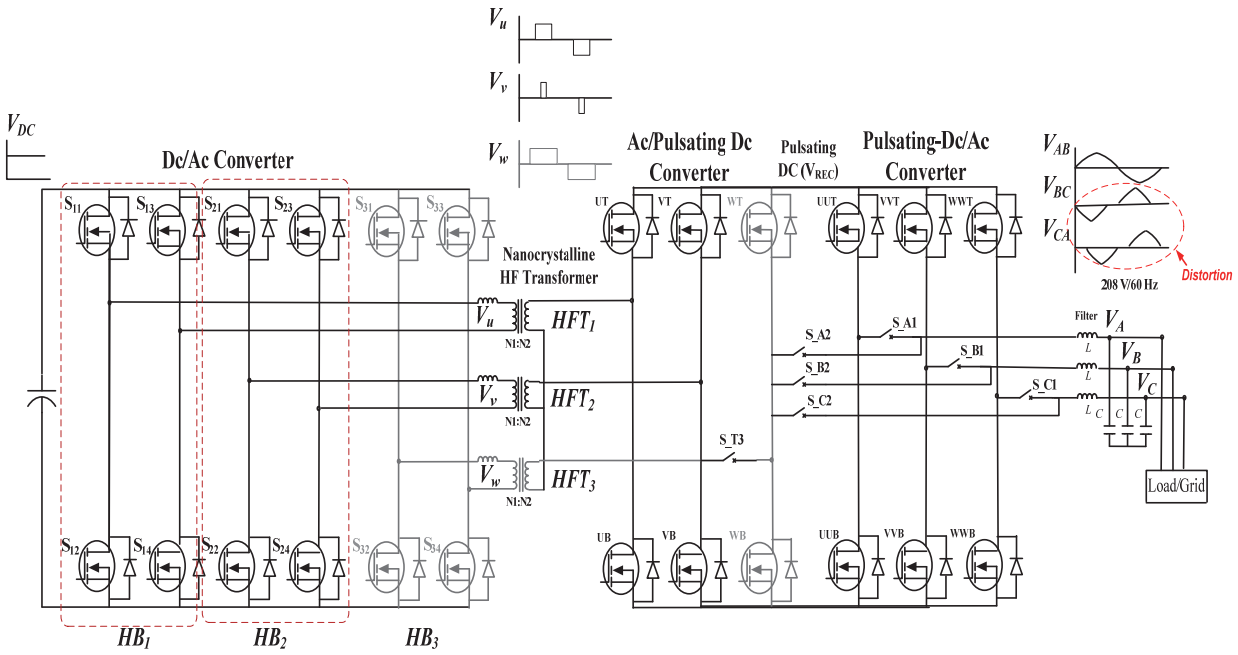


Fig. 40. A failure in a phase of Ac/Pulsating-Dc Converter causes the same distortion in the output line voltages as if the same fault is lost in the Dc/Ac Converter. Failure of phase c in the Ac/Pulsating Converter causes a distortion pattern from which the fault diagnosis algorithm considers a fault in phase c of both Converters.

4. Case 4: FTSS for Fault in Pulsating-Dc/Ac Converter

In Table IX, a fault diagnosis algorithm was developed for failure in switching devices in Pulsating-Dc/Ac Converter. No matter what type of failure happens (short circuit between any of the MOSFET terminals), the faulty circuit will be isolated upon detection of excess current or V_{DS_Sat} depending on the protection circuits included in the power modules. But as mentioned earlier, this only prevents extra damage to other devices and load. Yet, the output line voltages of the HFL inverter should be restored. Hence, upon detection of a failure in Pulsating-Dc/Ac Converter, the fault diagnosis algorithm identifies the failed converter arm and restoration action starts immediately based on the type of lost phase. For instance, if the fault occurs in phase a, upon being identified by fault diagnosis algorithm, the following actions are taken in order to restore the output line voltages:

1. S_A1 and S_T3 will be opened
2. S_A2 is closed
3. PWM commands for UUT and UUB are applied to WT and WB respectively
4. PWM signals for $\{S_{1X}, X=1,\ldots,4\}$and $\{S_{2X}, X=1,\ldots,4\}$are changed as in the case if phase w is lost in the Dc/Ac Converter (Table X). Also PWM signals for $\{S_{3X}, X=1,\ldots,4\}$ are disabled.
5. PWM commands for UT, UB, VT, and VB are changed as in the case if phase w is lost in the Ac/Pulsating-Dc Converter (Table X).

Now that fault diagnosis algorithm and FTSS for all of the possible faults in all of the stages in the HFL inverter of Fig. 32 are covered, the overall scheme is presented in Fig. 41.

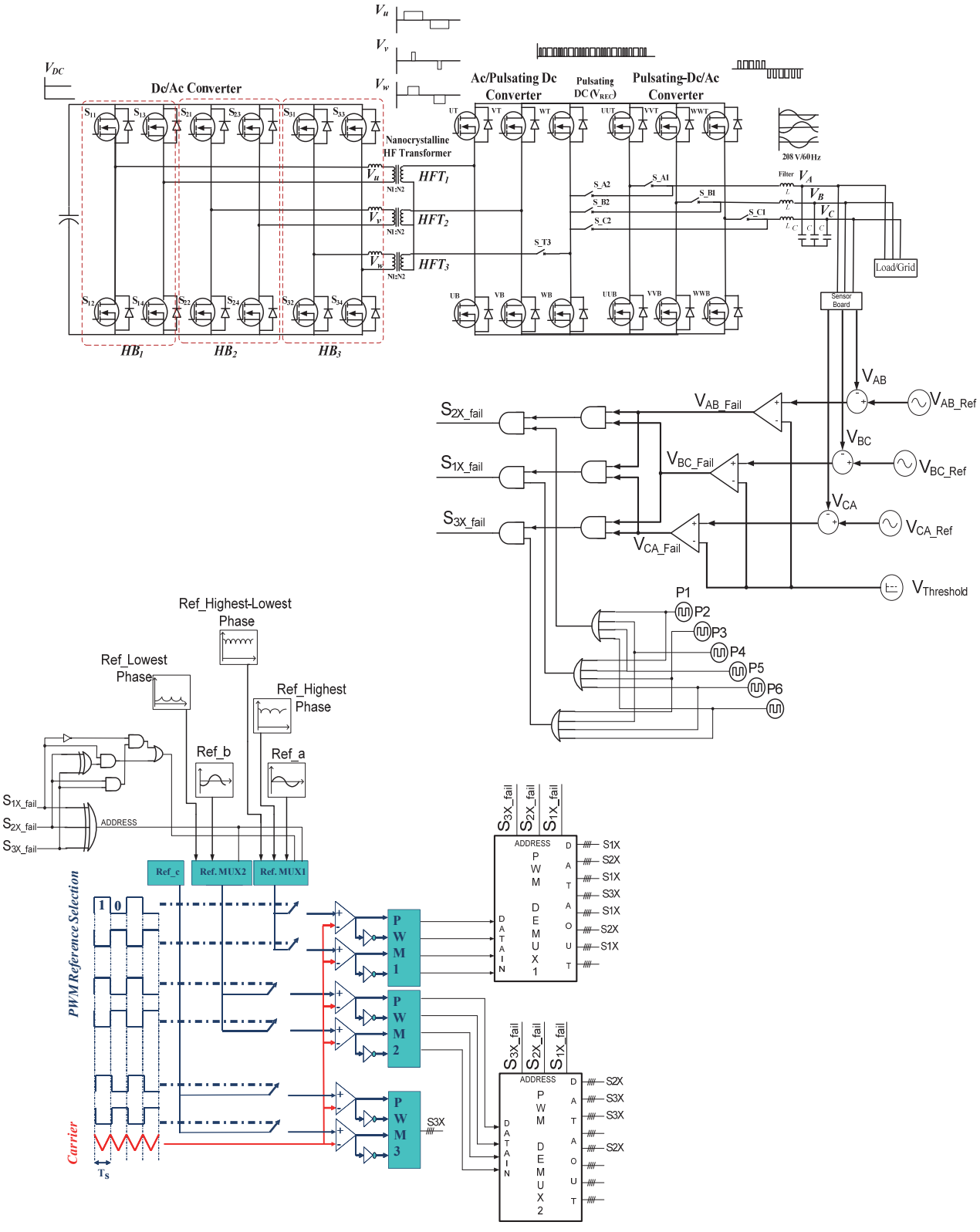
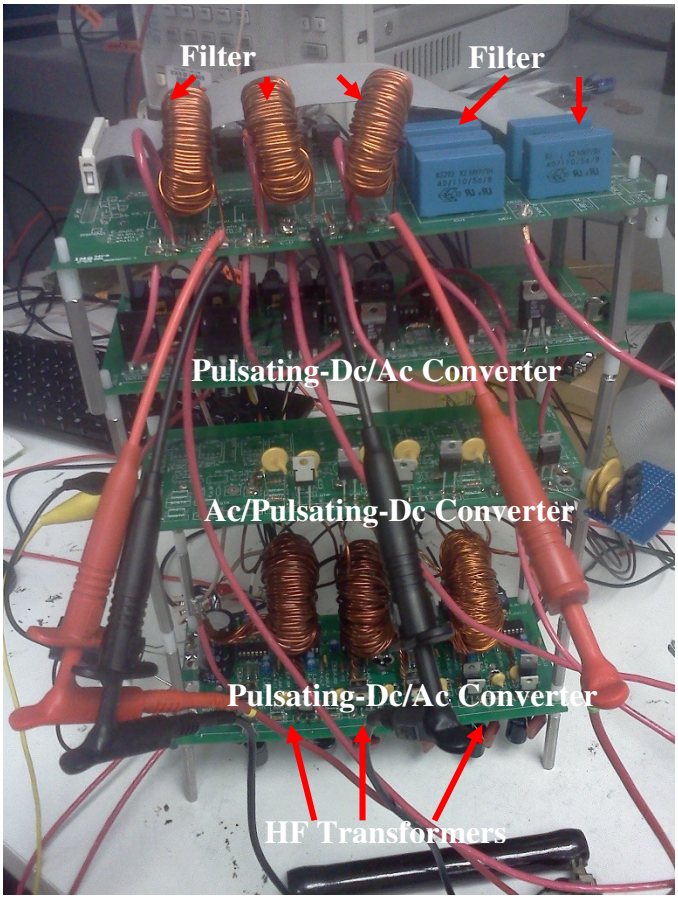


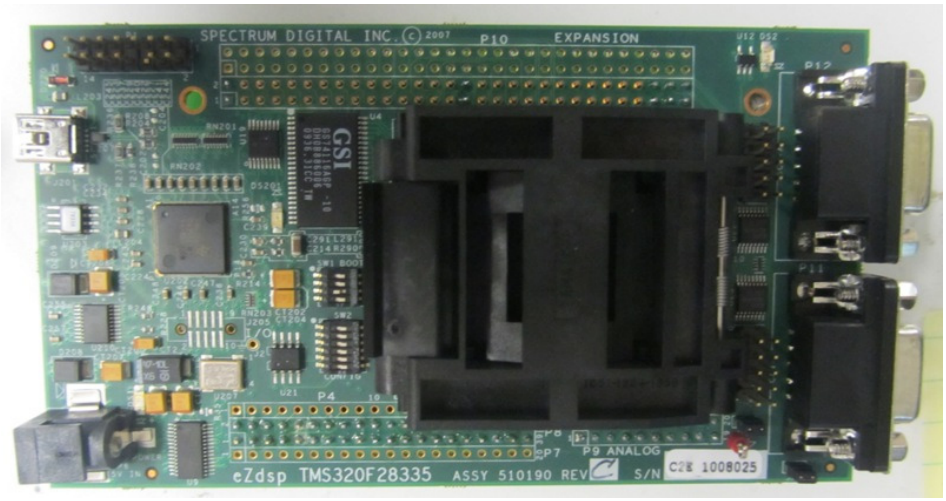
Fig. 41. Illustration of the overall fault diagnosis algorithm and FTSS for an isolated and multi-stage HFL inverter

E. Experimental Results

In the previous sections it was shown that in all of the possible fault scenarios, no matter in which stage a failure occurs, output line voltage restoration is based on a operation transition from three to two full bridges in the primary-side Dc/Ac Converter. Specifically, if the fault diagnosis algorithm detects loss of phase a in Dc/Ac Converter or Ac/Pulsating-Dc Converter, HB2 and HB3 will be keep on operating with modified PWM references. If the failure of phase a is detected in Pulsating-Dc/Ac Converter, restoration process replaces (UUT, UUB) with (WT, WB) MOSFETs feeding phase a of the load. However, since there are only two legs remained in the Ac/Pulsating-Dc Converter (i.e. UT,UB, VT,VB), Dc/Ac Converter should operate with only two full bridges HB1, and HB2 (with modified PWM references). As such, the restorating operation of Dc/Ac Converter which is the key part of the proposed FTSS is verified through experimental results in this section. Experimental results for the proposed FTSS are obtained using a HFL inverter prototype with the following specifications: nominal input voltage of 40 V, nominal output voltage of 208 V line-to-line (rms), switching frequencies of 20 kHz and 40 kHz for the Dc/Ac and the Pulsating-Dc/Ac Converters, respectively. The output power is 1 kW and the output LC filter has an inductance of 1 mH and a capacitance of 1 μF per phase. Fig. 42 shows the developed prototype and the DSP controller board. Table XI summarizes some technical specifications of the developed prototype.



(a)



(b)

Fig. 42. (a) A 1-kW isolated and multi-stage HFL prototype developed for validation of the proposed FTSS scheme. (b) TI series TMS320F28335 DSK board that generates the switching signals.

TABLE XI. PHYSICAL SPECIFICATIONS OF THE INVERTER PROTOTYPE.

Input voltage	40 V
Output voltage	208 V
Switching frequency (Dc/Ac Converter)	20 kHz
Switching frequency (Pulsating-Dc/Ac and Ac/Pulsating Dc Converters)	40 kHz
Rated power	1000 W
Controller board	TMS320F28335

To verify the FTSS, two different scenarios are tested using a TMS320F28335-DSP based controller and the relevant power-stage results are provided to ascertain the effectiveness of the FTSS under different fault conditions.

1. Scenario 1: Single Phase Outage (Transition from Three Full-bridge Converters to Two Full-bridge Converters in the Dc/Ac Converter)

In this scenario, prior to the onset of the fault, three full-bridge converters of the Dc/Ac Converter are generating three bipolar pulse trains containing the information of all of the three phases. At the onset of the fault, the full-bridge converter corresponding to phase w fails. Consequently, the information of phase c is no longer available to the Pulsating-Dc/Ac Converter. Fig. 43 shows the pattern of distortion in the output line voltages V_{AB} and V_{CA}. Restoration onsets by changing the PWM references for the remaining two full-bridge converters so as to provide the information of the highest and the lowest phases to the Ac/Pulsating-Dc

Converter. PWM references (according to Table X) for the Dc/Ac Converter MOSFETs before and after loss of one full-bridge converter in the first fault scenario are shown in Fig. 44.

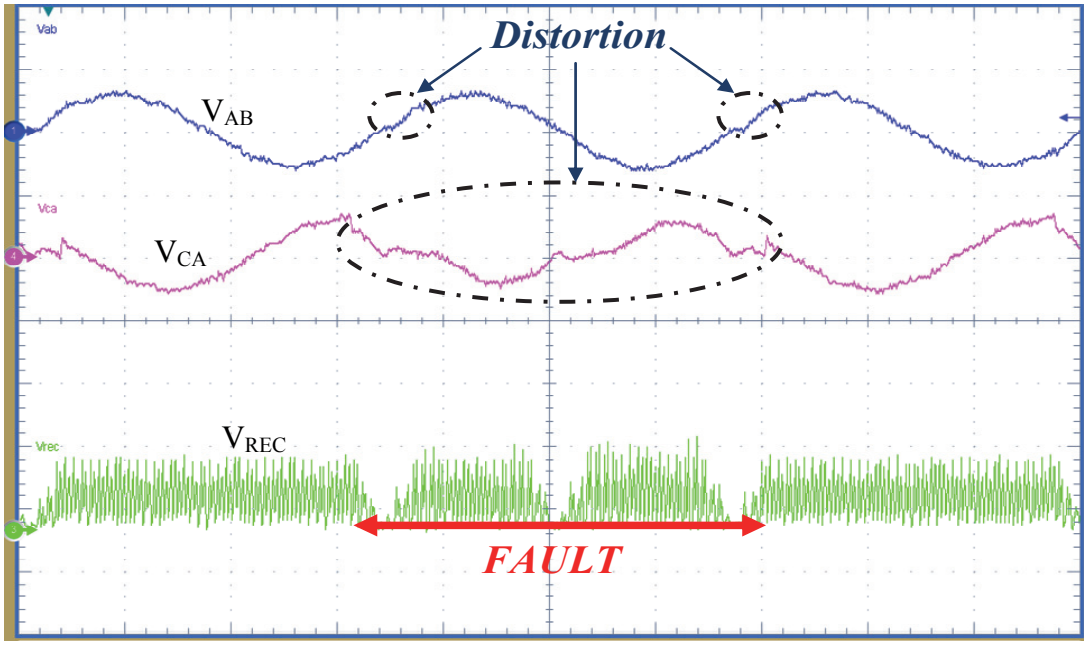


Fig. 43. Effect of a single phase outage (phase w) on the output line-voltages V_{AB} (top), V_{CA} (middle), and V_{REC} (bottom) of the HFL inverter in Fig. 32. It is shown that failure of phase w causes a more severer distortion in V_{CA} rather than in V_{AB}.

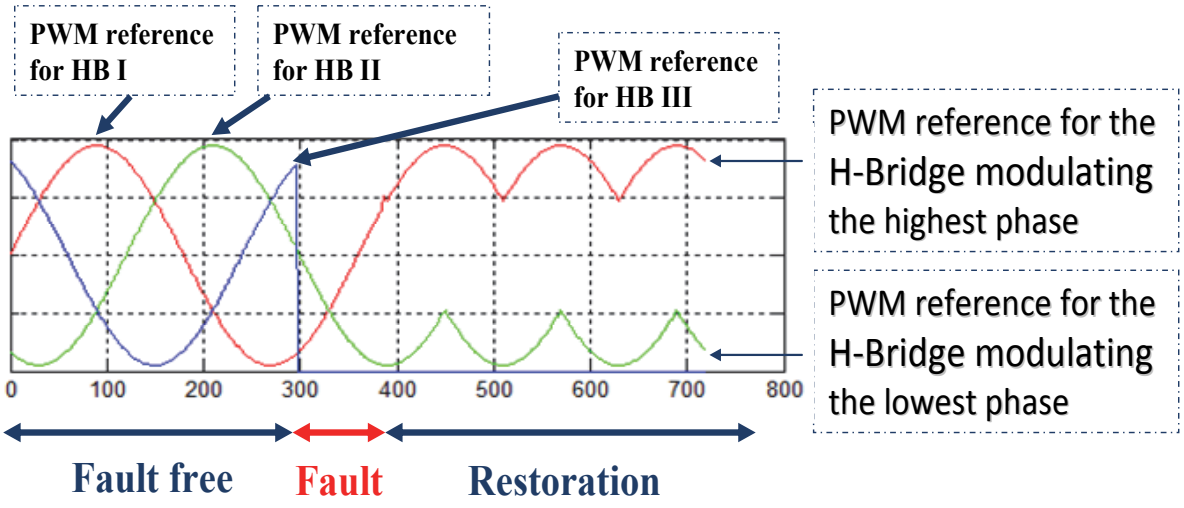


Fig. 44. PWM references for the Dc/Ac-Converter switches before and after loss of one full-bridge converter in the first fault scenario.

Fig. 45 shows that amplitude of V_{CA} and I_C fall to almost zero in the fault interval since the lost full-bridge converter is the one generating information of phase c. V_{REC} amplitude also falls to zero in the fault interval.

Fig. 46 illustrates the distortions incurred in V_{AB} and I_A due to the loss of the full-bridge converter generating information of phase c. Note that as explained earlier, since the lost phase is w, it does make a huge distortion on V_{AB} and I_A. However, since at the onset of the fault V_C is the highest phase and has reached the peak value, it causes a drastic voltage collapse on V_{CA}.

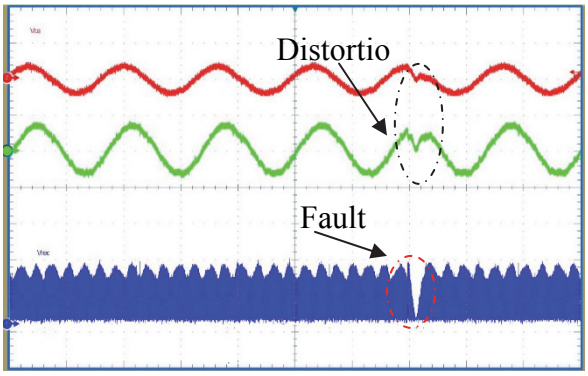


Fig. 45. V_{CA} (top), I_C (middle), and V_{REC} (bottom) in the fault scenario 1: Loss of one full-bridge converter in Dc/Ac Converter.

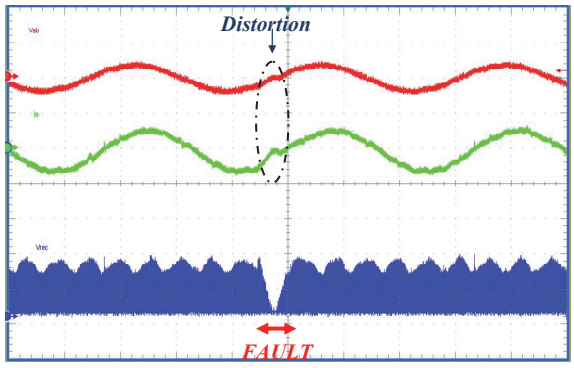


Fig. 46. V_{AB} (top), I_A (middle), and V_{REC} (bottom) in the fault scenario 1: Loss of one full-bridge converter in Dc/Ac Converter.

Fig. 47 demonstrates V_{CA}, V_u, V_v, and V_w and a larger view of these waveforms in the fault-free, fault, and restoration operation. V_u, V_v, and V_w represent output voltages of three HF Transformers in Fig. 32. Fig. 47b is the larger view of these waveforms at 75 degrees (fault-free operation mode). Note that, V_u and V_v have the highest and the lowest pulse widths respectively. Fig. 47d shows the same at 690 degrees in which V_{CA} is reaches the peak. Note that since FTSS has changed the PWM references according to table. VI, V_u and V_v have the highest and the lowest pulse-widths respectively. Assuming the HFL inverter is operating under fault-free

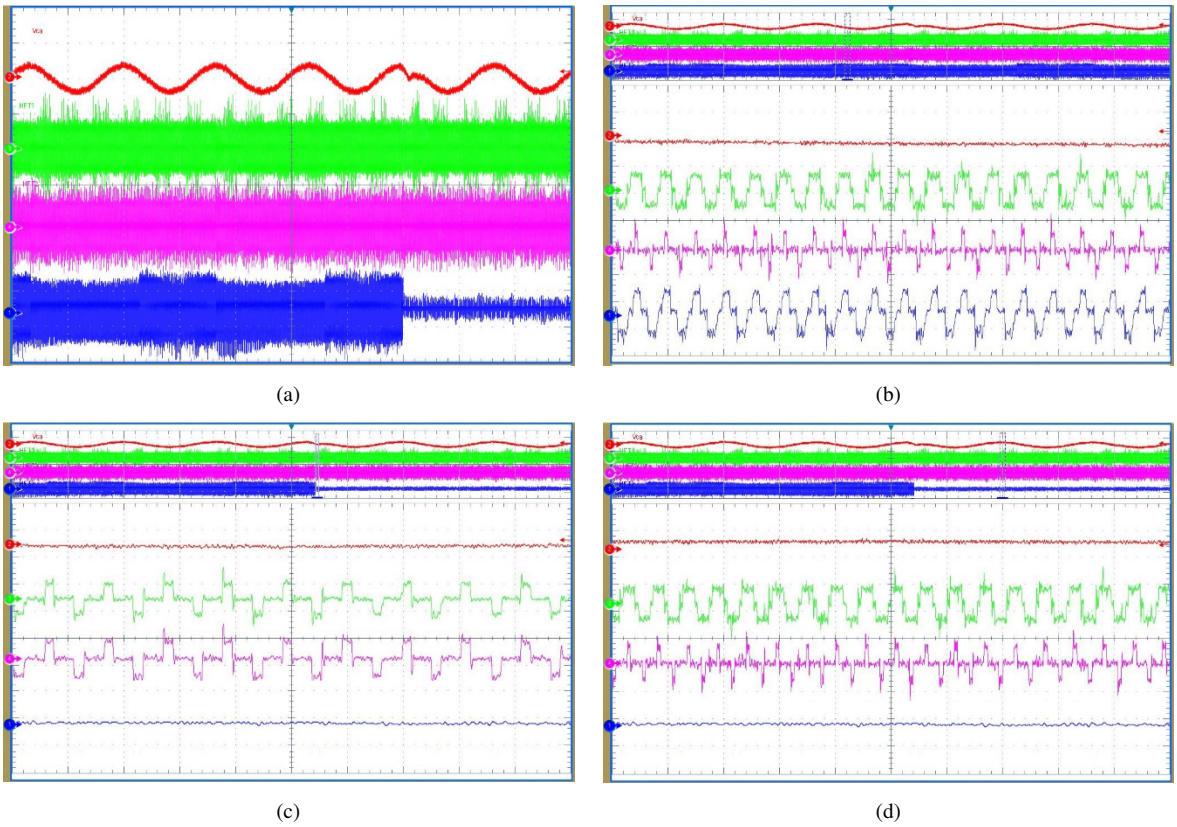


Fig. 47 (a). From top to bottom: V_{CA}, V_u, V_v, and V_w, (b) fault-free operation interval, (c) interval of the first fault scenario, and (d) restoration interval.

conditions and based on Table X, at 690 degree, V_u, V_v, and V_w are supposed to have the lowest, intermediate, and the highest pulse-width respectively.

2. Scenario 2: Single-Phase Outage Followed by a Double-Phase Outage

This case demonstrates the impact of FTSS when one of the two remaining Dc/Ac Converter phases fails while restoration is ongoing to recover the inverter from the earlier loss of another Dc/Ac Converter phase. In particular, the full-bridge converter generating the highest phase is

lost due to a second fault at 210 degrees. Restoration onsets at 300 degrees when the PWM reference for the only active full-bridge converter of the

Dc/Ac Converter is changed as demonstrated in Fig. 48. The new PWM reference is actually obtained by subtracting the two references applied prior to the onset of this fault. Fig. 49 demonstrates the adverse effect of this fault on the output line voltages of the HFL inverter. Following the second fault, V_{AB} and V_{BC} have a magnitude of zero before restoration initiates. Fig. 49c and Fig.18d show a larger view of the output of the two HF Transformers in Fig. 32 as well as V_{BC} under fault-free and restoration modes of operation. Subsequent to the adjustment of the PWM reference for the remaining active phase following FTSS, V_{AB} and V_{BC} are restored and operation is sustained.

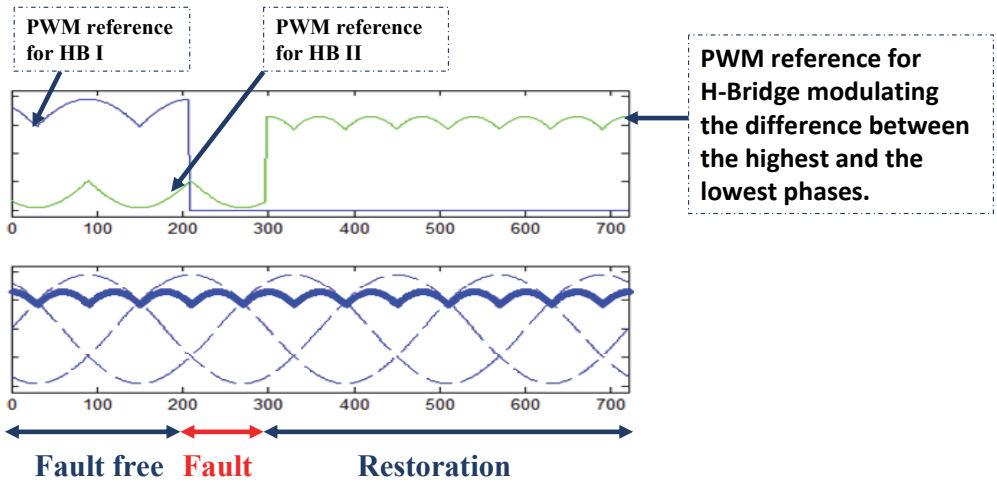


Fig. 48. PWM references for the Dc/Ac-Converter switches before and after loss of another full-bridge converter in the second fault scenario: double-phase outage.

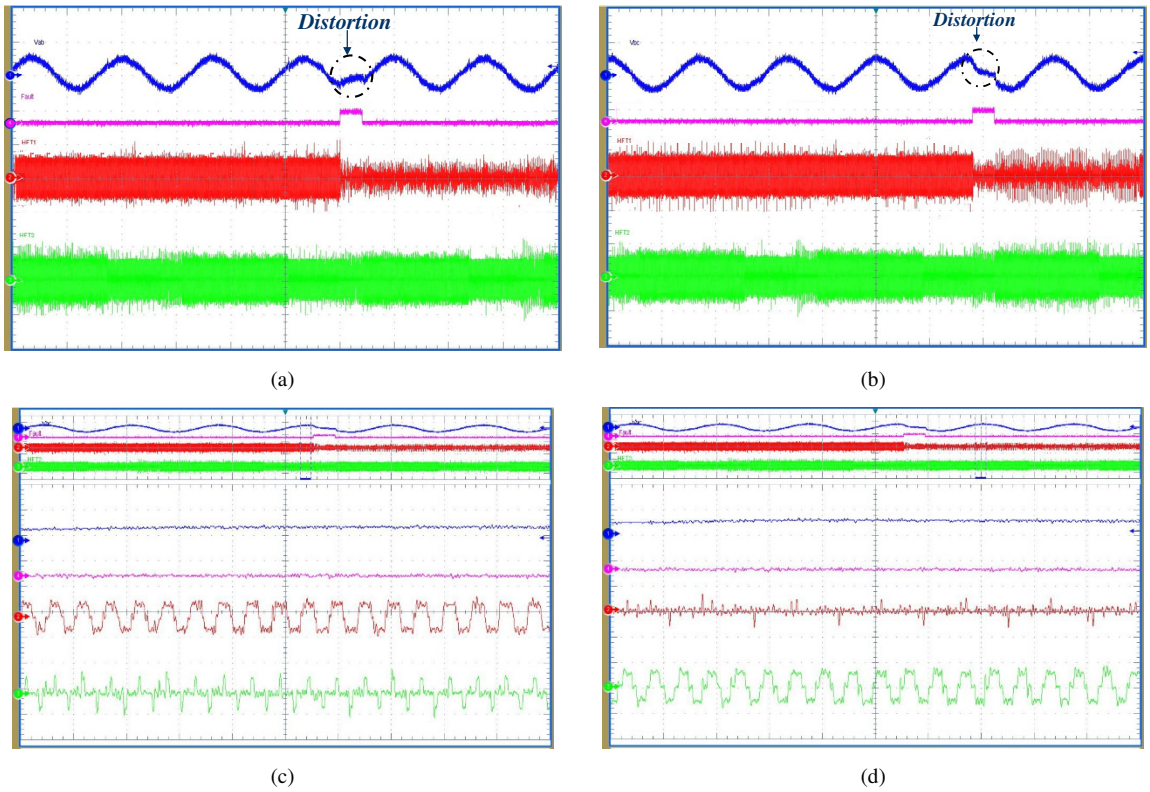


Fig. 49. Fault scenario 2: double-phase outage. (a). V_{AB} , (b). From top to bottom: V_{BC}, signal indicating the onset of failure of one of the Dc/Ac Converter phases at rising edge and the onset of fault-tolerant control action at the trailing edge. Larger view of V_u, and V_v in (c) fault-free operation, and (d) restoration interval.

F. Conclusions

A novel fault-tolerant switching scheme (FTSS) is proposed for all of the three stages in a multi-stage isolated high-frequency-link (HFL) inverter. The proposed FTSS is designed based on the inherent redundancy of one phase in the primary side Dc/Ac Converter and Ac/Pulsating-Dc Converter and is based on changing the PWM references for the remaining full-bridge converters upon detection of the fault using a proposed fault diagnosis system. The new switching scheme provides the continuity of service of the inverter while maintaining acceptable dc-link and output voltages when one or even two phases of the Dc/Ac Converter ceases to generate any output, or when one phase in Ac/Pulsating-Dc Converter or Pulsating-Dc/Ac

Converter fails. Effect of the time (or phase angle) at which a fault happens was discussed and based on a comprehensive analysis of the latter a fault diagnosis algorithm is proposed. In the diagnosis step, the distortion pattern of the three line voltages V_{AB}, V_{BC}, and V_{CA} are diagnosed. As explained in Section III of this chapter, by analyzing the pattern of distortion in each of the three line voltages with six sectors, we can determine the lost phase and the faulty stage. In the next step, based on the type of lost phase(s) and faulty stage, the PWM reference for the remaining phase(s) is changed so as to restore the output line voltages of the inverter. The effectiveness of the FTSS under various fault scenarios was investigated through experimental results on a 1-kW prototype and found to be satisfactory.

IV. OSBC-BASED HYBRID MODULATION OF THE HFL INVERTER OUTPUT STAGE: JOINT-OPTIMIZATION OF SWITCHING LOSS REDUCTION AND VOLTAGE REGULATION / GRID CONTROL

A. Introduction

In Chapter 2, switching-loss reduction was jointly optimized with other goals such as voltage regulation for standalone and grid-connected operating modes of the HFL inverter. In doing so, reduction of the switching frequency for all of the switching devices was considered to be optimized. However, another more general approach is to commutate selectively for some switching devices through selection of appropriate switching sequences rather than reduction of switching frequency for all of the switches. The requirement to realize this is to have the information of the highest line voltage being encoded in the Pulsating-Dc link voltage (V_{REC}) which is achieved through SPWM of the Dc/Ac Converter and rectification of the Ac/Pulsating-Dc Converter.

Hybrid-modulation (HM) principles are discussed in Chapter 3 and is presented in [11],[57]-[61]. HM encodes the information of the highest line voltage in V_{REC} in every sector P_1 to P_6. HM reduces the switching losses in the Pulsating-Dc/Ac Converter by permanently turning on a pair of (top, bottom) MOSFETs in those legs associated with the highest line voltage at each sector. However, this is a heuristic algorithm and not necessarily the optimal one. If we can find

a way to exploit the very powerful optimization tool of OSBC to generate these switching sequences autonomously based on minimization of a predefined cost function, this would be a step forward in the formulation of loss-mitigation techniques even for other HFL topologies beside the one under consideration in this Dissertation.

In this chapter, it is shown that by slightly modifying the cost function used for OSBC-based voltage regulation or grid control, one can reduce switching losses reasonably and almost replicate the HM switching scheme through proper selection of switching sequences for every sectors P_1 to P_6.

B. Methodology

In order to realize the proposed OSBC-based HM, one needs to define the switching functions and switching sequences, capture the model of the HFL inverter, and synthesize the necessary cost function based on the performance objectives. The first step is covered in Chapter two. In there, it is shown that, the isolated multi-stage HFL inverter is modeled using a simplified model consisting of a pulsating-voltage source (containing the information of V_{REC}) connected to a three-phase VSI which operates in standalone and grid-connected modes of operation. This is illustrated in Fig. 50. For the Pulsating-Dc/Ac Converter (modeled in Fig. 50 using a VSI), switching functions S_a, S_b, and S_c are defined for legs generating phase voltages a, b, and c respectively. Based on these switching functions, a set of fundamental switching states and switching sequences (Tables I and II) are defined.

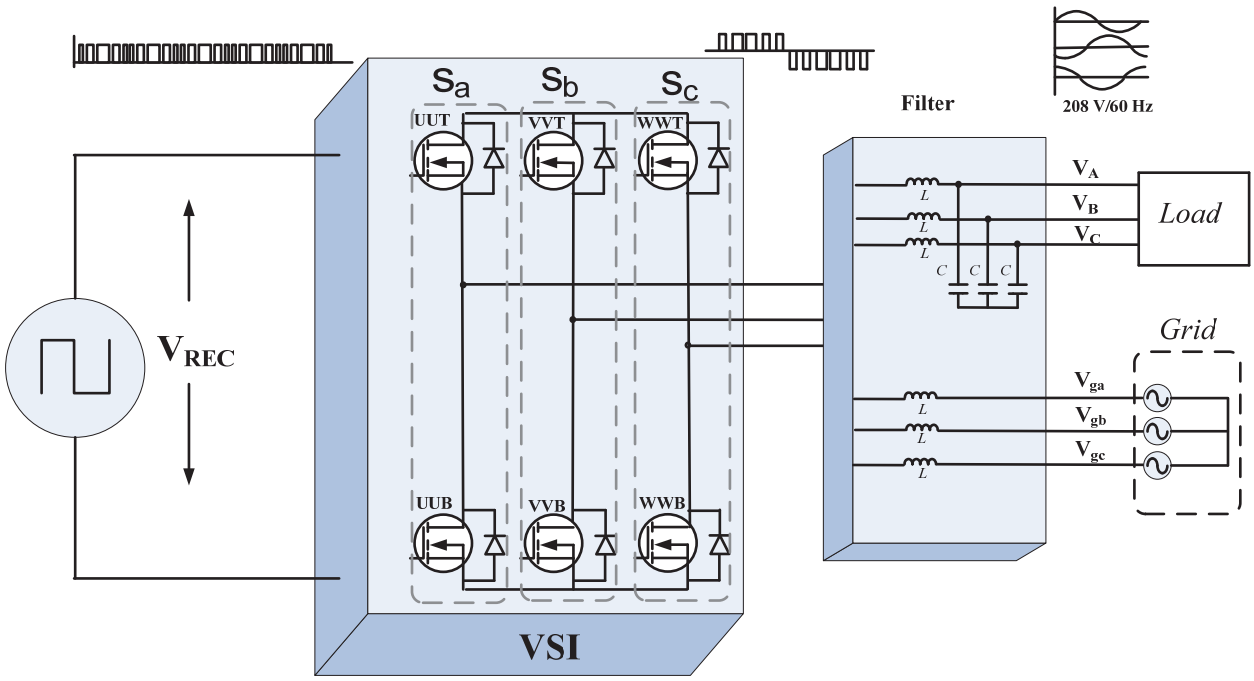
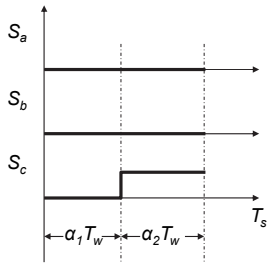
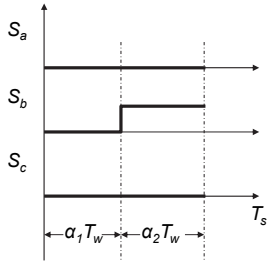
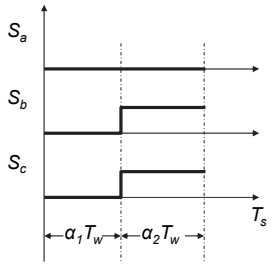
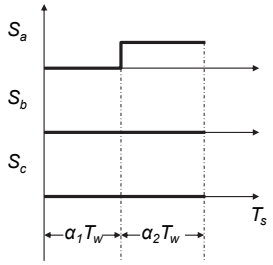
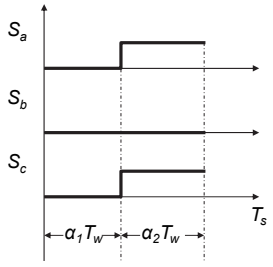


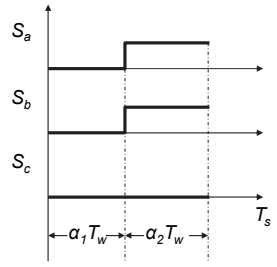
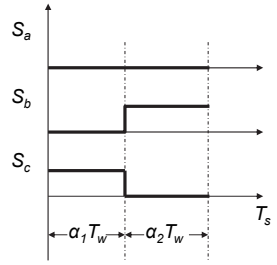
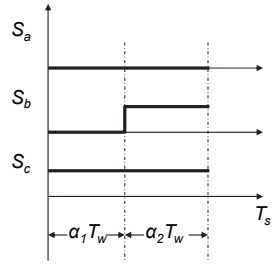
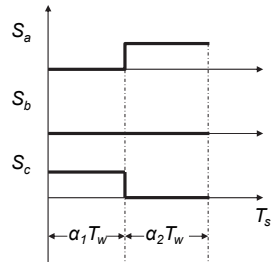
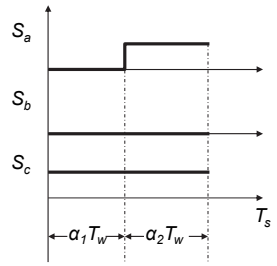
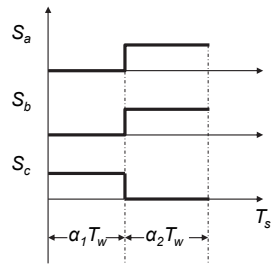
Fig. 50. Simplified topology of HFL inverter used for PWL modeling with reduced number of switching functions.

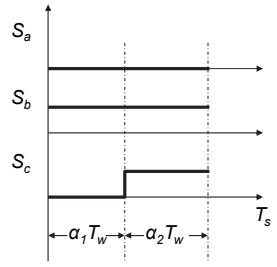
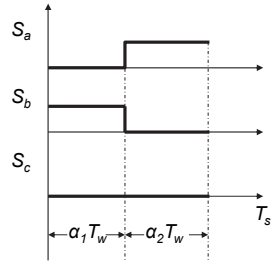
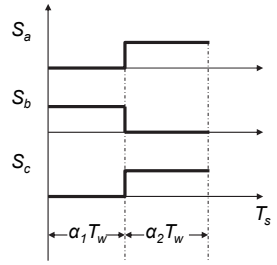
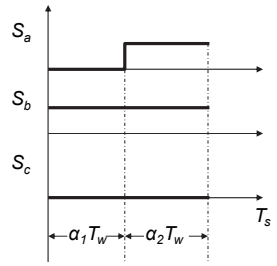
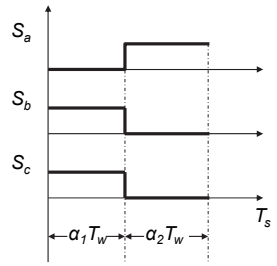
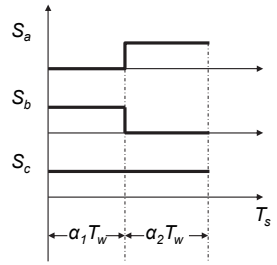
TABLE XII. DEFINITION OF SWITCHING STATES

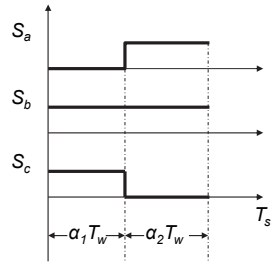
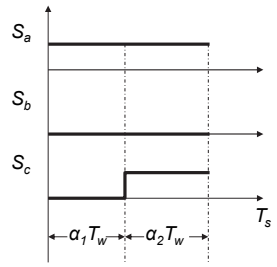
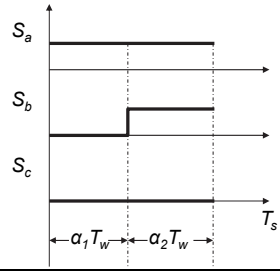
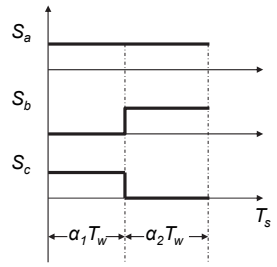
Switching State Number (SSN)	Sa	Sb	Sc
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

TABLE XIII. DEFINITION OF SWITCHING SEQUENCES

Switching Sequence	First Switching State	Second Switching State	Realization
1	1	2	
2	1	3	
3	1	4	
4	1	5	
5	1	6	

6	1	7	
7	2	3	
8	2	4	
9	2	5	
10	2	6	
11	2	7	

12	3	4	
13	3	5	
14	3	6	
15	3	7	
16	4	5	
17	4	6	

18	4	7	
19	5	6	
20	5	7	
21	6	7	

The second step which is modeling was covered in detail in Chapter 2 as well. However, it should be noted that for implementation of the proposed OSBC-based HM, the PWL model of the HFL inverter in stationary reference frame is used for either standalone and grid connected modes of operation. For standalone as well as grid-connected modes of operation the following PWL model is used:

$$\dot{X}_{abc} = A_{abc}X_{abc} + B_{abc} \tag{27}$$

For standalone mode of operation, matrices A_{abc} and B_{abc} are defined as:

$$A_{abc}=\begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix}, B_{abc}=\frac{V_{REC}}{3L}\times B'\times \bar{S}_{abc}, B'=\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad (28)$$

where $\bar{S}_{abc}=[S_a,S_b,S_c]^T$ and $X_{abc}=[i_a,i_{b,}i_c,v_a,v_b,v_c]^T$. For grid-connected mode of operation the PWL model matrices are defined as:

$$A_{abc}=\begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}, B_{abc}=\frac{1}{3L}\times B'\times \bar{S}_{abc}-\overline{V_g}_{abc} \quad (29)$$

where $X_{abc}=[i_a,i_{b,}i_c]^T$ and $\overline{V_g}_{abc}=[\,v_{g_a},v_{g_b},v_{g_c}]^T$.

The next step is to synthesize a suitable cost function. Optimization of this cost function should result in generation of those switching sequences which cause the minimum number of commutations in every sector P_1 to P_6 for MOSFETs in the Pulsating-Dc/Ac Converter. Note that this procedure requires a joint-optimization of a number of goals depending on the mode of operation. For instance, if operating in standalone mode, voltage regulation will be jointly optimized along with switching-loss reduction.

We assume that the switching sequences consist of two switching states, SS1 and SS2. Based on the definition of switching states in Table XII the following logic (written as a pseudo code) could be concluded:

if (SSN1 > 4) S_{a1}=1; else S_{a1} = 0; end

if (SSN2 > 4) S_{a2}= 1; else S_{a2}= 0; end

if (SSN1 == 3) || (SSN1 == 4) | |(SSN1 == 7) S_{b1} = 1; else S_{b1} = 0; end

if (SSN2 == 3) || (SSN2 == 4) || (SSN2 == 7) S_{b2} = 1; else S_{b2} = 0; end

if mod(SSN1, 2) == 0 S_{c1} = 1; else S_{c1} = 0; end

if mod(SSN2, 2) == 0 S_{c2} = 1; else S_{c2} = 0; end

where SSN1 and SSN2 are the corresponding number of the first and the second switching states, and S_{x1} and S_{x2} ($x = a, b, c$) are states of the first and the second switching functions (the first and the second switching states) respectively.

Using the above logic, the first and the second switching states for each and every switching function S_a, S_b, and S_c are determined which equips one with a parameter to be used in the cost function. If the HFL inverter operates in the standalone mode, one may define the cost function for joint optimization of regulation of the load voltage and reduction in the switching loss; that is,

$J = J_{VR} + J_{SLR}$

where $J_{VR} = w_1(v_a^* - v_a)^2 + w_2(v_b^* - v_b)^2 + w_3(v_c^* - v_c)^2$ and

$$J_{SLR} = w_4 \times \hat{L}oss_{SW} \tag{30}$$

where w_1, w_2 w_3 and w_4 are the weighting factors, J_{VR} represent voltage regulation (VR) objective while J_{SLR} represents SLR. Symbol $\hat{L}oss_{SW}$ represents an estimation of switching losses in the Pulsating-Dc/Ac Converter, which was discussed in Chapter 2. In here, we use the same relation with a slight difference to represent the switching losses for all of the MOSFETs in Pulsating-Dc/Ac Converter (Fig. 51 shows the definition of I_D and V_D):

$$\hat{L}oss_{SW} = 0.5 \times I_D \times V_D \times \left(t_{SW(ON)} + t_{SW(OFF)}\right) \times \{(S_{a1} - S_{a2}) + (S_{b1} - S_{b2}) + (S_{c1} - S_{c2}) \tag{31}$$

Note the (31) estimates the switching loss of the Pulsating-Dc/Ac Converter in one switching cycle depending on the switching sequences for each of the three legs. Hence, and for instance, if all of the three legs switch in a switching cycle, the total switching loss of this converter in that

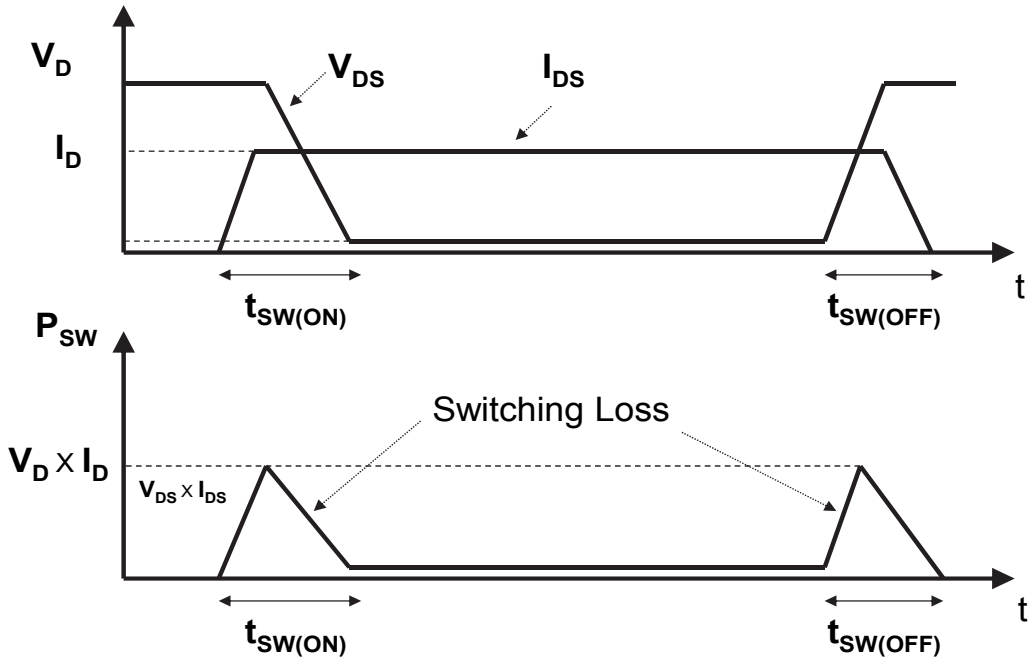


Fig. 51. Illustration of switching loss for a switching device such as a MOSFET.

switching cycle would be equal to $0.5 \times I_D \times V_D \times \left(t_{SW(ON)} + t_{SW(OFF)}\right) \times 3$. However, if OSBC generates such switching sequences so that only one of the three legs does the switching and the other two do not change their states in a switching cycle, the total switching loss of the converter in this switching cycle will be reduced to $0.5 \times I_D \times V_D \times \left(t_{SW(ON)} + t_{SW(OFF)}\right) \times 1$.

This loss mitigation algorithm can be extended to OSBC of a HFL inverter operating in grid-connected mode as well. In the single-objective OSBC, the primary goal is to control the injected power to the grid. By modifying the cost function, OSBC will perform a joint optimization of

grid control as well as switching loss minimization through selection of switching sequences leading to fewer commutations. Such a cost function appears to be of the following form:

$J = J_{GC} + J_{SLR}$ where $J_{GC} = w_1(i_a^* - i_a)^2 + w_2(i_b^* - i_b)^2 + w_3(i_c^* - i_c)^2$ and

$$J_{SLR} = w_4 \times \hat{L}oss_{SW} \tag{32}$$

where w_1, w_2 w_3 and w_4 are the weighting factors, J_{GC} represent grid control (GC) objective while J_{SLR} represents SLR. $\hat{L}oss_{SW}$ is an estimation of switching losses in the Pulsating-Dc/Ac Converter which was discussed earlier in this chapter for standalone mode of operation.

C. Results

The cost function (30) is used to perform a multi-objective OSBC of a HFL inverter operating in standalone mode connected to a 1-kW resistive load (Fig. 50). The goal is to verify that the joint optimization of the VR and SLR leads to generation of switching sequences with a fewer commutations yielding reduced switching loss as compared with single-objective OSBC (VR).

Fig. 52 shows the result of single-objective OSBC algorithm (incorporating J_{VR} cost function in (30)) implemented on the HFL inverter feeding a 1-kW resistive load in standalone mode of operation for one line cycle. For the top and the middle traces, the first and the second switching states (in a two step switching sequence) selected from the search space of Table XIII by OSBC are shown. It is noted that, the green trace show the switching states of the hybrid modulation scheme described in the introduction. The bottom trace shows the three-phase output voltages. Also note that there is just a little commonality between these switching states and those of the hybrid modulation.

Fig. 53 shows the same set of results (as in Fig. 52) but using a multi-objective OSBC cost function ($J = J_{VR} + J_{SLR}$). It is noted that, the first and the second switching states obtained using the multi-objective OSBC and those of the hybrid modulation scheme (shown in green) have commonality. Hence, the total switching losses are reduced by a rate of 54% as compared with the hard-switching schemes using sine-wave PWM (SPWM). The rate of switching loss

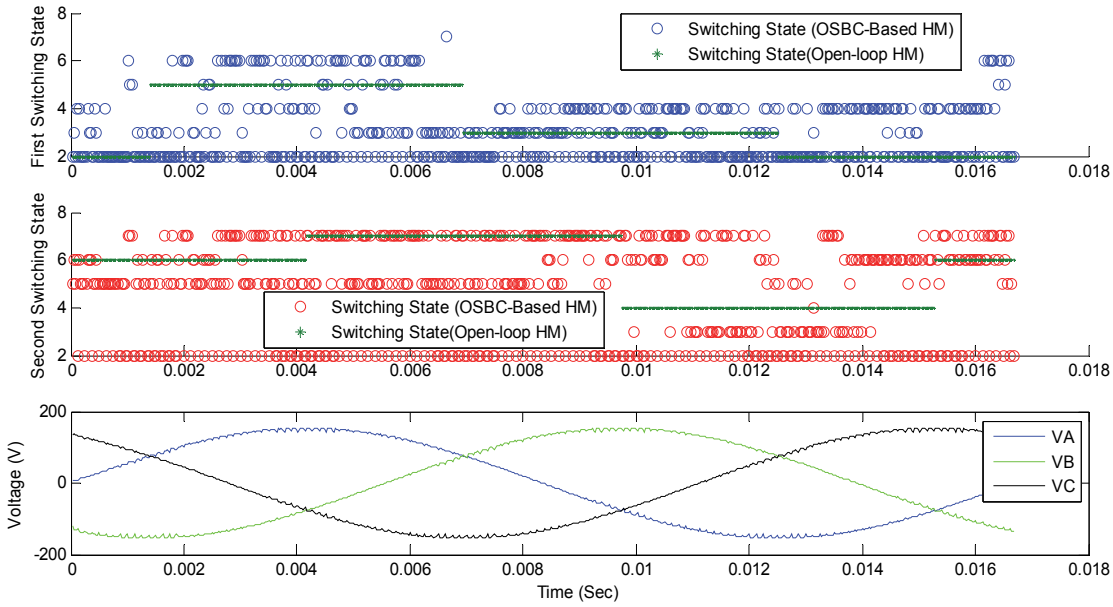


Fig. 52. Single-objective OSBC (VR) for standalone mode of operation of the HFL Inverter shown in Fig. 50 with a 1 kW load. (Top). The first switching sequence for a period of $\propto_1 T_W$, (middle). The second switching sequence for a period of $\propto_2 T_W$, (bottom). Three phase output voltages.

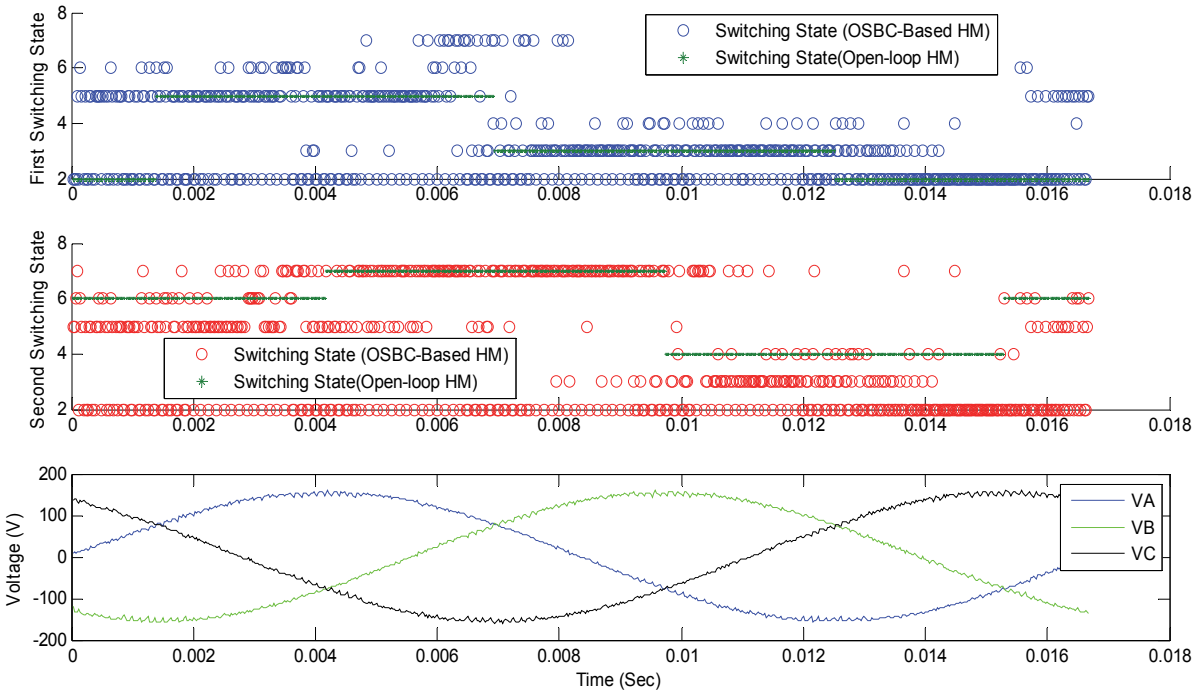


Fig. 53. Multi-objective OSBC (VR+SLR) for standalone mode of operation of the HFL Inverter shown in Fig. 50 with a 1 kW load. (Top). The first switching sequence for a period of $\propto_1 T_W$, (middle). The second switching sequence for a period of $\propto_2 T_W$, (bottom). Three phase output voltages.

reduction in Fig. 52 (using single-objective OSBC algorithm incorporating J_{VR} cost function in (30)) is 34%.

The same set of results is taken for the HFL inverter operating in the grid-connected mode of operation feeding 1-kW active power to the grid. Control is achieved using a single-objective OSBC algorithm incorporating J_{GC} cost function versus a multi-objective OSBC algorithm incorporating $J_{GC} + J_{SLR}$ cost function in equation 32. Fig. 54 shows the results of single-objective OSBC while Fig. 55 shows the results of multi-objective OSCB. Note that as Fig. 55 shows, there is a remarkable rate of coincidence between the first and the second switching states obtained using the multi-objective OSBC and those of the hybrid modulation scheme (shown in green). As a result, the total switching losses are reduced by a rate of 40% as compared with the hard switching schemes such as sine pulse width modulation (SPWM). The rate of switching loss

reduction in Fig. 54 (using single-objective OSBC algorithm incorporating J_{GC} cost function in (30)) is less than 15%.

Fig. 56 gives a comparison of the switching-loss reduction rates using SPWM, single-objective OSBC and multi-objective OSBC for the HFL inverter of Fig. 50 operating in standalone and grid-connected modes.

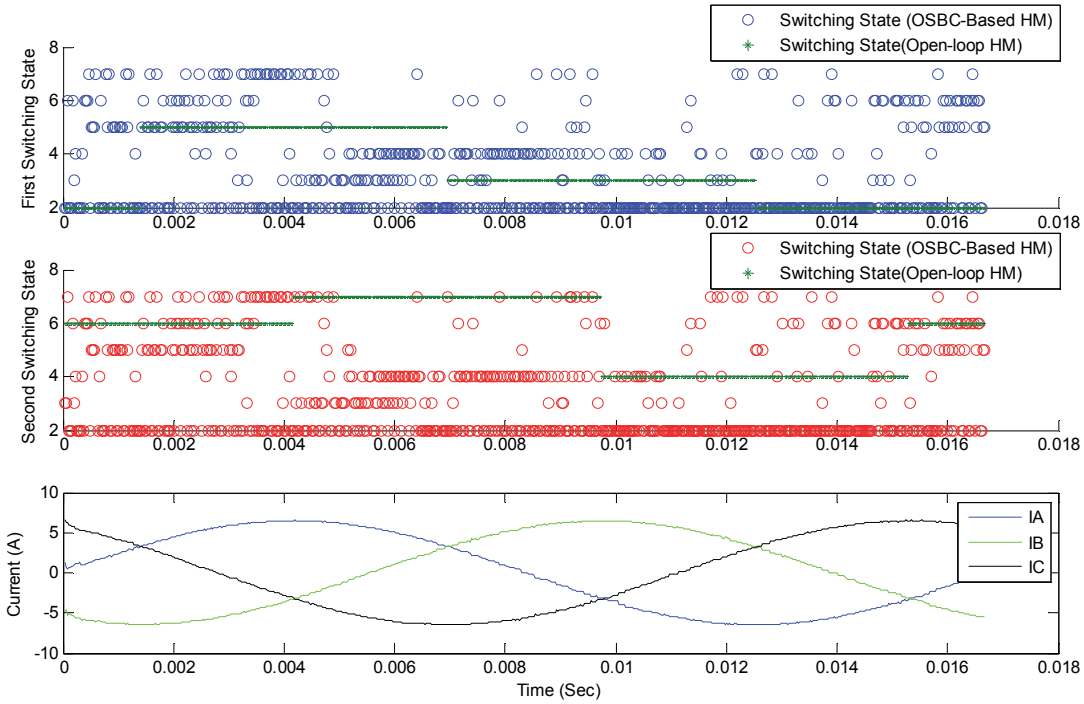


Fig. 54. Single-objective OSBC (GC) for grid-connected mode of operation of the HFL Inverter shown in Fig. 50 feeding 1 kW active power to the grid. (Top). The first switching sequence for a period of $\propto_1 T_W$, (middle). The second switching sequence for a period of $\propto_2 T_W$, (bottom). Three phase output currents.

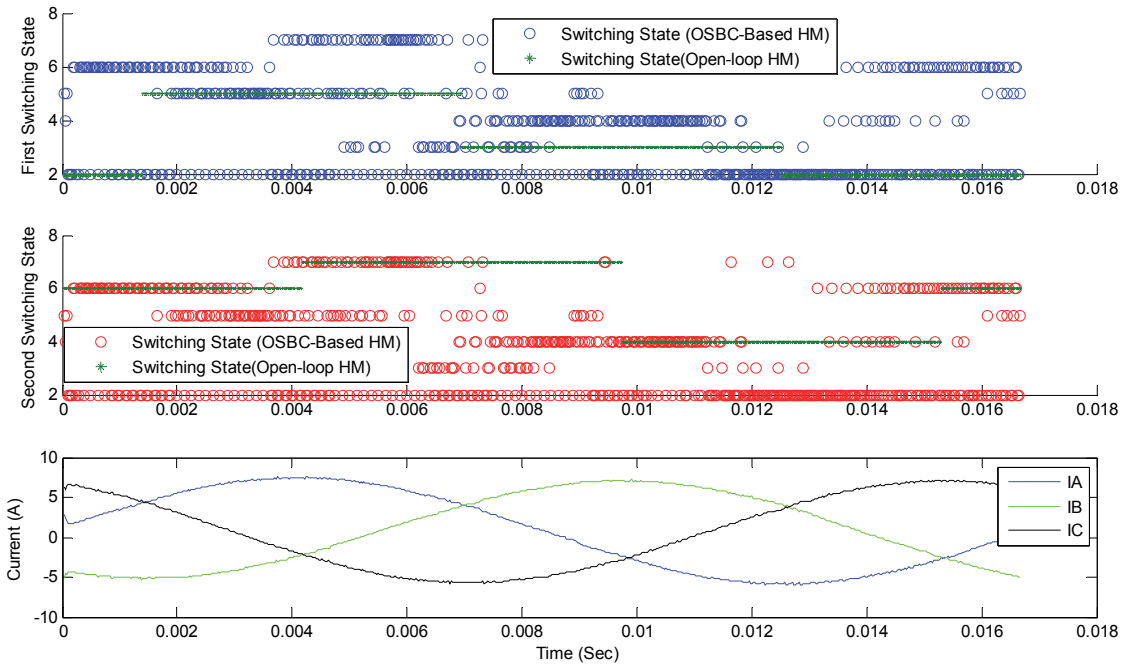


Fig. 55. Multi-objective OSBC (GC+SLR) for grid-connected mode of operation of the HFL Inverter shown in Fig. 50 feeding 1 kW active power to the grid. (Top). The first switching sequence for a period of $\propto_1 T_W$, (middle). The second switching sequence for a period of $\propto_2 T_W$, (bottom). Three phase output currents.

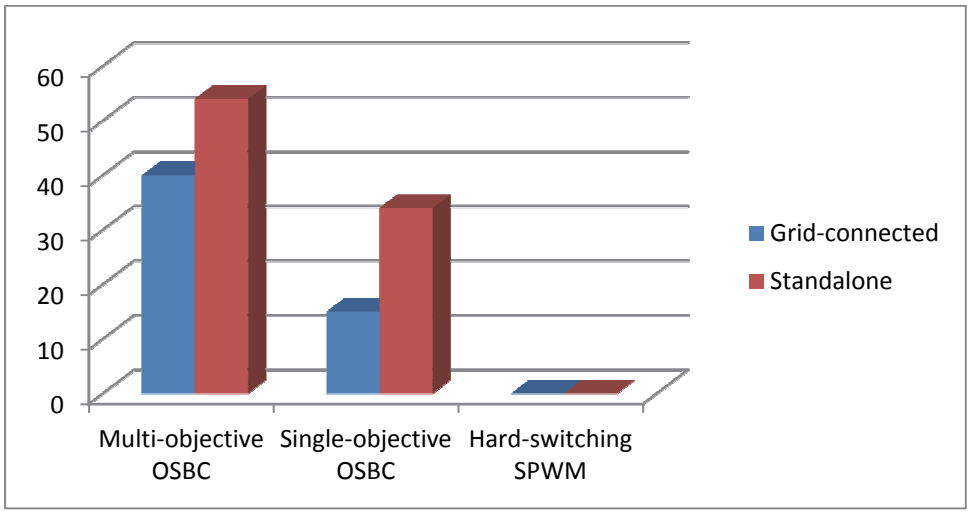


Fig. 56. Percent of switching-loss reduction using hard-switching SPWM, single-objective OSBC, and multi-objective OSBC for the HFL Inverter of Fig. 50 operating in standalone and grid-connected modes.

D. Conclusions

A switching-loss reduction (SLR) scheme is proposed for a HFL inverter represented as a VSI powered by a pulsating-dc input voltage source containing the information of the highest line. The SLR scheme is based on a multi-objective OSBC. Depending on the mode of operation, the primary control goal as foreseen in the single-objective OSBC (i.e., VR in standalone and GC in grid-connected mode of operation) is joint optimized with a SLR control goal. The mechanism to realize this SLR algorithm is to minimize the number of commutations in the switching devices of the VSI while controlling the output voltage / injected current into the grid in standalone/grid-connected mode of operation. It was shown through relevant results that using this SLR scheme, the switching losses can be reduced up to 54% as compared with hard-switching techniques such as SPWM. This percentage of SLR is still a bit less than 67% rate obtained using the heuristically developed hybrid modulation which can be increased by modifying the computer code. However, the main advantage of this methodology is the preclusion of the need to analyze the switching patterns of the Pulsating-Dc/Ac Converter and in its capability to be applicable for other HFL converter topologies.

V. CONCLUSIONS AND FUTURE WORK

A. Conclusions

In this Dissertation, an isolated multi-stage high-frequency-link (HFL) inverter is considered as one of the most suitable candidate topologies for interfacing renewable energy sources to the standalone load / utility grid. Such an inverter yields high power density as a direct result of removing the bulky dc-link capacitor, modular design, fault-tolerance operability, and high efficiency. However, removal of a bulky dc-link capacitor leads to the following challenges:

1- Lack of an intermediate buffer stage between different power stages of the HFL inverter results in an overlap among control actions implemented in different stages;
2- Stiffness of the HFL inverter is reduced against source / load transients because there is no temporary energy storage such as a bulky dc-link capacitor.

Hence, in order to take the full advantage of this topology for renewable energy applications, the above issues need to be addressed properly. Regarding the above challenges, note that:

1- The potential solution to implement different control objectives effectively in such a buffer-less multi-stage topology needs an optimization-oriented algorithm;
2- A high-bandwidth power conversion is required to provide fast enough dynamic response for the power stage. However, this requires a high switching frequency which also increases the switching losses and degrades the efficiency of the HFL inverter.

To support the first point, an optimal control was chosen. Considering the second point, instead of increasing the switching frequency / losses, another approach is to control the

switching sequence of the inverter in such a way so that optimal dynamic response is achieved for a given switching frequency.

In order to realize such a controller:

a) Instead of using an average model of the HFL inverter, a PWL model was proposed which retains the fast-scale parameters of the power-conversion system;
b) Instead of a two-step implementation (i.e., controller / modulator), a single-stage approach integrating the control and modulation blocks is chosen. Such a closed-loop controller does not need a predefined modulation scheme and hence the switching sequence can be generated on the fly simply based on a single or multi-objective cost function;
c) Using the proposed PWL model of the HFL inverter, the unified controller / modulation approach is implemented in an optimization framework referred to as the OSBC.

A comprehensive study on the proposed OSBC algorithm based on the PWL model of a HFL inverter operating under standalone as well as grid-connected modes of operation is provided. In essence, the discontinuous modeling which is a part of OSBC retains both the fast-scale as well as the slow-scale dynamics which in turn makes it possible to control multi-scale parameters at the same time through a predefined optimization algorithm. This results in a superior dynamic performance of the OSBC controller as compared to traditional linear controllers that are designed based on averaged modeling approach. Another inherent capability of OSBC as verified is the possibility of multi-objective control which is due to the optimization nature of OSBC algorithm. This feature is found in MPC algorithm as well. However, the main and the biggest advantage of OSBC over MPC and sliding-mode control is restriction of the search space

to only reachable switching sequences using a composite-Lyapunov function (CLF). This feature enables OSBC controller to change the switching sequences with varying operating mode dynamically under stability bound. Further, the reduction of the search space leads to a reduced time for the execution of optimal control loops.

Although a superior dynamic response and multi-objective control algorithm is developed for the HFL inverter and effectiveness of the OSBC is verified, all of these achievements are attained only if a reliable operating condition is provided for the power-conversion system. As such, a novel fault-tolerant switching scheme (FTSS) is proposed for all of the three stages of the multi-stage isolated HFL inverter so as to justify that the proposed unified controller can operate even if there is fault in any stage of the HFL inverter. The FTSS is designed based on the inherent redundancy of one phase in the primary side Dc/Ac Converter and Ac/Pulsating-Dc Converter and ensures reliable operation by changing the PWM references for the remaining full-bridge converters upon onset of fault. FTSS provides the continuity of service of the inverter while maintaining acceptable dc-link and output voltages when one or even two phases of the Dc/Ac Converter ceases to generate any output, or when one phase in Ac/Pulsating-Dc Converter or Pulsating-Dc/Ac Converter fails. The effectiveness of the FTSS under various fault scenarios is investigated using experimental results on a 1-kW prototype and found to be satisfactory.

Finally, a switching-loss-reduction (SLR) scheme is synthesized for the same HFL inverter by representing it as a VSI fed by a pulsating-dc input voltage source. This SLR scheme is based on a multi-objective OSBC. Depending on the mode of operation, the primary control goal as captured in the single-objective OSBC is jointly optimized with the SLR control goal. The mechanism to realize this SLR algorithm is to minimize the number of commutations in the

switching devices of the VSI while controlling the output voltage / injected current into the grid in standalone / grid-connected mode of operation. It was shown through relevant results that using this SLR scheme, the switching losses can be reduced up to 54% as compared with hard-switching techniques such as SPWM. This percentage of SLR is still a bit less than 67% rate obtained using the heuristically developed hybrid modulation. However, unlike the latter, there is no need to analyze the switching patterns of the Pulsating-Dc/Ac Converter.

B. Future Work

As an extension to the work presented in this Dissertation, a PWL model of the primary-side Dc/Ac Converter can be modeled using its switching functions and incorporated to the overall model for the HFL inverter. However, algorithms and techniques need to be developed to reduce the search space because using a complete PWL model for all of the stages of the HFL inverter increases the search space surprisingly. Having derived such a model, many other possibilities such as combination of switching sequences on the primary-side Dc/Ac Converter and secondary-side Pulsating-Dc/Ac Converter can be incorporated in the OSBC. Regarding the SLR scheme, such a complete PWL model can possibly result in achieving more efficient SLR algorithms using a combination of switching sequences on the primary-side Dc/Ac Converter and secondary-side Pulsating-Dc/Ac Converter. Also, the proposed SLR scheme can be designed and implemented on other HFL energy conversion topologies. Finally, throughout the various chapters of this Dissertation, mainly the fundamental switching sequences are being incorporated for control optimization. As a subsequent step, one can explore mutated switching sequences

which are combinations of the fundamental switching sequences used in this work to implement the OSBC.

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