Switching Transition Control of Insulated-Gate Power Semiconductor Devices

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THESIS

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This thesis is dedicated to my mother “Mandana” who was my true support from the first day in school, my father “Nader”, my brother “Farid”, my grandfather “Baba Bahram”, my grandmother “Maman Feri” who always provide me continuous love and support. Finally, and most importantly, I would like to dedicate my thesis to my wife “Sayeh” for her support, encouragement, quiet patience and unwavering love. She is truly the best gift I have received in my life. Thank you for being my best friend. I owe you everything!

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LIST OF ABBREVIATIONS

PSD	Power Semiconductor Device
OTPT	Optically Switched Power Transistor
HF	High Frequency
HV	High Voltage
EMI	Electro-magnetic Interference
EMC	Electro Magnetic Compatibility
SMPS	Switched-mode Power Supply
CM	Common Mode
DM	Differential Mode
PWM	Pulse Width Modulation
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ET	Electrically Triggered
OT	Optically Triggered
PLL	Phase-locked Loop

SUMMARY

As the industry demands move toward more compact and high-power-density applications, it is desirable to increase the switching frequency of the power semiconductor devices (PSDs) to reduce the size and cost of the passive elements. On the other hand, increasing the switching frequency results in higher switching loss in PSDs. Therefore, voltage and current slopes during the switching transitions need to be increased to decrease the duration of the switching transition and switching loss. However, adverse current and voltage slopes during the switching transitions are the main sources of the noise, EMI issues and switching stress such as over current and overvoltage. Consequently, a solution to empower one to gain an optimal performance in terms of switching loss, device stress and EMI is desirable.

Several EMI and stress reduction techniques have been introduced in the literature to mitigate the undesirable affect of high *di/dt* and *dv/dt*. Those approaches include but not limited to: Active and passive clamps, snubber circuits, Active and passive EMI filters and soft switching techniques. The main drawbacks of the above-mentioned approaches are adding additional bulky and expensive passive and/or active devices to the power circuit, modification of the original topology and complexity of the control.

Active and passive gate drive (or switching transition control) techniques are used to control EMI, device stress and switching losses by shaping the current and voltage slopes of the switching transitions of a PSD. In contrast to previously mentioned EMI and stress reduction techniques, switching transition controllers are placed in the control and gate drive stages and do not need any change in the original topology of the power circuit. Active gate drive circuits are controlling the *di/dt* and/or *dv/dt* of turn-off and/or turn on switching transitions of PSDs to gain the optimal performance regarding EMI, device stress and switching losses. The main limitations of the state

of the art switching transition controllers are lack or limited adjustability of *di/dt* and *dv/dt*, and lack or limited ability to independently control *di/dt*, *dv/dt* and delay to gain an optimal performance in terms of loss, device stress and EMI.

This dissertation outlines novel optical-based and electrical-based switching transition controllers for insulated gate power semiconductor devices such Si and SiC MOSFETs and IGBTs. The main advantage of the proposed controllers is unified independent control of *di/dt* and *dv/dt* of turn-on and turn-off switching transition. This feature gives more degree freedom to designer in different applications to gain an optimal performance regarding the switching loss, device stress and EMI noise. The other unique feature of the optical-based controllers is using optical beam to trigger and control the switching transition of PSDs that reduces the susceptibility to the external noise.

Initially an optical-based two level switching transition controller is outlined. This controller is able to independently control the turn-off *di/dt* and *dv/dt* of the power MOSFETs by adjusting the optical intensity in each region of control. Independent controllability of turn-off *dv/dt* and *di/dt* is guaranteed by predicting the onset of transition between the regions of control considering the optical-to-electrical and circuit propagation delays. Subsequently, an electrical switching transition controller is presented for high speed SiC MOSFETs. This controller adjusts the di/dt and *dv/dt* of the turn-off switching transition by closed-loop control of the gate current. It independently control the very fast *di/dt* and *dv/dt*s of the SiC MOSFET by predicting the onset of transition between *dv/dt* and *di/dt* control regions. Finally, an optical-based four-level switching transition controller is outlined that is able to independently control the delay, *di/dt*, *dv/dt* and voltage tail of the turn-on transition of the IGBTs. This controller comprises of three control

blocks that predict the onset of transition between the four control regions. Each control parameter can be controlled individually by adjusting the optical intensity in that region.

I. Introduction

Insulated gate power semiconductor devices (PSDs), such as IGBT and MOSFET, are widely used in hard-switched power electronics applications with a broad range of power rating and applied voltage. These hard-switched applications include switched mode power supplies (SMPS), motor drives, solar inverters, and battery chargers [1]-[4]. As the industry moves toward to higher frequencies to increase the power density, the switching loss increases. Therefore, it is desirable to increase the voltage and current slopes (*dv/dt* and *di/dt*) of the switching transition to decrease the switching loss. However, adverse voltage and current slopes cause excessive device stress and electro-magnetic interference (EMI) because of the parasitic elements of the PSD and power circuit.

International standards for electromagnetic compatibility (EMC) require power electronics converters to meet certain noise levels [5]-[8]. Furthermore, EMI noises may cause a malfunction in the control circuit of the power converter or other sensitive electronic devices. High *dv/dt* and *di/dt* during switching transition are the main sources of EMI in power electronics circuits. EMI noises generated by the power electronics converters are categorized as conducted and radiated noises [9]. Conducted noise is propagated through circuit wires and interconnections while radiated noise is spatially propagated. High *dv/dt* is the primary source of the common mode (CM) noise which causes a displacement current in the parasitic capacitances of the circuit. This displacement current causes imbalance and fluctuation of the reference ground as well as shortening the life of machine bearing and stator insulation[10]. On the other hand, high *di/dt* generates differential mode (DM) noise. High *di/dt* current loops in the circuit are also responsible for the radiated EMI [5]. Furthermore, high *di/dt* causes voltage overshoot at turn-off transition of

the PSD, because of parasitic and/or leakage inductances in the commutation path. Moreover, it generates current overshoot at turn-on transition due to reverse recovery action of the freewheeling diode.

Several EMI reduction techniques have been introduced in the literature. Active and passive snubber circuits are employed to reduce the voltage and current slopes and diminish the EMI noise and device stress. However, additional active and/or passive components are needed in the power stage. Additional components in the power stage usually increase the size, cost, complexity and loss of the circuit. [11],[12]. Active Clamp circuits are implemented to decrease the device overvoltage and consequent high-frequency ringing in the turn-off transition [13]. However, these approaches are ineffective when the CM-EMI-noise reduction is needed. Also, they require additional passive devices as well as additional active PSDs in the power stage. Needless to say that, additional gate drive stages and control circuits are needed to drive the additional PSDs. Another approach to decrease conducted EMI noise is using active and passive EMI filters [14], [15]. Similar to previous methods in [11]-[13], EMI filters usually decrease the power density and increase the volume and weight of the circuit. This drawback is because of using additional components in the power circuit, especially bulky and costly inductors. Moreover, EMI filters are incapable of decreasing the device stress. Soft switching techniques are interesting ways to decrease EMI noise as well as the device stress and switching loss [16],[17]. They are categorized as zero voltage switching (ZVS) and zero current switching (ZCS). However, the ZVS technique is usually not realizable in light loads in power electronic converters rather than resonant converters. Also, these techniques usually require modification in the power stage as well as the control techniques, which increases the size and cost of the circuit and make the control more difficult. Soft switching techniques are usually successful to mitigate the EMI

noise. However, employing soft switching techniques in some topologies does not lead to a significant reduction of EMI noise to meet the EMC standards [18], [19]. Other approaches like parasitic cancellation [20], interleaving [21], balance approach [22], grounding and shielding [5], [9]are also proposed in the literature. However, the main downsides of these EMI and stress reduction techniques that modify the power stage are: added passive and active power-rated components that increase the cost and weight and control complexity of the original hard-switched converter.

Active and passive gate drive (or switching transition control) techniques are used to control EMI, device stress and switching losses by shaping the current and voltage slopes of the switching transitions of a PSD. In contrast to previously mentioned EMI and stress reduction techniques that require modifications and/or additional devices in the power stage, switching transition controllers are placed in the control and gate drive stages and do not need any change in the original topology of the power circuit. Active gate drive circuits are controlling the *di/dt* and/or *dv/dt* of turn-off and/or turn on switching transitions of PSDs to gain the optimal performance regarding EMI, device stress and switching losses.

A. Switching Transition Control of Insulated Gate PSDs

1. Inductive Load Switching of Insulated Gate PSDs

Most of the PSDs in the power electronics circuits are used under the inductive load. Fig. 1. shows the equivalent circuit of the clamped-inductive circuit using a simple IGBT model. Parasitic inductances of DC-link, Busbar and collector of the IGBT are summed and shown as L_S. L_σ corresponds the inductance seen from emitter terminal of the IGBT. Following we will derive the equations for the *di/dt* and *dv/dt* of the IGBTs in turn-on and turn-off transitions. It is noted

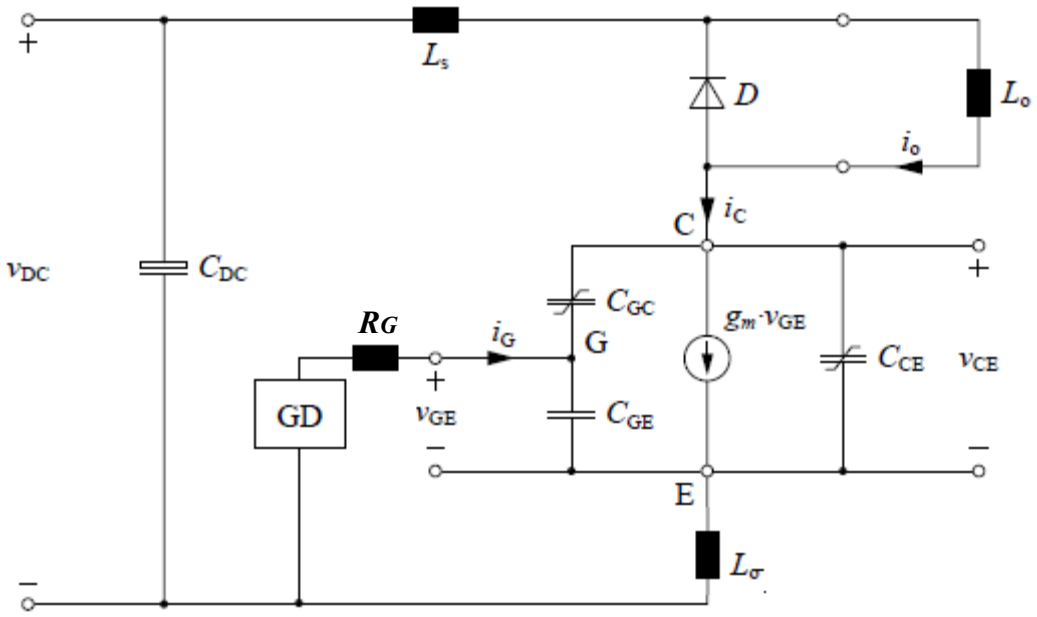


Fig. 1. Equivalent circuit of the clamped-inductive circuit using a simple IGBT model.

that, in the remaining paper, the terms *dv/dt* and *di/dt* are used to represent the rate of change of voltage across and the rate of change of current through a general PSD. While, dv_{DS}/dt and di_D/dt are used to represent the rate of change of voltage across and the rate of change of current through a power MOSFET, and dv_{ce}/dt and di_c/dt are used to represent the rate of change of voltage across and the rate of change of current through an IGBT.

Collector current and gate voltage of an IGBT are related by the following equation:

$$i_c = g_m . v_{GE} \tag{1}$$

In (1), i_c is the collector current of the IGBT, while g_m is the forward transconductance of the IGBT and v_{GE} is the gate-to-emitter voltage of the IGBT. Therefore, di_c/dt is derived by the following relation:

$$\frac{di_c}{dt} = \frac{dv_{GE}}{dt} . \left(g_m + v_{GE} \frac{dg_m}{dv_{GE}} \right) \tag{2}$$

Neglecting the term $(v_{GE} . dv_{GE}/dg_m)$, di_c/dt can be approximated as:

$$\frac{di_c}{dt} = \frac{dv_{GE}}{dt}. g_m = \frac{i_G}{C_{GE}} . g_m \quad (3)$$

In (3), C_{GE} is the gate to emitter capacitance of the IGBT, and i_G is the gate current of the IGBT. Based on (1-3), di_c/dt can be controlled by adjusting the gate current. In the turn-off transition, gate current is derived by writing the KVL in the gate loop:

$$i_G = -\frac{v_{GE}+L_\sigma.(di_C/dt)}{R_G} \quad (4)$$

In (4), R_G is the gate resistance. The gate-to-emitter voltage of the IGBT is approximated using the following equation:

$$v_{GE} = v_{th} + i_c/g_m \quad (5)$$

In (5), v_{th} is the gate threshold voltage. Using (1-5) and (1-4) in (1-3), In (1-3), di_c/dt can be approximated using the following equation during the turn-off transition of IGBT:

$$\frac{di_c}{dt} \approx -\frac{(v_{th}+i_C/2.g_m)}{R_G.C_{GE}/g_m+L_\sigma} \quad (6)$$

In a similar manner the turn-off di_D/dt of power MOSFETs is expressed using the following equations:

$$\frac{di_D}{dt} = \frac{i_G}{C_{GS}} . g_{fs} \quad (7)$$

$$\frac{di_D}{dt} \approx -\frac{(v_{th}+i_D/2.g_{fs})}{R_G.C_{GS}/g_{fs}+L_\sigma} \quad (8)$$

In (7), C_{GS} is the gate-to-source capacitance of the MOSFET, and g_{fs} is the forward transconductance of MOSFET. Similarly, the turn-on *di/dt* of IGBT and MOSFET are respectively derived in (9) and (10):

$$\frac{di_c}{dt} \approx \frac{v_G-(v_{th}+i_C/2.g_m)}{R_G.C_{GE}/g_m+L_\sigma} \quad (9)$$

$$\frac{di_D}{dt} \approx \frac{v_G-(v_{th}+i_D/2.g_{fs})}{R_G.C_{GS}/g_{fs}+L_\sigma} \quad (10)$$

The *dv/dt* of IGBT can be expressed by the following equation:

$$\frac{dv_{ce}}{dt} = -\frac{i_G}{C_{GC}} \quad (11)$$

In (11), C_{GC} is the gate-to-collector capacitance of the IGBT. In the inductive load switching of the IGBT, the current passing through IGBT is almost fixed during the voltage rise and voltage fall intervals. Therefore, one can neglect the term $L_\sigma.(di_C/dt)$ in (4). Hence, the voltage slopes of the IGBT in turn-on and turn-off transitions are, respectively, shown by the following equations:

$$\frac{dv_{ce}}{dt} = -\frac{v_G-(v_{th}+i_c/g_m)}{C_{GC}.R_G} = -\frac{v_G-V_{Miller}}{C_{GC}.R_G} \quad (12)$$

$$\frac{dv_{ce}}{dt} = \frac{(v_{th}+i_c/g_m)}{C_{GC}.R_G} = \frac{V_{Miller}}{C_{GC}.R_G} \quad (13)$$

In (12) and (13), V_{Miller} is the Miller voltage. In the same manner, the voltage slopes of the MOSFET are, respectively, derived for turn-on and turn-off transitions as follows:

$$\frac{dv_{DS}}{dt} = -\frac{v_G-(v_{th}+i_D/g_{mfs})}{C_{GD}.R_G} = -\frac{v_G-V_{Miller}}{C_{GD}.R_G} \quad (14)$$

$$\frac{dv_{DS}}{dt} = \frac{(v_{th}+i_c/g_m)}{C_{GD}.R_G} = \frac{V_{Miller}}{C_{GD}.R_G} = \frac{i_G}{C_{GD}} \quad (15)$$

High *di/dt* at turn-off causes an overvoltage across the PSD. This overvoltage is because of the parasitic and/or leakage inductances in the commutation path. The amount of overvoltage is derived by the following relation:

$$\Delta v_{ov} = (L_\sigma + L_s).di/dt \tag{16}$$

The peak reverse-recovery current (IRR_{peak}) of the free-wheeling diode (FWD) is also a function of the current slope, temperature (T) and load current(I_{L0}):

$$IRR_{Peak} = (\frac{di}{dt})^{1/2}.f(I_{L0},\mathrm{T}) \tag{17}$$

2. Passive Gate Drives

Passive gate drive techniques are using additional passive components in the gate drive circuit of a PSD. Commonly, they use an additional gate resistance or add an external capacitor in parallel to the gate-to-collector and/or gate-to-emitter parasitic capacitances of an IGBT (gate-to-drain and/or gate-to-source parasitic capacitances of a MOSFET). Increasing the gate resistance, decreases the voltage and current slopes and diminishes the EMI noise as well as device stress. However, it results in higher switching loss. Putting an additional capacitor in parallel with the Miller capacitance of a PSD, increases the total Miller capacitance. Therefore, the *dv/dt* of the switching transition and CM EMI noise decreases while there is no change in the *di/dt*. Although the method of increasing the Miller capacitance has less switching loss as compared to the approach of increasing the gate resistance, but it imposes more device stress in turn-off transition. The higher device stress is because of the higher *di/dt* of this method that results in more voltage overshoot and/or high frequency oscillation due to parasitic inductances in the commutation path.

The *di/dt* can be limited by adding a capacitance in parallel to the gate-to-emitter capacitance of an IGBT [23]. However, the turn-on delay and gate driver losses are increased because of the larger amount of the gate-to-emitter capacitance.

Passive transition control techniques do not have any adjustability in the control of the *dv/dt* and *di/dt*. Therefore, dynamic optimization of the switching performance in terms of EMI, device stress and switching losses is not possible in the operating range of a PSD. Hence, Active gate drive techniques have been introduced in the literature to dynamically control the switching transition of a PSD. Active gate drive techniques are generally classified in three categories: controlling the gate resistance, controlling the gate voltage and controlling the gate current.

3. Switching Transition Control by Controlling the Gate Resistance

Simplified concept of switching transition control by controlling the resistance of the gate is shown in Fig. 2. Takizawa *et al*.[24], have employed switchable gate resistors to control the turn-on and turn-off transition of an IGBT. As the turn-on command is received by the gate drive circuit, the gate is charged by maximum current through a low impedance path provided by two parallel resistors. Therefore, the turn-on delay is decreased. As soon as the collector current begins to rise, one of the resistors is taken out of the charging path. Hence, the gate resistance increases and *di/dt* and peak reverse recovery current decreases. At the end of the current rise interval and start of the voltage fall interval, the deactivated resistive path is activated again. Hence, the gate of the IGBT is charged by maximum current, *dv/dt* is increased and switching loss is decreased. The positive *di/dt* value is sensed by the gate driver and one of the resistive paths is deactivated just in the current rise interval. The same concept is implemented for the turn-off transition. The gate is charged by the maximum current through two parallel resistors in the turn-

off delay and voltage rise intervals. Afterwards, one of the resistive paths is deactivated during the current fall interval. As a result, the turn-on delay and *di/dt* are decreased while the *dv/dt* is increased. Consequently, the switching losses, EMI noise generated by high *di/dt* and peak overvoltage are all diminished. However, this method is not able to adjust the *dv/dt* and *di/dt*. Therefore, the optimal switching performance in terms of loss, EMI and device stress is not granted using the proposed methods in [24].

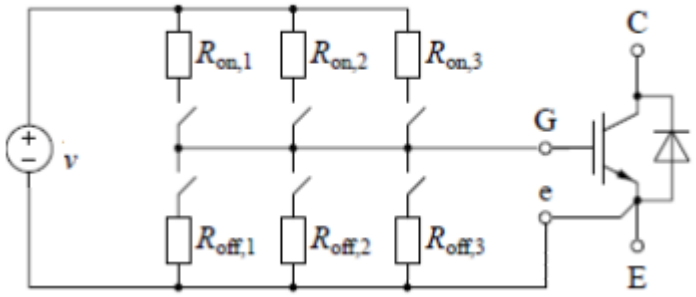


Fig. 2. Simplified concept of switching transition control by controlling the gate resistance

A similar concept has been used for the turn-off transition of the power MOSFETs in [25]. In this scheme, a low impedance path is provided for the discharging path of the gate of a power MOSFET during the turn-off delay and voltage rise intervals. This low impedance path decreases the turn-off delay and increases the turn-off *dv/dt* to decrease the turn-off switching losses. The drain current of the MOSFET falls when the voltage reaches the bus voltage. The low impedance path is deactivated using a delay circuit by the beginning of the current fall interval. Therefore, a higher resistance is placed in the discharging path of the gate of the MOSFET. Consequently, the turn-off *di/dt* and subsequent high frequency oscillation is decreased. As a result, the over voltage stress across the MOSFET and EMI noise generated by high *di/dt* are decreased. However, the presented approach in [25] also suffers from the lack of adjustability over the *di/dt* and *dv/dt*. Furthermore, because a fixed delay is used to detect the start of the current fall region, the

switching performance is suboptimal in entire operating range, except the designed operating point. This suboptimal performance is due to the fact that a change in the operating condition would result in an early or late change in the gate resistance. This may result in undesired overvoltage or excessive loss that will be thoroughly explained in chapter II.

A three stage gate driver for IGBTs is presented in [26]. In this gate driver, a resistor with a low resistance is placed in the charging path of the gate of the IGBT to reduce the turn-on delay. After the threshold voltage has been detected by the detection circuit, a resistor with a higher resistance is placed in the gate circuit to reduce the *di/dt* and peak reverse-recovery current. Afterwards, the resistance of the charging path of the gate is decreased again to reduce the Miller plateau and increase the *dv/dt*. The same three stage approach is used to decrease the *di/dt* and increase the *dv/dt* in the turn-off transition. However, one would face a significant error in detection of the different stages in case of changing in the operating conditions. The reason is that, the gate voltage is compared to a constant reference value to detect the gate threshold and Miller voltages which are respectively correspond to the start of the current rise and voltage fall regions. However, the threshold voltage of the gate and Miller voltage are respectively dependent on the temperature and load current and may change significantly.

The main drawback of the active gate drive techniques which control the resistance of the gate is the lack of adjustability of the switching *di/dt* and *dv/dt*. Another drawback of these methods is imprecise detection of the *di/dt* and *dv/dt* control regions. The lack of adjustability and imprecise detection, results in the suboptimal switching performance of the PSD over the operating range.

4. Switching Transition Control by Controlling the Gate Current

Simplified concept of switching transition control by controlling the gate current is shown in Fig. 3. In these control methods that are based on controlling the gate current, additional current is injected or taken out from the gate of the PSDs in selected transition intervals. Controlling the gate current have employed in [27] and [28] to control the turn-off transition of IGBTs. In this method, a high value gate resistance is chosen and placed in the gate charging path of the IGBT. The value of the gate resistance is selected such that the turn-on *di/dt* and reverse recovery current are decreased. Therefore, the device stress and EMI are also diminished in the current rise interval. When the collector current reaches it maximum value, the gate drive circuit injects an additional current to the gate of the IGBT in the voltage fall interval. The voltage fall interval is followed in series with the current rise interval and begins when the collector current reaches it maximum value. The injected current to the gate of the IGBT, results in a higher *dv/dt* which shrinks the voltage fall duration and decreases the switching loss. The moment at which an additional current is injected to the gate of the IGBT is initiated using a delay circuit. However, this delay is not self adjusted and needs to be tuned in case of changing in the operating condition. Furthermore, the *di/dt* and *dv/dt* during the turn-on transition are not adjustable. Therefore, the optimal performance is not attainable over the operating range of the device, since the driver can only be tuned for one operating point which is usually the nominal operating condition. This method is further improved in [29], [30], to solve the delay problem, using a phase-locked-loop (PLL) circuit to detect the Miller plateau.

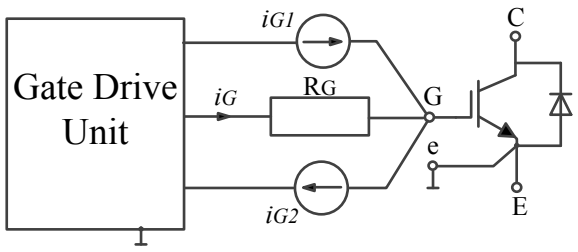


Fig. 3. Simplified concept of switching transition control by controlling the gate current.

A three stage drive concept similar to [26] has been proposed in [31], [32]. The only difference is the adjustability of the *di/dt* in the current rise and current fall intervals which is not possible in [26]. Similar to [26], the gate is charged by maximum current to reduce the turn-on delay. Unlike [26], the charging current of the gate of the IGBT is adjusted during the current rise interval of the IGBT using a controllable current source. Adjustability of the *di/dt* enables one to control the EMI noise and peak reverse recovery current over the operating range of the device. After the current rise interval has ended, the instant of the voltage fall is detected using parasitic inductance of the Kelvin emitter of the IGBT. Afterwards, the gate is charged by maximum current to increase the *dv/dt* and decrease the switching loss. In the turn-off transition, initially the gate is discharged by maximum current to reduce the turn-off delay. Gate current is then controlled during the voltage rise and current fall stages. Although, this approach offers controllability over *di/dt* at turn-on and turn-off transitions, the *dv/dt* is not adjustable. Moreover, the value of the *dv/dt* is dependent on the value of the *di/dt* in the turn-off transition.

References [33] and [34] have implemented two active gate drive circuits to control the switching transition of an IGBT during turn-on and turn-off transitions. At turn-on transition, the gate is charged by the conventional gate current, and additional current is injected to the gate of the IGBT during the turn-on delay and voltage fall intervals. This additional current is provided by an additional path. High gate current at these intervals decreases the turn-on delay as well as

the turn-on switching loss. The additional current path is deactivated during the current fall interval by sensing the generated voltage over the parasitic inductance of the Kelvin emitter of the IGBT. Therefore, the *di/dt*, peak reverse recovery current and EMI are decreased while switching loss and turn-on delay are mitigated. A similar concept has been implemented to control the turn-off switching transition. Similarly, the gate is discharged by maximum current through the conventional path and an additional current path, during the turn-off delay and voltage rise intervals. Discharging the gate by the maximum current, decreases the turn on delay and switching loss. The additional discharging path is then deactivated during the current fall interval to decrease the turn-off overvoltage and EMI noise. The falling instant of the collector current is detected by sensing the overvoltage across the parasitic inductance of the Kelvin emitter of the IGBT. However, *di/dt* and *dv/dt* cannot be adjusted using the presented approaches in [33], [34]. Therefore, the optimal performance in terms of the EMI noise, switching loss and device stress is not granted.

Similar approaches as [33] are proposed in [35]-[37] to control the turn-off switching transition of power MOSFETs. Similar to [33], the gate is discharged by the maximum current during the turn-off delay and voltage rise intervals. The high rate of the discharging of the gate, results in a lower turn-on delay and lower switching loss due to the higher rate of the *dv/dt*. During the current fall interval, an additional current is injected to the gate of the MOSFET that results in a lower *di/dt* and overvoltage during this interval. Although the *di/dt* is not adjustable using [35] and [36], it is adjustable using the proposed approach in [37]. The reason is that the injected current to the gate of the MOSFET is controllable using the proposed approach in [37]. However, all of the methods in [35]-[37] do not have any controllability over the *dv/dt* .

Closed-loop active-gate-drive circuits are proposed in [38], [39] to control the switching transition of an IGBT. In these references, four current-source circuits are implemented to adjust the *dv/dt* and *di/dt* in turn-on and turn-off transitions of an IGBT. The *dv/dt* is adjusted by a current-mirror circuit which controls the gate current using a feedback current. This feedback current is proportional to the *dv/dt* of IGBT. The feedback current is provided by an external capacitor in parallel with the Miller capacitance of the IGBT. These *dv/dt* control circuits are only activated when the voltage gradient is present over the collector and emitter terminals of an IGBT. Similarly, the voltage drop over the parasitic inductance of the Kelvin emitter of the IGBT is used as a feedback signal for the *di/dt* control circuits. The current source circuits use the feedback signal to accordingly adjust the gate current and thus control the *di/dt* in the turn-on and turn-off transitions. Although the full adjustability of *di/dt* and *dv/dt* is possible using the proposed circuits in [38], [39], four individual circuits are needed to control the *di/dt* and *dv/dt* in turn-on and turn-off transitions. A similar approach is used to adjust the *dv/dt* of the switching transition of an IGBT, [40]. However, using the presented approach in [40], only one circuit is needed for *dv/dt* control of both turn-on and turn-off transitions.

5. Switching Transition Control by Controlling the Gate Voltage

Most of the active-gate-drive methods based on controlling the gate voltage either use an event feedback to change the gate voltage or dynamically control the transition performance using the closed loop feedback of *di/dt* and/or *dv/dt* . However, Grbovic [41] proposed an IGBT gate driver based on the open-loop control of the gate voltage to control the turn-on switching performance. The *di/dt* is adjusted by controlling the slope of the gate-emitter voltage using a voltage shape generator. Afterwards, maximum voltage is applied to the gate circuit to shrink the Miller plateau and increase the *dv/dt*. Therefore, not only the peak reverse recovery current is

controlled using the voltage shape generator, but also the switching loss is decreased by decreasing the voltage fall duration. However, the controllability of the voltage slope is limited using this approach.

Simplified concept of the active gate drive by means of controlling the gate voltage is shown in Fig. 4. In this concept the gate of an insulated gate PSD is subject to a multi level voltage. Each level is adjusted such that the desired switching performance is achieved. The duration of each level is also adjusted by event feedbacks. An active gate drive circuit to control the turn-on *di/dt* and turn-off *dv/dt* of IGBTs is proposed in [42]. In this approach, an intermediate voltage level, which is less than the maximum applied voltage and greater than the threshold voltage of the IGBT, is applied to the gate of the IGBT during the current rise interval in the turn-on transition. Therefore, the slope of the collector-to-emitter current of the IGBT is adjusted using the intermediate voltage level. As a result, the peak reverse recovery current is controlled. By the end of the reverse recovery period, the control circuit applies the maximum voltage to the gate of the IGBT to charge the gate-to-emitter capacitance with the maximum current. Hence, the voltage fall duration as well as the turn-on losses is decreased. However, the controllability over the turn-on *dv/dt* is limited. During the voltage rise and current fall intervals of the turn-off transition, an intermediate voltage is applied to the gate of the IGBT during. This intermediate voltage is less than the gate threshold voltage. As a result, the *di/dt* is reduced. Although, the turn-off delay and voltage overshoot are decreased using this approach, the switching loss is increased. The reason is lack of independent controllability of *di/dt* and *dv/dt* which results in a reduced rate of fall of the collector-to-emitter voltage.

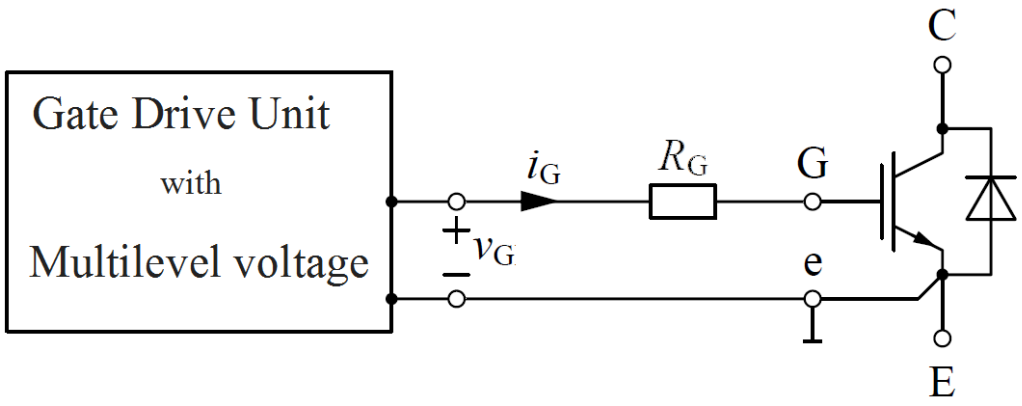


Fig. 4. Simplified concept of switching transition control by controlling the voltage using event feedbacks.

Closed loop gate drive circuits are proposed in [43]-[45] which control the *di/dt* of turn-on and turn-off transitions. The *di/dt* generates voltage across the parasitic inductance of the Kelvin emitter of the IGBT. This voltage is sensed and compared to a reference value and error is fed to an amplifier and buffer stage to regulate the desired *di/dt*. It has been shown that the proposed approaches can control the peak reverse recovery in turn-on and voltage overshoot in turn-off transitions by adjusting the *di/dt*. However, the *dv/dt* is not controllable by the proposed approach in [43]-[45].

In reference [46], an open-loop gate driver similar to [42] is presented to control the turn-off *di/dt* of the IGBTs. The idea of [46] is to apply a pulse voltage with duration of t_p to the gate of the IGBT in the current fall region to decrease the *di/dt* and consequent voltage overshoot and high-frequency oscillations. However, the fundamental parameter of the pulse such as t_p and the time at which the pulse begins has to be adjusted manually. Therefore, the optimal performance of the IGBT is limited. Moreover, there is no controllability over *dv/dt*.

A closed loop gate driver which controls the turn-off transition of IGBTs has been proposed in [47]. This gate driver controls the voltage gradient across the collector-to-emitter terminals of IGBTs using the feedback of the collector-to-emitter voltage. The collector-to-

emitter voltage is sensed and compared to a reference ramp signal. The error is then fed to an op-amp and buffer stages to drive the gate of the IGBT. However, because of the shape of the reference ramp, the actual *dv/dt* has some deviation from the reference ramp, especially in low amount of voltages. The reason is that, when the reference ramp begins to rise, the controller should initially discharge the gate of the IGBT and the voltage gradient does not occur across the collector-to-emitter terminals of the IGBT until the gate voltage reaches the Miller plateau. To compensate this drawback, authors have changed the ramp signal and added a primary step prior to the ramp in the reference voltage [48], [49]. This step allows the gate of the IGBT to discharge to the Miller plateau level. Therefore, the IGBT is ready to follow the reference ramp as soon as it begins. However, generating the reference signal is quite difficult using the analog circuits. Although, the *dv/dt* follows the reference voltage using the above mentioned approaches and voltage overshoot is decreased, the *dv/dt* cannot be adjusted to a different value without changing the circuit components. Furthermore, the controllability over the turn-off *di/dt* and voltage overshoot is limited. Moreover, additional switching losses are incurred because of the initial step of the reference voltage. This method is then improved in [50], in which a field programmable gate array (FPGA) is used to dynamically adjust the duration of the initial step of the reference voltage and its voltage slope based on the feedback signals. Therefore, adjustable *dv/dt* is achieved, and an excessive loss due to the initial step in the reference voltage is decreased. The presented work in [48] is also evolved in [51]-[52] by adding analog feedback loops of the voltage gradient and gate voltage. These additional feedback loops decrease the undesired effect of the initial step of the reference voltage and increases the stability of the control loop. Also, authors have employed two different step levels of the reference voltage in [53]-[54] instead of a

single step level in [48], to minimize the undesired effect of the initial step of the reference voltage.

Lobsiger and Kolar [55], have presented a closed-loop gate driver to dynamically control the *di/dt* and *dv/dt* of the switching transitions of the IGBTs. Two feedback loops and a proportional-integral (PI) stage are used to control the switching transition in this method. Feedback loops consist of a *di/dt* feedback loop and a *dv/dt* feedback loop. The di/dt feedback loop is deactivated using a clipping circuit in the *dv/dt* control region and vice versa. The di/dt and dv/dt are individually controlled by a reference voltage and circuit-dependent feedback gains. However, using the same reference voltage for both di/dt and dv/dt along with the constant feedback gains in each switching-transition period makes it difficult to adjust dv/dt without bounding adjustability of di/dt and vice-versa.

Closed-loop digital control of the slope of the collector-to-emitter voltage and collector current of the IGBTs is developed in [56],[57]. In this approach, the collector current, collector-to-emitter voltage and gate voltage of the IGBT are sampled using the Analog to digital (A/D) converters. The sampled data is then fed to an FPGA in which the data is processed, and the desired output is generated based on the different states of the switching transition. The generated output is then fed to a digital to analog (D/A) converter followed by a buffer stage to provide the desired current level with the specified duration for the gate of the IGBT. Therefore, the complete control of the switching transition is attained. Because of the large transition delays of the A/D and D/A conversion of the feedback signals, the output command, and required time for processing the data using the FPGA, the real-time control of the switching transition is only attainable for transitions slower than few microseconds. Therefore, iterative and adaptive approaches are implemented to control the switching transition in the next cycles based on the

provided data from the previous cycles. However, the accurate control is not granted for a significant change in the operating condition which affects the subsequent switching transitions. The other drawbacks are the limitation in the bandwidth of the sensing of the feedback signals and generating the output signal which bounds the accuracy of the control.

B. Motivation and Objective of Doctoral Research

As outlined in the previous sections, the high frequency requirement of modern power electronics applications requires reducing the switching loss and increasing the power density. This is achieved through increasing the voltage and current slopes of PSDs in the switching transition. On the other hand, the high *dv/dt* and *di/dt* in the switching transitions generate voltage and current overshoot as well as conducted and radiated noise. Therefore, several power stage solutions are presented in the literature to decrease the device stress and EMI noise. Power stage solutions require modification in the original topology and/or adding active and/or passive components. Therefore, the total cost and size of the system increases. Furthermore, control of the power electronics converter may become more complicated. Hence, active gate drive solutions are introduced to optimally control the switching transition in terms of losses, device stress and EMI by shaping the switching transition using the gate drive circuits. Active gate drive solutions are divided into three categories: controlling the gate resistance, controlling the gate voltage and controlling the gate current. Because of intertwined nature of the switching *di/dt* and *dv/dt*, the independent controllability over the *dv/dt* and *di/dt* is not realized in most of the active gate drive methods.

Although controlling the switching transitions of electrically-triggered (ET) PSDs has been explored, limited work has been conducted on the switching-transition control of optically-

triggered (OT) PSDs. Recent work on monolithic and hybrid OT PSDs [58]-[63] have demonstrated the feasibility of using a single optical link for both pulse-width-modulation (PWM) and switching-transition control of a PSD using a controller, which is spatially separated from the PSD power stage. The direct optical link precludes the possibility of signal corruption by external EMI. However, the optical-to-electrical conversion delay is appreciable as compared to the total duration of the switching transition which adversely affects the performance of the transition controller with feedback [61],[62].

This doctoral dissertation outlines the turn-off switching-transition control of an OT hybrid PSD in chapter 2. The OT hybrid PSD comprises two GaAs-based OTPTs and a SiC MOSFET. The outlined mechanism for optical control can be extended to Si power MOSFETs as well because of similarities in device behavioral dynamics [64],[65].. The OTPTs are placed in the charging (turn-on) and discharging (turn-off) paths of the gate of the SiC MOSFET. Unified turn-off dv/dt and di/dt control are achieved using a single circuit by modulating the intensity of the optical beam that triggers the OTPT, which controls the turn-off of the SiC MOSFET. A laser driver is designed to dynamically adjust the optical intensities for dv/dt and di/dt control. The independent control of turn-off dv/dt and di/dt is achieved by means of a control circuit which compensates for the total delay in the control loop. It also predicts the moment of transition between dv/dt and di/dt regions of control. The experimental results are also provided in chapter II. It is shown that the controller can independently control the turn-off *dv/dt* and *di/dt* in different load currents and applied voltages. Chapter 3 presents a novel closed-loop active-gate-control (AGC) circuit for high-voltage SiC MOSFETs, used in the high-voltage, high-frequency and high-power-density applications. The proposed controller independently adjusts the switching *di/dt* and *dv/dt* by closed-loop control of the gate current and enables one to

reach optimal performance in terms of loss, device stress, and EMI. The *di/dt* is adjusted to control the overvoltage stress and peak reverse recovery current while the *dv/dt* is adjusted to control the common mode (CM) noise and switching loss. The *dv/dt* is the primary source of the common mode noise in power electronics converters. Dynamic control of switching *dv/dt* has been somewhat overlooked in the state-of-the art works based on Si based power semiconductor devices (PSDs), and maximum achievable *dv/dt* is used to decrease the switching loss. However, the magnitude of generated *dv/dt* in the high-voltage SiC-based applications is appreciable because of the exceptionally higher switching speed of the SiC MOSFETs as compared to Si IGBTs. In contrast to other works, the proposed controller dynamically and independently controls the turn-off *di/dt* and *dv/dt* of a SiC MOSFET using closed-loop control of the gate current. Independent control of turn-off *di/dt* and *dv/dt* is achieved using a delay compensation circuit. This circuit compensates the total delay in the feedback loop and predicts the onset of transition between *dv/dt* and *di/dt* control regions. The proposed control circuit operation and advantages are presented and verified by experimental results in chapter 3.

Chapter 4 presents the turn-on switching-transition control of an OT IGBT. The IGBT is triggered by two GaAs-based OTPTs. Switching dynamics of IGBT is controlled by modulating the optical intensity to the base of OTPT using a laser driver. Turn-on transition control adjusts the turn-on delay such that the switching transition control has minimum effect on the PWM modulation of the converter. It also decreases the overshoot of the turn-on current that is generated by reverse-recovery current (IRR) of the free-wheeling diode (FWD) due to high *di/dt* during turn-on. Moreover, it adjusts the turn-on *dv/dt* to control the switching loss and electro-magnetic interference (EMI) while keeps the PSD in the safe-operating area. Additionally it reduces the voltage tail and associated switching loss by detecting the voltage tail and increasing

the optical intensity in that region. In contrast to other works, the proposed control method independently adjusts the turn-on delay, *di/dt* and *dv/dt* and reduces the voltage tail in different operating conditions. The onset of transition between delay, *di/dt*, *dv/dt* and voltage-tail control regions is determined using a self-contained control circuit [75]. The control circuit generates a command that initiates the transition between the two control regions. This command is then delayed to account for the total delay in the OTPT and feedback loop. Subsequently, the actual onset of transition is sensed, and the error between the delayed command and actual onset of transition is compensated using a PI compensator. The proposed control circuit operation and advantages are presented and verified by experimental results.

II. Optically-switched-drive Based Unified Independent dv/dt and di/dt Control for Turn-off Switching Transition of Power MOSFETs

(Parts of this section, including figures and text, are based on my paper [73], ©2015 IEEE)

A. Turn-off Transition Behavior and General Control Scheme

The standard clamped-inductive test circuit and control block diagram for optical transition control are shown in Fig. 5. The test circuit comprises a bridge leg with the hybrid device package (comprising M1 and the two OTPTs) placed in the low side and a self-gated SiC MOSFET (M2) in the high side. MOSFET M2 has characteristics similar to the characteristics of the SiC MOSFET in the hybrid package. OTPT1 and OTPT2 work complementarily and turn the SiC MOSFET (M1) on and off, respectively.

As indicated in Fig. 6, when the turn-off command is initiated by the PWM signal at t_0 , the laser driver provides the current level L_1 (proportional to the external voltage control command V_1 shown in Fig. 5) for the laser with its wavelength centered at 808 nm. The laser delivers an optical power corresponding to the current level L_1 to the base region of the OTPT2 via an optical link. OTPT2 then turns-on, after some delay, at t_d, allowing the gate charge of M1 to be discharged through it. The turn-on delay of OTPT as a function of optical power has been measured using the resistive circuit of Fig. 2-7 employing the point to point method. The results are then plotted in Fig. 7. The higher optical intensity results in smaller turn-on delay due to the higher rate of photo-generated carrier density inside the OTPT as shown in Fig. 7. More information about the characteristics and behavior of OTPT is provided in [67],[68].. After the OTPT is turned on, the gate-to-source voltage (v_{GS}) of M1 starts to fall until it reaches the Miller

plateau voltage (V_{Miller}); subsequently, the drain-to-source voltage (v_{DS}) of M1 begins to rise. The slope of v_{DS} is approximated using the following relation:

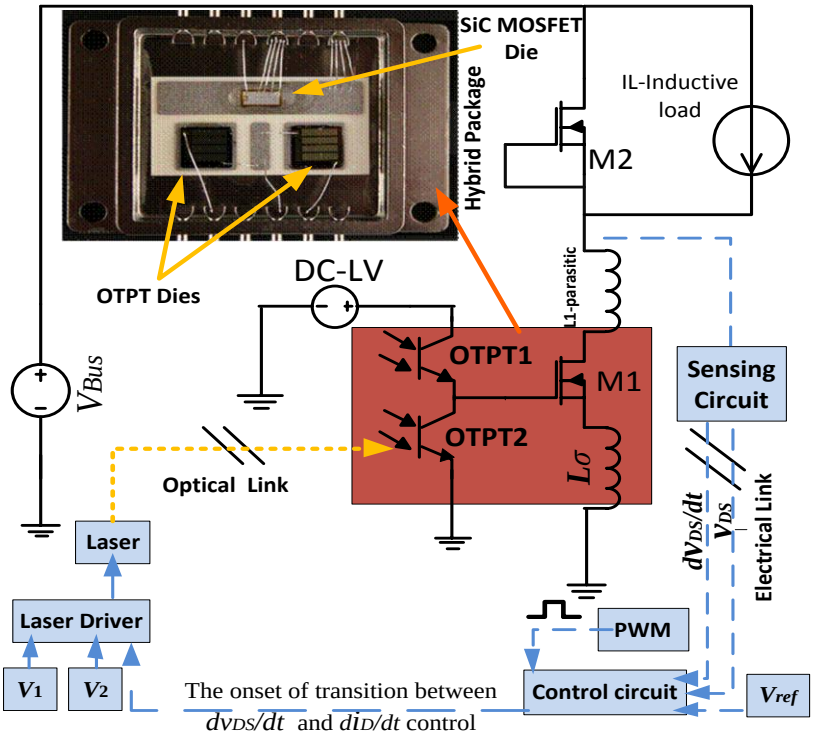


Fig. 5**:** Test circuit and control block diagram. *V*1 and *V*2, respectively, control dv_{DS}/dt and di_D/dt of M1 in the dv_{DS}/dt - and di_D/dt -control regions of operation as illustrated in Fig. 2. The threshold condition, for the onset of transition between the dv_{DS}/dt and the di_D/dt -control regions, is provided in Section II-A-1, ©2015 IEEE.

$$dv_{DS}/dt \approx \frac{v_{GS,TH}+i_D/g_{fs}}{R_G C_{GD}} = \frac{V_{Miller}}{R_G C_{GD}}. \tag{1}$$

In (1), g_{fs} is the forward transconductance of M1, i_D is the drain current, C_{GD} is the gate-to-drain capacitance of M1 also known as Miller capacitance, R_G is the gate resistance, and $v_{GS,TH}$ is the threshold voltage of M1. However, the gate-to-drain capacitance of MOSFETs is a nonlinear function of v_{DS}. C_{GD} of M1 is approximated as a two-step function of drain-to-source voltage of M1 as shown in Fig. 8:

$$C_{GD} = \begin{cases} C_{GD,avg1} & ; \ v_{DS} < v_{DS1} \\ C_{GD,avg2} & ; \ v_{DS} \geq v_{DS1} \end{cases} \tag{2}$$

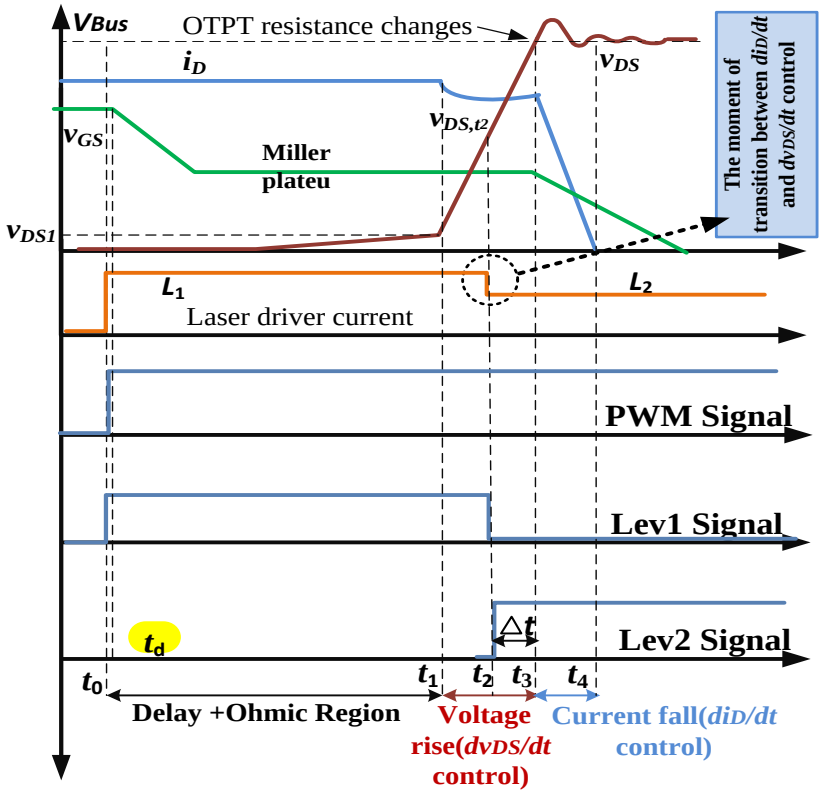


Fig. 6**:** Turn-off behavior of the MOSFET and control circuit key waveforms. The output currents L_1 and L_2 of the laser driver are proportional to the voltage commands V_1 and V_2, which dictate the dv_{DS}/dt and di_D/dt dynamics of M1 in the dv_{DS}/dt and di_D/dt control regions, ©2015 IEEE.

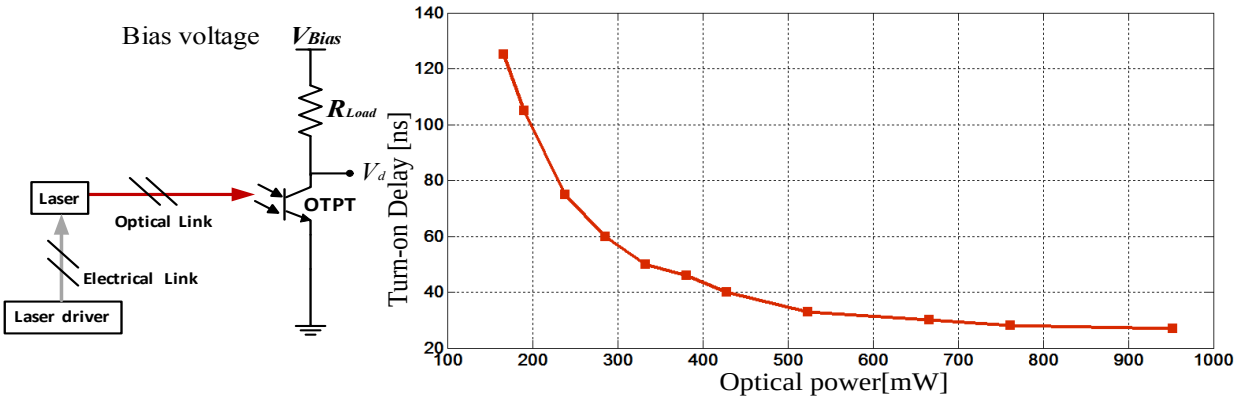


Fig. 7**:** Turn-on delay of OTPT vs. the optical power, using the resistive-load circuit. V_{Bias}= 10V, R_{Load}=200Ω, frequency=50kHz and duty cycle=50%, ©2015 IEEE.

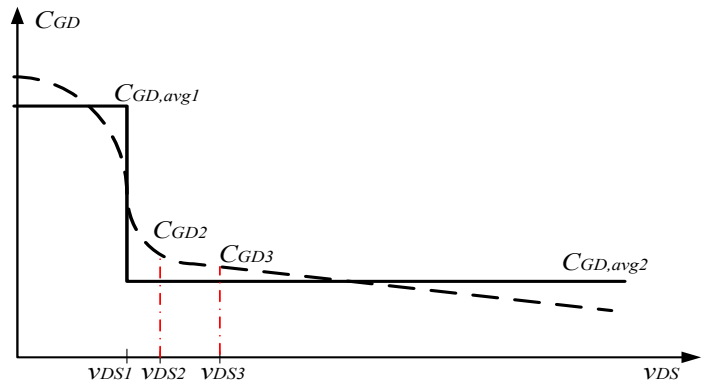


Fig. 8**:** Gate-to-Drain capacitance of M1 (also known as Miller capacitance) as a function of drain-to-source voltage, ©2015 IEEE.

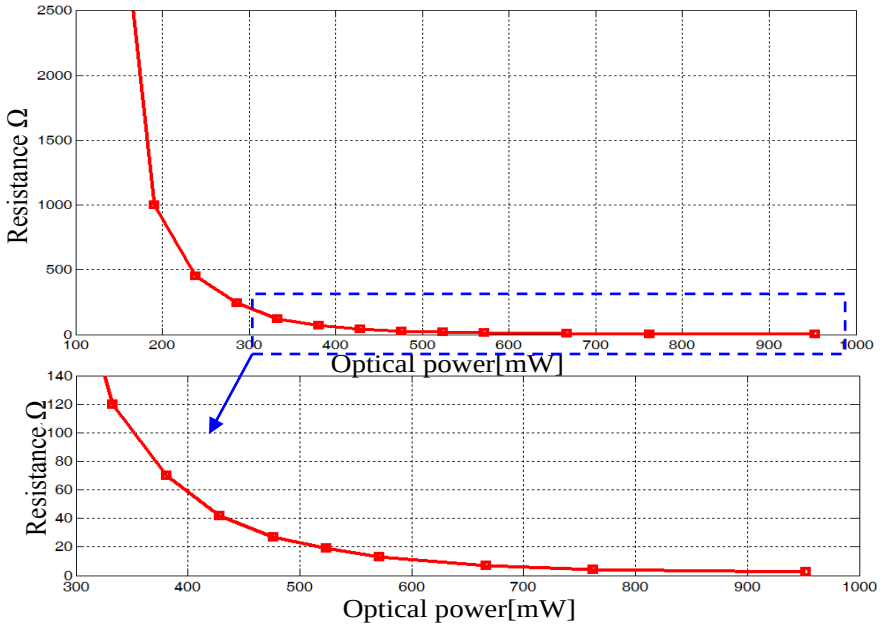


Fig. 9**:** Resistance of OTPT vs. the optical power, using the resistive-load circuit of Fig 7, ©2015 IEEE.

Equation (2) is mostly true for other types of power MOSFETs and even IGBTs, as well[[41]. Typically, $C_{GD,avg1}$ is dramatically higher than $C_{GD,avg2}$. Therefore, slope of the drain-to-source voltage of M1 before v_{DS} reaches the turning point v_{DS1} (corresponding to the time t_1 in Fig. 6), is significantly lower as compared to the duration in which $v_{DS} \geq v_{DS1}$. The interval in which v_{DS} is lower than v_{DS1} is referred as ohmic region, as shown in Fig. 6. Furthermore, the

interval in which v_{DS} is higher than v_{DS1} and lower than the bus voltage (V_{Bus}) is referred as dv_{DS}/dt control region (corresponding to the interval between t_1 and t_3 in Fig. 6).

According to (1), the dv_{DS}/dt can be controlled by varying the resistance in the discharging path of the gate. The latter in turn is adjusted by changing the optical intensity of OTPT2. Current level L_1 of the laser driver sets the optical intensity in the dv_{DS}/dt control region . Resistance of OTPT as a function of optical power is measured using the resistive circuit of Fig. 7 and data is plotted in Fig. 9.

When v_{DS} matches the bus voltage (V_{Bus}) at t_3, current i_D falls which causes an overvoltage across M1 due to the parasitic inductances in the commutation path. This region is referred to as the di_D/dt control region. The overvoltage (Δv_{ov}) across the drain-to-source terminals of M1is given by the following expression:

$$\Delta v_{ov} = L_c . \frac{di_D}{dt} \tag{3}$$

Where L_c is the sum of the parasitic inductances in the commutation path, which includes the parasitic inductances of M1 and M2, bus-parasitic inductance, and trace inductances. In the di_D/dt control region, $di_D/dt$is given by the following expression:

$$\frac{di_D}{dt} \approx -\frac{V_{GS,TH}+i_D/2g_{fs}}{R_G C_{iss}/g_{fs}+L_\sigma}. \tag{4}$$

In (3), C_{iss} is the input capacitance of M1 and L_σ is the sum of parasitic inductances seen from the source of M1. Following (3), the di_D/dt is controlled by varying the resistance of the discharging path of the gate of M1. This resistance is adjusted by changing the optical intensity of OTPT2, as shown in Fig. 3. Current level (L_2) of the laser driver sets the optical intensity in

the di_D/dtcontrol region and L_2 is proportional to the external voltage control command V_2, as shown in Fig. 5.

Of course, while the control of dv_{DS}/dt and di_D/dt in their respective regions of operation is important, a seamless transition between the dv_{DS}/dt and di_D/dt control regions is equally important. In the following subsection, we derive this threshold condition for transition between the two control regions and outline its implementation.

1. Threshold Condition for Transition Between dv_{DS}/dt and di_D/dt Control Regions

The transition between L_1 and L_2, thereby transitioning from the dv_{DS}/dt to the di_D/dt control region, is initiated by the control circuit illustrated in Fig. 5. This transition guarantees the independent control of di_D/dt and dv_{DS}/dt. Following, [34] and [39], an easy way to detect the onset of the di_D/dt control region is to detect the change in the di_D/dt from near zero to a significantly larger value. If this approach is adopted, the onset of transition is initiated later than the desired instant due to control-loop and OTPT-related delays. So, one may lose the control over di_D/dt in all or a part of this di_D/dt control region, which may lead to excessive device stress or switching loss as illustrated in Fig. 10. Another approach [25] for predicting the onset of the di_D/dt control region is based on detecting the saturation region of the voltage corresponding to dv_{DS}/dt control region in Fig. 6. and initiating the transition between the dv_{DS}/dt and the di_D/dt control regions after a fixed delay. However, the error in the prediction of onset of transition is significant in applications where the dv_{DS}/dt varies over a wide range.

Therefore, in the proposed scheme, to ensure the independent control of dv_{DS}/dt and di_D/dt , a simple control circuit is designed which predicts the onset of transition between the dv_{DS}/dt and di_D/dt control regions based on the actual dv_{DS}/dt and the scaled bus-voltage

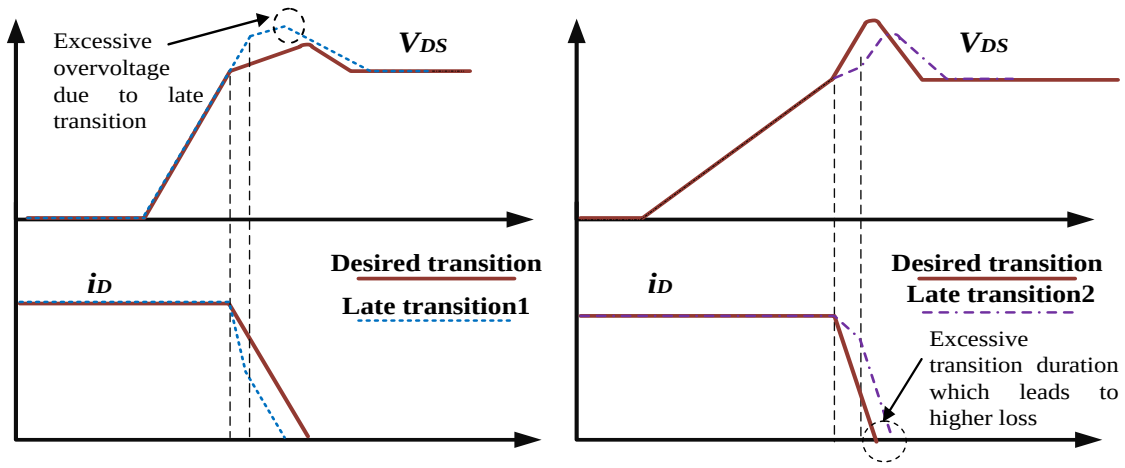


Fig. 10**:** Effect of late transition between the dv_{DS}/dt and di_D/dt control regions on device stress and switching loss, ©2015 IEEE.

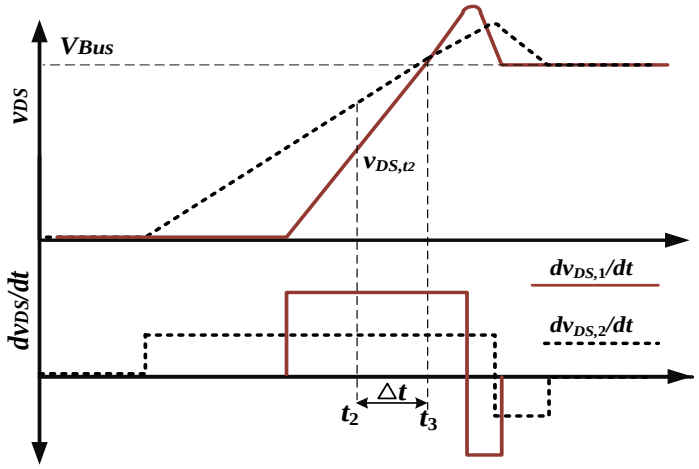


Fig. 11**:** Signals v_{DS} and dv_{DS}/dt, at the desired time (t_2) of transition for two different dv_{DS}/dt, considering the constant delay of Δ*t* seconds in the feedback loop, ©2015 IEEE.

reference (v_{ref}). The di_D/dt control region onsets at t_3, when v_{DS} reaches the bus voltage (V_{Bus}) as shown in Fig. 6. and Fig.11. However, considering a combined constant delay of Δ*t* seconds due to the feedback and due to the delay in the actuation of OTPT2, the control circuit initiates the transition between dv_{DS}/dt and di_D/dt control regions at time t_2 (= t_3 – Δ*t*). An accurate

onset of transition ensures the independent controllability of the dv_{DS}/dt and di_D/dt control regions.

Now, using Fig. 11, one can show that for any given dv_{DS}/dt the following equality holds:

$$v_{DS,t2} + (dv_{DS,t2}/dt).\Delta t = V_{Bus}. \quad (5)$$

In (5), $v_{DS,t2}$ and $dv_{DS,t2}/dt$ represent, respectively, the values of v_{DS} and dv_{DS}/dt at time t_2. Assuming the scaling factors of α_1, α_2 and α_3 associated with sensing V_{Bus}, v_{DS} and dv_{DS}/dt, respectively, the following equations hold:

$$v_{ref} = \alpha_1.V_{Bus} \quad (6)$$

$$\acute{v}_{DS,t2} = \alpha_2.v_{DS,t2} \quad (7)$$

$$d\acute{v}_{DS,t2}/dt = \alpha_3.(dv_{DS,t2}/dt). \quad (8)$$

In (7), $\acute{v}_{DS,t2}$ represents the value of sensed v_{DS} at time t_2 with a scaling factor of α_2. In (8), $d\acute{v}_{DS,t2}/dt$ represents the value of sensed dv_{DS}/dt at t_2 with a scaling factor of α_3. Substituting (6)-(8) into (5) yields the following relation:

$$\frac{\acute{v}_{DS,t2}}{\alpha_2} + \frac{d\acute{v}_{DS,t2}/dt}{\alpha_3}.\Delta t = \frac{v_{ref}}{\alpha_1}. \quad (9)$$

Because Δt is considered to be a constant, (8) can be rewritten as follows:

$$\beta_1.\acute{v}_{DS,t2} + \beta_2.(d\acute{v}_{DS,t2}/dt) = v_{ref}. \quad (10)$$

In (9), β_1 equals to (α_1/α_2) and β_2 equals to $(\alpha_1.\Delta t/\alpha_3)$. Using (9), the threshold condition for transition from the dv_{DS}/dt to di/dt control region is found to be:

$$(\beta_1.\acute{v}_{DS} + \beta_2.(d\acute{v}_{DS}/dt)) - v_{ref} \geq \varepsilon. \quad (11)$$

In (11), $\acute{v}_{DS}$ and $d\acute{v}_{DS}/dt$ represent, respectively, the sensed values of v_{DS} and dv_{DS}/dt at any time with scaling factors of α_2 and α_3 while ε represents a very small positive value. Essentially, (11) indicates that there is a time t (ideally $t = t_2 = t_3 - \Delta t$) at which the difference between $\beta_1.\acute{v}_{DS} + \beta_2.(d\acute{v}_{DS}/dt)$ and v_{ref} is either zero or very close to zero. This concept is used to design a controller which compensates for the delay in the feedback loop and ensures a seamless transition between dv_{DS}/dt and di_D/dtcontrol regions.

The control circuit and laser driver schematics are shown in Fig. 12. The coefficients β_1 and β_2 are considered to be equal to make the design of the control circuit easier. Therefore, the coefficients α_1 and α_2 have the following relation:

$$\beta_1 = \beta_2 = \beta \Longrightarrow \frac{\alpha_1}{\alpha_2} = \frac{\alpha_1}{\alpha_3}\Delta t \Longrightarrow \alpha_2 = \frac{\alpha_3}{\Delta t} \quad (12)$$

The sensed v_{DS} and dv_{DS}/dt are scaled with proper coefficient β and added using the OP1, as shown in Fig. 12, Where $\beta = R_1/3.(1 + R_3/R_2)$. The output of OP1 is then compared with v_{ref} using a comparator to monitor if the threshold condition in (2-11) is met. If (2-11) is satisfied, the control circuit initiates the transition from dv_{DS}/dt to di_D/dt control region by setting Lev1 to logic state 0 and Lev2 to logic state 1 using the D-FF and AND operators of Fig. 12.

Because of the negative dv_{DS}/dt in the di_D/dt control region, the threshold condition might not be satisfied in the di_D/dt control region. Therefore, a D flip-flop is used to prevent undesirable fluctuations of the logic states of signals Lev1 and Lev2 in the di_D/dt control region. The truth table for the control circuit can be found in the Table. 1. In Table. 1, X means no change in the state of the signal. Any negligible error in initiating the onset of transition (i.e.,

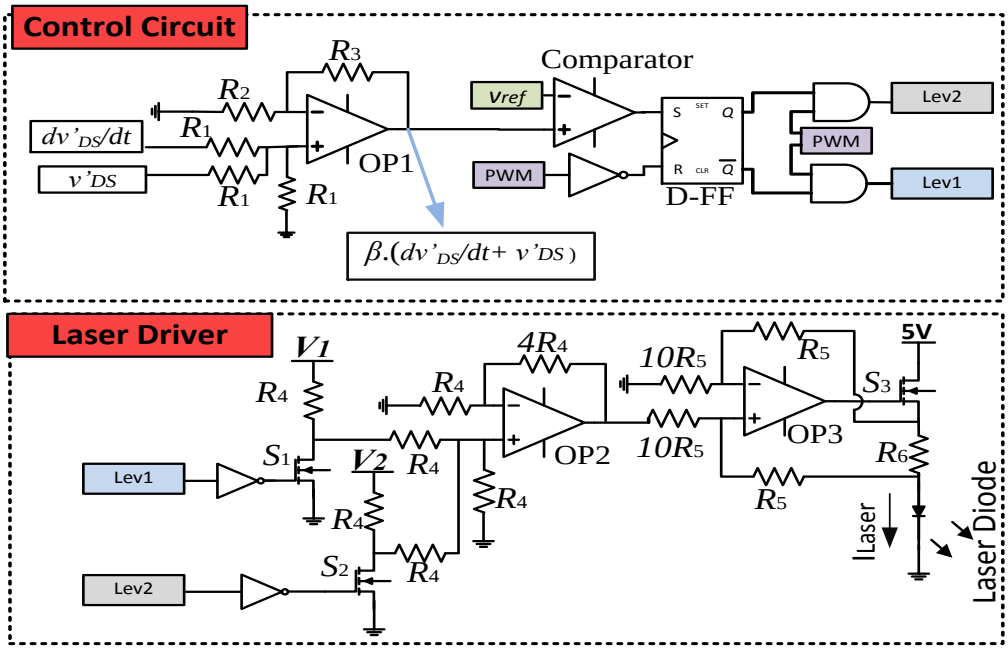


Fig. 12. Schematics of the control circuit and the laser driver, ©2015 IEEE.

$\varepsilon \neq 0$ and instead $\varepsilon \approx 0$) is due to the non-idealities in the circuit elements, nonlinearities, and error in the estimation of the total delay of the feedback loop.

Subsequent to the change in the logic states of Lev1 and Lev2, the laser driver changes its output current (I_{Laser}) from L_1 to L_2 (which is proportional to V_1 and V_2) and is given by the following relation:

$$I_{Laser} = \begin{cases} \gamma.V_1 = L_1 & \text{, when Lev1 signal is high} \\ \gamma.V_2 = L_2 & \text{, when Lev2 signal is high} \\ 0 & \text{, when PWM signal is low} \end{cases} \quad (13)$$

In (13), γ is a circuit-dependent constant and it is equal to $\gamma = 0.1/R_6$. The outputs of the flip-flop Q and $\overline{Q}$, in the Fig. 2-5, work complementarily. Furthermore, the Lev1 and Lev2 signals are derived using the AND operation of the PWM signal with $\overline{Q}$ and Q, respectively. Therefore, Lev1 and Lev2 signals in (13) are complement to each other in the duration when the PWM signal is high and they are both low when PWM signal is low, as illustrated in Fig. 6. and Table.

1. Following (1), (3), and (13), one can adjust dv_{DS}/dt and di_D/dt by respectively controlling V_1 and V_2, which in turn control the output current of the laser driver to magnitudes of L_1 and L_2. Modulating the optical intensity by the proposed laser driver, along with the implementation of the threshold condition (11), enables one to attain the unified dv_{DS}/dt and di_D/dt control.

TABLE I**:** Truth table of the control circuit.

Comparator	$\overline{\text{PWM}}$	Q	$\overline{\text{Q}}$	Lev1	Lev2
1	0	1	0	0	1
0	1	0	1	0	0
1	1	1	1	0	0
0	0	X	X	X	X

2. Availability of Independent dv_{DS}/dt and di_D/dt Control

In section II-A-1, the threshold condition for independent control of turn-off dv_{DS}/dt and di_D/dt was derived. Subsequently, the control circuit was designed based on the aforementioned threshold condition. However, the threshold condition was derived considering the following assumptions:

a) The Δt (total delay in the feedback loop and OTPT) is fixed.

b) The dv_{DS}/dt is fixed from the time at which the transition command initiates (t_2) up to the desired moment of transition at t_3. Essentially the dv_{DS}/dt is fixed during the delay time of OTPT.

c) Δt is less than the duration of dv_{DS}/dt control region. ($\Delta t < (t_3\text{-}t_1)$).

Based on the mathematical analysis and threshold condition in section II-A-1, the control circuit can independently control the turn-off dv_{DS}/dt and di_D/dt as long as the above

assumptions are valid. Therefore, the domain of validity of the above assumptions shall be analyzed to specify the boundaries for the availability of independent dv_{DS}/dt and di_D/dt control.

In section II-A-1, it is assumed that the Δt is fixed. However, Δt varies proportionally to the difference between the optical intensities in the dv_{DS}/dt and the di_D/dt control regions. In this control scheme, the turn-on and turn-off delays of OTPT are not important, but the important delay is defined as the total time that it takes for the resistance of OTPT to change from the value R1 (corresponding to the optical intensity P_1 and the laser current of $L1$) and reaches the final resistance value of R2 (corresponding to the optical intensity P_2 and the laser current of L_2). To derive the transition delay of OTPT when it is subject to a step change in its receiving optical intensity, OTPT is tested using the resistive-load circuit of Fig. 7. In this setup, OTPT receives the optical intensity of P_1 through the laser and optical link which causes the voltage drop of V_{d1} across the OTPT. Subsequently, the optical intensity is varied from P_1 to P_2 which makes the voltage drop V_{d2} across the OTPT. The delay is measured between the time at which the optical intensity is changed to P_2 and the time at which the voltage drop across OTPT reaches 90% of its final value (V_{d2}). The measured delay time for different values of P_1 and P_2 is derived using the point to point method, and plotted in Fig. 13.

If optical intensities P_1 and P_2 are equal (P_1=P_2), the transition delay is essentially zero. However, the value of transition delay in this case is selected such that the plot of Fig. 2-9 is smooth.

Now consider the case in which the optical intensity P_1 is applied to the OTPT in the dv_{DS}/dt control region, to control the turn-off dv_{DS}/dt. Similarly, the optical intensity P_2 is

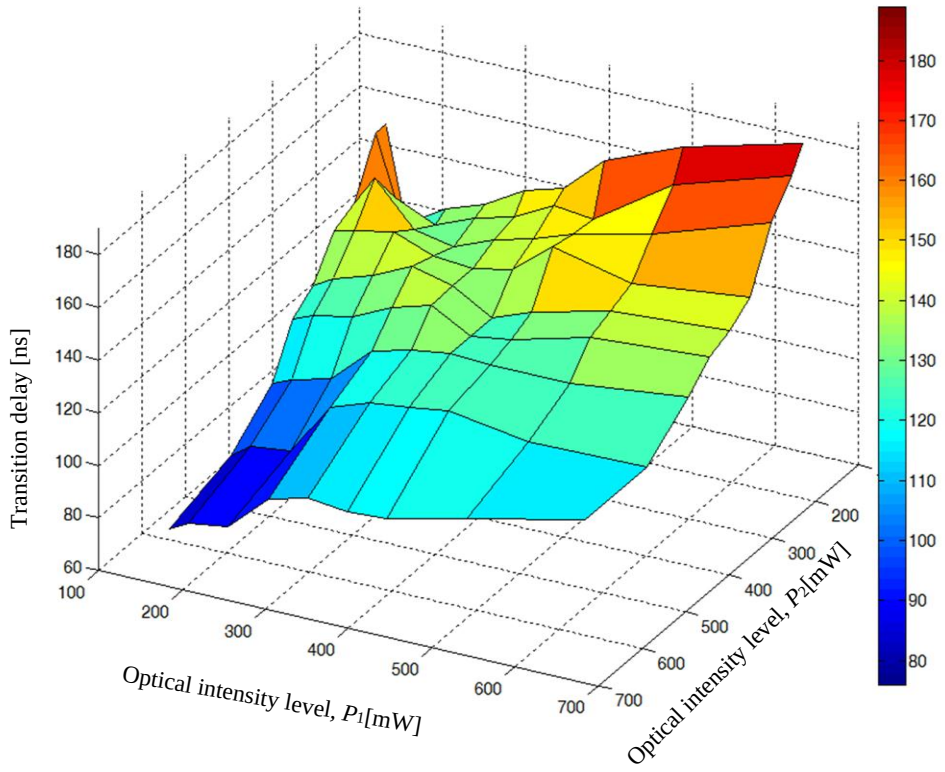


Fig. 13. Measured transition delay of resistance of the OTPT when the optical intensity changes from P_1 to P_2, ©2015 IEEE.

applied in the di_D/dt control region to control the turn-off di_D/dt. Therefore, the transition delay for the resistance of OTPT2 to change from R1 (corresponding to the optical intensity P_1) and reaches the value of R2 (corresponding to the optical intensity P_2) is Δt_1, based on Fig. 13. Considering the implemented transition delay in the control circuit is equal to Δt, the transition error because of the variable transition delay of OTPT2, (E_{r1}), is defined by the following expression:

$$E_{r1} = \Delta t_1 + \Delta t_c - \Delta t \tag{14}$$

In (14), Δt_c is the delay of the control circuit. If $E_{r1} > 0$, it affects the controllability over di_D/dt in the di_D/dt control region, and if $E_{r1} < 0$, it affects the controllability over dv_{DS}/dt in the

dv_{DS}/dt control region. Therefore, the proportional error due to the variable transition delay of OTPT2, ($E_{r1}\%$), is defined as:

$$\begin{cases} E_{r1}\% = \frac{E_{r1}}{t_{rise}} = \frac{E_{r1}}{i_D}.di_D/dt \times 100\% & \text{, if } E_{r1} > 0 \\ E_{r1}\% = \frac{E_{r1}}{t_{fall}} = \frac{E_{r1}}{V_{Bus}-v_{DS1}}.dv_{DS}/dt \times 100\% & \text{, if } E_{r1} < 0 \end{cases} \quad (15)$$

In (15), t_{rise} is the rise time of the drain-to-source voltage of M1, and t_{fall} is the fall time of the drain current of M1. In this study the independent transition control of turn-off dv_{DS}/dt and turn-off di_D/dt is valid, if $E_{r1}\% \leq 10\%$.

The control circuit in section II-A-1 is designed using the threshold condition and considering the fixed dv_{DS}/dt in the dv_{DS}/dt control region. However, because of nonlinear behavior of C_{GD} the actual dv_{DS}/dt in the dv_{DS}/dt control region is not fixed. Therefore, the actual dv_{DS}/dt has some deviation from average dv_{DS}/dt which is defined by $C_{GD,avg2}$. This deviation might results in a transition error, especially in the case of high dv_{DS}/dt in which the value of v_{DS} at t_2 ($v_{DS,t2}$) is close to v_{DS1}. t_2 is the time at which the transition from dv_{DS}/dt to di_D/dt control region is initiated by the control circuit, as shown in Fig. 6.

Following (2-2) and Fig. 2-4, the average C_{GD} in the dv_{DS}/dt control region is equal to $C_{GD,avg2}$. Therefore, the average dv_{DS}/dt which is defined by $C_{GD,avg2}$, is equal to $dv_{DS,avg}/dt$. Thus, the drain-to-source voltage of M1 at which the threshold condition is satisfied and transition is initiated is derived by the following expression, using (5):

$$v_{DS2} = V_{Bus} - (dv_{DS,avg}/dt).\Delta t \quad (16)$$

However, if v_{DS2} is close to v_{DS1}, the value of C_{GD} at v_{DS2} (C_{GD2}) is higher than the value of $C_{GD,avg2}$, as shown in Fig.2-4. Because C_{GD2} is higher than $C_{GD,avg2}$, the slope of the drain-to-

source voltage of M1 at v_{DS2} is lower than the $dv_{DS,avg}/dt$, according to (2). Therefore, the value of dv_{DS}/dt at v_{DS2} is not high enough to satisfy the threshold condition. As a result, the threshold condition is satisfied and transition is initiated, after some delay, at v_{DS3} ($v_{DS3} > v_{DS2}$). v_{DS3} is derived using the following expression:

$$v_{DS3} = V_{Bus} - (dv_{DS3}/dt).\Delta t \tag{17}$$

In (2-17), dv_{DS3}/dt is the dv_{DS}/dt at voltage v_{DS3} corresponding to C_{GD3} in Fig. 2-4. The transition is initiated Δt seconds after v_{DS} reaches v_{DS3}. However, the actual time that it takes for v_{DS} to reach V_{Bus} (beginning of the di_D/dt control region) is derived using the following equation:

$$\Delta t_2 = \frac{dv_{DS3}/dt}{dv_{DS,avg}/dt} . \Delta t \tag{18}$$

In (18), it is assumed that the average dv_{DS}/dt from v_{DS3} to V_{Bus} is equal to $dv_{DS,avg}/dt$.Therefore, the transition error due to variable dv_{DS}/dt in the dv_{DS}/dt control region, (Er_2), is equal to:

$$Er_2 = \Delta t - \Delta t_2 = (1 - \frac{dv_{DS3}/dt}{dv_{DS,avg}/dt}) . \Delta t = (1 - \frac{C_{GD,avg2}}{C_{GD3}}) . \Delta t \tag{19}$$

Because C_{GD3} is always greater than $C_{GD,avg2}$ in high $dv_{DS,avg}/dts$, Er_2 is positive. Positive Er_2 means that, the transition error does not affect the controllability over dv_{DS}/dt in the dv_{DS}/dt control region, but it affects the controllability over the di_D/dt in the di_D/dt control region. If the amount of the transition error (Er_2) is considerable comparing to t_{fall} of M1, the independent controllability of dv_{DS}/dt and di_D/dt is not granted. Therefore, the proportional error due to variable dv_{DS}/dt in the dv_{DS}/dt control region, ($Er_2\%$), is defined as follows:

$$Er_2\% = \frac{Er_2}{t_{fall}} \times 100\% = Er_2 \times \frac{di_D/dt}{i_D} \times 100\% \quad (20)$$

In this study, $Er_2\% \leq 10\%$ is considered as an acceptable error for independent controllability of dv_{DS}/dt and di_D/dt.

Following, the procedure of calculating the quantitative boundaries of dv_{DS}/dt and di_D/dt for having the independent controllability of dv_{DS}/dt and di_D/dt is described. Initially, the maximum applicable di_D/dt, ($di_{D,max}/dt$), is derived for a given load current and bus voltage, using (2-3) and considering the maximum allowable overvoltage. Then, the minimum fall time of drain current of M1, ($t_{fall,min}$), is calculated using the following expression:

$$t_{fall,min} = \frac{i_D}{di_{D,max}/dt} \quad (21)$$

Subsequently, P_2 is calculated using (4) and Fig. 9. Knowing P_2, Δt is selected using Fig. 13, such that the conditions in (14) is satisfied. Afterwards, Er_2 is calculated knowing the maximum admissible $Er_2\%$ for $t_{fall,min}$, using (20). Then, the value of C_{GD3} is derived using (19), and the corresponding voltage for C_{GD3} (v_{DS3}) is derived using Fig. 8. Therefore, the maximum allowable dv_{DS}/dt is equal to:

$$dv_{DS,max} = \frac{V_{Bus} - v_{DS3}}{(1 - Er_2\%/100).\Delta t} \quad (22)$$

If $dv_{DS,max}$ is selected properly, one will not face the condition in which Δt is less than the duration of dv_{DS}/dt control region ($\Delta t < (t_3\text{-}t_1)$). However, if this condition happens, the independent controllability of turn-off dv_{DS}/dt and di_D/dt is not granted. The flowchart of the procedure of calculating the quantitative boundaries of dv_{DS}/dt and di_D/dt is shown in Fig. 14.

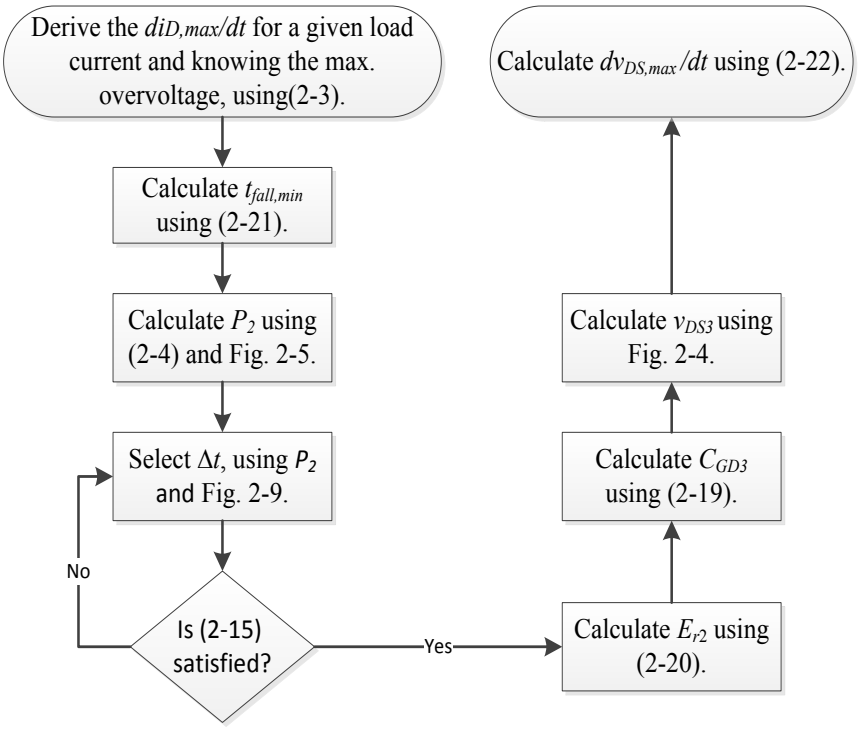
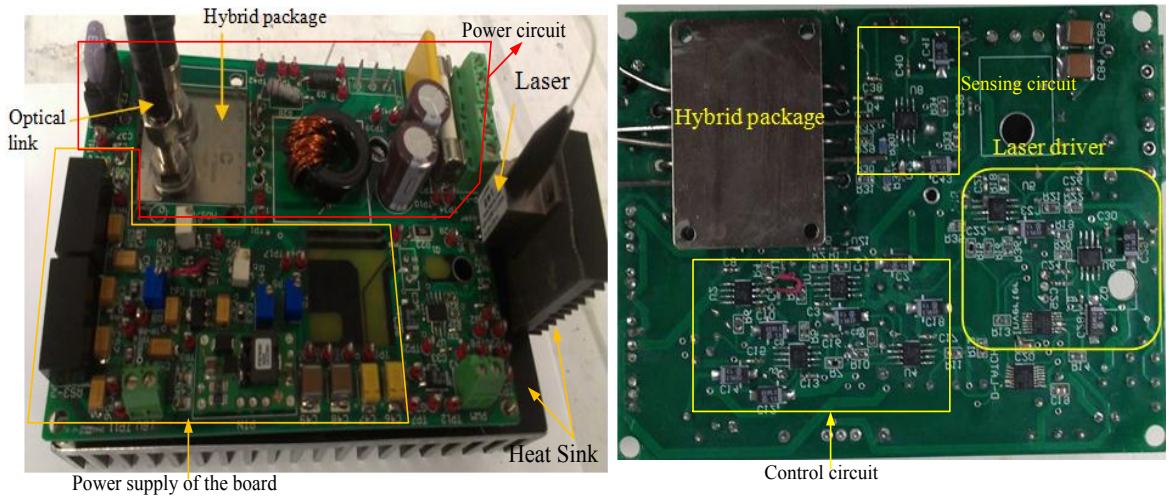


Fig. 14. The flowchart of the procedure of calculating the quantitative boundaries of dv_{DS}/dt and di_D/dt for independent control of turn-off dv_{DS}/dt and di_D/dt, ©2015 IEEE.

B. Experimental Results

The standard clamped-inductive test circuit of Fig. 5, along with the proposed control circuit are designed and fabricated as shown in Fig. 15. The fabricated set up includes the power circuit, the hybrid device package, power-supply circuits and the laser on the top side of the board and the control circuit, laser driver and sensing circuits on the bottom side of the board. The implemented SiC power MOSFET is CMF10120D with break-down voltage (BV) of 1200V, current rating of 24A, C_{GD}=7pF, *Ciss*=928pF and *Coss*=68pF. A 2W, 808nm fiber-coupled laser is used to trigger the OTPT2, as shown in Fig. 2-11. The threshold current of the laser is 0.4 A, and its output optical power as a function of input current is shown in Fig. 16. An additional inductor is used in the commutation path to simulate the effect of the leakage inductance in the isolated

dc/dc converters such as cuk, flyback and forward. Voltage sensing circuit has a band-width (BW) of



(a) (b)

Fig. 15. Fabricated test set up: (a) top side of the board which includes the power circuit, laser and power-supply circuits; (b) bottom side of the board which includes the control circuit, sensing circuits and laser driver, ©2015 IEEE.

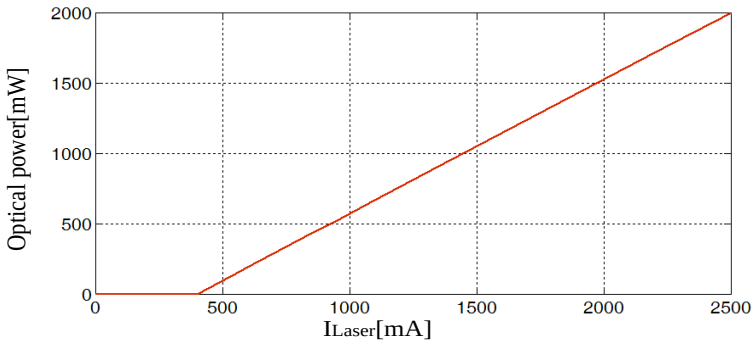


Fig. 16. Output optical power of the laser at the end of the fiber-optic cable as a function of laser current(I_{Laser}), ©2015 IEEE.

200MHz and delay of 5ns. The experimental waveforms are measured using Tektronix DPO7104, which has the BW of 1GHz. A 25 MHz differential voltage-probe along with a 50MHz current sensors are used to provide the signals for the oscilloscope. Subsequently, the measured data is plotted using MATLAB software.

Experimental results for the independent optical control of the di_D/dt of M1 with fixed dv_{DS}/dt are shown in Fig. 7. The output current of the laser-driver (I_{Laser}) remains the same in the dv_{DS}/dt control region. This leads to the same resistance for OTPT2, which is placed in the discharging path of the gate of M1, for all the cases. As the result, the current through OTPT2 and the turn-off dv_{DS}/dt in the dv_{DS}/dt control region is kept similar for all of the cases following (1). A step change in the output current of the laser driver initiates the onset of transition from the dv_{DS}/dt to the di_D/dt control region. The proper time of transition ensures independent controllability in the dv_{DS}/dt and di_D/dt control regions. Therefore, one is able to control the slope of the drain current in the di_D/dt control region without affecting the controllability over slope of the drain-to-source voltage in the dv_{DS}/dt control region. This is illustrated in Fig. 17. As current level (L_2) of the laser driver in the di_D/dt control region decreases the turn-off di_D/dt , the voltage overshoot and oscillation reduce as well. Fig. 17 validates that, the di_D/dt of M1 is dynamically controlled by controlling the current flowing through OTPT2 (i.e., I_{OTPT2}). The latter is dependent on the optical intensity of OTPT2, which in turn, is dependent on the output-current level of the laser driver.

The gate-to-drain and input capacitances of the SiC power MOSFETs are dramatically lower than their Si counterparts with the same rating. (i.e. compare the C_{GD}=77pF and C_{iss}=21nF of IXFL32N120P, to C_{GD} and C_{iss} of M1). Therefore, a higher gate resistance (which can be 10 to 20 times higher) is needed for a SiC MOSFET to ensure that it has the same dv_{DS}/dt as compared to its Si counterpart, following (2-3). A higher gate resistance in the case of having the same dv_{DS}/dt, results in a dramatically lower gate current. Furthermore, during the discharging time of the C_{iss} of M1, OTPT acts like a constant current-source and prevents the current spike of the gate current which is a common phenomenon in the conventional gate drive circuits, as

shown in Fig. 17. This behavior also results in the longer turn-off delay for M1. If the traditional gate drive with a fixed gate resistance is used, the gate voltage exponentially decreases by the following equation until it reaches the Miller voltage (V_{Miller}):

$$v_{GS} = V_{CC}.e^{-t/R_G C_{iss}} \tag{23}$$

In (23), V_{CC} is the gate bias voltage. Therefore, the delay time for this case is derived by the following equation:

$$t_{d-R} = R_G C_{iss}\,.\,ln(V_{CC}/V_{Miller}) \tag{24}$$

In (24), t_{d-R} is the turn-off delay time of M1 with the conventional fixed-gate-resistance method. On the other hand, if the OTPT is used in the gate circuit of M1, the gate current (i_G) is derived using following expression:

$$i_G = \frac{V_{CC}-V_{Miller}}{t_{d-O}}.C_{iss} = \frac{V_{Miller}}{R_G} \tag{25}$$

In (25), t_{d-O} is the turn-off delay time of M1 in the case of using the proposed optical approach. Therefore, t_{d-O} is derived using the following equation:

$$t_{d-O} = R_G C_{iss}\,.\frac{V_{CC}-V_{Miller}}{V_{Miller}} \tag{26}$$

Consequently, the ratio of turn-off delay time for the two cases is:

$$\frac{t_{d-O}}{t_{d-R}} = \frac{(V_{CC}/V_{Miller}-1)}{ln(V_{CC}/V_{Miller})} \tag{27}$$

Following (27) and depending on the load current of M1, one can conclude that using the proposed approach the turn-off delay of M1 is 1.3-2.5 times longer as compared to the conventional fixed-resistance method, in the case of having the same dv_{DS}/dt.

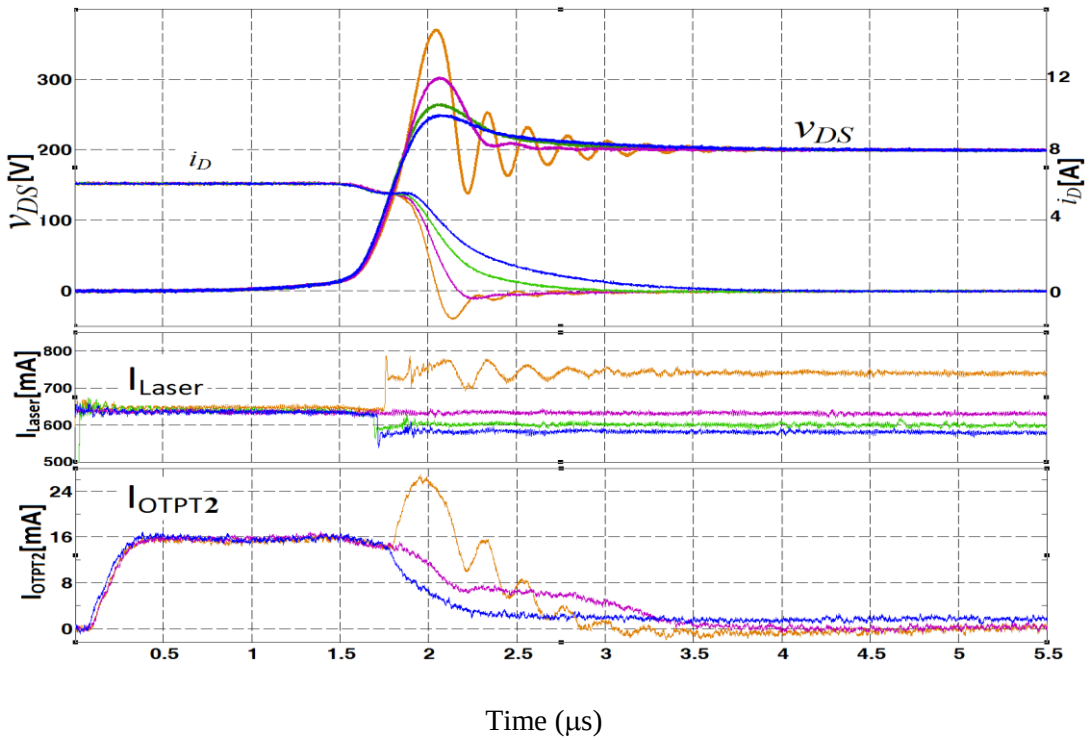


Fig. 17. Measured turn-off waveform of v_{DS}, i_D, I_{Laser}, and I_{OTPT2} with varied di_D/dt and a fixed dv_{DS}/dt, ©2015 IEEE.

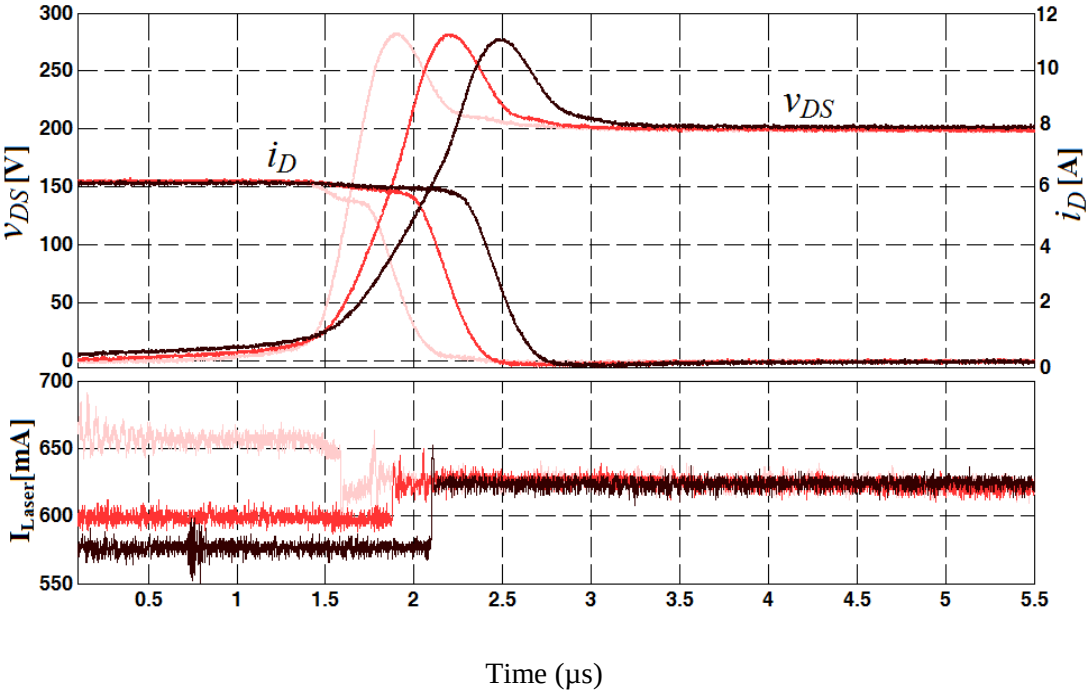


Fig. 18. Measured turn-off waveforms of v_{DS}, i_D, and I_{Laser} with varied dv_{DS}/dt and a fixed di_D/dt, ©2015 IEEE.

The experimental results for the independent optical control of the dv_{DS}/dt of M1 with fixed i_D/dt , are shown in Fig. 18. The turn-off dv_{DS}/dt increases by increasing the current level of the laser driver in this region. The onset of transition from dv_{DS}/dt to di/dt control region is set properly by control circuit for different values of dv_{DS}/dt. This ensures the independent dv_{DS}/dt and di_D/dt controls. Therefore, one is able to control the drain-to-source voltage slope in the dv_{DS}/dt control region without affecting the controllability of slope of the drain current in the di_D/dt control region, as shown in Fig. 18. The output-current levels of the laser driver remain the same in the di_D/dt control region which lead to the same resistance for OTPT2. Therefore, di_D/dt and overvoltage for all the cases are same according to (3) and (4). di_D/dt can be adjusted regardless of the value of dv_{DS}/dt in the dv_{DS}/dt control region by varying the current level of the laser driver.

The test circuit and control block diagram for the high-side-drive case is shown in Fig. 19. Experimental results for the independent optical control of the di_D/dt of M1 with the fixed dv_{DS}/dt, as well as, the independent optical control of the dv_{DS}/dt of M1 with the fixed di_D/dt for the case of high-side drive are shown respectively in Fig. 20 and Fig. 21. The results are similar to the results of the case of low-side drive, which validates the feasibility of the proposed control for high-side drive cases as long as an isolated voltage for the gate-voltage bias of M1 is provided.

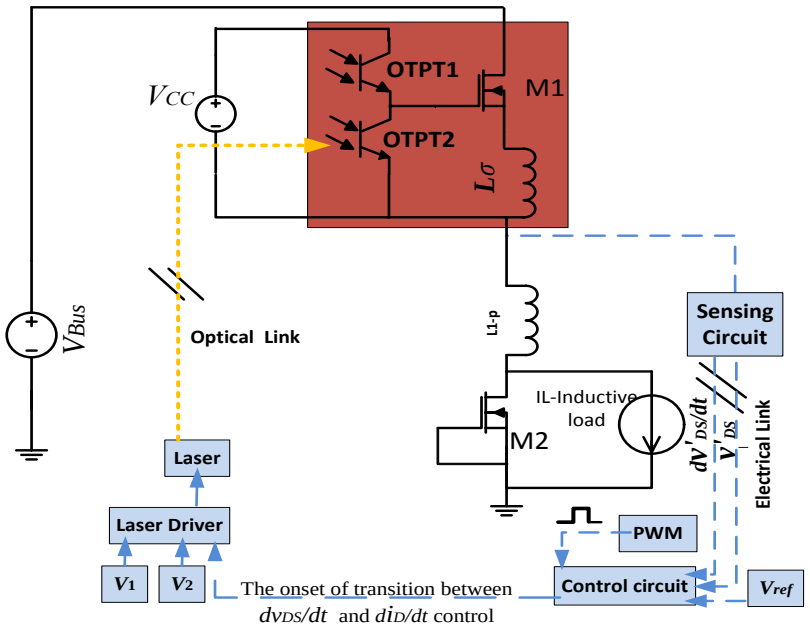


Fig. 19. Test circuit and control block diagram for the high-side drive case, ©2015 IEEE.

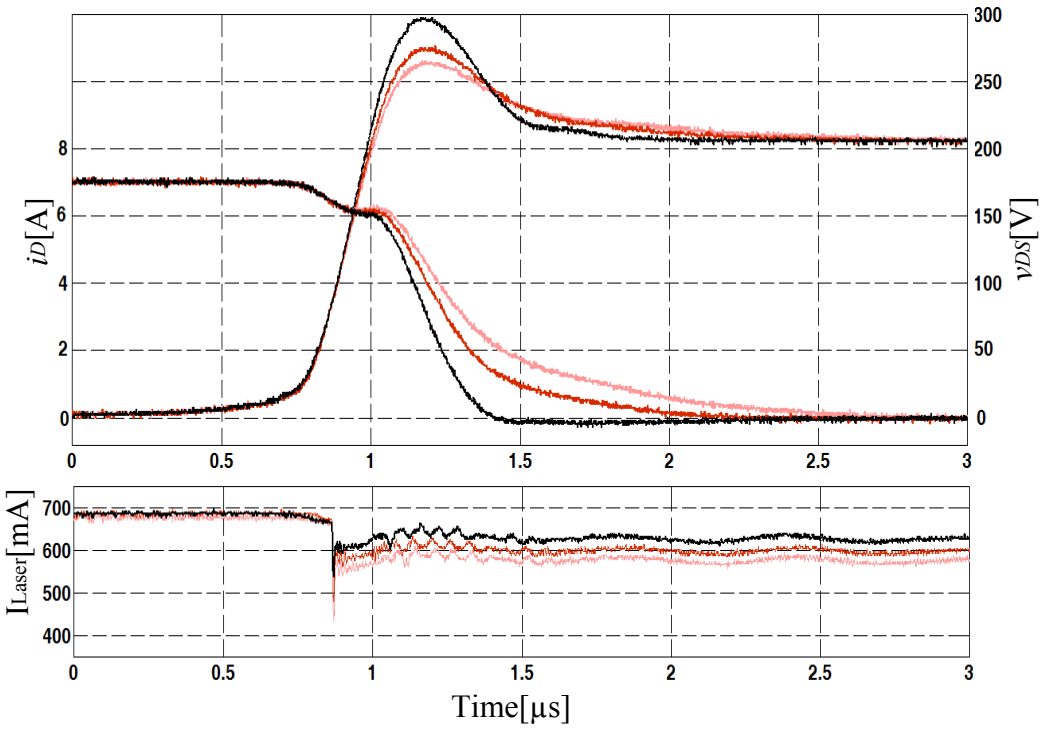


Fig. 20. Measured turn-off waveform of v_{DS}, i_D and I_{Laser} with varied di_D/dt and a fixed dv_{DS}/dt for the high-side drive case.

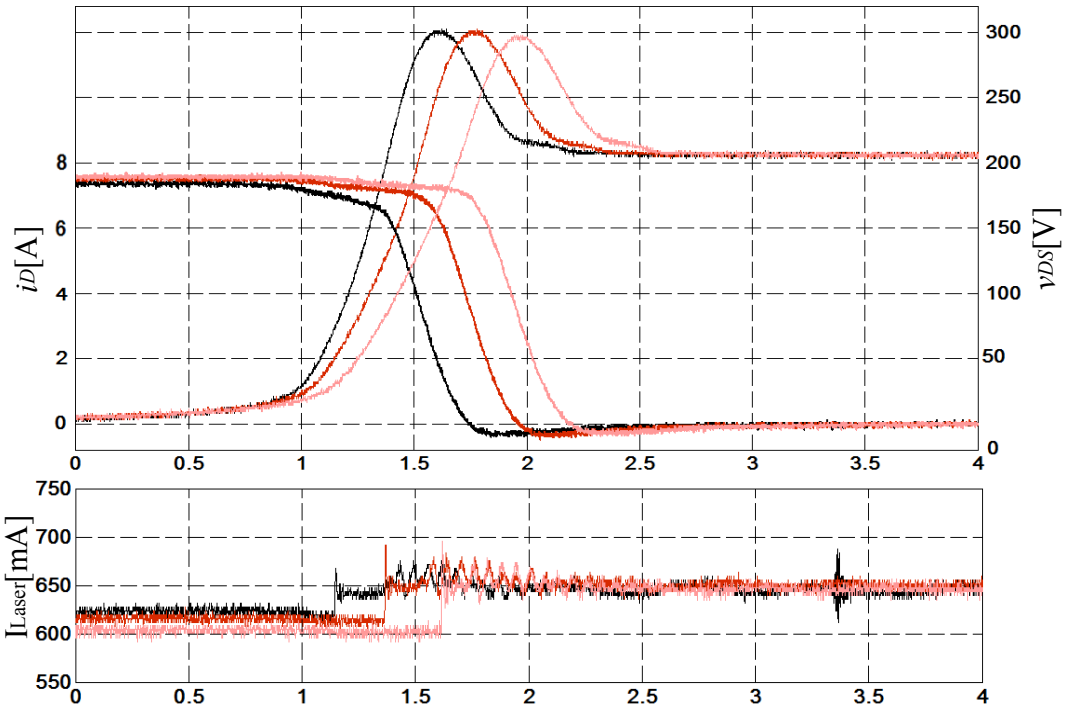


Fig. 21. Measured turn-off waveforms of v_{DS}, i_D, and I_{Laser} with varied dv_{DS}/dt and a fixed di_D/dt for the high-side drive case.

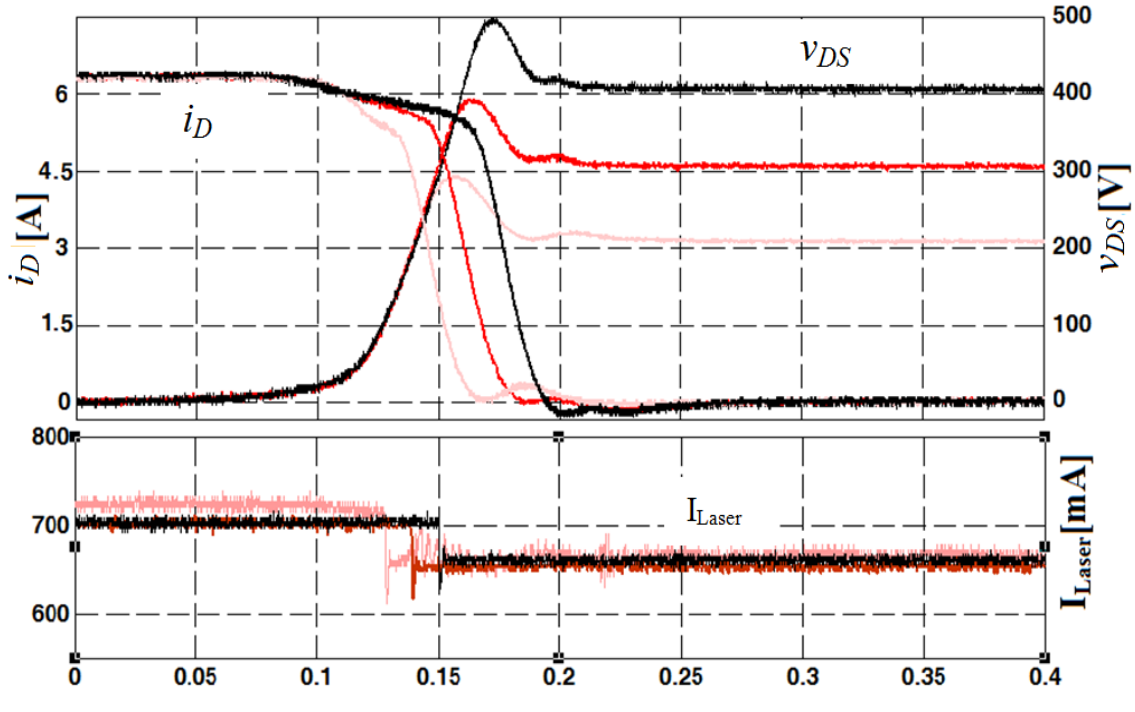


Fig. 22. Measured turn-off waveform of v_{DS}, i_D, and I_{Laser} for different bus voltages, ©2015 IEEE.

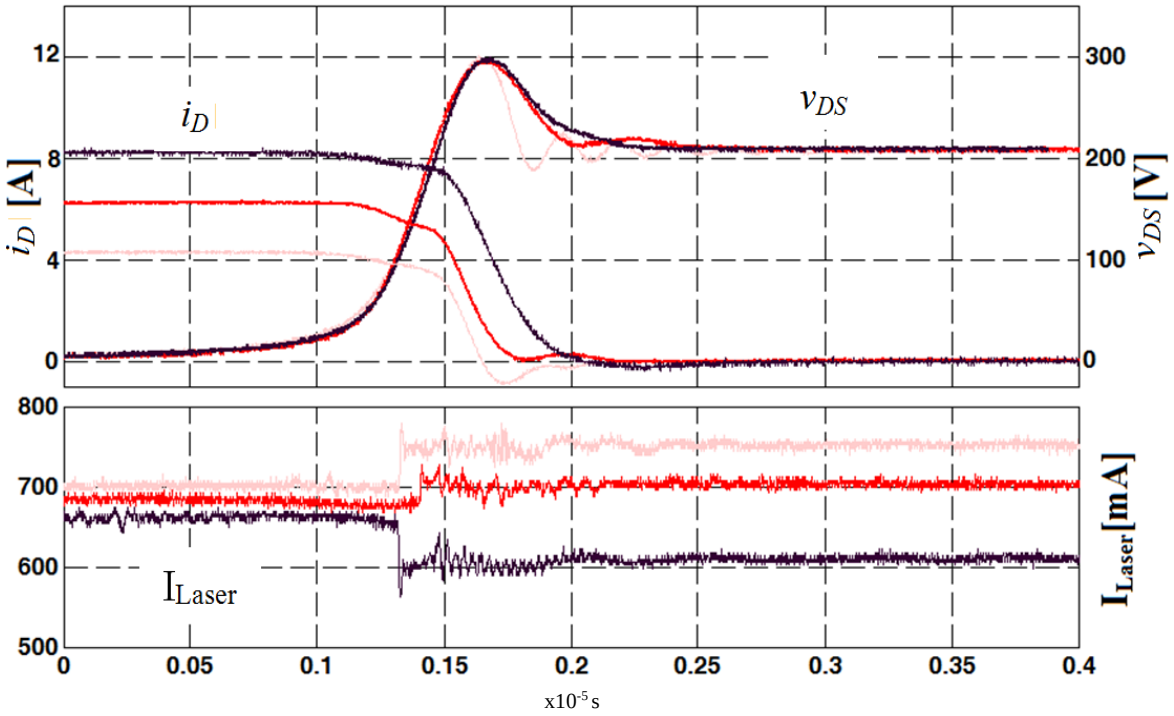


Fig. 23. Measured turn-off waveforms of v_{DS}, i_D, and I_{Laser} for different load currents, ©2015 IEEE.

To verify the control circuit adaptability in different operating conditions, the v_{DS}, i_D, and I_{Laser} are measured for variation of the bus voltage and load current as depicted in Figs. 22 and 2-23, respectively. The control circuit naturally initiates the transition from the dv_{DS}/dt to the di_D/dt control region by changing the current levels of the laser driver at the desired points, taking into account the loop delay as discussed earlier. According to (1) and (4), and considering the same load and thermal conditions, the output-current level of the laser driver remains approximately constant in each of the regions of control for different bus voltages to attain the same dv_{DS}/dt and di_D/dt, as shown in Fig. 22. Similarly, to attain the same dv_{DS}/dt and di_D/dt for different load currents, I_{Laser} decreases in each region of control as the load current increases, which is depicted in Fig. 23.

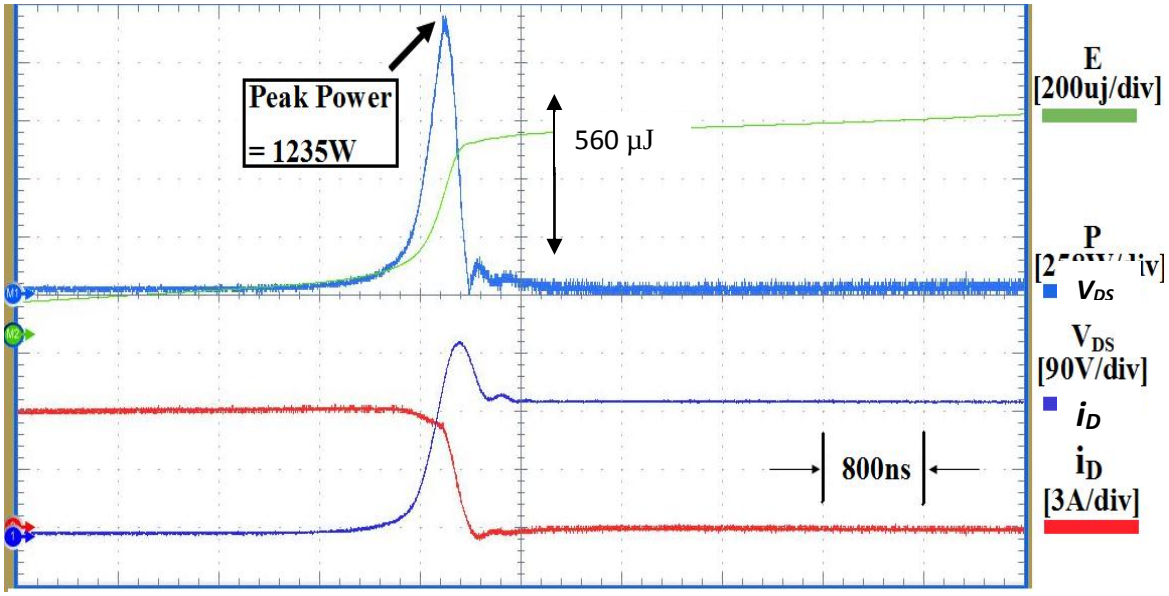


Fig. 24. Measured switching loss and energy for conventional approach [16] to driving the gate. In this approach, the intensity of the optical beam for OTPT2 is kept constant in the dv_{DS}/dt and di_D/dt regions of control, ©2015 IEEE.

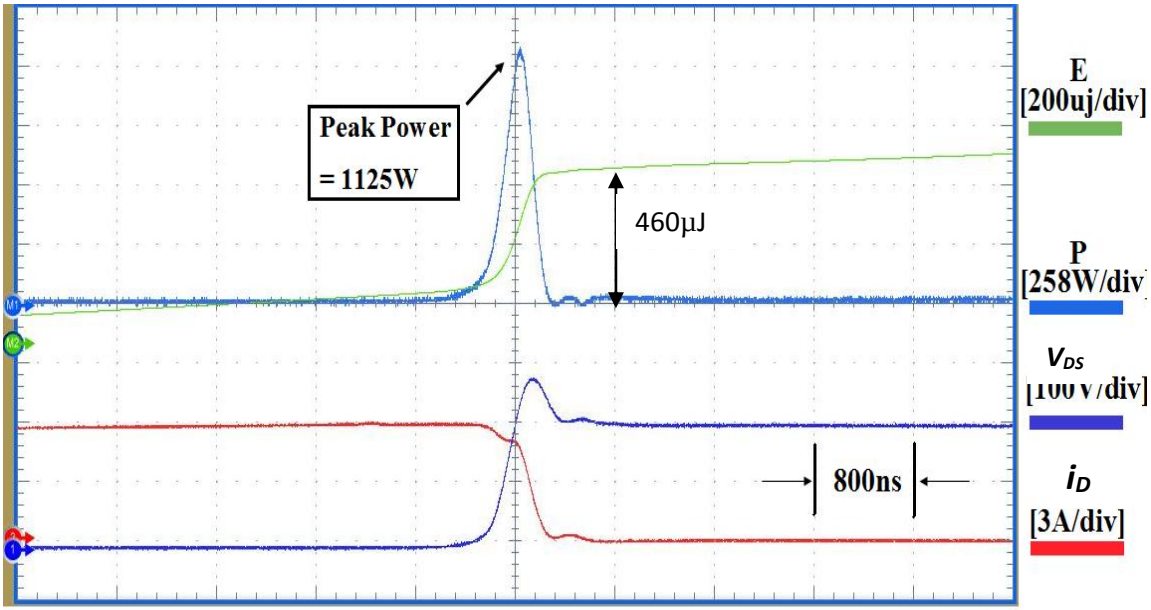


Fig. 25. Measured switching loss and energy for the proposed optical-transition controller. The peak-power reduction of 110 W along with the switching-energy reduction of 100 µJ and 17% reduction of overvoltage stress are achieved using the optical-transition controller as compared to the conventional gate drive, ©2015 IEEE.

The measured turn-off switching losses and energy obtained using a conventional approach to drive the gate and that obtained using the proposed optically-switched transition controller are shown in Figs. 24, and 25, respectively. The intensity of the optical beam for OTPT2 is kept constant in the two regions of control for the conventional approach, similar to the proposed approach in [61]. This emulates the discharge of the gate of M1 under condition of fixed gate resistance for dv_{DS}/dt and di_D/dt regions of control. In contrast, for the proposed controller, the dv_{DS}/dt and di_D/dt are so adjusted such that not only the peak-power loss and switching energy are reduced but the peak overvoltage stress is decreased as well compared to the results obtained using the conventional approach. Using the new controller, the peak-power reduction of 110 W along with the switching-energy reduction of 100 µJ and 15 V reduction of overvoltage stress are achieved. This is achieved in part by increasing the dv_{DS}/dt. Furthermore, the di_D/dt is slightly decreased to reduce the peak voltage stress and minimize the adverse effect of the reduction of di_D/dt on the switching loss.

In the case of maximum di_D/dt of 43A/µs in 6A load current and using the flowchart of Fig. 10, the Δt is selected to be 150ns and implemented in the control circuit. Therefore, the dv_{DSmax}/dt is calculated to be equal to 1030V/µs in 200V, based on the explained procedure in section II-A-2 and using (21). The minimum dv_{DSmax}/dt for the case of maximum di_D/dt is around 200V/µs, and the minimum di_D/dt for the case of maximum dv_{DSmax}/dt is around 4.7A/ µs, based on Figs. 13 and 9, and using (11), (4) and (15).

C. Conclusion

A novel unified independent dv/dt and di/dt control of an optically-triggered (OT) hybrid power semiconductor device (PSD), which contains a SiC MOSFET as the main PSD and

two GaAs-based OT power transistors (OTPTs) as the gate driver, has been outlined. It has been shown that the unified control of turn-off dv_{DS}/dt and di_D/dt is achieved by modulating the optical intensity of the OTPT2 using a single circuit. Independent control of dv_{DS}/dt and di_D/dt is achieved by predicting the onset of transition between the corresponding control regions using the unified control circuit. The control circuit performance has been verified through experimental results over a wide operating range including variation of dv_{DS}/dt, di_D/dt, load current, and bus voltage. It has been shown that, the proposed optical controller is able to attain the desired switching-transition behavior using independent control of dv_{DS}/dt and di_D/dt, which is not possible in the conventional gate drivers. Although the new optical controller is designed for an OT PSD, the control concept is also applicable for ET PSDs where the delay of the event feedback-loop is significant compared to the total duration of the switching transition.

III. Closed-Loop Control of Turn-off Transition of High-Voltage SiC MOSFETS

(Parts of this section, including figures and text, are based on my paper [74], ©2015 IEEE)

A. Introduction

Wide band-gap (WBG) PSDs, such as SiC MOSFETs, are the promising candidates to replace the existing Si-based PSDs in the modern power electronics applications. The reason is the superior properties of the WBG PSDs including higher voltage-blocking capability, better thermal performance, lower on-state resistance, and better switching performance [71]-[73]. Although high switching speed of the SiC MOSFETs has the benefit of increasing the power density, it may cause EMI and stress problems. High switching speed of the SiC MOSFETs results in adverse current and voltage slopes (*di/dt* and *dv/dt*, respectively). High *dv/dt* is the primary source of the common mode (CM) noise in power electronics applications. On the other hand, adverse *di/dt* causes voltage and current overshoots and oscillations due to the parasitic elements and non-idealities in the commutation path, as well as the PSD. Consequently, it is essential to control the switching *dv/dt* and *di/dt* of SiC MOSFETs to reach an optimal performance in terms of switching loss, device stress, and electro-magnetic interference (EMI).

Si MOSFETs are conventionally used in low-voltage high-frequency applications while the Si IGBTs are used in high-voltage low-frequency applications. Therefore, the amount of the generated *dv/dt* using the Si PSDs is usually not in the range that becomes problematic. Hence, focus of the state of the art methods on controlling the switching transition are more towards controlling the switching *di/dt* rather than the switching *dv/dt*. However, by recent introduction of high-voltage high-speed SiC MOSFETs in the market, it is equally important to control the

switching *dv/dt*, as well as the switching *di/dt*, to reach an optimal performance in terms of loss, device stress, and EMI. Therefore, a closed-loop gate driver for high speed SiC MOSFETs is presented in this Chapter. The proposed method dynamically and independently adjusts the *di/dt* and *dv/dt* of the turn-off transition using the closed-loop control of the gate current. The proposed controller also compensates the total delay in the feedback loop and initiates the transition between *dv/dt* and *di/dt* control regions to ensure the independent controllability of *dv/dt* and *di/dt*.

B. Proposed Closed-Loop Gate Driver

Key waveforms of a MOSFET during the turn-off transition and under inductive load are shown in Fig. 26. Block diagram of the proposed control scheme is shown in Fig. 27. The proposed controller independently adjusts the turn-off dv_{DS}/dt and di_D/dt by closed-loop control of the gate current. It consists of the Closed-loop gate driver, Reference selector and the Delay compensator circuit (DCC). Schematic of the Reference selector circuit and DCC are, respectively, shown in Fig.28 and Fig. 29. The closed-loop gate driver sets the gate current in each control region based on the corresponding reference voltage:

$$i_G = \begin{cases} v_{ref,dv/dt}.Kg & ,in\ the\ dv/dt\ \ control\ region \\ v_{ref,di/dt}.Kg & ,in\ the\ di/dt\ \ control\ region \\ v_{ref,on}.Kg & ,in\ turn-on\ transition \end{cases} \quad (1)$$

In (1), $v_{ref,di/dt}$ is the reference voltage in the *di/dt* control region, $v_{ref,dv/dt}$ is the reference voltage in the *dv/dt* control region, $v_{ref,on}$ is the reference voltage in the turn-on transition, and *Kg* is a circuit dependent feedback gain. Substituting (1) in equations (7) and (15) from chapter I, the *dv/dt* and *di/dt* are respectively adjusted using the following relations:

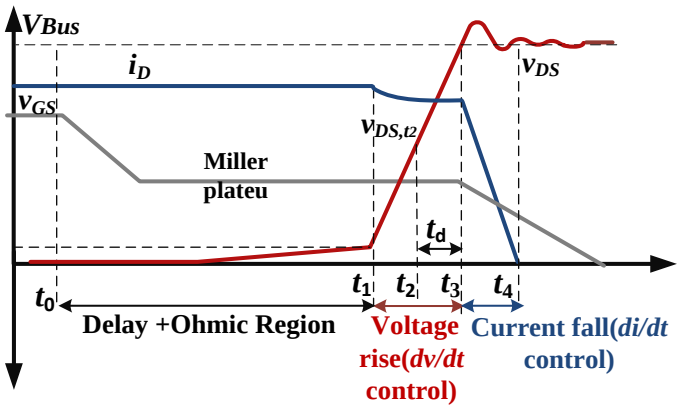


Fig. 26. Key waveforms of the MOSFET (M1) during turn-off, , ©2015 IEEE.

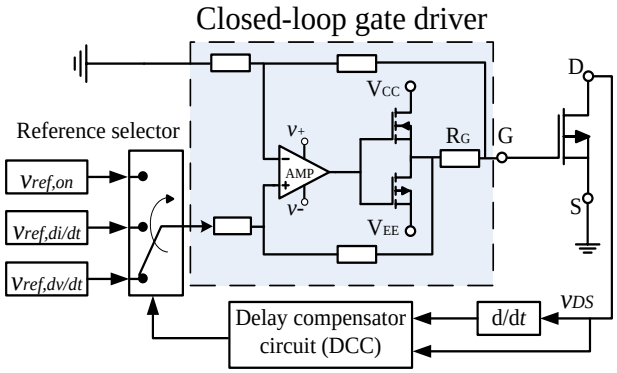


Fig. 27. Block diagram of the proposed control scheme, ©2015 IEEE.

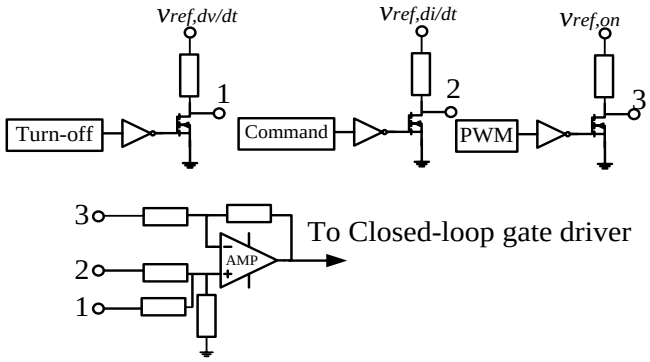


Fig. 28. Schematic of the Reference selector circuit, ©2015 IEEE.

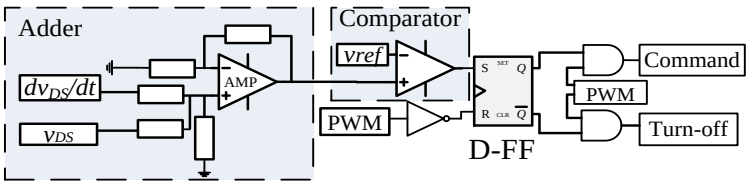


Fig. 29. Schematic of the Delay compensator circuit (DCC) , ©2015 IEEE.

$$\frac{dv_{DS}}{dt} = \frac{v_{ref,v} \times Kg}{C_{GD}} \tag{2}$$

$$\frac{di_D}{dt} = -\frac{v_{ref,i} \times Kg}{C_{GS}} \cdot g_{fs} \tag{3}$$

The reference voltages in each regions of control are provided for the closed-loop gate driver by the Reference selector circuit. The DCC initiates the onset of transition between the two regions of control. The onset of transition is initiated in the proper time considering the total delay in the feedback loop. The onset of turn-off *di/dt* is detected by sensing the voltage drop across the Kelvin emitter of the IGBT in the conventional Si-based AGD circuits. This voltage drop is then fed back to the control circuit to initiate the transition between the *dv/dt* and *di/dt* control regions. However, this method cannot be adopted to be used together with the high-speed SiC MOSFETs. The reason is that the feedback-loop delay cannot be neglected comparing to the total transition duration of the SiC MOSFETs. Therefore, a Delay compensator circuit is designed to compensate the delay in the feedback loop and predict the start of the turn-off *di/dt* region as shown in Fig. 29. The DCC then sends the Command to the Reference selector to change the reference value from $v_{ref,dv/dt}$ to $v_{ref,di/dt}$. Taking into account the total delay in the feedback loop, The DCC sends the command to change the reference value earlier than the

beginning of the *di/dt* control region. Assuming the constant total delay of t_{delay} in the feedback loop and according to Fig. 26, the following equation holds:

$$v_{DS,t2} + (dv_{DS,t2}/dt).t_{delay} = V_{Bus} \quad (4)$$

Equation (4) is used to design the Delay compensator circuit. The sensed v_{DS} and dv_{DS}/dt are added with appropriate coefficients. Subsequently, the result is compared to the sensed bus voltage (V_{ref}). Result of the addition of v_{DS} and dv_{DS}/dt always becomes higher than V_{ref} at t_{delay} seconds before the onset of the *di/dt* control region. The onset of *di/dt* control region also coincides with the moment at which the v_{DS} reaches the V_{Bus}. If output of the Adder is higher than V_{ref}, the DCC generates the Command for the Reference selector. Reference selector then, changes the reference voltage from $v_{ref,dv/dt}$ to $v_{ref,di/dt}$. When the command has been received from the DCC, the Reference selector activates the voltage level $v_{ref,di/dt}$ and deactivates the voltage level $v_{ref,dv/dt}$. The Reference selector circuit provides a negative single-level reference voltage for the gate driver during the turn-on transition. The reference voltage during the turn-on transition is negative since the direction of the gate current during the turn-on transition is opposite of the direction of the gate current during the turn-off transition. The reference voltage during the turn-on transition is also adjustable. Therefore, one can adjust the dv_{DS}/dt or di_D/dt during the turn-on transition. Using the same reference value for both turn-on *di/dt* and *dv/dt*, the value of turn-on dv_{DS}/dt depends on the value of turn-on di_D/dt and vice versa.

C. Experimental Results

A prototype of the proposed control scheme including the closed-loop gate driver, DCC and Reference selector circuit, along with a clamped-inductive test circuit was developed as shown in Fig. 30. The prototype of Fig. 30 is used to obtain the following experimental results.

Fig. 30. Fabricated prototype of the proposed closed-loop active gate driver along with the clamped-inductive test circuit of Fig.26. A part of the board is used to derive the results. Rest of the board is used to derive the results of chapter four, ©2015 IEEE.

Two CREE CMF10120D SiC MOSFETs (1.2 kV, 24A) are used in the half-bridge configuration to form the clamped-inductive test circuit in the fabricated prototype. Results are derived using a digital oscilloscope and plotted using MATLAB software.

Experimental results of independent control of turn-off dv_{DS}/dt of the SiC MOSFET with the fixed di_D/dt are shown in Fig. 31. It is shown that the turn-off dv_{DS}/dt can be independently adjusted while the value of turn-off di_D/dt remains unchanged. Worthy to note that the amount of di_D/dt can be also adjusted as it will be shown in further results. The dv_{DS}/dt have been selected to be 4 kV/µs, 2.3 kV/µs and 1.6 kV/µs . However, the value of di_D/dt has been kept at 150 A/µs. Because of the approximately same di_D/dt for the three study cases in Fig. 3-6, voltage overshoot is almost equal for those three cases. During the voltage rise region, a part of the load current is used to charge the parasitic capacitance across the drain-to-source terminals of the SiC MOSFET. Therefore, one can observe a slight decrease in the drain current during the voltage

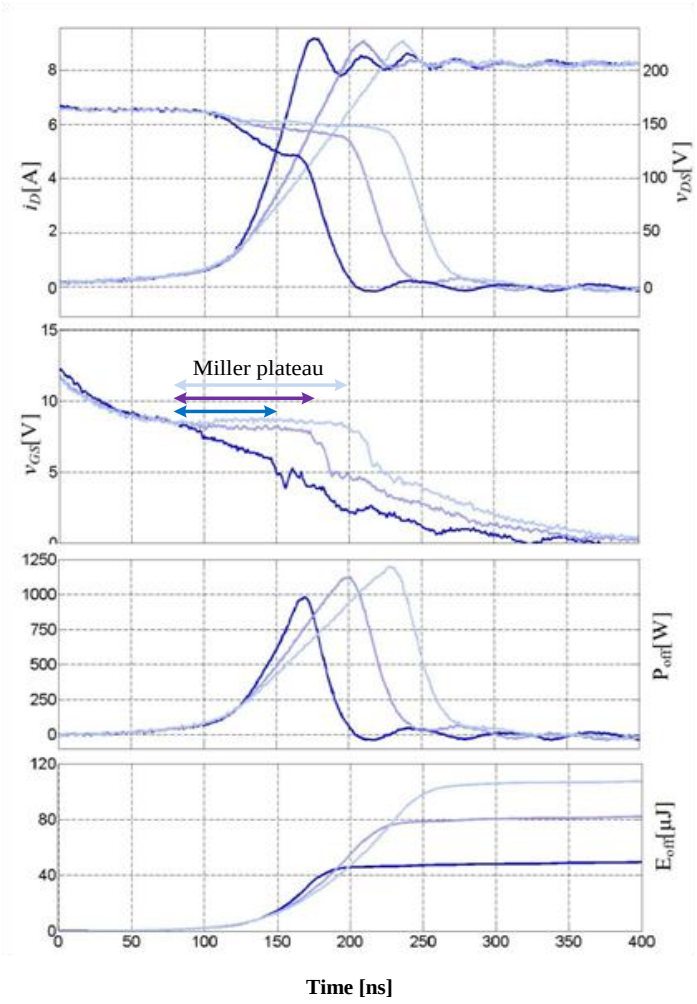


Fig. 31. Measured turn-on waveforms of v_{DS}, i_D and v_{GS} along with the calculated values for P_{off} and E_{off} while the voltage slope varies and current slope is fixed. The dv_{DS}/dts are selected to be: 4 kV/µs, 2.3 kV/µs and 1.6 kV/µs and di_D/dt is 150 A/µs, ©2015 IEEE.

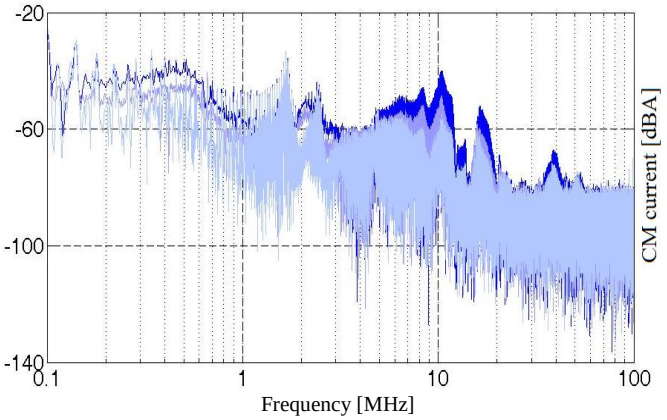


Fig. 32. Spectrum of the input CM current, ©2015 IEEE.

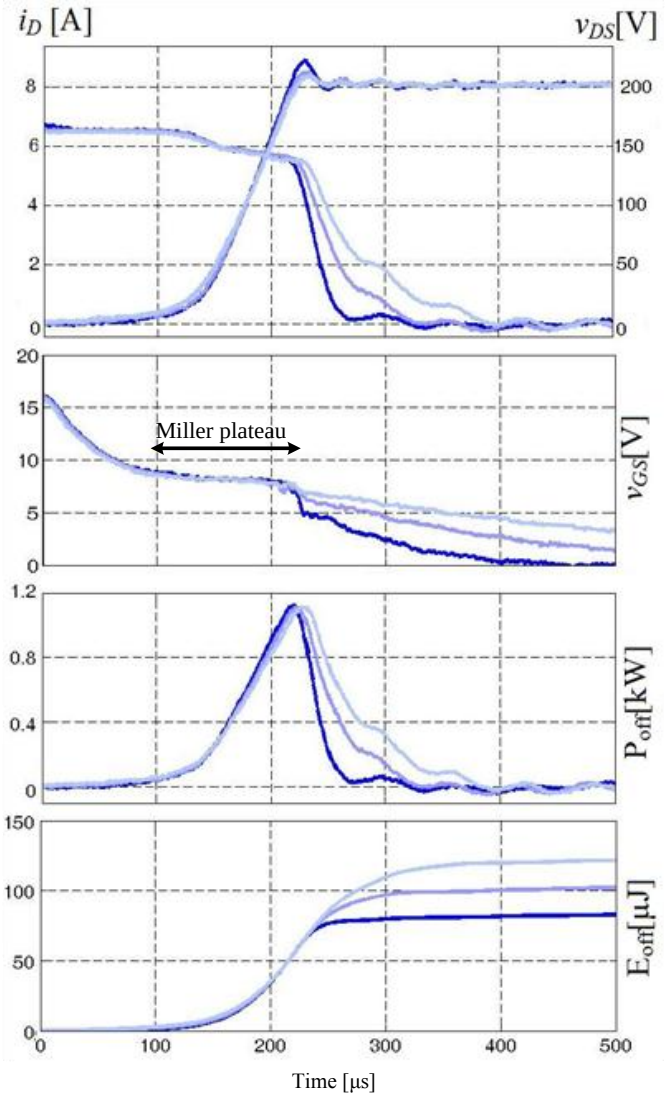


Fig. 33. Measured turn-on waveforms of v_{DS}, i_D and v_{GS} along with the calculated values for P_{off} and E_{off} while the current slope varies and voltage slope is fixed. The di_D/dts are selected to be: 150 A/μs, 75 A/μs and 45 A/μs and dv_{DS}/dt is 2.3 kV/μs**,** ©2015 IEEE.

rise interval. The higher is the slew rate of the v_{DS} the greater is the reduction in the drain current. Although the load current is the same for the study cases, different current levels during the voltage-rise interval results in different levels for the Miller voltage of the gate of the SiC MOSFET as shown in Fig. 31. Increasing the dv_{DS}/dt makes the Miller plateau to shrink as shown in Fig.31. As a result, the peak of turn-off switching power loss (Poff) is reduced and s

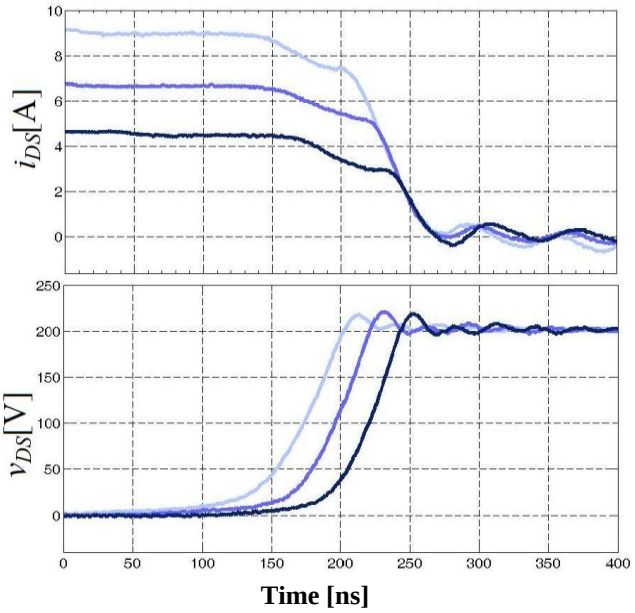


Fig. 34. Measured turn-off waveforms of v_{DS} and i_D for different load currents at di_D/dts=100 A/μs and dv_{DS}/dt= 3.75 kV/μs, ©2015 IEEE.

turn-off energy (Eoff) is diminished. Increasing the dv_{DS}/dt has the benefit of reducing the switching loss. However, it has the drawback of increasing the CM noise. Input CM current habeen measured, and the spectrum of the input CM current has been plotted in Fig. 32. According to Fig. 32, one can find a significant reduction in the magnitude of CM current around the frequency of 10 MHZ as the *dv/dt* decreases.

Experimental results of independent control of turn-off di_D/dt with the fixed dv_{DS}/dt are shown in Fig. 33. It is shown that the turn-off di_D/dt can be independently adjusted while the value of turn-off dv_{DS}/dt remains unchanged. The value of dv_{DS}/dt has been kept at 2.3 kV/μs for the tree study cases. However, the current slopes have been selected to be 150 A/μs, 75 A/μs and 45 A/μs. As the di_D/dt increases the amount of voltage overshoot increases. Because of the same dv_{DS}/dt for the three study cases in Fig. 33, the duration of Miller plateau as well as the level of the Miller voltage remains equal for the variation of di_D/dt. As the di_D/dt decreases the peak of P_{off} decreases but the turn-off energy increases.

To verify the proper operation of the proposed closed-loop gate driver, the proposed control has been tested in different load conditions as shown in Fig. 34. It has been shown that the dv_{DS}/dt and di_D/dt have been kept at a preselected value in different load currents. As a result, the voltage overshoots remain at the same value.

D. Conclusion

A novel closed-loop active gate controller for high-speed and high-voltage SiC MOSFETs has been outlined in this paper. The turn-off *dv/dt* and *di/dt* are adjusted by closed-loop control of the gate current in the corresponding control regions. Independent control of turn-off *dv/dt* and *di/dt* is achieved by means of a delay compensator circuit which compensates the total delay in the feedback-loop and changes the reference value for the closed-loop gate driver at the proper moment. The delay compensator circuit has enabled the dynamic and independent control of switching transition in the range of sub hundred nanoseconds. It has been shown that by independent controlling of both *di/dt* and *dv/dt* one can control the switching loss, device stress and EMI (e.g. CM noise).Therefore, an optimal switching performance in terms of switching loss, device stress and EMI is reachable. A prototype of the proposed AGC circuit was fabricated and tested to verify the feasibility of the control scheme.

IV. Self-Contained Control of Turn-on Transition of IGBTs

Parts of this section, including figures and text, are based on my paper [75], ©2014 IEEE)

A. Problem Identification

As outlined in chapter I, the work on independent control of *dv/dt* and *di/dt* of the switching transition has been limited in the literature. Therefore, Independent *dv/dt* and *di/dt* control of turn-off transition of power MOSFETs has been introduced in chapters 2 and 3. Furthermore, the presented concept in chapters II and III can be extended to IGBTs due to similar behavior in switching transition as described in chapter I. The presented work in chapter II is essentially a two-step controller. In this two-step controller, an optical intensity P_1 corresponds to the laser current of L_1 is transmitted into the base region of the OTPT in the turn-off delay and voltage-rise intervals to adjust the turn-off *dv/dt*. On the other hand, an optical intensity P_2 corresponds to the laser current of L_2 is transmitted into the base region of the OTPT in the turn-off current-fall interval to adjust the turn-off *di/dt*. In the turn-off transition, current fall region is followed in series with the voltage rise region. The proposed controller in chapter II assumes that the *dv/dt* is fixed during the voltage rise region and predicts the moment at which the current fall region starts considering the total delay in the feedback loop. The current fall region begins when the drain-to-source voltage of MOSFET reaches the Bus voltage. Therefore, the controller predicts the moment of transition by monitoring the drain-to-source voltage of MOSFET, the rate of change of it and Bus voltage. If one wants to adopt this approach for turn-on transition, the controller should monitor the *di/dt* (instead of *dv/dt* at turn-off), current passing through the PSD and the maximum current of the PSD (which is the onset of transition between *di/dt* and *dv/dt* control regions). The reason is that unlike the turn-off transition at which the *di/dt*

control region is followed by *dv/dt* control region, in the turn-on transition *dv/dt* control region is followed by *di/dt* control region. However, this approach cannot be extended to turn-on transition. This is due to the fact that, in the turn-on transition the *di/dt* varies continuously by changing the instantaneous current following through the PSD, during the current-rise region. Therefore the controller will have a significant error based on the assumptions and analysis in chapter II-A-2. Furthermore, the onset of the voltage fall region is the moment at which the current of the insulated gate PSD reaches its maximum value, and this maximum value is equal to the load current in addition to the peak reverse recovery current (IRR) of the free-wheeling diode (FWD). Therefore, unlike the bus voltage in the turn-off transition, which is a continuous signal and easy to measure and record, the peak IRR cannot be sampled easily to be used as a reference in the controller. As a result, predicting the onset of transition between *di/dt* and *dv/dt* control regions is not granted using the proposed method in chapter II. The other drawback of the presented work in chapter II is the lack of controllability over the turn-off delay. As outlined in chapter II, the same optical intensity is used in the turn-off delay and voltage rise intervals. Therefore, the turn-off delay is highly dependent on the *dv/dt* value. Therefore, by varying the *dv/dt* to reach the desired switching transition performance the turn-off delay also changes. Furthermore, the turn-off delay is also a function of temperature and load current. Hence, a change in the operating condition results in a change in the duration of the turn-off delay. This change in the turn-off delay affects the duty cycle of the PSD, which may interfere with the control of the converter, especially in high frequency operation. This situation even becomes worse while using the OTPT. This is due to the fact that the OTPT behaves like a current source in the delay interval. Therefore it prevents the commonly seen current spike in the gate current of

the PSD.As a result, the delay is significantly longer as compared to the conventional fixed resistance methods, as outline in chapter II.

A novel photonic control mechanism to control the turn-on transition of insulated gate power semi-conductor devices (PSDs) is outlined in this chapter. Turn-on transition control decreases the overshoot of current of PSD caused by the reverse-recovery current (IRR) of the free-wheeling diode (FWD) due to the high current slope .It also adjusts the turn-on *dv/dt* to control the switching loss and electro-magnetic interference (EMI) while keeps the PSD in the safe-operating area. Moreover, it controls and reduces the duration of the turn-on delay and voltage tail. Decreasing the voltage tail reduces the switching loss, and fixing the turn-on delay makes the duty-cycle-based slow-scale control simpler. In contrast to other works, the proposed control method independently adjusts the turn-on delay, turn-on *di/dt, and dv/dt* and voltage tail in different operating conditions. The onset of transition between the two adjacent control regions is determined using a self-contained control circuit. The error between the desired and actual onset of transition is compensated using a partially activated PI compensator. Another feature of the presented work is using a single optical link for both pulse-width modulation (PWM) and switching transition control of an optically-triggered drive system comprising an IGBT as the main PSD and a pair of GaAs-based optically-triggered power transistors (OTPTs) serving as the driver for the IGBT. The proposed control circuit operation and advantages are presented and verified by experimental results.

B. Control Mechanism for the Turn-on Transition

The standard clamped inductive test circuit and control block diagram for optical transition control is shown in Fig. 35. The test circuit comprises a bridge leg with an optically-

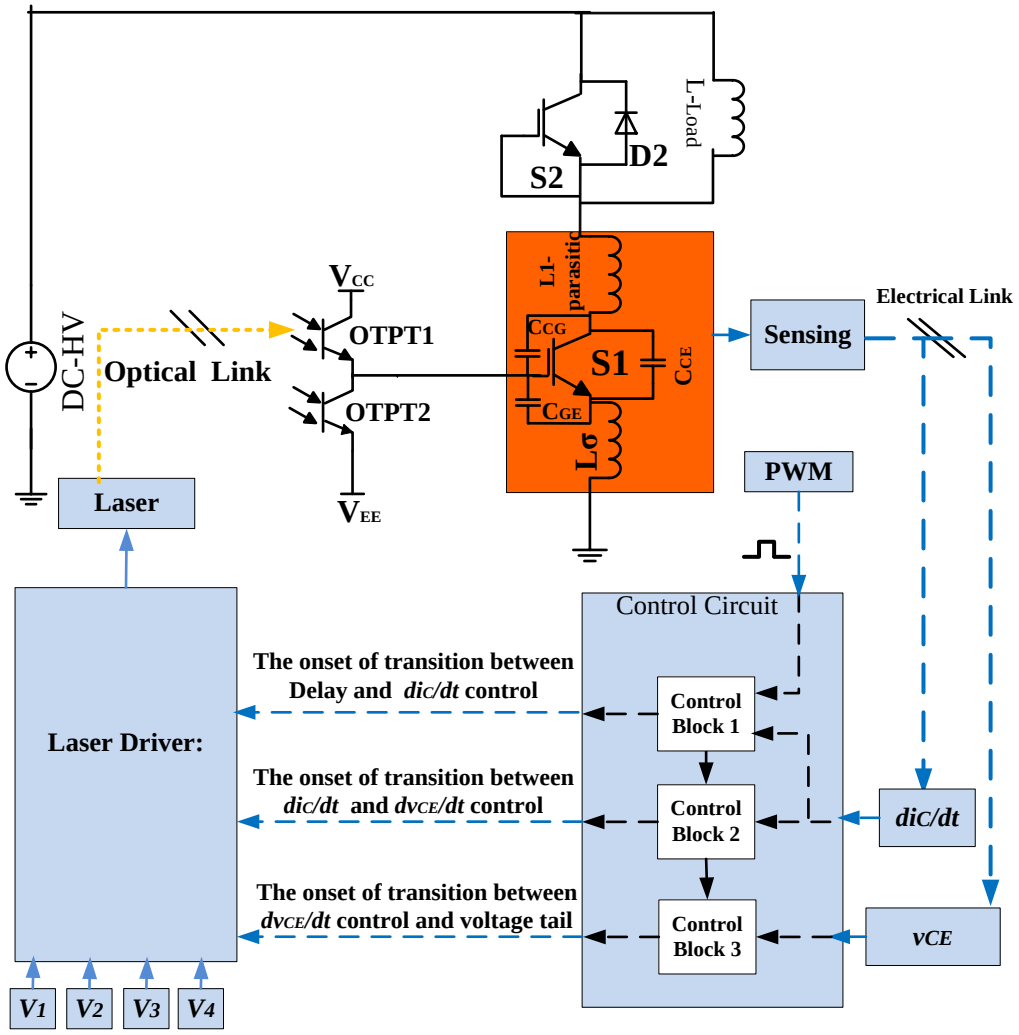


Fig. 35. Test circuit and control block diagram. *V*1, *V*2, V2 and *V*3, respectively, adjust the turn-on delay, the i_C/dt , dv_{CE}/dt and voltage tail of S1 in the turn-on delay, di_C/dt , dv_{CE}/dt and voltage tail-control regions of operation as illustrated in Fig. 4-2.

triggered IGBT (S1) in the low side and a self-gated IGBT (S2) in the high side. The bridge leg is the most widely used configuration in the hard-switched power- electronics applications. OTPT1 and OTPT2 are, respectively, used to charge and discharge the gate of S1. Internal anti-parallel diode of S2 is used as FWD which is marked as D2. OTPT1 and OTPT2 work complimentary and turn the (S1) on and off, respectively.

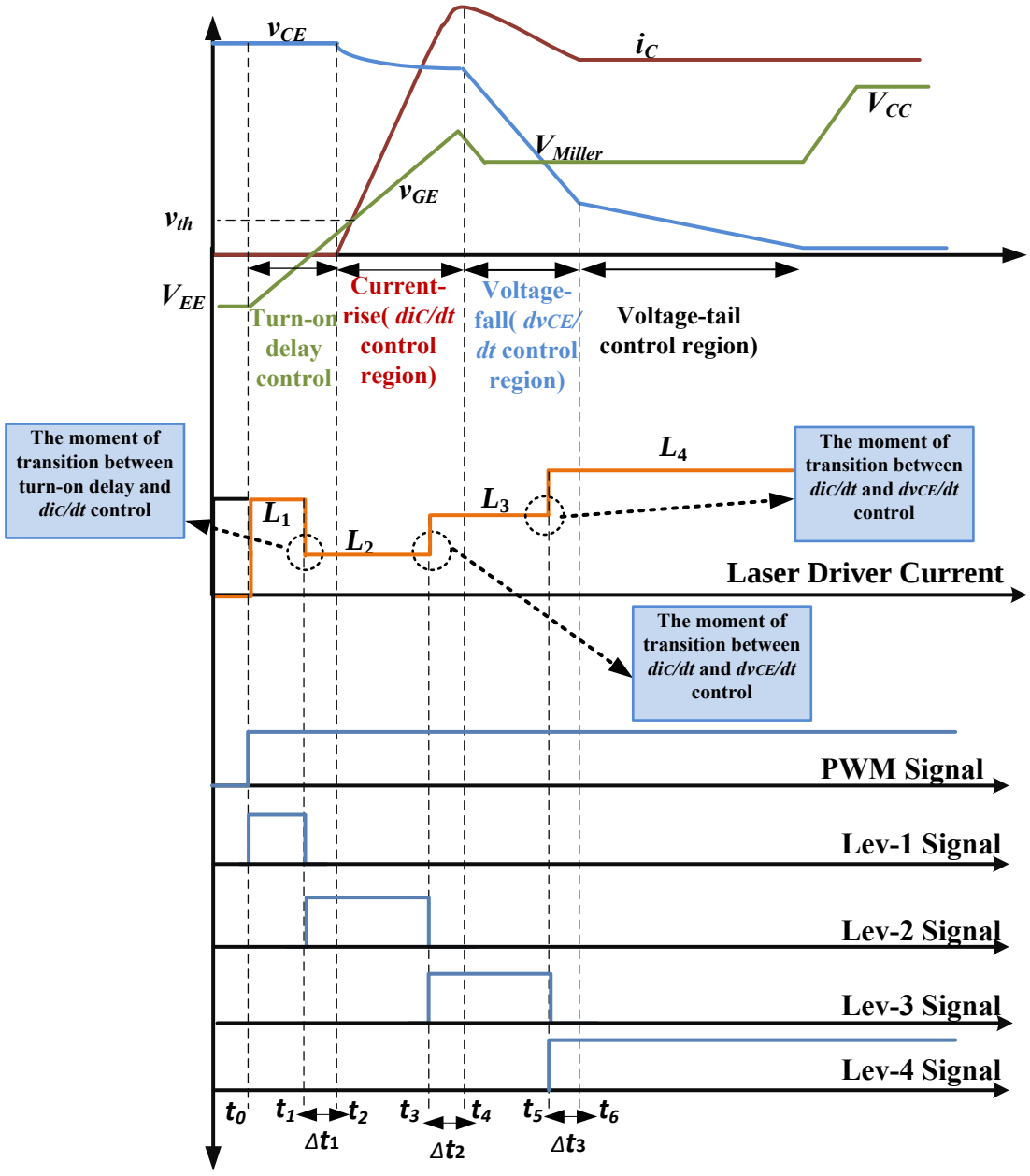


Fig. 36. Turn-on behavior of the IGBT and control circuit key waveforms. The output currents L_1, L_2, L_3 and L_4 of the Laser Driver are proportional to the voltage commands $V1$, $V2$, $V3$ and $V4$ which dictate the duration of the turn-on delay, di_C/dt , dv_{CE}/dt and voltage tail dynamics of S1 in the turn-on delay di_C/dt, dv_{CE}/dt, and voltage-tail control regions.

As indicated in Fig. 36, when the turn-on command is initiated by the PWM signal at t_0, the laser driver provides the current level L_1 (proportional to the external voltage control command V_1 shown in Fig. 35) for the laser with its wavelength centered at 808nm. The laser

delivers an optical power corresponding to the current level L_1 to the base region of OTPT1 via an optical link. Subsequently, OTPT1 turns-on allowing the input capacitance of S1 (C_{iss}) to be charged through it. The gate-to-emitter voltage (v_{GE}) of S1 starts to rise from V_{EE} until it reaches the gate threshold voltage (v_{th}) at t_2; this interval (the interval between t_0 and t_2) is referred to as the turn-on delay interval. The duration of the turn-on delay interval is derived by the following relation:

$$\text{Turn-on delay} = t_2 - t_0 = C_{iss}.\frac{v_{th}-V_{EE}}{i_G} \quad (1)$$

According to (1), turn-on delay can be adjusted by controlling the gate current. The latter, in turn, can be adjusted by varying the optical intensity of OTPT1 which is proportional to V_1. Subsequently, the collector-to-emitter current (i_C) of S1 starts to rise and the load current transfers from D2 to S1. The slope of the collector-to-emitter current (di_C/dt) of S1 at the moment when the sign of the current of D2 changes is derived by the following relation:

$$\frac{di_c}{dt} \approx \frac{V_{CC}-v_{th}-I_{L0}/g_m}{R_{OTPT1}.C_{GE}/g_m+L_\sigma} \quad (2)$$

In (2), L_σ is the inductance seen from the emitter of S1, g_m is the forward trans-conductance of the S1, C_{GE} is the gate-to-emitter capacitance of S1, V_{CC} is the positive bias voltage of the gate circuit, I_{L0} is the load current and R_{OTPT1} is the effective resistance of OTPT1. According to (2), di_C/dt in this interval can be controlled by adjusting the resistance of OTPT1.The latter in turn can be controlled by varying the optical intensity of OTPT1 which is proportional to V_2 as stated earlier. The peak-reverse-recovery current of D2 (IRR_{Peak}) is a function of di_C/dt, load current and temperature (T) :

$$IRR_{Peak} = (\frac{di_C}{dt})^{1/2}.f(I_{L0}, \text{T}) \quad (3)$$

Independent controllability of turn-on delay and di_C/dt requires the resistance of OTPT1 to change at the moment at which the current-rise interval starts at t_2. Therefore, the change in the optical intensity of OTPT1 shall be initiated earlier than t_4 considering the total delay in the feedback loop and OTPT related delays. Assuming the total delay of Δt_2 seconds in the feedback loop and OTPT, it is desirable that the current level of the laser driver changes at t_1 as shown in Fig. 36. t_1 is Δt_1 seconds earlier than t_2. When i_C reaches the load current plus IRR_{Peak} at t_4, D2 starts blocking the voltage and the collector-to-emitter voltage (v_{CE}) of S1 starts to fall. During the fall phase of v_{CE}, the v_{GE} stays constant at the Miller voltage level (V_{Miller}). The Miller voltage level is dependent on the load current. Therefore, the slope of the collector-to-emitter voltage of S1 is expressed by the following equation:

$$\frac{dv_{CE}}{dt} \cong -\frac{V_{CC}-v_{th}-I_{L0}/g_m}{R_{OTPT1}.C_{GC}} = -\frac{V_{CC}-V_{Miller}}{R_{OTPT1}.C_{GC}} \quad (4)$$

In (4), C_{GC} is the gate-to-collector capacitance of S1 (also known as Miller capacitance). According to (4), dv_{CE}/dt in this interval can be controlled by adjusting the optical resistance of OTPT1. The latter in turn can be controlled by varying the optical intensity of OTPT1. On the other hand, the optical intensity of OTPT1 is set by the current level of the laser driver L_3 (which is proportional to the external voltage control command V_3 shown in Fig. 35). Therefore, one can conclude that the current level L_2 of laser driver controls di_C/dt, while current level L_3 controls dv_{CE}/dt.

Independent controllability of di_C/dt and dv_{CE}/dt requires that the resistance of OTPT1 changes at the moment at which the voltage-fall interval starts at t_4. Therefore, the change in the optical intensity of OTPT1 shall be initiated earlier than t_4 considering the total delay in the feedback loop and OTPT related delays. Assuming the total delay of Δt_2 seconds in the feedback

loop and OTPT1, it is desirable that the current level of the laser driver changes at t_3 as shown in Fig. 36. t_3 is Δt_2 seconds earlier than t_4.

According to (4) dv_{CE}/dt is inversely related to the value of C_{GC}. However, C_{GC} in IGBTs usually tends to be nonlinear such that the C_{GC} dramatically increases at lower voltages. This nonlinear behavior is similar to what was observed earlier in Power MOSFETs in chapter II. Significant increment of C_{GC} in lower voltages causes alleviation in the amount of dv_{CE}/dt which leads to a tail in the collector-to-emitter voltage during the turn-on transition. This voltage tail generates an excessive amount of switching loss which is not desirable. Effective resistance of OTPT1 can be decreased in this region to increase the dv_{CE}/dt and decrease the switching loss. This is achieved through detecting the voltage tail region, which starts at t_6, and increasing the optical intensity in this control region by increasing the current to current level (L_4).

In order to independently control the turn-on delay, di_C/dt, dv_{CE}/dt and voltage tail, the control needs to initiate the transition between these regions of control at a proper moment. These transitions shall be initiated by the control circuit earlier than the actual onset of transition considering the total delay in the OTPT1 and feedback loop. The proposed control system is comprised of three control blocks that are responsible for the three onsets of transitions between the four control regions. Control block-1 guarantees the independent control of the turn-on delay and turn-on di_C/dt by initiating the transition at a proper time. Control Block-2 and Control-Block-3 are respectively responsible for transition from di_C/dt to dv_{CE}/dt control regions and dv_{CE}/dt to voltage tail control regions ensuring independent controllability of di_C/dt, dv_{CE}/dt and the voltage tail. As the control blocks predict the onsets of transitions, they send the commands to the laser driver to adjust the optical intensity of the laser. These adjustments are made

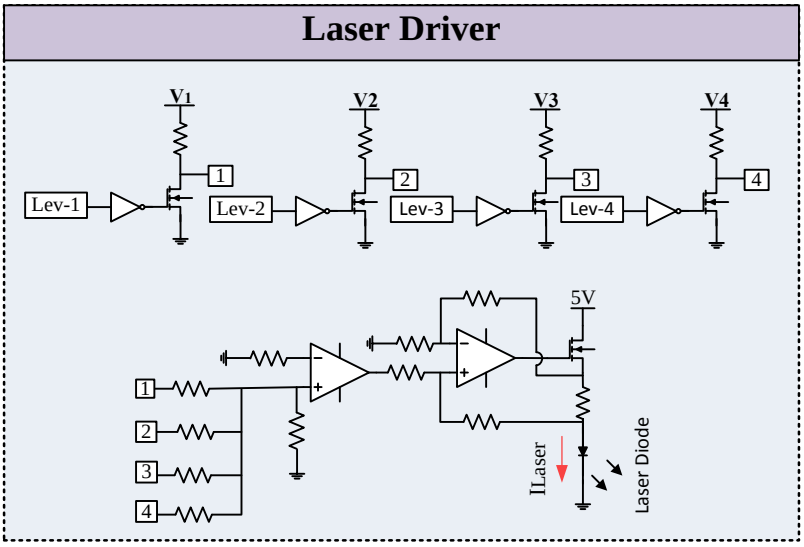


Fig. 37. Schematic of the Laser Driver circuit. *V*1, *V*2, *V*3 and *V*4, respectively, control the turn-on delay, di_C/dt, dv_{CE}/dt and voltage tail in their respective control regions.

according to the requirements of the each control region and at a time prior to actual onset of transition considering the delays.

The effective resistance of OTPT1 is controlled independently in each region of control to gain a desired performance. Controlling the resistance of OTPT1 is achieved through modulating the optical intensity to the base region of OTPT1. The optical intensity is determined by the amount of current passing through the laser.

The Laser Driver is a voltage-to-current converter which sets the output current through the laser proportional to its input voltage. Schematic of the Laser Driver is shown in Fig. 37. The output current through the laser is given by the following equation:

$$\mathrm{I_{Laser}} = \begin{cases} \alpha.V_1 = L_1 & ,\text{when Lev} - 1 \text{ signal is high} \\ \beta.V_2 = L_2 & ,\text{when Lev} - 2 \text{ signal is high} \\ \gamma.V_3 = L_3 & ,\text{when Lev} - 3 \text{ signal is high} \\ \rho.V_3 = L_4 & ,\text{when Lev} - 4 \text{ signal is high} \\ 0 & ,\text{when PWM signal is low} \end{cases} \quad (5)$$

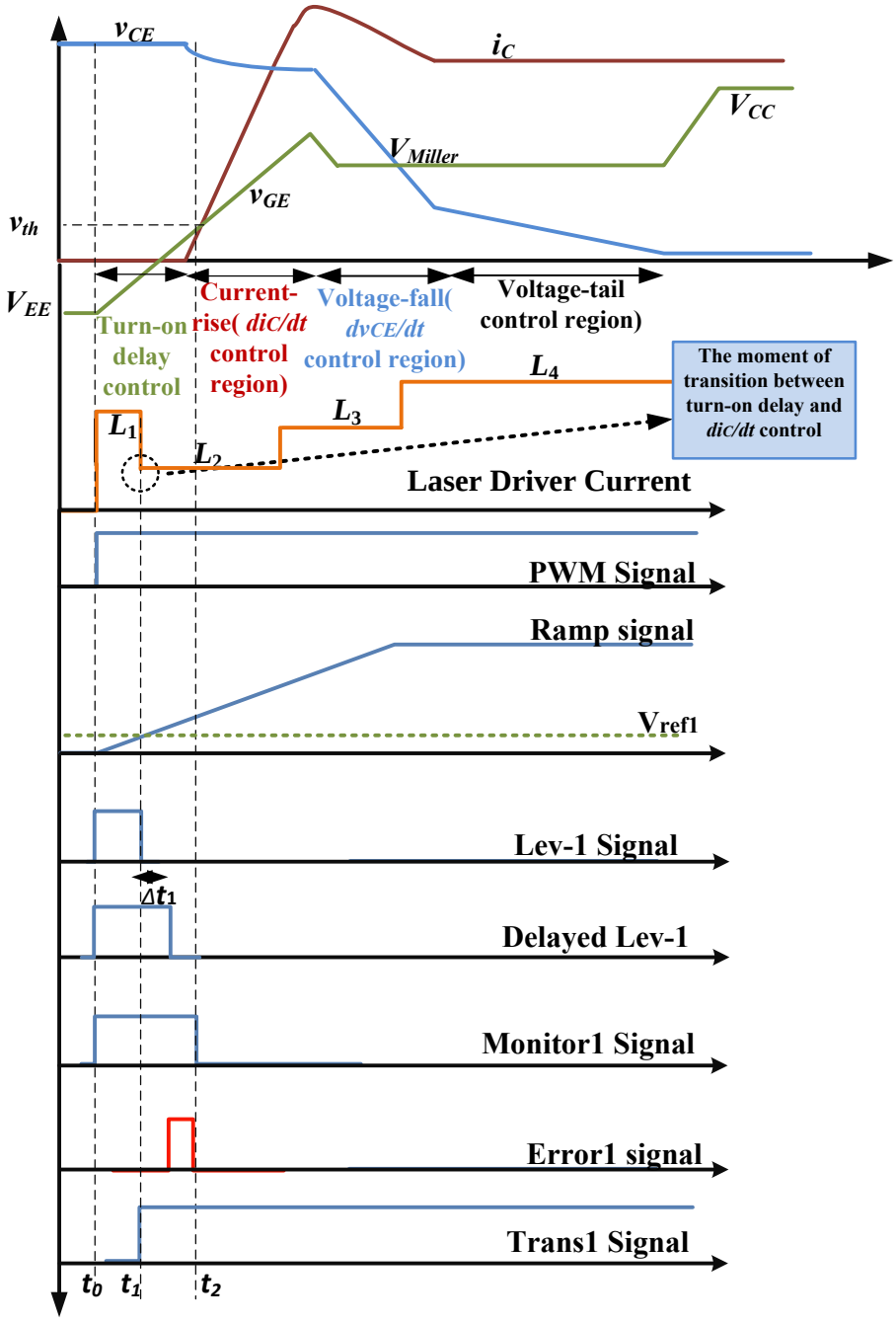
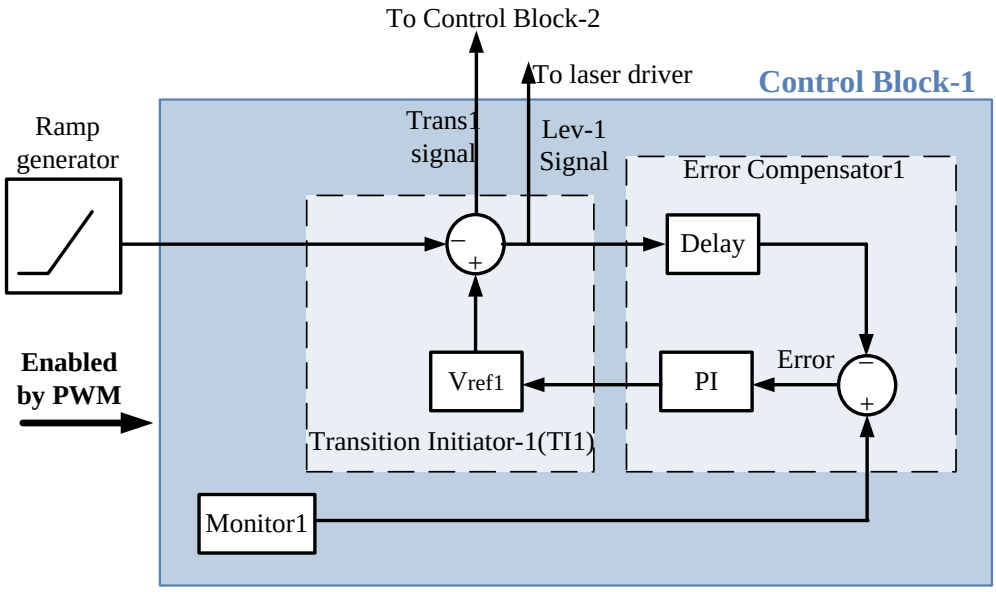
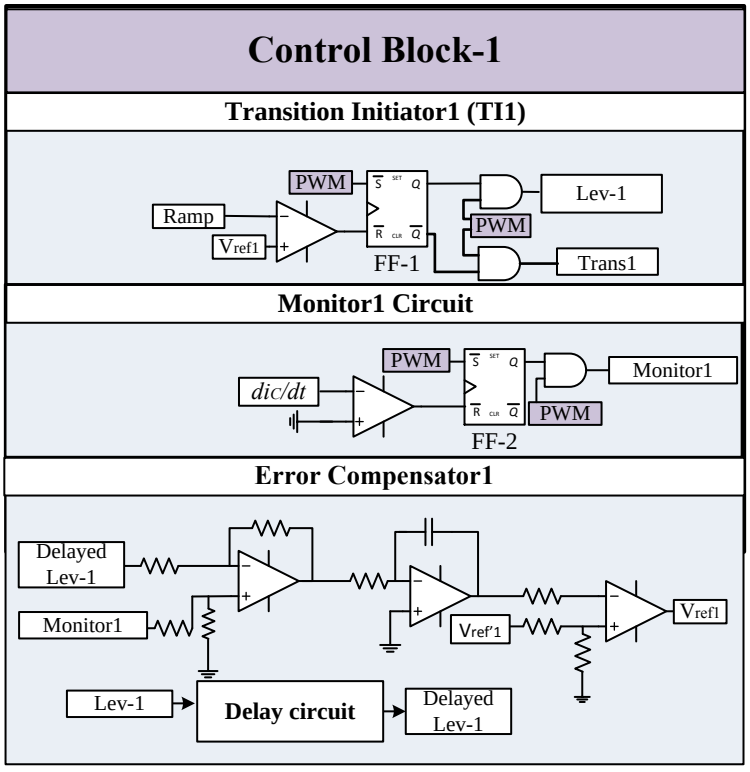


Fig. 38. Turn-on behavior of the IGBT and Control Block-1 key waveforms.

In (5), α, β, γ and ρ are circuit-dependent constants.



(a)



(b)

Fig. 39. Control Block1: (a) Block diagram, (b) schematic. Control Block1 comprises of Transition Initiator1 circuit, Monitor1 circuit and Error Compensator1 circuit, ©2015 IEEE.

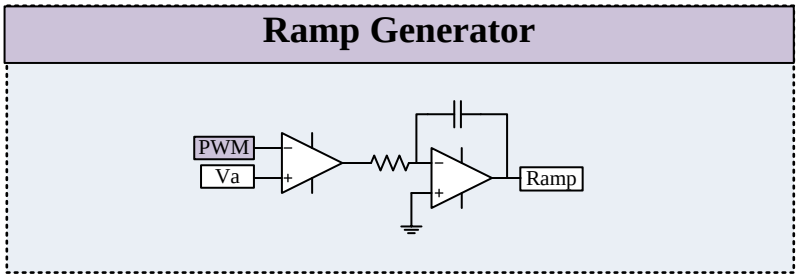


Fig. 40**.** Schematic of the Ramp Generator circuit. Ramp Generator circuit is a major component of each three control blocks ©2015 IEEE.

Control Block-1 Major waveforms, block diagram, and circuit schematics are respectively shown in Figs. 38-39(b). When the turn-on command initiates by setting the PWM signal to H logic state, the ramp generator generates a ramp signal as shown in Fig. 38 .This ramp is used as a major component for the three control blocks. This ramp signal starts from zero and eventually hits the positive rail and stays there as long as the PWM signal is at H state. When the PWM signal resets to L state, the output value of the ramp generator also sets back to its negative rail. The slope of the ramp should be selected such that the ramp hits the positive rail after the turn-on switching transition has completed. Schematic of the ramp generator circuit is shown in Fig.40 .It is comprised of a comparator and an op-amp-based integrator.

As the PWM signal sets to H state, the Lev-1 signal and Monitor-1 signal are also set to H state. Lev-1 signal is the output of the Transition Initiator1 (TI1) circuit of the Control Block-1, and Monitor-1 Signal is the output of the Monitor1 circuit of the CB1, as shown in Figs. 38, and 39(b). Subsequently, Lev-1 signal activates the input voltage *V1* of the Laser Driver; and laser driver provides the current level of $\alpha V1$ for the laser. This current provides an optical intensity of *P1* at the base region of OTPT1 and turns it on. Gate of S1 is charged at a rate relative to *P*1. According to Fig. 38, when the value of the ramp signal becomes greater than

vref1 signal, TI1 circuit resets the Lev-1 signal and sets the Trans1 signal. Therefore, the input *V1* of the laser driver is deactivated and simultaneously Control Block-2 (CB2) is activated setting the Lev-2 signal to H state. Lev-2 signal activates the input *V2* of the Laser Driver as shown in Fig. 36. As a result, the Laser Driver changes the current level from $\alpha V1$ to $\beta V2$, and laser provides an optical power *P2* for the OTPT1 and accordingly changes its effective resistance. The optical intensity *P2* is usually set to a value lower than the optical intensity of *P1* to increase R_{OTPT1} in the di_C/dt control region. The reason is that, a lower R_{OTPT1} is required in the delay region to increase the gate current and decrease the delay duration. However, the value of R_{OTPT1} needs to be increased in the di_C/dt control region to decline the di_C/dt and consequent current overshoot.

As stated earlier, when the value of the ramp signal becomes greater than the Vref1 signal, Lev-1 signal resets to L state and Trans1 signal sets to H state which sets the Lev-2 signal to H state. Setting the Lev-2 signal and resetting the Lev-1 signal, changes the optical intensity from P1 to P2 that adjusts the R_{OTPT2} to desired values for Delay control region and di_C/dt control region. Due to optical to electrical conversion delay in the OTPT1 and circuit propagation delays, the change from P1 to P2, or in other words change from the current level L1 to L2 in the Laser Driver, shall be initiated Δt seconds before the start of the di_C/dt control region where Δt equals to the total delay in the control loop. The reason is that the Δt is appreciable as compared to the duration of the control regions. Therefore, if a simple sensing method is used to detect the di_C/dt control region and sends a command to adjust the required R_{OTPT1} in the di_C/dt control region, the effective change in the R_{OTPT1} takes place Δt seconds after the start of the control region. Hence, this Δt seconds delay modifies the value of di_C/dt in an undesirable form. The proposed self-contained control method predicts the onset of transition and initiates the change in

the current level of the Laser Driver, hence the optical power to the OTPT1, at a proper time earlier than the start of the di_C/dt control region and considering the delays. This ensures the independent controllability of the turn-on delay and turn-on di_C/dt. It is also required that the control circuit guarantees the independent controllability in different operating conditions such as varying load, di_C/dt and etc.

CB1 has a di_C/dt Monitor circuit that monitors the actual onset of transition between turn-on delay and di_C/dt control regions. The output of this Monitor circuit, which is called Monitor1 signal hereafter, is then set to H state by the PWM signal and at the beginning of the turn-on cycle. Monitor1 signal is reset to L state at the beginning of the di_C/dt control region by sensing a di_C/dt across S1. On the other hand, Lev-1 signal is delayed by Δt seconds taking into account the total delay in the control loop. If the Laser Driver initiates the transition between di_C/dt and delay control region at the desired moment, the Monitor1 signal and delayed Lev-1 signal are identical. The delayed Lev-1 signal and Monitor1 signal are then compared in the Error compensator 1 circuit of the CB1, as shown in Fig. 39, and if they are not identical an error is generated and fed to a PI compensator. The PI compensator adjusts the Vref1 such that Monitor1 signal and delayed Lev-1 signal are identical ensuring the independent controllability of the delay and di_C/dt control regions. This self-contained control circuit adjusts the onset of transition of the current of the Laser Driver should any changes in the operating condition happens.

Control Block-2 major waveforms, block diagram, and circuit schematics are respectively shown in Figs. 41-42 (b). When the Control Block-2 receives the Trans1 signal from the Control Block-1, it sets the Lev-2 signal and Monitor2 signals to H state. Lev-2 signal is the output of the Transition Initiator2 (TI2) circuit of the Control Block-2, and Monitor2 Signal is the output of the Monitor 2 circuit of the Control Block-2, as shown in Figs. 41 and 42(b). Subsequently,

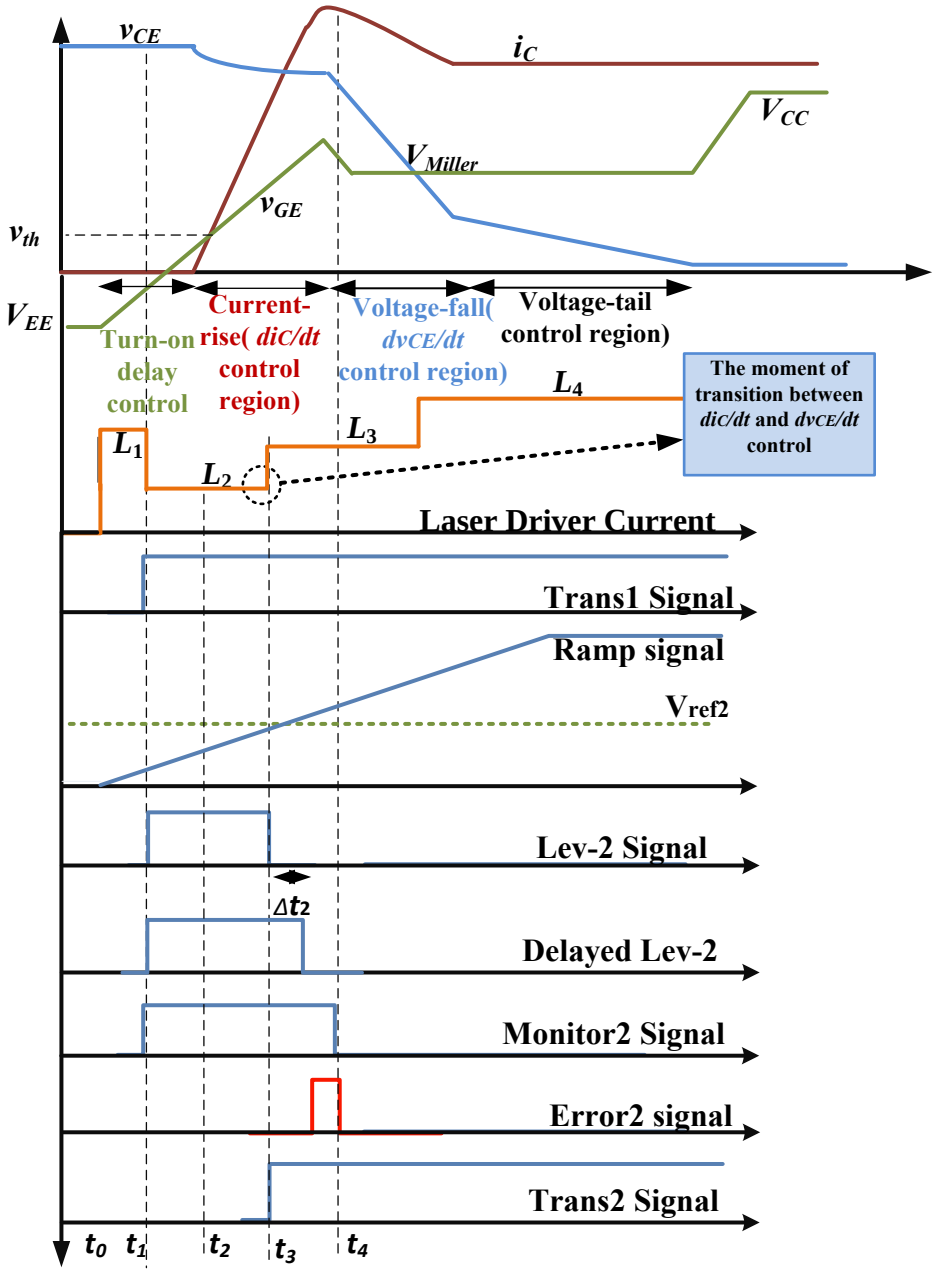
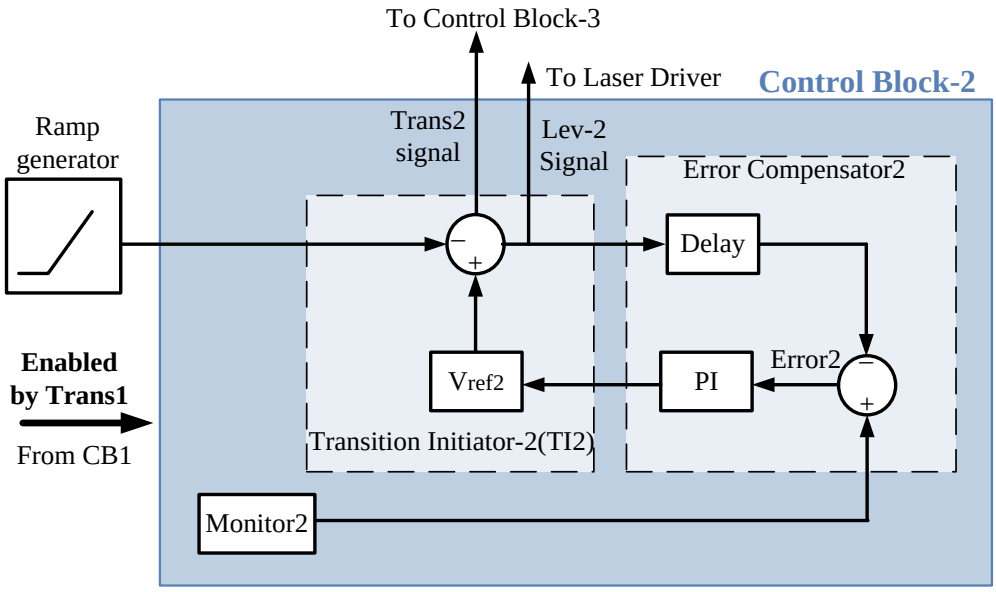
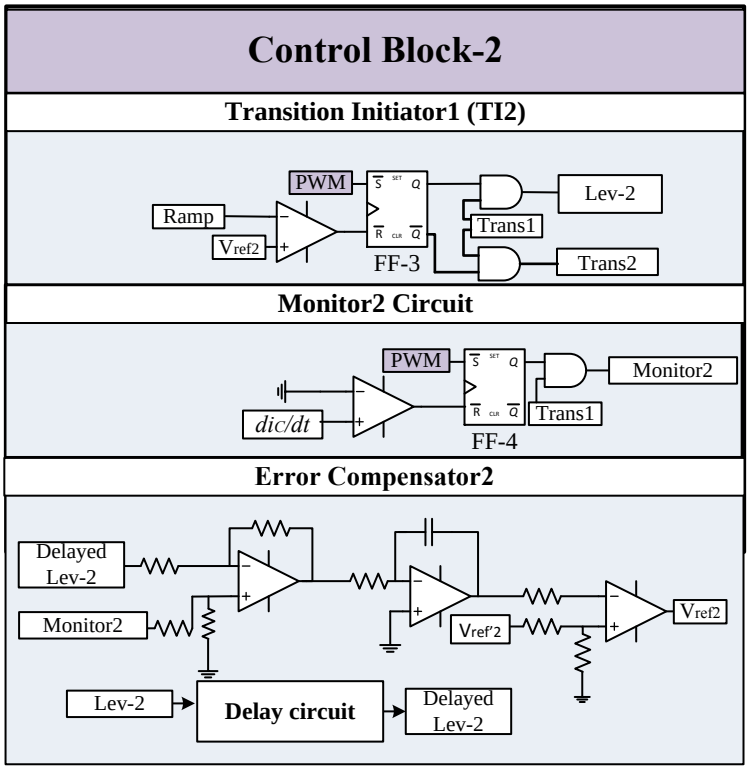


Fig. 41. Turn-on behavior of the IGBT and Control Block-2 key waveforms.

Lev-2 signal activates the input voltage *V2* of the Laser Driver; and Laser Driver provides the current level of *βV2* for the laser. This current provides an optical intensity of *P2* at the base region of OTPT1 and changes the R_{OTPT1}. The R_{OTPT1} at this region sets the value of di_C/dt. According to Fig.4-1, when the value of the ramp signal becomes greater than V_{ref2} signal, TI2



(a)



(b)

Fig. 42**.** Control Block-2: (a) Block diagram, (b) Schematic. Control Block2 comprises of Transition Initiator2 circuit, Monitor2 circuit and Error Compensator2 circuit.

circuit resets the Lev-2 signal and sets the Trans2 signal. Therefore, the input *V2* of the laser driver is deactivated and simultaneously Control Block-3 (CB3) is activated setting the Lev-3 signal to H state. Lev-3 signal activates the input *V3* of the Laser Driver as shown in Fig. 42. As a result, the Laser Driver changes the current level from $\beta V2$ to $\gamma V3$, and laser provides an optical power *P3* for the OTPT1 and accordingly changes its effective resistance. The optical intensity *P3* is usually set to a value higher than the optical intensity of *P3* to reduce the R_{OTPT1} in the dv_{CE}/dt control region. The reason is that, a higher R_{OTPT1} is required in the di_C/dt control region to decrease the gate current and decline the di_C/dt. However, the value of R_{OTPT1} needs to be decreased in the *dvCE/dt* control region to increase the *dvCE/dt* and reduce the switching loss.

As stated earlier, when the value of the ramp signal becomes greater than the Vref2 signal, Lev-2 signal resets to L state and Trans2 signal sets to H state which sets the Lev-3 signal to H state. Setting the Lev-3 signal and resetting the Lev-2 signal, changes the optical intensity from *P2* to *P3* that adjusts the R_{OTPT1} to desired values for di_C/dt and dv_{CE}/dt control region. Due to optical to electrical conversion delay in the OTPT1 and circuit propagation delays, the change from *P*2 to *P*3, or in other words change from the current level *L*2 to *L*3 in the Laser Driver, shall be initiated Δt seconds before the start of the dv_{CE}/dt control region where Δt equals to the total delay in the control loop. The reason is that the Δ*t* is appreciable as compared to the duration of the control regions. Therefore, if a simple sensing method is used to detect the dv_{CE}/dt control region and sends a command to adjust the required R_{OTPT1} in the dv_{CE}/dt control region, the effective change in the R_{OTPT1} takes place Δ*t* seconds after the start of the control region. Hence, this Δ*t* seconds delay modifies the value of dv_{CE}/dt in an undesirable manner. The proposed self-contained control method predicts the onset of transition and initiates the change in the current level of the Laser Driver, hence the optical power to the OTPT1, at a proper time earlier than the

start of the dv_{CE}/dt control region and considering the delays. This ensures the independent controllability of the turn-on di_C/dt and dv_{CE}/dt . It is also required that the control circuit guarantees the independent controllability in different operating conditions such as varying load, di_C/dt and etc.

CB2 has a di_C/dt Monitor circuit that monitors the actual onset of transition between di_C/dt and dv_{CE}/dt control regions. The output of this Monitor circuit, which is called Monitor2 signal hereafter, is then set to H state by the Trans1 signal and at the beginning of the di_C/dt control region. Monitor2 signal is reset to L state at the end of the di_C/dt control region which is the start of the dv_{CE}/dt control region by sensing a sign change in di_C/dt across S1. On the other hand, Lev-2 signal is delayed by Δt_2 seconds taking into account the total delay in the control loop. If the Laser Driver initiates the transition between di_C/dt *and* dv_{CE}/dt control regions at the desired moment, the Monitor2 signal and delayed Lev-2 signal are identical. The delayed Lev-2 signal and Monitor2 signal are then compared in the Error compensator2 circuit of the CB2, as shown in Fig, 42, and if they are not identical an error is generated and fed to a PI compensator. The PI compensator adjusts the Vref2 such that Monitor2 signal and delayed Lev-2 signal are identical ensuring the independent controllability of the di_C/dt *and* dv_{CE}/dt. This self-contained control circuit adjusts the onset of transition of the current of the Laser Driver should any changes in the operating condition happens.

Control Block-3 major waveforms, block diagram, and circuit schematics are respectively shown in Figs. 43-44(b). When the Control Block-3 receives the Trans2 signal from the control Block-2, it sets the Lev-3 signal and Monitor3 signals to H state. Lev-3 signal is the output of the Transition Initiator3 (TI3) circuit of the Control Block-3, and Monitor3 Signal is the output of the Monitor3 circuit of the Control Block-3, as shown in Figs. 43 and 44(b). Subsequently, Lev-3

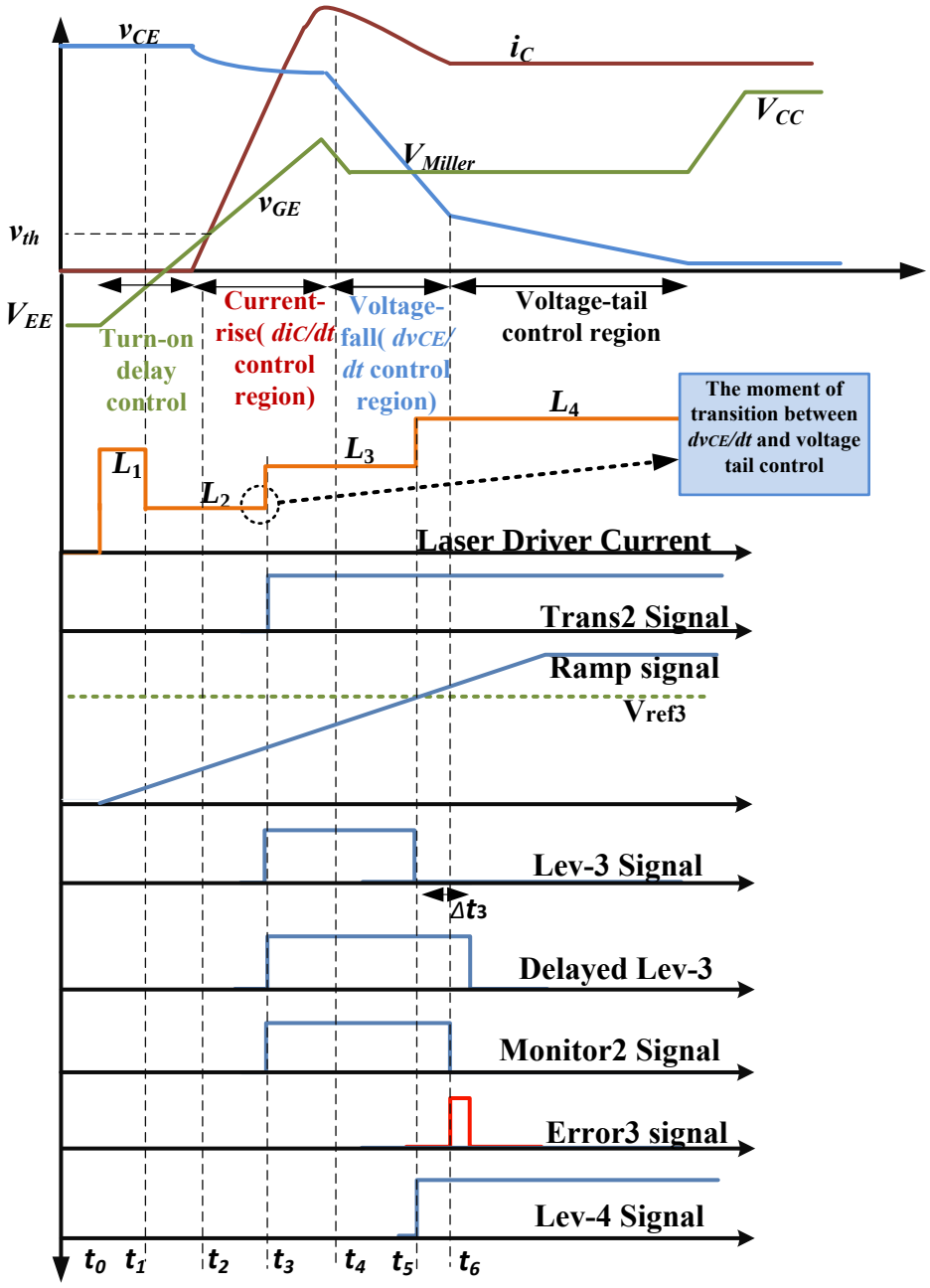
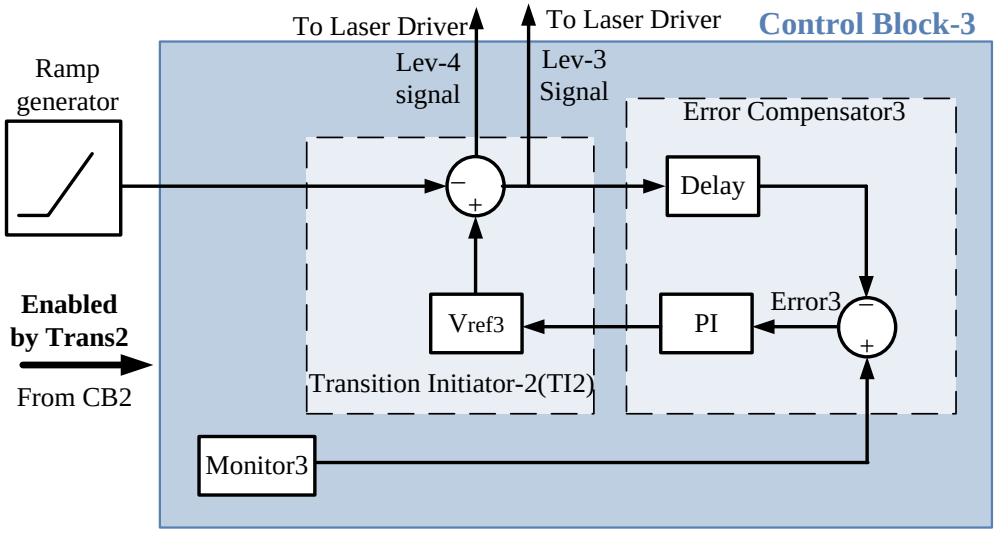
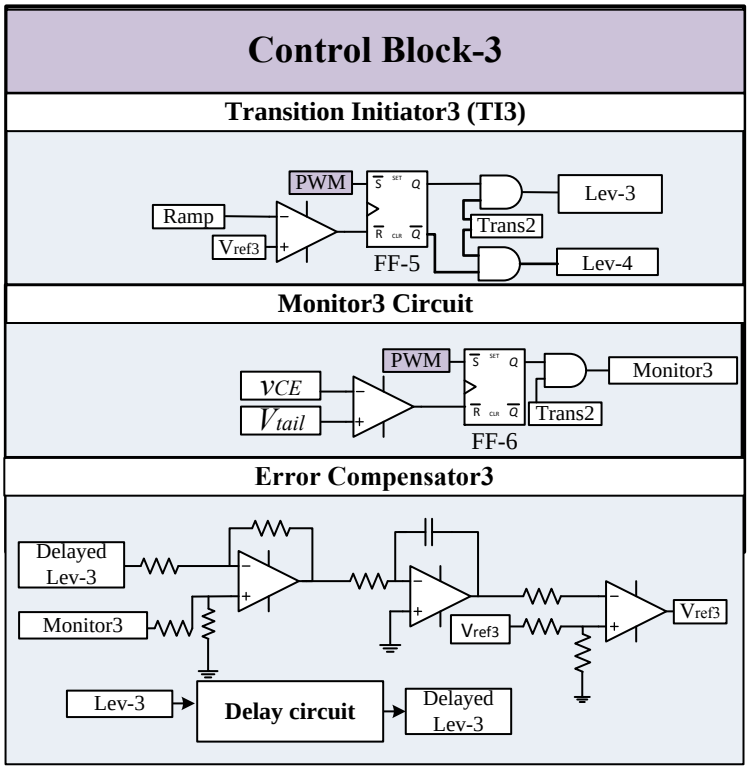


Fig. 43. Turn-on behavior of the IGBT and Control Block-3 key waveforms.

signal activates the input voltage *V3* of the Laser Driver; and Laser Driver provides the current level of $\gamma V3$ for the laser. This current provides an optical intensity of *P3* at the base region of OTPT1 and adjusts the R_{OTPT1}. R_{OTPT1} at this region sets the value of dv_{CE}/dt. According to



(a)



(b)

Fig. 44. Control Block-3: (a) Block diagram, (b) Schematic. Control Block3 comprises of Transition Initiator3 circuit, Monitor3 circuit and Error Compensator3 circuit.

Fig.43, when the value of the ramp signal becomes greater than V_{ref3} signal, TI3 circuit resets the Lev-3 signal and sets the Lev-4 signal. Therefore, the input *V3* of the laser driver is deactivated and simultaneously input *V4* is activated by setting the Lev-4 signal to H state. As a result, the Laser Driver changes the current level from $\gamma V3$ to $\rho V4$ and laser provides an optical power of *P4* for OTPT1 and accordingly changes its effective resistance. The optical intensity *P4* is usually set to a value higher than the optical intensity of *P3* to further reduce the R_{OTPT1} in the voltage-tail control region. The reason is that, the C_{GC} reduces dramatically in the voltage tail control region and declines the dv_{CE}/dt. This reduction in dv_{CE}/dt generates an excessive switching loss. Therefore, R_{OTPT1} is reduced in this region to prevent an undesired reduction in the dv_{CE}/dt and to shorten the duration of the voltage tail region.

As stated earlier, when the value of the ramp signal becomes greater than the Vref3 signal, Lev-3 signal resets to L state and Lev-4 signal sets to H state. Setting the Lev-4 signal and resetting the Lev-3 signal, changes the optical intensity from *P3* to *P4* which adjusts the R_{OTPT1} to desired values for dv_{CE}/dt and voltage tail control region. Due to optical to electrical conversion delay in OTPT1 and circuit propagation delays, the change from P3 to P4, or in other words change from the current level L_2 to L_3 in the Laser Driver, shall be initiated Δt3 seconds before the start of the voltage-tail control region where Δt3 equals to the total delay in the control loop. The reason is that the Δt3 is appreciable as compared to the duration of the control regions. Therefore, if a simple sensing method is used to detect the voltage tail control region and sends a command to adjust the required R_{OTPT1} in this control region, the effective change in the R_{OTPT1} takes place Δt_3 seconds after the start of the control region. Hence, this Δt_3 seconds delay modifies the value of dv_{CE}/dt in an undesirable manner. The proposed self-contained control method predicts the onset of transition and initiates the change in the current level of the Laser

Driver, hence the optical power to the OTPT1, at a proper time earlier than the start of the voltage tail control region and considering the delays. This ensures the independent controllability of the turn-on dv_{CE}/dt and voltage tail. It is also required that the control circuit guarantee the independent controllability in different operating conditions such as varying load, di_C/dt and etc.

CB3 has a voltage Monitor circuit that monitors the actual onset of transition dv_{CE}/dt and voltage tail control regions. The output of this Monitor circuit, which is called Monitor3 signal hereafter, is then set to H state by the Trans2 signal and at the beginning of the dv_{CE}/dt control region. Monitor3 signal is reset to L state at the end of the dv_{CE}/dt control region which is the start of the voltage tail control region by comparing the v_{CE} to a threshold value for tail voltage (V_{tail}). On the other hand, Lev-3 signal is delayed by Δt_3 seconds taking into account the total delay in the control loop. If the Laser Driver initiates the transition between *dv*CE*/dt* and voltage tail control regions at the desired moment, the Monitor3 signal and Delayed Lev-3 signal are identical. The delayed Lev-3 signal and Monitor3 signal are then compared in the Error compensator3 circuit of the CB3, as shown in Fig, 44, and if they are not identical an error is generated and fed to a PI compensator. The PI compensator adjusts the *Vref*3 such that Monitor3 signal and Delayed Lev-3 signal are identical ensuring the independent controllability of the dv_{CE}/dt and voltage tail. This self-contained control circuit adjusts the onset of transition of the current of the Laser Driver should any changes in the operating condition happens.

C. Experimental Results

A prototype of the proposed control scheme and clamped -inductive test circuit of Fig. 35 was fabricated as shown in Fig. 45. The prototype board includes the three control blocks,

Fig. 45. Fabricated prototype of the proposed control scheme with the clamped-inductive test circuit of Fig. 35.

Laser Driver circuit, board power supply circuits and the clamped-inductive test circuit. The prototype of Fig. 45 is used to obtain the following experimental results. Two International Rectifier's (IRG4PH20KDPbF) IGBTs (1.2 kV, 11A) are used in the half-bridge configuration to form the clamped-inductive test circuit in the fabricated prototype. Results are derived using a digital oscilloscope and plotted using MATLAB software.

Experimental results of the control circuit independently adjusting the turn-on di_C/dt while the other control parameters are fixed are shown in Fig. 46. The di_C/dts in the three operating conditions are selected to be 40A/µs, 26A/µs and 18A/µs, the dv_{CE}/dt is fixed at 700V/µs and the turn-on delay is fixed at 350ns. It is worthy to remind that the current level passing through the laser sets the optical intensity at the base region of OTPT1, and the optical intensity sets the value of R_{OTPT1}. According to Fig. 9, R_{OTPT1} increases in a nonlinear manner as I_{laser} decreases. As shown in Fig.46, the turn-on delay is fixed for all the cases by passing the same current level through the laser (I_{laser}). The same current through the laser sets an equal optical intensity at the base region of the OTPT1, therefore, the same resistance in the gate

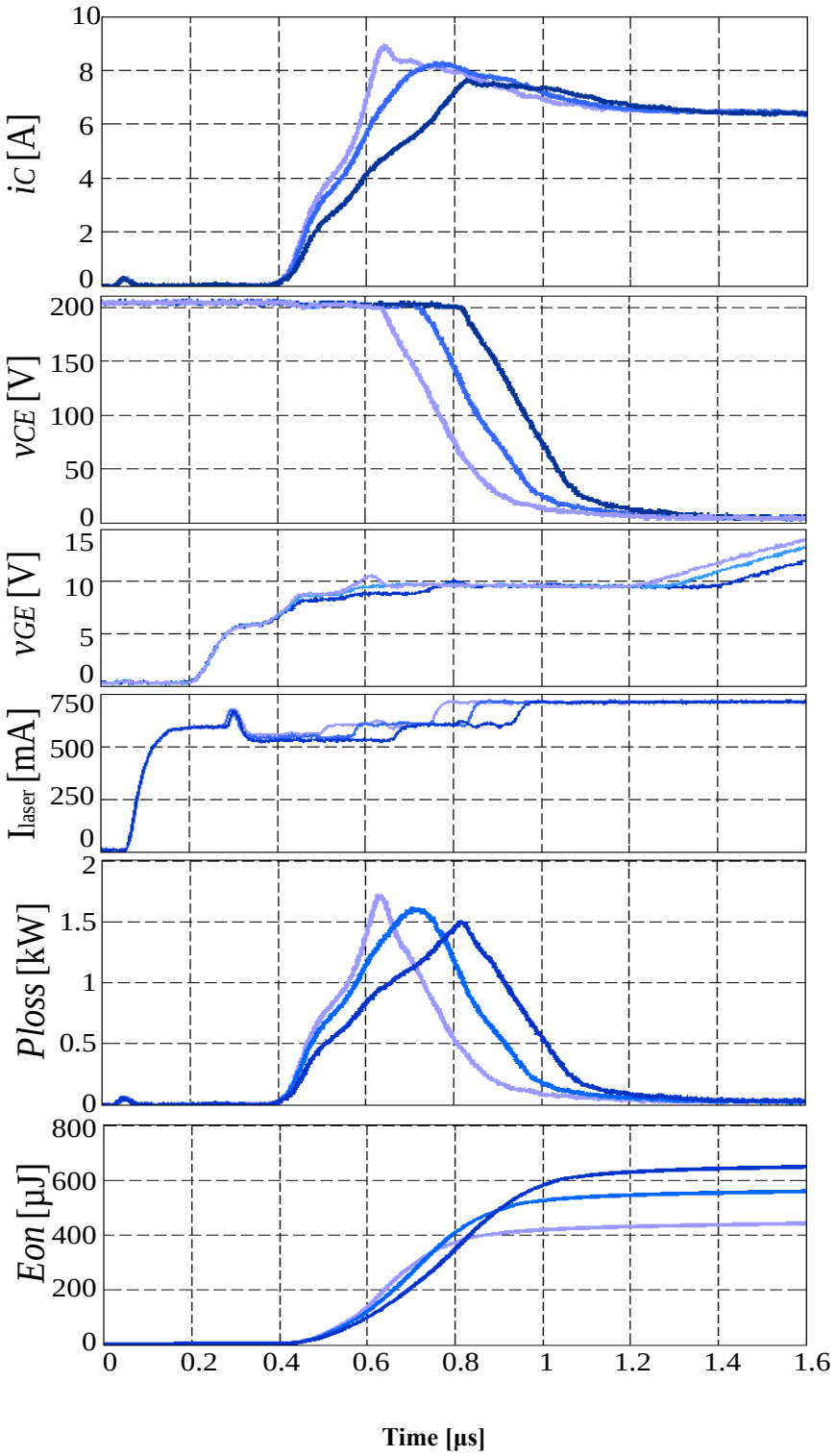


Fig. 46. Measured turn-on waveforms of v_{CE}, i_C, v_{GE} and I_{Laser} and calculated waveforms of instantaneous power loss (P_{loss}) and turn-on switching energy (E_{on}) with varied current slop (di_C/dt) of 40A/µs, 26Aµs and 18A/µs while voltage slope (dv_{CE}/dt) is fixed at 700v/µs and turn-on delay is fixed at 350ns.

charging path of S1. The control block-1 initiates the transition from the delay to di_C/dt control region at a proper time before the start of di_C/dt control region by varying I_{laser} to a desired value. Current level in the delay region is selected to be higher than the current level in the di_C/dt control region. The reason is that a lower resistance is required in the delay region to charge the gate with maximum current and reduce the delay duration according to (1). However, a higher resistance is needed in di_C/dt control region to limit the gate current and reduce the di_C/dt. Decreasing the I_{laser} at the di_C/dt control region increases R_{OTPT1} and reduces the di_C/dt according to equation (2). As the di_C/dt reduces, the current overshoot is declined as shown in the Fig. 46. The dv_{CE}/dt is kept fixed by applying the same I_{laser} at dv_{CE}/dt control region. The control circuits initiates the transition from dv_{CE}/dt to voltage tail control region by increasing the current level of the laser at an appropriate time. The current level is increased in the voltage tail region to compensate for nonlinear increment of the Miller capacitance and consequent reduction of the dv_{CE}/dt. Therefore, the duration of the Miller plateau of the gate-to-emitter voltage is approximately remained the same for all cases. As indicated in Fig. 46, as the di_C/dt and the peak reverse recovery current also increases which leads to higher peak power loss. However, increasing the di_C/dt shrinks the duration of the di_C/dt control region and reduces the turn-on switching energy. Therefore, there is a tradeoff between the device stress and switching loss.

Fig. 47 shows the experimental results of the performance of the control circuit in adjusting the dv_{CE}/dt while the other control parameters are fixed. The dv_{CE}/dt in the three operating conditions is selected to be 850V/µs, 530V/µs and 320V/µs while the di_C/dt and turn-on delay are respectively fixed at 350ns and 32A/µs. The turn-on delay is fixed in the three operating conditions by applying the same current to the laser. The control circuit initiates the transitions between the turn-on delay and di_C/dt control regions by decreasing the current level of

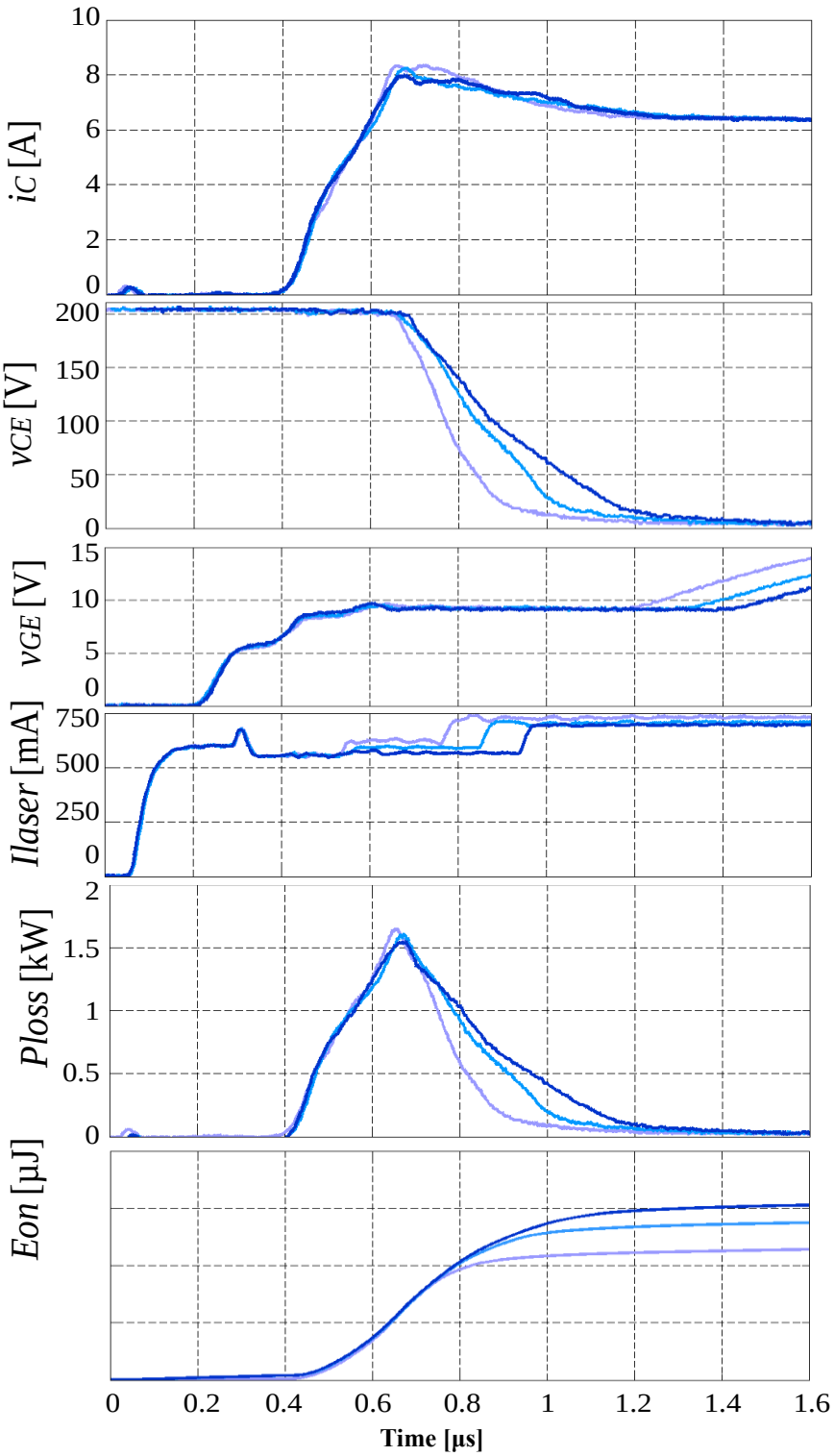


Fig. 47. Measured turn-on waveforms of v_{CE}, i_C, v_{GE} and I_{Laser} and calculated waveforms of instantaneous power loss (P_{loss}) and turn-on switching energy (E_{on}) with varied voltage slope (dv_{CE}/dt) of 850V/µs, 530V/µs and 320V/µs while current slop (di_C/dt) is fixed at 32A/µs and turn-on delay is fixed at 350ns.

the laser in the di_C/dt control region to decrease the di_C/dt and current overshoot. The control circuit kept the di_C/dt at 32A/μs for all cases by passing the same current through the laser during the di_C/dt control region. The Control Block-2 initiates the transition between the di_C/dt and dv_{CE}/dt control regions by increasing the current of the laser to a proper value at the desired moment earlier than the start of the dv_{CE}/dt control region. The current level is increased in the dv_{CE}/dt control region to increase the dv_{CE}/dt and reduce the switching loss by decreasing the total duration of the switching transition. The control circuit adjusts the dv_{CE}/dt values by controlling the current level of the laser. As shown in Fig. 47, the dv_{CE}/dt is increased by increasing the current level of the laser driver which decreases the R_{OTPT1}.In order to reduce the adverse effect of nonlinearity of the Miller capacitance and decrease the voltage-tail interval, the control circuit initiates the transition between the dv_{CE}/dt and voltage tail control regions. This transition is initiated at the desired moment prior to the start of the voltage-tail control region and by increasing the current level of the laser. The current level in the voltage tail control region is not equal for three cases. The current levels in the voltage-tail control region are selected such that v_{CE} in each case has a smooth fall trajectory. As shown in Fig. 47, the peak power loss is almost the same for the three cases due to having the same di_C/dt and current overshoot. However, as the dv_{CE}/dt increases the turn-on switching energy decreases due to the reduction of the duration of the dv_{CE}/dt and voltage tail control regions.

Control circuit performance at different load conditions is shown in Fig. 48. The load currents are selected to be 4A, 6A and 8A. The control circuit keeps the turn-on delay, di_C/dt and dv_{CE}/dt at same values in the three load conditions. This is achieved through proper initiation of transition between the control regions and adjusting the current level of the laser in each control region. The turn-on delay is remained equal for the three load conditions by keeping the current

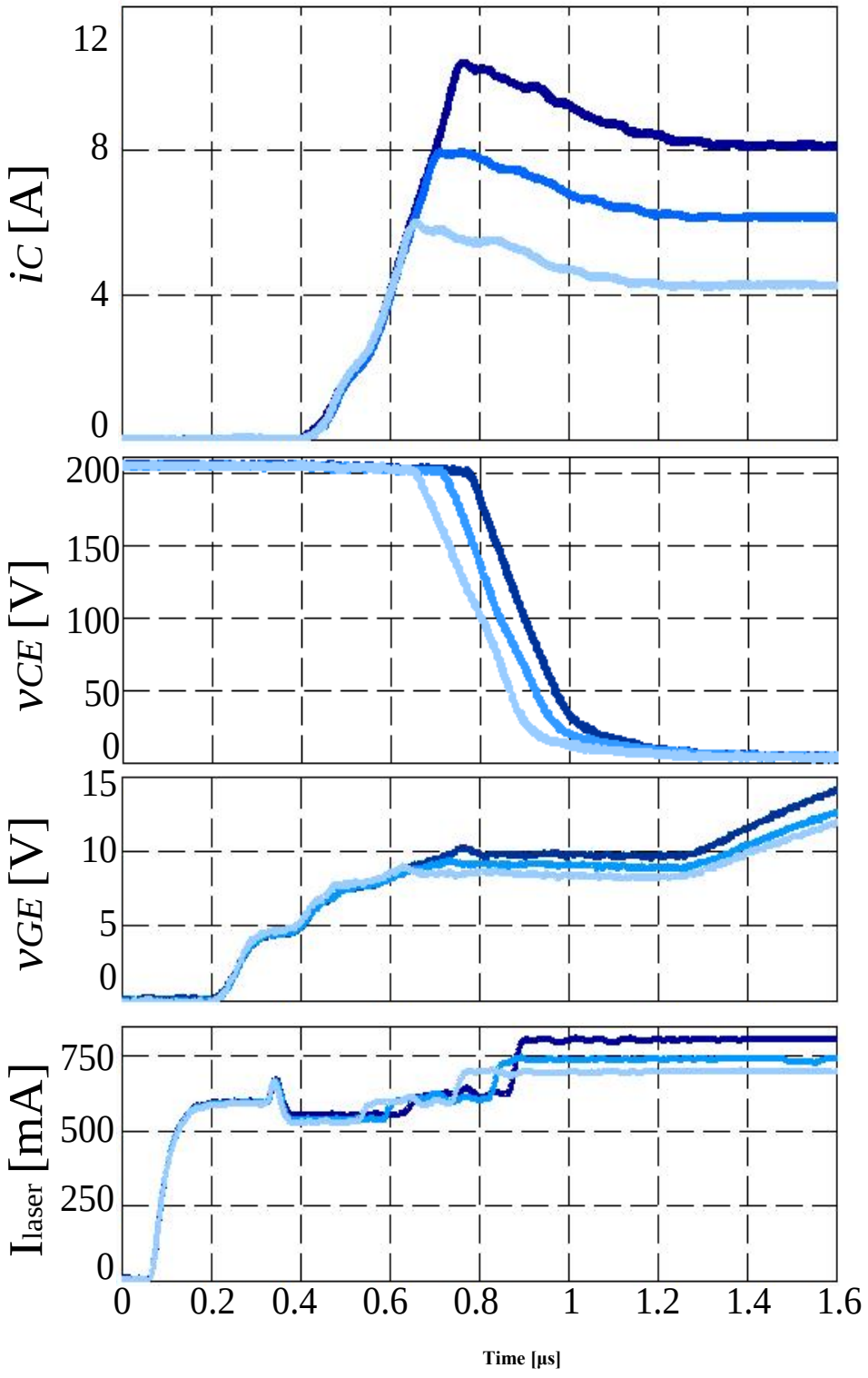


Fig. 48. Measured turn-on waveforms of v_{CE}, i_C, v_{GE} and I_{Laser} in the load current conditions of 4A, 6A, and 8A.

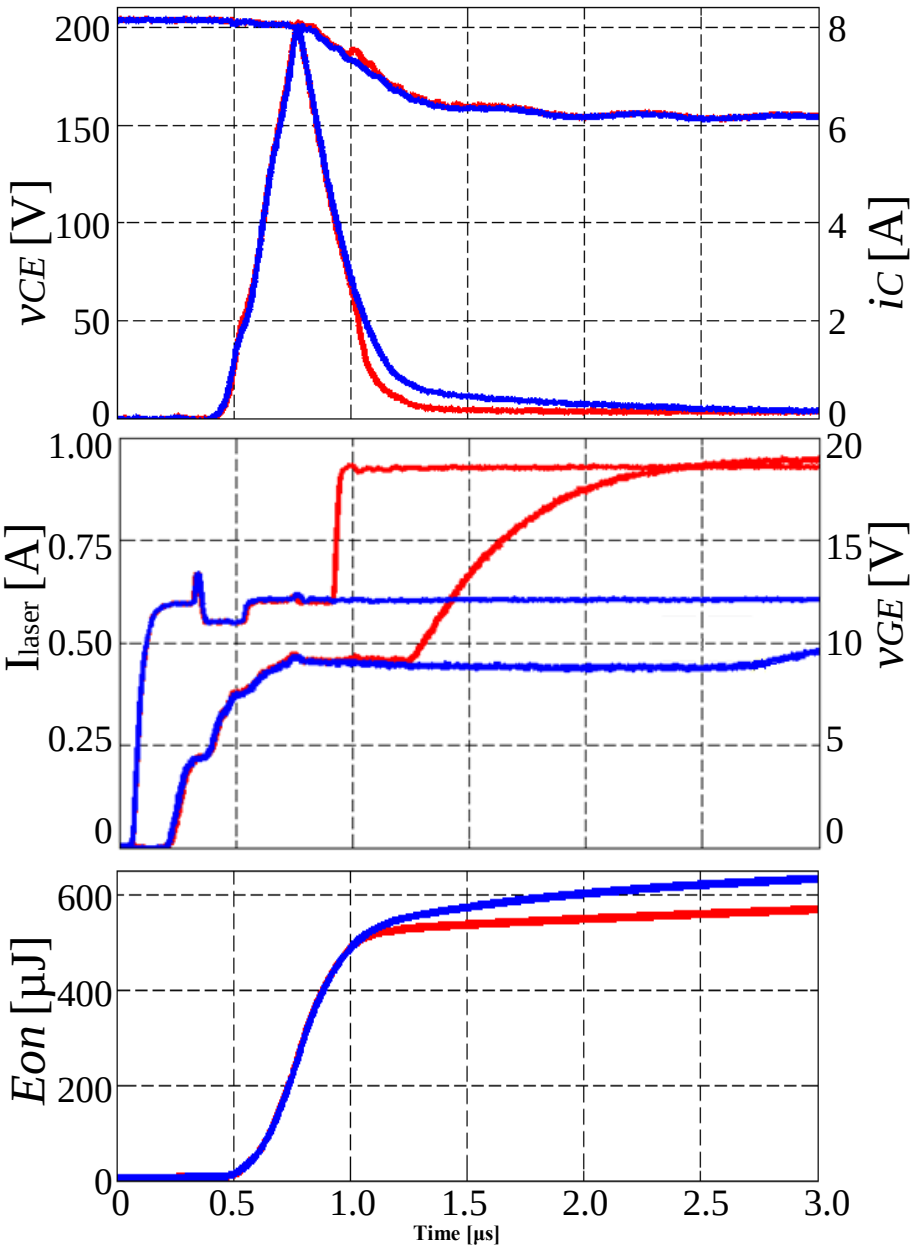


Fig. 49. Measured turn-on waveforms of v_{CE}, i_C , v_{GE} and I_{Laser} ,and calculated waveforms of turn-on switching energy (E_{on}) for the two cases of three-level and four -level control. Control block-3 is disabled in the case of three-level control and enabled in the case of four-level control to show the significance of this control block.

level of the laser at the same value. The Miller plateau voltage level increases by increasing the load current. In order to keep the di_C/dt at the desired value as the current increases one needs to decrease the R_{OTPT1} in the di_C/dt control region according to (2). Reduction in the value of R_{OTPT1}

is achieved by slightly increasing the current level of the laser in the di_C/dt control region and as the load current increases. Similarly, one needs to adjust the R_{OTPT1} in dv_{CE}/dt and voltage tail control regions to keep the dv_{CE}/dt and duration of voltage tail at the desired values. This reduction in R_{OTPT1} is also achieved by increasing the current level of the laser in the dv_{CE}/dt control region and as the load current increases.

Comparison between the four-level control and three-level control of the turn-on switching transition is shown in Fig. 49. All the three control blocks are used in case of the four-level control. However, the control block-3 is deactivated in case of three-level control. This comparison is made to show the significance of using the control block-3 to reduce the duration of the voltage tail region and decrease the switching loss Turn-on delay, di_C/dt and dv/dt are kept similar for both cases by applying the same current in the turn-on delay, di_C/dt and dv_{CE}/dt control regions. Control Block-3, in case of four-level control, significantly increases the current level of the laser driver in the voltage tail control region as compared to the three-level control for which the current level remains unchanged in the dv_{CE}/dt and voltage-tail control regions. As a result, one can see a significant reduction in the duration of the voltage tail control region as well as duration of the Miller plateau of v_{GS}. The duration of Miller plateau is reduced from approximately 2μs in case of the three-level control to 0.5μs in case of the four-level control. This significant reduction in duration of Miller plateau results in decrement in the turn-on switching energy (Eon). The turn-on switching energy is decreased by 10% in case of applying the control block-3 in four level control scheme as compared to the three-level control scheme. This 10% reduction in switching energy is equal to 63mJ where the four-level control decreases the turn-on switching energy from 625mJ to 562 mJ.

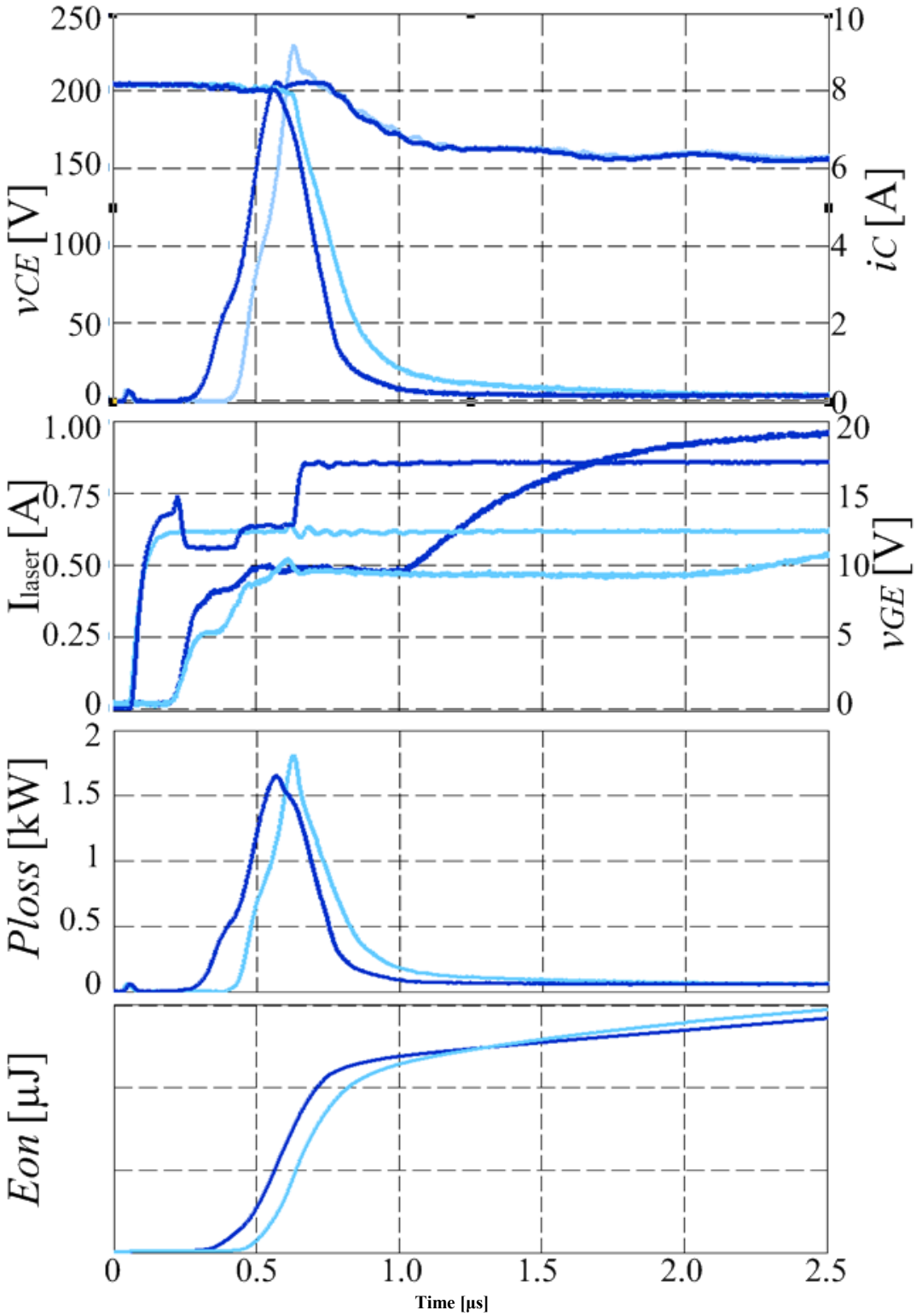


Fig. 50. Measured turn-on waveforms of v_{CE}, $i_{C,}$, v_{GE} and I_{Laser} ,and calculated waveforms of instantaneous power loss (P_{loss}) and turn-on switching energy (E_{on}) for proposed control method (light blue) and conventional fixed resistance method (dark blue).

Performance of the proposed control method is compared with the performance of the conventional fixed resistance method in Fig. 50. The current level of the laser is remained the same in all control region for conventional control method to apply a fix resistance in the gate charging path of S1. As shown in Fig. 50, the turn-on delay is reduced for the proposed method by increasing the I_{laser} in the delay region, as compared to the conventional control method. Turn-on delay is reduced from 330ns for the conventional method to 200nsfor the proposed method. The current level of laser is decreased for the proposed method in the di_C/dt control region as compared to the conventional control. This reduction in the I_{laser} results in reduced di_C/dt and current overshoot as compared to the conventional fixed resistance control method. However, the dv_{CE}/dt is increased in the dv_{CE}/dt control region in case of the proposed method. This increment in the dv_{CE}/dt is achieved by increasing the current level of laser in this region. The current level of laser is further increased in the voltage-tail control region to further reduce the duration of this region and duration of the Miller plateau. The duration of Miller plateau is decreased from approximately 2.2μs in case of conventional control to 0.5μs in case of the proposed control. Applying the proposed control method not only results in less turn-on delay and switching stress but also slightly reduces the turn-on switching energy , as shown in Fig. 50. However, these improvements in most of the parameters of the switching transition are achieved by increasing the dv_{CE}/dt which may lead to an increment in the EMI noise. Therefore, on e can conclude that there is always a trade-off between switching loss, stress and EMI noise. Worthy to note that other switching-transition performances are obtainable using the proposed control method due its ability to independently control the turn-on delay, di_C/dt, dv_{CE}/dt and voltage tail.

D. Conclusion

A novel four-level control for turn-on transition of an optically-triggered IGBT is outlined in this chapter. The proposed control scheme can independently control the turn-on delay, turn-on di_C/dt, dv_{CE}/dt and voltage tail using a controller and Laser Driver. The proposed controller is comprised of three control blocks which initiate the transition between the four control regions. Each control block of the self-contained control scheme initiates the transition based on a predefined set point and measures the error between the actual and desired onset of transition. Then, the error is fed to a PI compensator and set point is adjusted accordingly. Turn-on delay, di_C/dt, dv_{CE}/dt and voltage tail are controlled by adjusting the current level of the laser in their respective control regions. Subsequently, the laser adjusts the receiving optical intensity of an OTPT which is placed in the charging path of the gate of an IGBT. The intensity of the light set the resistance of OTPT. It has been shown by experimental results that the proposed control method is feasible in independently controlling the turn-on delay, di_C/dt, dv_{CE}/dt and voltage tail. It has been also shown the control circuit is able to keep the parameters of the switching transition, in terms of delay, di_C/dt, dv_{CE}/dt, and voltage tail in different load conditions. The significance of the control block-3 in reducing the duration of the voltage tail and switching energy was validated. The proposed method was compared to the conventional fixed resistance method and was able to simultaneously improve the delay, switching stress and switching loss.

V. Conclusion and Future Work

A. Conclusion

Power electronics industry is moving toward to high-power-density applications. In order to increase the power density, the size, volume and cost of the passive elements in the circuit needs to be decreased. This reduction is achieved by increasing the frequency of the active switches. As the switching frequency increases, the slopes of the currents and voltages of power switches needs to be increased to reduce the switching loss. However, adverse current and voltage slopes during the switching transitions are the main source of EMI noise and device stress. High *di/dt* generates current overshoot during the turn-on transition and voltage overshoot during the turn-off transition. High *di/dt* current loops in the circuit are also responsible for the radiated noise. On the other hand High *dv/dt* is the main source of the common-mode noise.

Power stage solutions have been employed in the literature to mitigate the adverse effect of high *di/dt* and *dv/dt* during the switching transitions. These solutions add passive and/or active components to the power circuit or modify original topology. Addition of active and passive power-rated components increases the cost, size and complexity of system. Control stage solutions neither add power-rated components nor modify the original topology of the circuit. The control-stage solutions, which are known as active and passive gate drives and switching transition controllers, control the EMI, device stress and switching loss by controlling the gate circuit of the power semiconductor devices. Independent control of the important parameters of switching transition, such as delay, *di/dt* and *dv/dt*, enables one to gain an optimum performance in terms of device stress, switching loss and EMI.

In this dissertation, an optically-based switching transition control was proposed. In this method, laser beams are used to turn-on and turn-off two optically triggered power transistors (OTPTs) that are respectively placed in the charging and discharging paths of the gate of a SiC MOSFET. Modulating the optical intensity enables one to dynamically control the effective resistance of the OTPTs. Therefore, the gate resistance can be adjusted independently for *di/dt* and *dv/dt* control regions during the turn-off switching transition. It has been shown that the independent controllability of the turn-off *dv/dt* and *di/dt* is achieved by the proposed control circuit. The control circuit predicts the onset of transition between *dv/dt* and *di/dt* control regions by monitoring the *dv/dt*, v_{DS} and bus voltage. It also compensates the optical-to-electrical conversion delay of OTPT and delays associated to the feedback circuit. . Using laser beam and optical link to send the PWM data precludes the susceptibility to external noise and increases the reliability. A prototype including a laser driver, standard clamped-inductive test circuit and proposed control circuit was developed to verify the feasibility of the proposed control scheme.

An electrically-based closed-loop gate drive was proposed to control the turn-off switching transition of high speed SiC MOSFETs. The closed-loop gate drive ensures that the *di/dt* and *dv/dt* of the turn-off switching transition are following the reference values. This is achieved by adjusting the gate current in the respective regions of control. The onset of transition between the *di/dt* and *dv/dt* control regions is predicted using the proposed control circuit that predicts the onset of transition and compensates the total delay in the feedback loop. Compensating the delay using the proposed control scheme guarantees the independent controllability of turn-off *dv/dt* and *di/dt* even in a sub-hundred nanosecond switching transition. Independent control of turn-off *dv/dt* and *di/dt* enables one to reach an optimum performance in terms of switching loss, device stress and EMI noise. The proposed control was verified through experimental results.

A novel control scheme for controlling the turn-on transition of an optically triggered IGBT was proposed. Controlling the turn-on transition is achieved by modulating the optical intensity received by an OTPT that is placed in the charging path of the gate of an IGBT. It has been shown that by adjusting the light intensity one can control the effective resistance of OTPT, thus the gate resistance of the IGBT. A laser driver was designed which receives a reference for each control region and provides an appropriate current for the laser. Laser then shines through the base region of OTPT adjusting the gate resistance according to the optical intensity. The proposed for-level control scheme independently controls the turn-on delay, *di/dt*, and *dv/dt* and voltage tail. Independent controllability of the four control regions is guaranteed by three control blocks which are responsible to initiate the transition between the four control regions. The control blocks monitor the actual and desired onset of transitions considering the total delay in the OTPT and feedback loop. If the actual and desired onsets of transitions between the control regions do not match an error is generated. This error is then compensated using a PI compensator ensuring the independent controllability of the four control regions. The proposed control scheme was verified by experimental results.

B. Future Work

As a future work beyond the dissertation, one can use the control concepts to design a mixed-signal controller which can be able to control both the turn-off and turn-on switching transitions. Using the mixed-signal control enables one to take advantage of benefits of both analog and digital control. Digital microcontrollers can implement feedback compensation and use the previous data to implement a self-contained control much easier than the analog

circuits. However, the main limitation of digital controllers is the sampling rate and propagation delay associated with digital-to-analog and analog-to-digital conversions. Therefore, reconstruction of a sampled voltage or current waveform during the fast switching transition would be cumbersome. As a result, one can only sample the important parameters during the switching transition using an analog circuit and use those parameters as inputs to control loops implemented in microcontrollers.

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