A Differential-Mode Current-Sourced High-Frequency-Link Photovoltaic Inverter

BY

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THESIS

Submitted as partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Chicago, 2013

Chicago, Illinois

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LIST OF SYMBOLS

C_{o1} : Upper output capacitor in Module 1.

C_{o2} : Lower output capacitor in Module 2.

C_{o3} : Upper output capacitor in Module 3.

C_{o4} : Lower output capacitor in Module 4.

D : Constant dc offset in the duty ratio of the switches.

d_1 : Duty ratio of Module 1.

d_2 : Duty ratio of Module 2.

d_r : ZCS duty ratio of the secondary-side switches.

E_L : Average energy stored in the input inductor.

E_{off} : Energy associated with the turning off of a switch.

E_{on} : Energy associated with the turning on of a switch.

f_s : Switching frequency of the inverter.

$G(s)$: Transfer-function of the PR compensator.

LIST OF SYMBOLS (Continued)

I_D : Drain current of a switch.

I_{FB} : Feedback current from the inverter to the controller.

i_{in1} : Input current to Module 1.

i_{in2} : Input current to Module 2.

i_L : Current through any input inductor in both modules.

i_{LS1} : Current through the leakage inductance, L_{S1}, of the transformer in Module 1.

i_{LS2} : Current through the leakage inductance, L_{S2}, of the transformer in Module 2.

I_{REF} : Reference current fed to the controller.

i_{S1} : Current through switch S_1.

i_{S2} : Current through switch S_2.

i_{S3} : Current through switch S_3.

i_{S4} : Current through switch S_4.

$i_{sw,rms}$: RMS value of the current through a switch.

i_{SW}(t) : Instantaneous value of the current through a switch.

k_p : Proportional gain of the PR compensator.

L_1 : Input inductor in Module 1.

L_2 : Input inductor in Module 1.

LIST OF SYMBOLS (Continued)

L_3 : Input inductor in Module 2.

L_4 : Input inductor in Module 2.

L_S : Value of leakage inductance of the transformer in both modules.

L_{S1} : Leakage inductance of the transformer in Module 1.

L_{S2} : Leakage inductance of the transformer in Module 2.

n : Order of harmonics.

n : Transformer turns ratio.

$P_{cond,Loss}$: Conduction loss occurring in a switch.

P_o : Output power of the inverter.

P_{SW} : Power loss associated with a switch during switching.

r_{ON} : On-state resistance of a switch.

S_1 : Primary-side switch in Module 1.

S_2 : Primary-side switch in Module 1.

S_3 : Primary-side switch in Module 2.

S_4 : Primary-side switch in Module 2.

S_{r1} : High-side secondary-side switch in Module 1.

S_{r2} : Low-side secondary-side switch in Module 1.

LIST OF SYMBOLS (Continued)

S_{r3} : High-side secondary-side switch in Module 2.

S_{r4} : Low-side secondary-side switch in Module 2.

T_{fi} : Time taken for the switch current to drop from I_D to zero.

T_{fv} : Time taken for the switch voltage to drop from V_{DS} to zero.

T_{ri} : Time taken for the switch current to rise from zero to I_D.

T_{rv} : Time taken for the switch voltage to rise from zero to V_{DS}.

T_{SW} : Switching period.

V_{DS} : Drain-Source voltage of a switch.

V_{Co1} : Voltage across output capacitor C_{o1}.

V_{Co2} : Voltage across output capacitor C_{o2}.

V_{Co3} : Voltage across output capacitor C_{o3}.

V_{Co4} : Voltage across output capacitor C_{o4}.

V_{FB} : Feedback voltage from the inverter to the controller.

V_{o1} : Output voltage of Module 1.

V_{o2} : Output voltage of Module 2.

V_{orms} : Root-Mean-Square (RMS) output voltage of the inverter.

V_{PV} : Input voltage to the inverter.

LIST OF SYMBOLS (Continued)

V_{REF} : Reference voltage fed to the controller.

V_{SW1} : Voltage across any primary-side switch in Module 1.

V_{SW2} : Voltage across any primary-side switch in Module 2.

X_c : Impedance offered by an output capacitor.

ω : Line frequency or fundamental frequency.

SUMMARY

Photovoltaic-inverter architectures include a dc/dc stage followed by a dc/ac conversion stage and a transformer. Some architectures employ a bulky 60 Hz line transformer while most other inverter designs are based on High-Frequency-Link (HFL) architectures. The HFL architecture employs the high-frequency transformer either in the dc/dc stage or in the dc/ac stage. The HFL architectures have higher power density than the inverters that uses a line transformer. As a step ahead, single–stage inverters are a definite solution to achieve a more compact Power-Electronics-Interface, Current-source inverters, in particular, have an inherent boosting capability, thereby reducing the need for a transformer with higher turns ratio. Also, a current-sourced topology eliminates the need for a bulky and expensive bus capacitor.

A differential-mode current-fed Zero-Current-Switching (ZCS) voltage-doubling PV inverter has been designed. This inverter has two modules of dc/dc converters that are connected differentially to the PV source. This inverter does not require a) 60-Hz transformer, b) front-end dc/dc converter, and c) can boost a low-voltage (30-60V) input to a 120V/60 Hz output using a unity-turns-ratio transformer because of the added voltage gain of the topology. Main switches are switched using ZCS. The inverter requires a smaller high-frequency transformer because of a) 100-kHz switching, b) bipolar transformer current and voltage in every switching cycle, and c) the transformer sees only half of the input current at any given instant. The modularity of the inverter extends the scope of the topology to be used as a dc/dc converter, single-phase inverter and also the possibility of extending the topology to both split-phase and three-phase. A harmonic compensation control is designed and implemented, to reduce the THD at the load, using a Proportional Resonant (PR) controller. The design and analysis of the inverter has been validated using SABER.

1. INTRODUCTION

1.1 **Motivation**

The global consumption of electrical energy is increasing steadily in an ever growing economy due to industrialization leading to a pressing need for an increase in the power generation capacity. This coupled with increasing fossil fuel cost, global warming and the need for a cleaner source of energy has shifted the focus to the renewable energy sources. The conventional methods of generating electricity are coal and oil based energy plants. These large power generation plants are located at specific geographical locations and the generated power is transferred relatively inefficiently to the end-users, through large transmission and distribution (T&D) networks over a very long distance. Apart from the drawbacks of harmful environmental emissions and T&D power loss, the conventional methods also have a lower reliability and cannot suffice to customers at all locations. The reliability of the traditional power system is estimated in the orders of 99.9% and is termed as the three-nine reliability which could cause an eight-hour outage annually per consumer [1]. This reliability is considered unacceptable for certain applications including military, hospitals. Besides reliability, the traditional power generation methods cannot suffice to consumers located in remote locations. All the above factors, have led to shifting the focus on distributed generation (DG) and renewable resources.

Photovoltaic (PV) energy sources are one of the renewable energy sources that has been gaining a lot of significance in the recent past. Fig. 1 shows some common applications of the PV based energy system. Since 2004, PV passed wind as the fastest growing renewable

energy source and since 2007 it has more than doubled every two years [2]. PV energy sources generate electricity in over 100 countries and are the fastest growing power generation technology. The global capacity of grid-connected PV was 7.6 GW in 2007, 16 GW in 2008, 23 GW in 2009, 40 GW in 2010 and 69 GW by the end of 2011. With this growth rate, by 2030, PV systems could be contributing approximately 1.8 TW which would suffice the needs of 14% of the global population. According to a 2011 projection by International Energy Agency (IEA), PV-based power generation may produce most of world's electricity within next 50 years. As of 2011, the price of PV module per MW has dropped by 60% since 2008. The average retail price of PV is estimated as 2.43 USD per Watt in 2011 for small-scale installations and less than 1 USD per Watt for large scale installations. With further reduction of the system cost, PV technology has the potential to become one of the main renewable energy sources for the future. However, this requires simultaneous research and development in the areas of PV source, power electronics interface (PEI) and loads. Although PV cell is an all electrical device without any moving parts, thereby having a low wear and tear and an increased lifetime (typically greater than 25 years), the power generating capacity may be reduced to 75-85% of its nominal value with years. Thus PV requires a compatible PEI. With regards to the PEI, focused effort is required to simultaneous challenges encompassing cost, efficiency, reliability and footprint.

1.2 Power Electronics Interface

With regards to the above context, the architecture and topology of the PEI attains significance. The PEI for the PV energy source needs to simultaneously address reliability, power density, cost and efficiency. Reliability can be attained by increasing the modularity of the system, reducing the stresses in the components and by increasing the efficiency of the system. Power density can be increased by decreasing the size of inductors, capacitors and transformers

by increasing the system frequency. It can further be increased by integrating the magnetics in the topology. Efficiency of the system is mainly attributed by the conduction and switching losses in the system. And the cost of the system can be decreased by utilizing fewer and cheaper components, by implementing modularity and redundancy.

Fig. 1: Few illustrations of stand-alone PV loads.

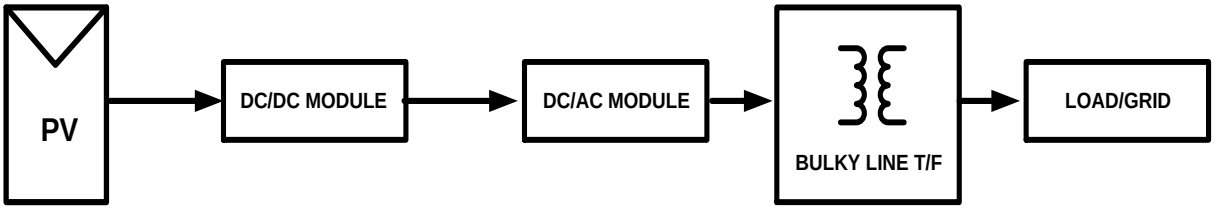

Fig. 2 (a): Possible configuration (1) of a PV system.

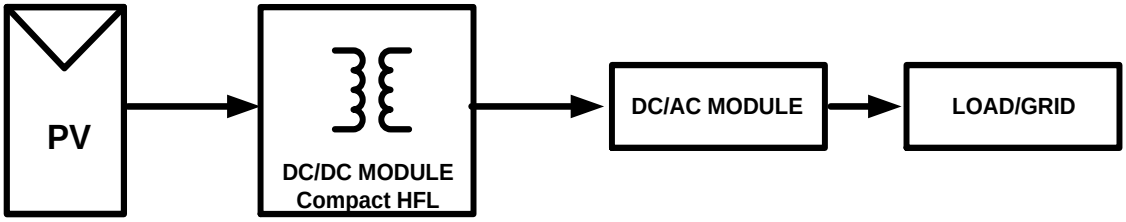

Fig. 2 (b): Possible configuration (2) of a PV system.

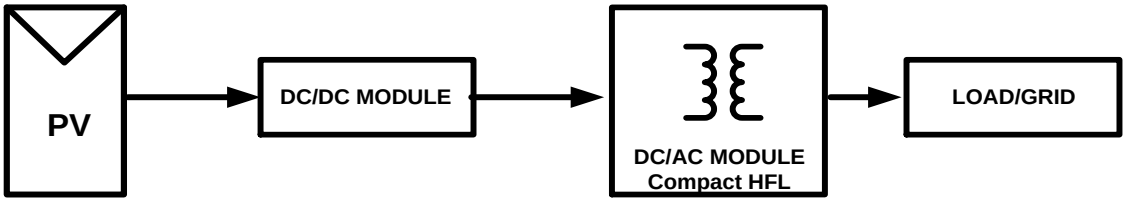

Fig. 2 (c): Possible configuration (3) of a PV system.

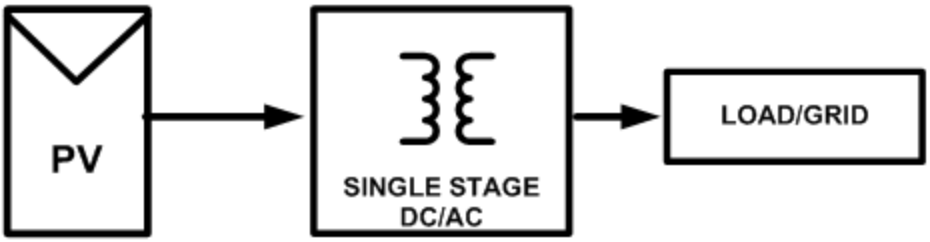

Fig. 2 (c): Possible configuration (3) of a PV system.

Fig. 2: Possible configurations of a PV system.

Redundancy is an important characteristic of any system aiming at all the needs of the PEI-modularity and reliability especially. This increases the scope of the system to be modified to suit the application. Few advantages of modularity are: a) ease of system configuration and flexibility; for example, if the application requirements are three-phase, additional modules can be incorporated in the system to cater the needs of the consumer; b) engineering and manufacturing costs and time are reduced. The frequency of the power electronics system also plays a major role to attain higher power density. The higher the operating frequency, the smaller and lighter the magnetics and capacitors. In addition, the dynamic characteristics of the system improve with increasing operating frequencies. The bandwidth of a control loop is usually determined by the corner frequency of the output filter, thereby; high operating frequencies allow for achieving a faster dynamic response to changes in the load current or input voltage.

As shown in Fig. 2, there are four fundamental architectural approaches that can meet the PEI needs. The architecture in Fig. 2a represents a conventional approach that requires bulky, expensive, high footprint line transformer. The architectures shown in Figs. 2b and 2c incorporate the galvanic isolation using a High-Frequency (HF) transformer in the dc/dc or dc/ac stages respectively. This yields a high power density but an increased number of power stages. As such,

for low power applications, the single-stage architecture shown in Fig. 2d, is a viable candidate. The Direct Power Conversion (DPC) in this architecture also precludes the need for an intermediate dc link capacitor.

1.2.1 Conventional Power Electronics Interfaces

Most interfaces have a dc/dc conversion stage followed by a dc/ac conversion stage. The basic functions of the dc/dc converter are boosting and regulating the low output from the renewable energy source. Some basic criteria for choosing a dc/dc converter for a renewable energy source input are:

- Large step-up ratio
- Low input current ripple
- Provide isolation between source and load

The dc/dc converters are either voltage-fed or current-fed and can be either a half-bridge or full bridge topology. Half-bridge topologies are used for low and medium power applications and full-bridge for higher power applications. The voltage-fed converters require a high winding ratio between primary and secondary sides of the HFL transformer since boosting action in voltage-fed converters is only performed by the transformer. Voltage-fed converters also require larger snubbers to handle the surges during the turning off of the switches. In current-fed converters, the presence of an inductor reduces the current ripple and also the electrolytic capacitor size, apart from providing an active boosting without relying much on the transformer turns ratio. Thus current-fed converters have a higher voltage conversion ratio and can also provide galvanic isolation. However, one major drawback of the current-fed topologies is higher voltage surges across the switches during turn-off of the switches due to the leakage inductance of the transformer is more severe than in the voltage-fed topologies.

1.2.1.1 Single-Stage Inverters

A single-stage inverter is an inverter that performs the power conversion from dc to ac- both stepping up the low dc voltage and modulating the sinusoidal load current and voltage, in a single stage. Many single-stage inverters, both isolated and non-isolated inverters have been proposed in the past.

One of the single-stage topologies proposed earlier was the differential-boost topology [3]. This topology achieves dc-ac conversion by connecting the inputs of two identical dc-dc boost converters in parallel with a dc source and the load is connected across the outputs of the two dc-dc converters. As opposed to the conventional buck Voltage Source Inverters (VSIs), this topology can generate an output voltage higher than the input voltage. Fig. 3 shows the single-stage differential boost topology.

The major advantages of this topology are the reduced number of switches and a simple topology. The disadvantages of the differential boost topology are : a) the topology is non-isolated; b) the switches are operated at a low switching frequency; c) the size of the magnetics are large leading to a larger footprint for a non-isolated topology.

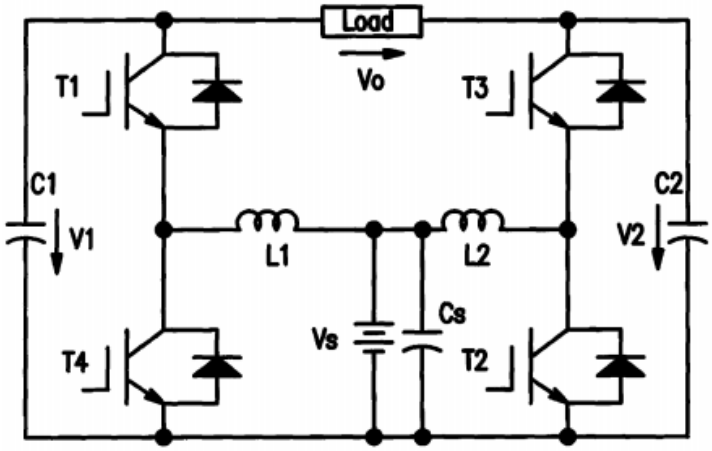

Fig. 3: Topology of differential boost inverter [3].

A differential buck-boost inverter, proposed in [4] is shown in Fig. 4. This operates similar to the differential boost inverter shown in Fig. 3. This inverter can produce an output voltage either higher or lower than the input dc voltage.

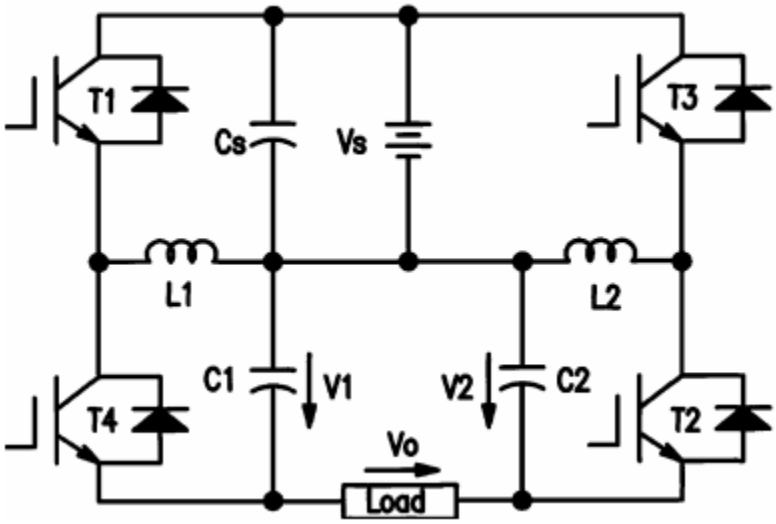

Fig. 4: Topology of differential buck-boost inverter [4].

Another single-stage buck –boost topology was proposed in [5] and the inverter's topology is given in Fig. 5. This topology overcomes the disadvantage of small input voltage range of the buck-boost topology proposed in [4]. But this inverter requires a split input dc voltage source. Two sets of input voltage sources and buck-boost chopper type circuits are connected in anti-parallel to the output capacitor, which generates the output topology. Both the chopper circuits are operated at fixed-frequency in discontinuous conduction mode (DCM). Both the buck-boost

topologies do not provide a high-frequency galvanic isolation though they have lower component count. They also operate at a lower switching frequency and incur switching losses.

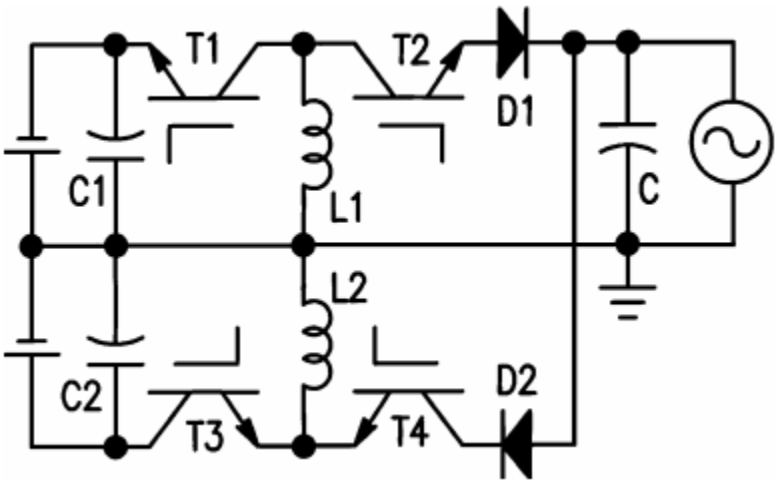

Fig. 5: Topology of differential buck-boost inverter [5].

Fig. 6 shows the topology of a single-stage flyback inverter proposed by Kjaer and Blaabjerg. [6] Two bidirectional flyback converters are connected in parallel to the input voltage source and the load is connected across the two converters. The major advantage of this topology over the above mentioned topologies is the galvanic isolation provided by the high-frequency transformers in both the flyback converters. But the galvanic isolation in this topology has increased foot print. The switches also incur switching losses and hence are limited to low switching frequency operation.

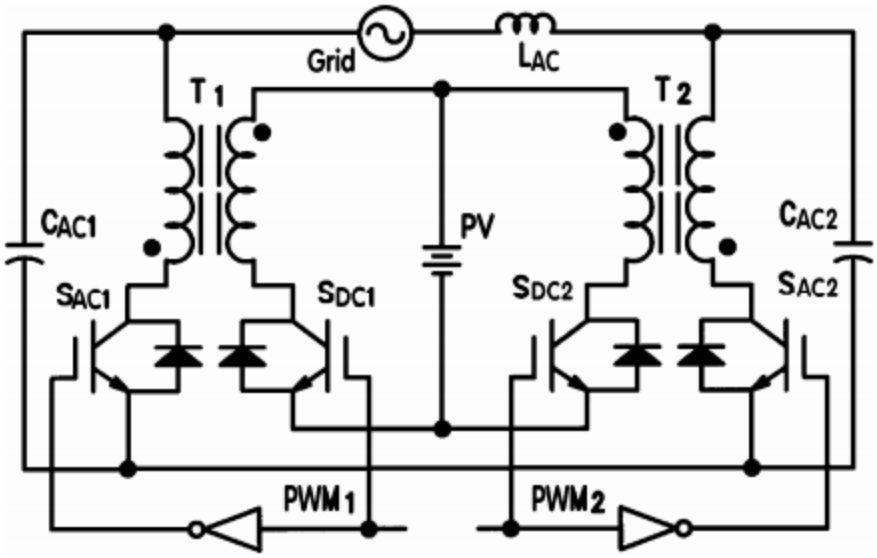

Fig. 6: Topology of single-stage flyback inverter [6].

Fig. 7 represents a single-stage full bridge buck-boost inverter proposed in [7]. This inverter has a full-bridge inverter with a LC resonant tank. The inverter has four main switches (S_1, S_2, S_3 and S_4), two diodes (D_1 and D_2), two resonant inductors (L_1 and L_2), one resonant capacitor (C), one filter inductor (L) and capacitor. The positive half- cycle at the output is generated with the switches S_1, S_3 and diode D_2 and the negative half-cycle is generated with the remaining three devices. Though the inverter topology has only four power switches and two diodes, only two switches are soft switched. Also, the generated sinusoidal waveform consists of quasi sinusoidal pulse robes. This topology also does not isolate the source and the load or grid.

A single stage buck-boost PWM power inverter proposed in [8] is given in Fig. 8. This inverter topology has two buck-boost choppers forming a four switch bridge and an additional two more power switches for synchronous commutation in each half cycle of the output. The major advantage of this topology is the galvanic isolation provided by the high-frequency transformer. But this topology is only suitable for low power applications (reported maximum power is 140 W).

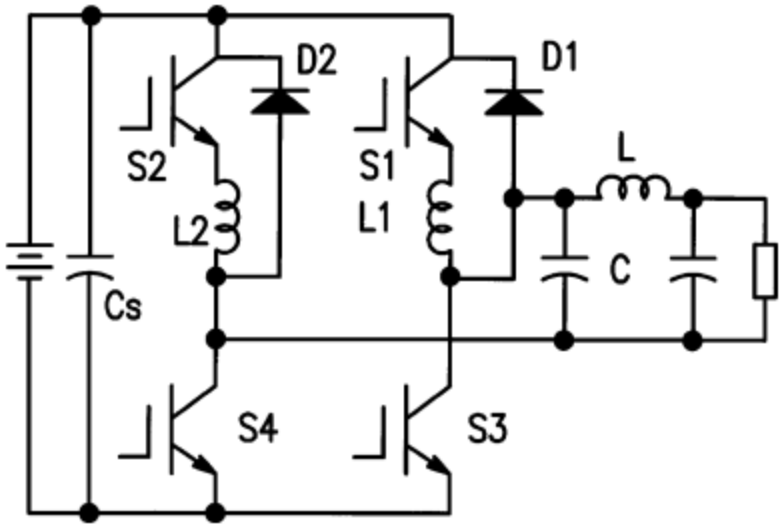

Fig. 7: Topology of single-stage full-bridge buck-boost inverter [7].

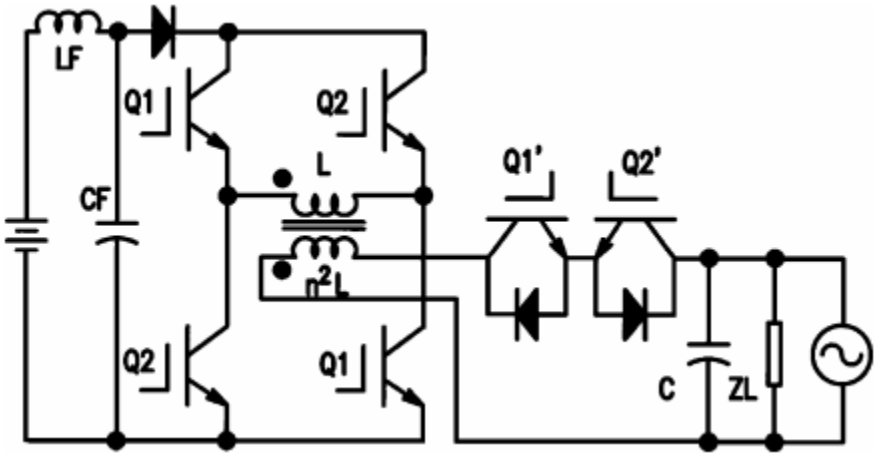

Fig. 8: Topology of single-stage buck-boost PWM power inverter [8].

Fig. 9 shows the topology of a transformerless voltage boosting inverter proposed in [9]. This topology is a buck-boost derived topology and has six power switches and an energy storage inductor, *L*. This topology was proposed for low power applications. The ac output is synthesized by charging the inductor, L from different directions in each half cycle. This topology is highly

compact without any huge magnetics but is only suitable for very low power applications (50 W). The absence of a galvanic isolation and the higher device for count for even low power applications are the major disadvantages of the topology.

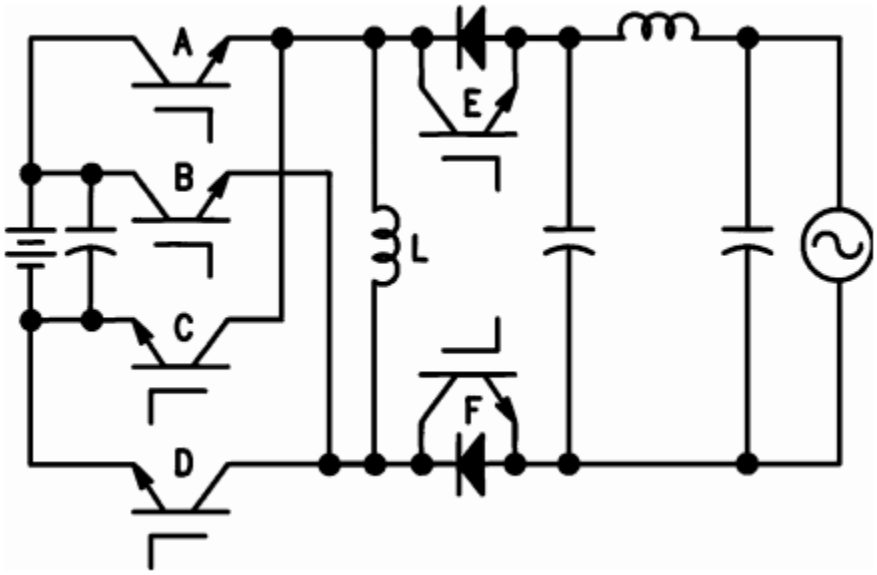

Fig. 9: Topology of a transformerless voltage boosting inverter [9].

One of the major advantages with the buck-boost derived topologies referred in this section is, though non-isolated, these topologies have an energy storage inductor, which prevents direct connection between the source and the load. But, the main issue with the buck-boost derived topologies is the high- peak inductor current stress due to the sudden transfer of energy through the inductors from source to load during each switching cycle. The buck-boost topologies also have lower boost capability when compared to the boost derived topologies. The differential boost proposed in [3] and the inverter proposed in [10] are free from the high inductor current stress but are non-isolated topologies.

Another single stage topology, differential Ćuk topology proposed in [11] is shown in Fig. 10. This topology achieves direct dc/ac conversion by connecting the load differentially across two bidirectional dc/dc Ćuk converters and modulating them sinusoidally with 180 degrees phase difference. This topology utilizes only four main switches, making the inverter topology simple and reducing the cost. The differential Ćuk inverter also has room for magnetics integration, thereby reducing the foot print of the inverter. But, this topology does not employ any soft switching techniques to aid the switching of the main switches. This topology also suffers from spikes in the magnetics.

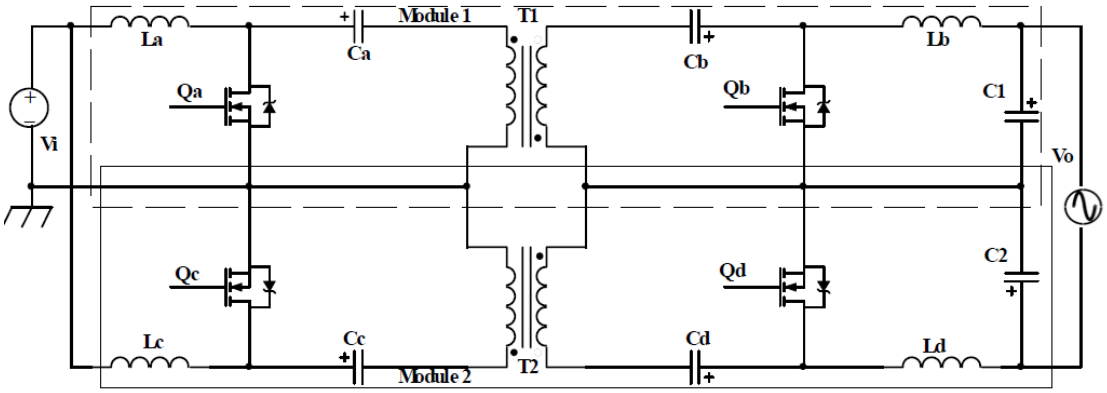

Fig. 10: Topology of the single-stage differential Ćuk inverter [11].

1.2 Proposed Power Electronics Interface

Most single-stage DPC architectures proposed in the past have increased foot print, no galvanic isolation, lower boost capability, stresses in the power switches due to hard switching, stress in the components due to spikes that arise because of difference in the energies between source and the load and are not suitable for medium power applications.

The proposed architecture (shown in Fig. 12) is based on such a topological approach. It is a differential mode (Fig. 11) current-fed ZCS based voltage-doubling PV inverter. This inverter has the following features:

- It can boost low-voltage (30-60 V) input to a 120-V/ 60-Hz output
- It does not require a bulky line transformer
- It does not require a front end dc/dc converter
- The topology has inherent voltage boost/gain property thereby reducing the reliance on the transformer turns ratio

Voltage-doubler or half-bridge is selected as it reduces the need for two switches and the transformer turns ratio to half. The inverter requires a smaller transformer because:

- The inverter switches at 100 kHz
- The transformer voltage and current are bipolar in every switching cycle
- Only half the input current flows through the transformer at any given instant of time.

Further, since the operation of the inverter is in differential mode, the ZCS scheme for individual dc/dc converters [16] retains in effectiveness for the inverter.

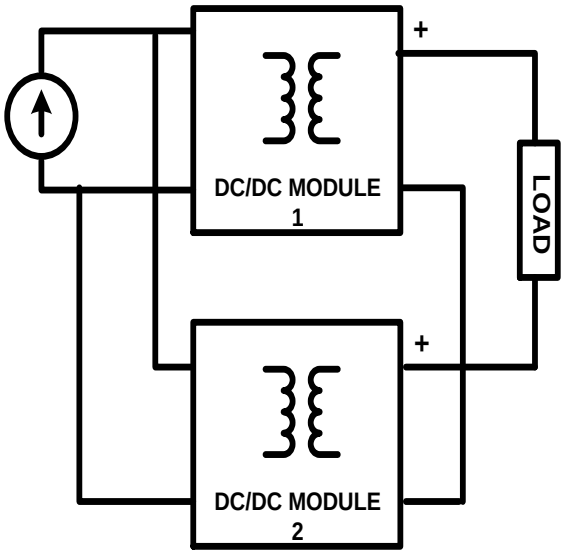

Fig. 11: Configuration of the proposed inverter.

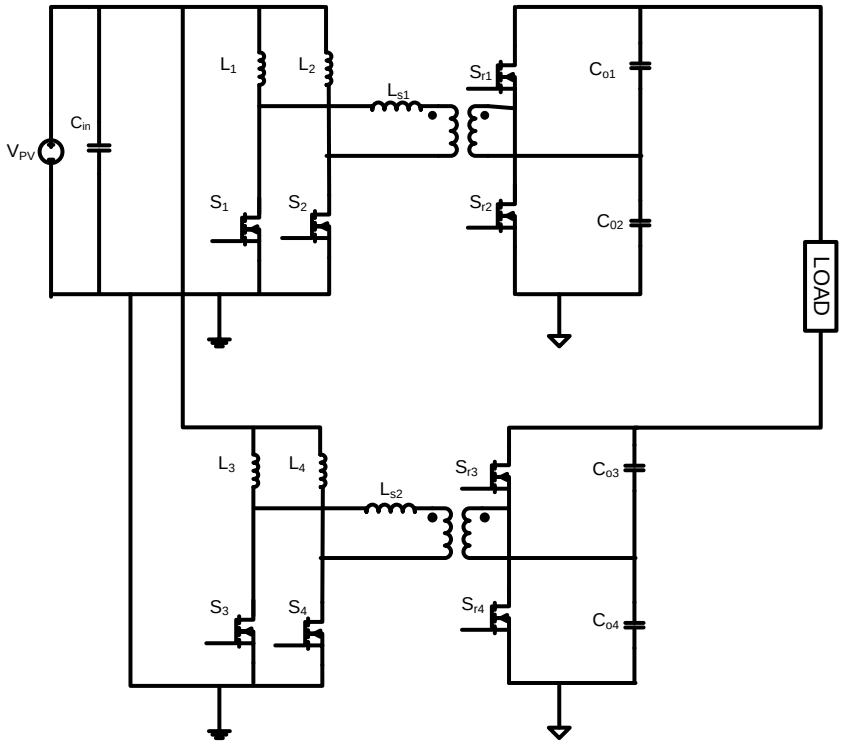

Fig. 12: Topology of the proposed PEI.

Fig. 11 shows the modular configuration of the inverter operating in differential mode. The two dc/dc converter modules are connected differentially. The primaries of the individual dc/dc converters in Fig. 12, sourced by PV source, are connected in differential mode and the output of the current-fed inverter is the difference of the outputs of the two individual dc/dc converter modules.

In addition to the modular differential-single-phase operation (Fig. 12), these inverters can also be extended to operate in three-phase mode. When the modules are defined as single stage inverter, like in Fig. 13, three such single-phase inverters can construct a three-phase at the output. When the modules are restricted to dc/dc converter, three modules of the dc/dc converter can create three phase output, like in Fig. 14. The inputs to the modules are connected in parallel to the source and the loads can be connected in either delta or wye fashion. So due to the above mentioned advantages and ability to operate with lower input voltage, these differential topologies are a good candidate for renewable energy applications which demand low cost and high efficiency. The modularity broadens the scope of the topology to be used for multiple renewable source applications based on the need; as a dc/dc converter or single-phase inverter or multi-phase inverter. These current-sourced configurations also have bidirectional operation which widens the application horizon.

The principles of operation of the single-phase inverter under hard-switching and soft-switching conditions are presented in chapter 2. The operation of the converter as a dc/dc converter is also presented in chapter 2. The design of the power stage and the control strategy of the inverter are presented in chapter 3.

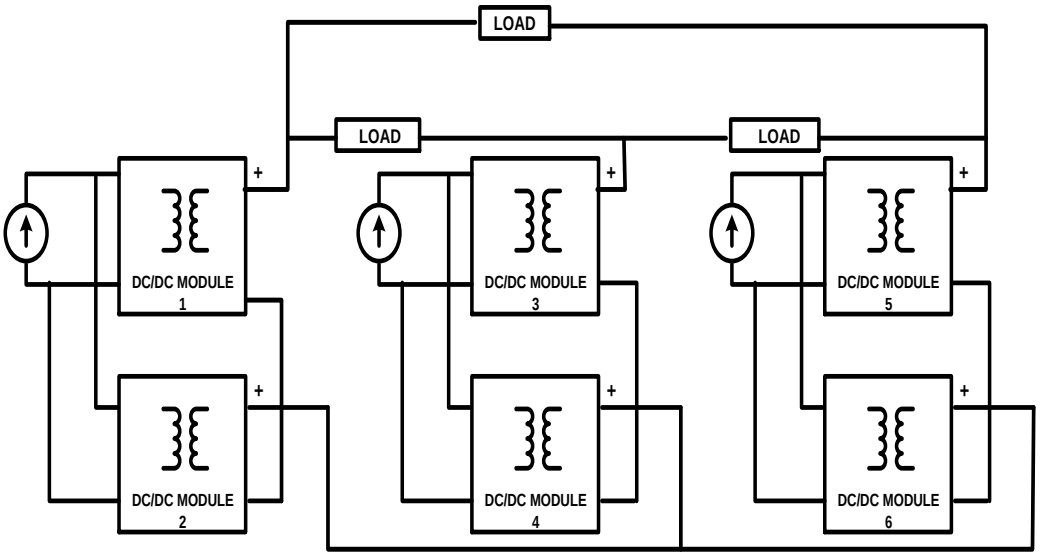

Fig. 13: Possible configuration of the three-phase inverter when module is defined at dc/ac converter level

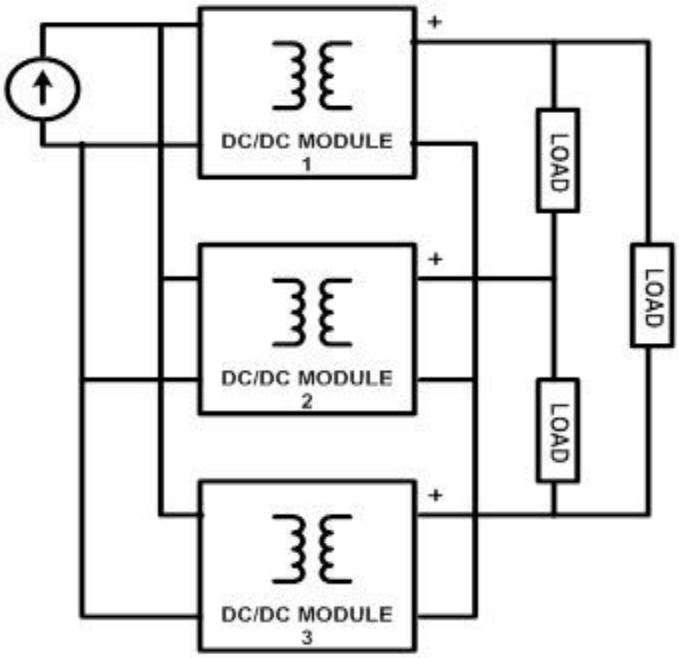

Fig. 14: Possible configuration of the three-phase inverter when module is defined at dc/dc converter level

2. PRINCIPLE OF OPERATION

The inverter has two individual dc/dc converter modules as shown in Fig. 16. The primaries of the two individual dc/dc converters, sourced by the photovoltaic energy source, are connected in differential mode and the output of the proposed current-sourced inverter is the difference of the outputs of the two individual dc/dc converter modules. Each module has two primary-side switches, namely S_1 and S_2 and S_3 and S_4 and corresponding secondary-side switches S_{r1} and S_{r2} and S_{r3} and S_{r4} respectively. The switching frequency of the inverter is 100 kHz. The switches in each module are modulated so that the individual converters produce a dc-biased sine wave output so that each converter only produces a unipolar voltage. The modulation of each converter is 180º out of phase with the other, so that the voltage excursion at the load is maximized. That is, switch pairs S_1 and S_2 and S_3 and S_4 are operated in the same way but with a phase difference of 180º. Since the load is connected differentially across the converters, the dc-bias appearing at either end of the load with respect to ground gets cancelled and the differential dc voltage across the load is zero. Switch pairs S_1-S_{r1}, S_2-S_{r2}, S_3-S_{r3} and S_4-S_{r4} are triggered with complementary pulses.

Under hard-switching condition, the output voltages of the individual converters are given by the following equations:

$$V_{o1} = \frac{2nV_{PV}}{1 - d_1}$$

$$V_{o2} = \frac{2nV_{PV}}{1 - d_2}$$

where d_1 and d_2 are the duty ratios of the primary-side switches of the first and second modules, respectively. The symbol n represents the turns ratio of the transformers in both the modules. The

output voltage of the inverter is the difference in the output voltages of the individual dc/dc converter modules and is given by the following equations:

$$V_o = V_{o1} - V_{o2}$$

$$V_o = \frac{2nV_{PV}}{1-d_1} - \frac{2nV_{PV}}{1-d_2}$$

$$V_o = 2nV_{PV}[\frac{d_1 - d_2}{(1-d_1)(1-d_2)}]$$

Let $d_1 = D + D'\sin(\omega t)$ and $d_2 = D - D'\sin(\omega t)$, then the voltage gain of the inverter is given by the following equation:

$$\frac{V_o}{V_{PV}} = 4n\sin(\omega t)\,[\frac{D'}{(1-D)^2 - D'^2\, sin^2(\omega t)}]$$

The voltage gain of the inverter depends on the transformer turns ratio and the duty ratio. Thus, an optimum balance between the turns ratio (n) and duty ratio is the key. The primary-side switches have a duty ratio range of 50% to 100%. The inverter cannot be operated below a duty ratio of 50% to avoid a condition of inconsistency in the input inductors currents.

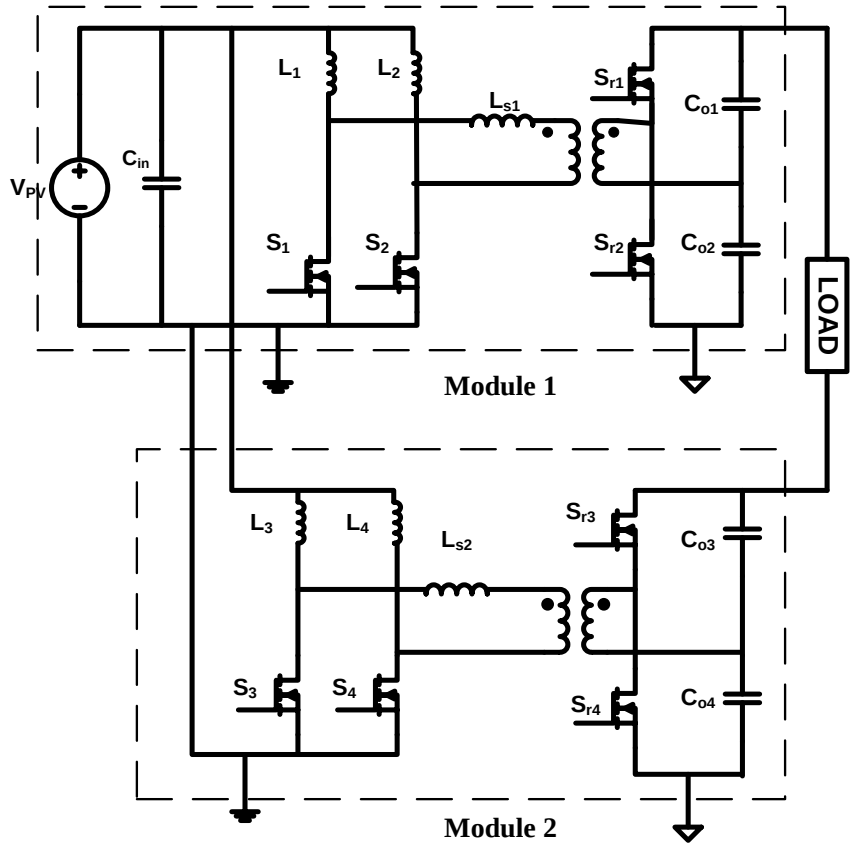

Fig. 15: Topology of the differential-mode inverter.

2.1 Hard-Switched Modes

The hard-switched modes of the topology in Fig. 15 are presented in Figs. 16-21. When S_1 and S_2 or S_3 and S_4 of each of the modules are turned on simultaneously, the boost mode of the individual converters is initiated. During this mode, the output capacitors of one module feed energy to the output capacitors of the other module through the load. For all other switching configurations, there is an exchange of power between the primary and secondary of the individual dc/dc converter module as well as from one dc/dc converter module to another. In addition, in these modes, there is a localized charging of output capacitor of one of the dc/dc converter modules. The direction of power flow between the individual modules depends on

the time-domain voltage and current waveforms. For instance, for a unity-power-factor passive load, during a positive line cycle of the output voltage (across the load), power flows from the PV source via the upper module to the bottom module while during the negative half cycle, power flows via bottom module to the upper module.

The operation of the inverter in the positive half cycle of the output is analyzed by the following modes:

Mode 1: Fig. 16 represents this hard-switched mode of the inverter. During this interval, the primary-side switches of both the modules, S_1, S_2, S_3 and S_4 are turned on. Hence, current in both the transformers is zero. Power to the load is supplied by the output capacitors of the upper module C_{o1} and C_{o2}. The output capacitors of the lower module, C_{o3} and C_{o4} are charged in this mode. The lower dc/dc converter acts as the receiving module in this mode. The input current in the upper and the lower modules from the PV source is given by i_{in1} and i_{in2}, respectively. The currents through the primary-side switches are given by the following equations:

$$i_{s1} = i_{s2} = \frac{i_{in1}}{2}$$

$$i_{s3} = i_{s4} = \frac{i_{in2}}{2}$$

Mode 2: Fig. 17 represents this hard-switched mode of the inverter. In this interval, primary-side switches of the upper and the lower module, S_1 and S_3 respectively, and secondary-side switches of the upper and the lower module, S_{r2} and S_{r4} respectively are turned on. The negative current raises through the leakage of the upper module's transformer, L_{S1} and the current through switch S_1 raises with the same slope as the current through L_{S1}. Output capacitor C_{o2} of the upper module is charged and capacitor C_{o1} discharges through the load, C_{o3}

and the secondary of the transformer of the lower module. Output capacitor C_{o4} of the lower module is also charged in this mode. The current through the leakage inductance L_{s2} of the transformer in the lower module is positive and begins to increase with the same slope as the current through the leakage inductance L_{S1}. The currents through the primary-side switches and the leakage inductors are given by the following equations:

$$i_{Ls1} = -\frac{V_{o1}}{2nL_{s1}}(\Delta t)$$

$$i_{Ls2} = \frac{V_{o2}}{2nL_{s2}}(\Delta t)$$

$$i_{s1} = \frac{i_{in1}}{2} + i_{Ls1}$$

$$i_{s3} = \frac{i_{in2}}{2} + i_{Ls2}$$

where Δt is the time interval for Mode 2.

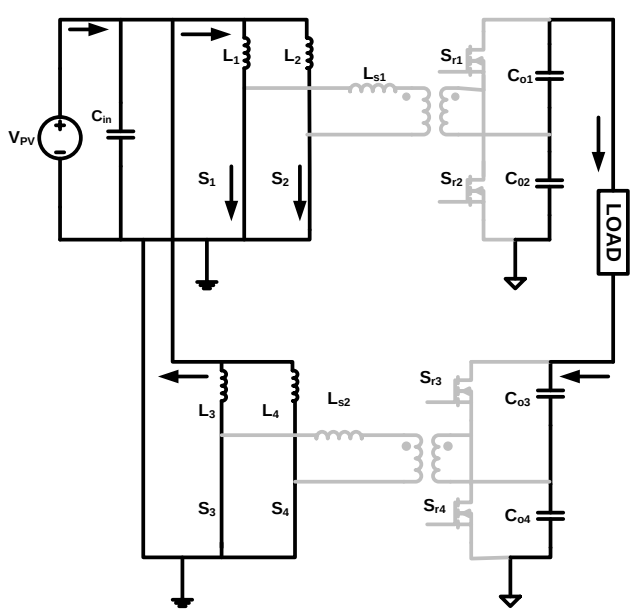

Fig. 16: Mode 1

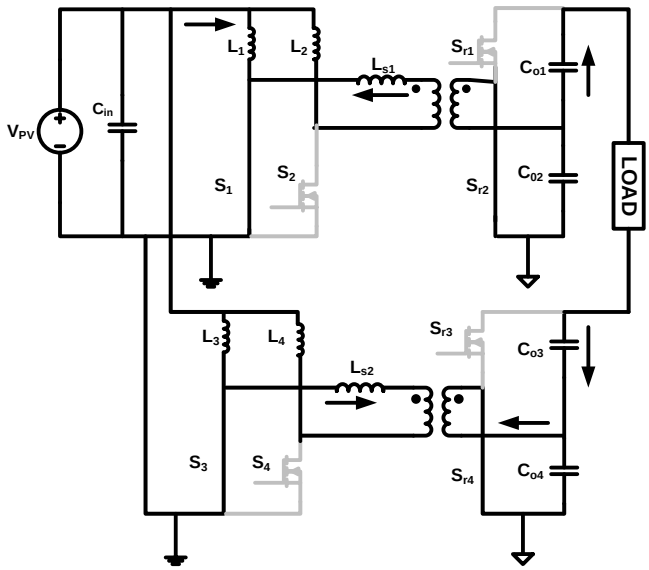

Fig. 17: Mode 2

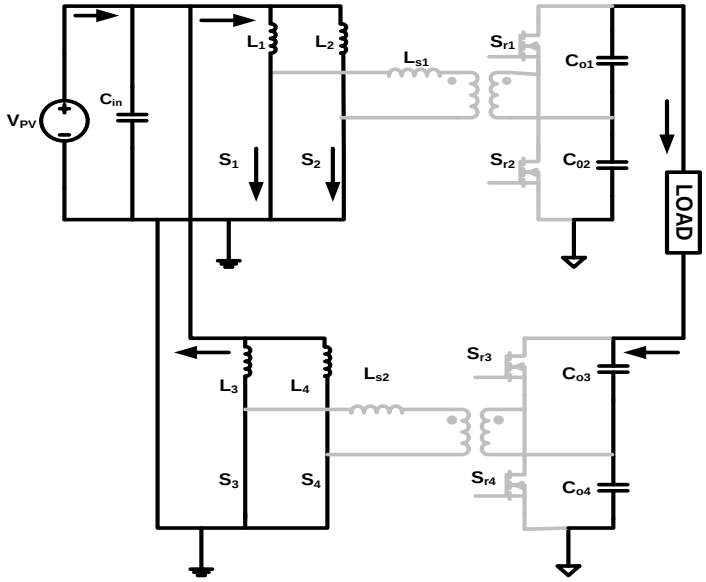

Fig. 18: Mode 3

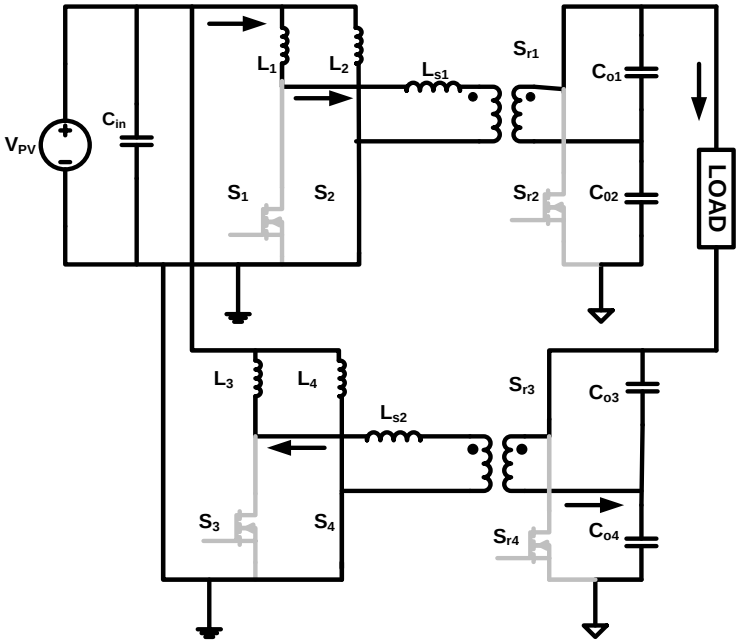

Fig. 19: Mode 4

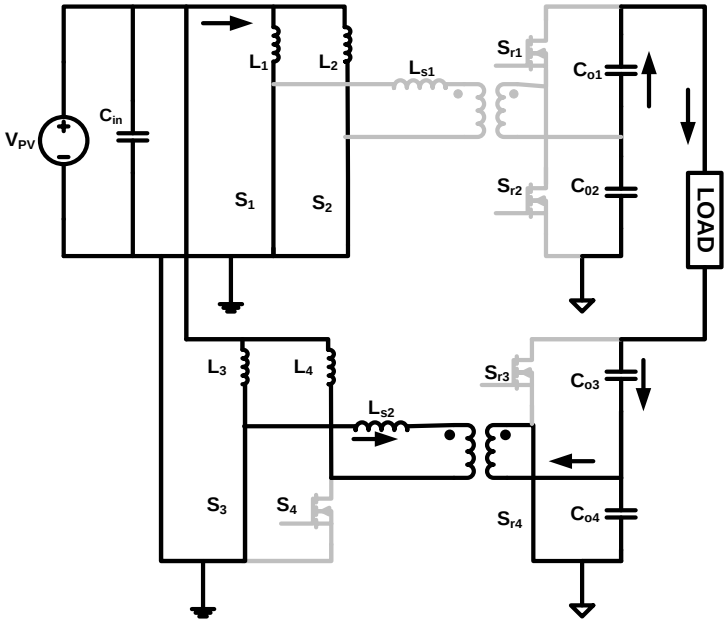

Fig. 20: Mode 5

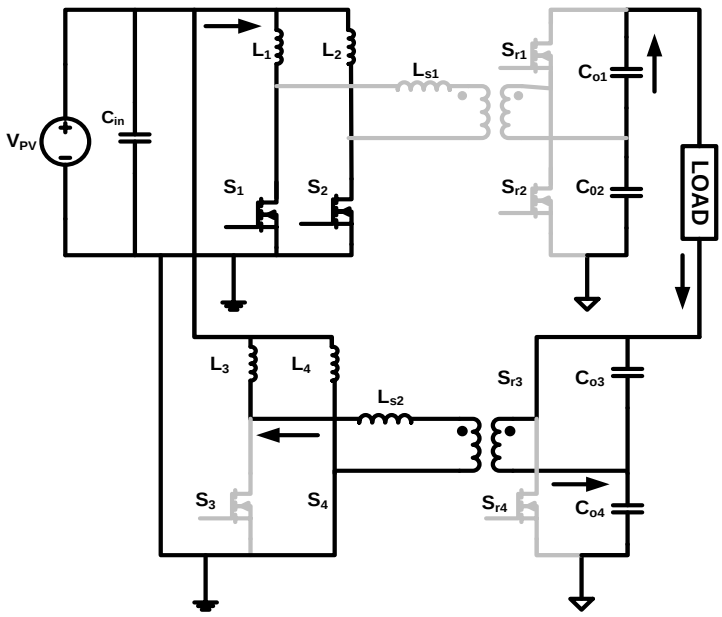

Fig. 21: Mode 6

Mode 3: Fig. 20 represents this hard-switched mode of the inverter. This mode is similar to the mode1 where all of the primary-side switches in both the modules are turned on and all of the secondary-side switches of both the modules are turned off. The current through the transformers in both the modules is zero. The output capacitors of the upper module feed the load and the lower module.

Mode 4: Fig. 21 represents this hard-switched mode of the inverter. In this mode, the primary-side switches of the upper and lower modules, S_2 and S_4 respectively and secondary-side switches of the upper and lower module, S_{r1} and S_{r3} respectively, are turned on. The current through the primary-side switch in the upper module, S_1 in Mode 3 is diverted to L_{S1} due to the voltage across the primary of the upper transformer, which in turn, is due to the voltage across output capacitor of the upper module, C_{o2}. Output capacitors C_{o1} and C_{o3} are charged by the PV source. Output capacitor C_{o2} discharges through the load, the transformers' secondary, and C_{o4}. Current through S_2 and the negative current through L_{S2} rise with the same slope as the

current through L_{S1}. The currents through the primary-side switches and the leakage inductors are given by

$$i_{Ls1} = \frac{V_{o1}}{2nL_{s1}}(\Delta t)$$

$$i_{Ls2} = -\frac{V_{02}}{2nL_{s2}}(\Delta t)$$

$$i_{s2} = \frac{i_{in1}}{2} + i_{Ls1}$$

$$i_{s4} = \frac{i_{in2}}{2} + i_{Ls2}$$

<u>Mode 5:</u> Fig. 20 represents this hard-switched mode of the inverter. In this mode, primary-side switches of the upper module, $S_1$and S_2 and primary-side switch of the lower module, S_3 and secondary-side switch of the lower module, S_{r4} are turned on. The current through the transformer in the upper module is zero. Output capacitors of the upper module, C_{o1} and C_{o2}, discharge through the load, output capacitor of the lower module, C_{o3}, and the secondary of the transformer of the lower module. Output capacitor C_{o4} of the lower module is also charged in this mode. The current through the leakage inductance of the lower module, L_{s2} is positive. The currents through switch S_3 and L_{s2} are given by

$$i_{s3} = \frac{i_{in2}}{2} + i_{Ls2}$$

$$i_{Ls2} = \frac{V_{o2}}{2nL_{s2}}(\Delta t)$$

Mode 6: Fig. 21 represents this hard-switched mode of the inverter. In this mode, primary-side switches of the upper module, S_1 and S_2, primary-side switch of the lower module, S_4, and secondary –side switch of the lower module, S_{r3} are turned on. The current in the transformer of the upper module is zero. Output capacitors of the upper module, C_{o1} and C_{o2}, discharge through the load, secondary of the transformer of the lower module, and capacitor C_{o4}. Output capacitor of the lower module, C_{o3} is also charged in this mode. The currents through L_{s2} and switch S_4 are given by

$$i_{Ls2} = -\frac{V_{o2}}{2nL_{s2}}(\Delta t)$$

$$i_{s4} = \frac{i_{in2}}{2} + i_{Ls2}$$

Table. 1: Possible switching states of the inverter under hard-switched operation.

Switching states of the inverter	S_1	S_2	S_3	S_4
a.	1	1	1	1
b.	1	0	1	0
c.	0	1	0	1
d.	1	1	1	0
e.	1	1	0	1
f.	0	1	1	1
g.	1	0	1	1

Modes 5 and 6 determine the maximum point and the zero crossing of the output. The zero crossing occurs when difference in the output of the two modules is zero; while the maximum point occurs when the difference of the individual outputs is maximum. The feasible switching states of the inverter are provided in Table. 1. The first set of three switching states (i.e. a-c) form major part of a switching cycle. The last set of four switching states (i.e. d-g) exists for a

shorter duration and may exist either in the positive half cycle or in the negative half cycle. Switching states, d-g, occur in the vicinity of the maximum, the minimum, or the zero-crossing point of the output voltage.

2.2 ZCS Operation of the Inverter

The ZCS operation of the individual dc/dc converter modules is retained for the differential operation of the converters. The following assumptions are made for the analysis of the ZCS operation of the inverter: a) the input inductors are assumed large enough so that the current through them can be considered constant; b) magnetizing inductance of the transformers are assumed infinitely large; c) all the components are ideal.

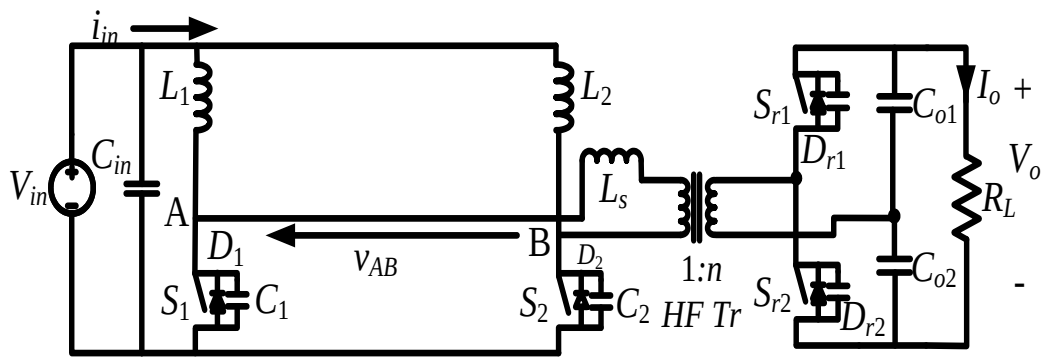

Fig. 22: Topology of individual dc/dc converter module.

2.2.1 ZCS Operation of the dc/dc converter

Fig. 22 represents the individual module while operating as a dc/dc converter. The primary-side switches of a single module, S_1 and S_2 are operated with gating signals that are phase shifted by 180º with an overlap. The overlap varies with the duty-ratio of the dc/dc converter which depends on the input voltage and the load demands. As in the inverter, the duty-ratio of the primary-side switches are always greater than 50% and those of the secondary-side switches are always less than 50%. Fig. 23 gives the timing diagram of the soft-switching of the dc/dc converter.

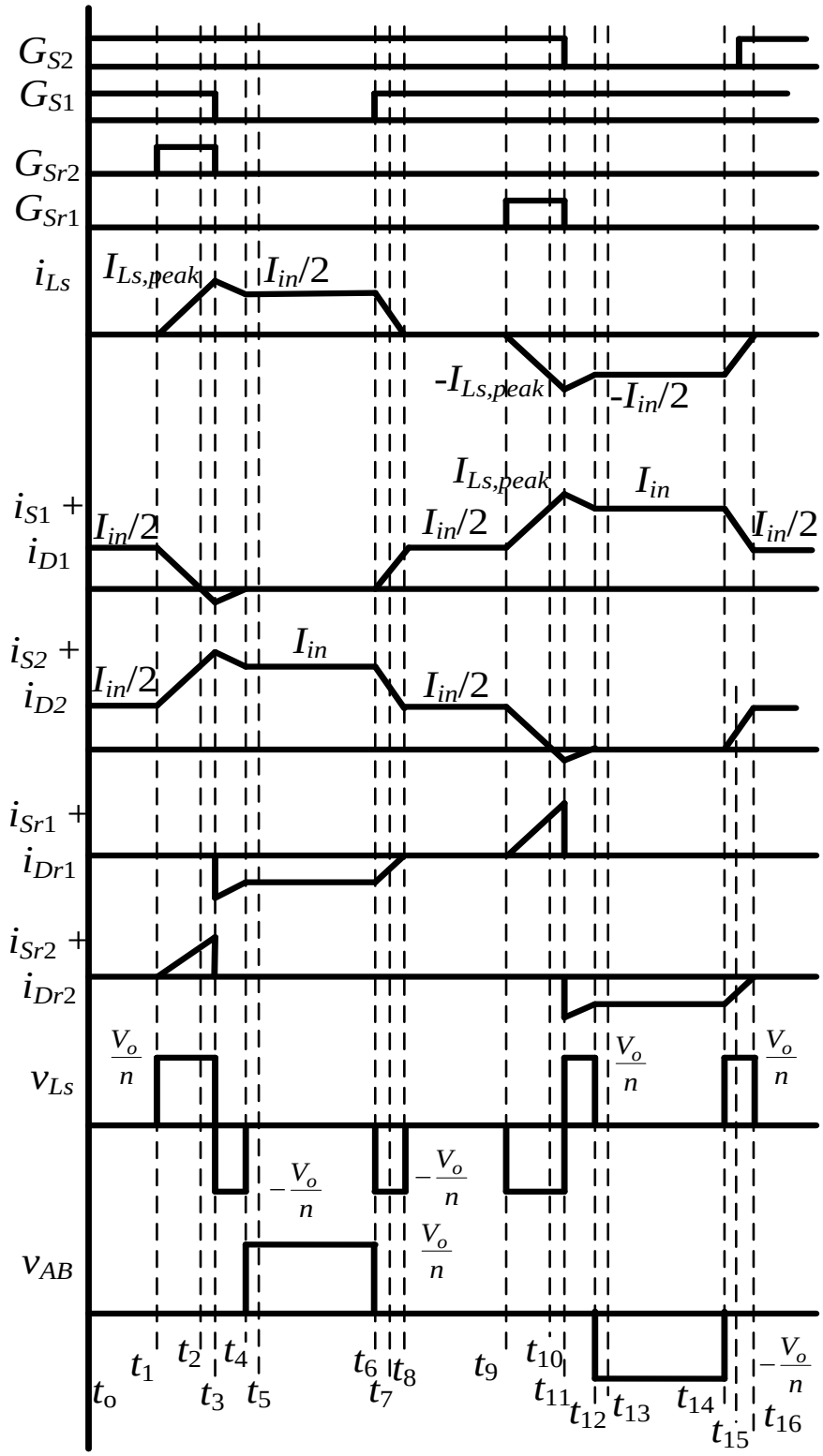

Fig. 23: Timing diagram of the dc/dc converter operation during half-cycle.

2.2.2 ZCS Operation of the inverter

The ZCS scheme of the inverter is different from the ZCS scheme of the dc/dc inverter because the input inductor current is time varying and hence the timing of the secondary-side switches for ZCS vary with the magnitude of the inductor current for maximum effectiveness. For ZCS operation, in between the Modes 1-6, every time a primary switch has to be turned off, one secondary switch is also turned on for a very short duration, leading to additional modes. For instance, secondary-side switch S_{r2} is turned on before the turn off of primary-side switch S_1 in the upper module. The duration for which S_{r2} has to be turned on depends on the current through switch S_1. The following modes are the additional ZCS modes of the inverter.

Mode 1→2: (Fig. 24) This mode is introduced to turn off primary-side switches S_2 and S_4 in the top and bottom modules respectively before Mode 2. Secondary –side switches S_{r1} and S_{r3} are turned on to aid ZCS of S_2 and S_4 in Mode 2. When S_{r1} is turned on, voltage across output capacitor C_{o1} is applied across the secondary of the transformer. This causes a voltage at the primary of the transformer and hence the current through switch S_2 is diverted to leakage inductor L_{s1}, allowing the switch to turn off in ZCS condition. The capacitor C_{o2} discharges through the load, C_{o3}, and the secondary of the transformer.

Mode 3→4: (Fig. 25) This mode is introduced to turn off primary-side switches S_1 and S_3 in the top and bottom modules respectively before Mode 4. Secondary-side switches S_{r2} and S_{r4} are turned on to aid ZCS of S_1 and S_3. When S_{r2} is turned on, the voltage across output capacitor C_{o2} is applied across the secondary of the transformer. This causes a voltage at the primary of the transformer and hence the current through switch S_1 is diverted to leakage inductance L_{S1}, allowing the switch to turn off in ZCS condition. In this mode the capacitor C_{o1} discharges through the load, capacitor C_{o3} and the secondary of the transformer.

Mode 4→5: (Fig. 26) This mode is introduced to turn off primary-side switch S_4 in the bottom module by turning on secondary-switch S_{r3} before Mode 5. When switch S_{r3} is turned

on, the voltage across output capacitor C_{o3} is applied across the secondary of the lower transformer. This causes voltage across the primary of the transformer and hence the current through primary switch S_4 is diverted to leakage inductance L_{S2}. Thus, S_4 turns off in ZCS condition.

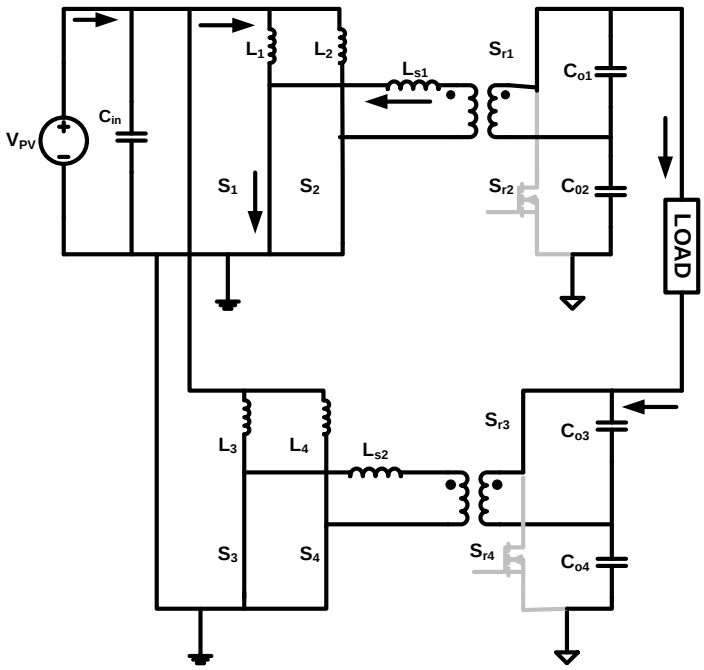

Fig. 24: Mode 1->2

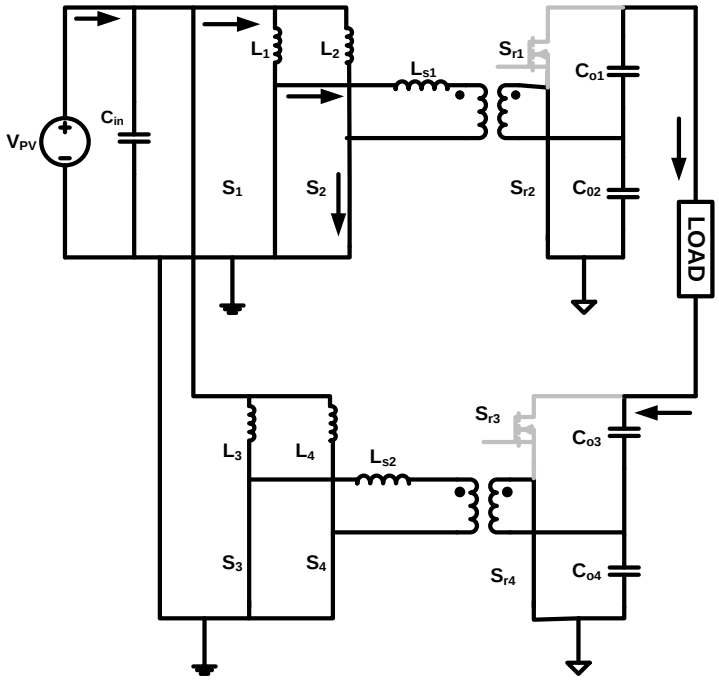

Fig. 25: Mode 3->4

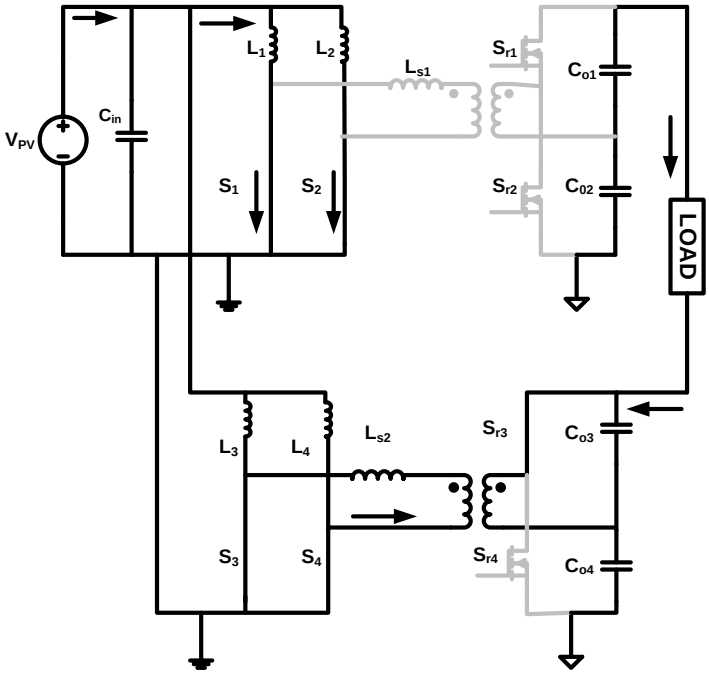

Fig. 26: Mode 4->5

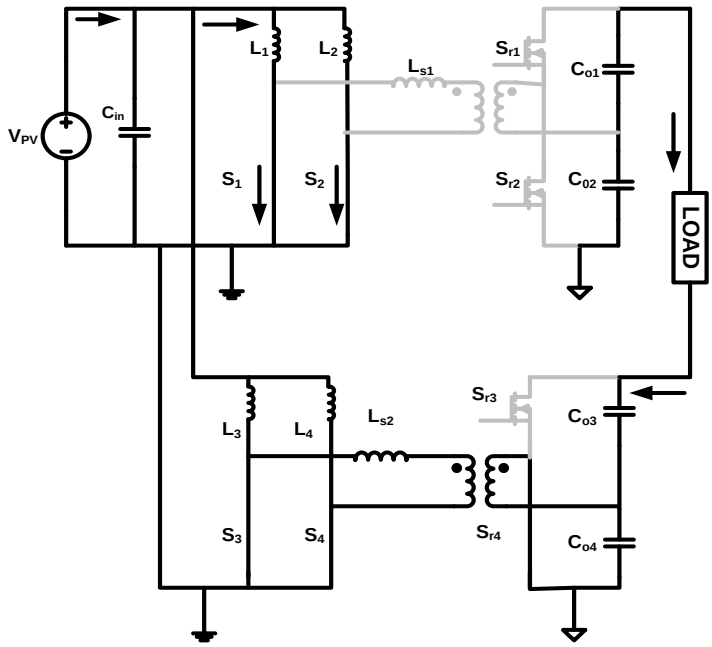

Fig. 27: Mode 5->6

<u>Mode 5→6</u>: (Fig. 27) This mode is introduced to turn off primary-side switch of bottom module S_3 by turning on S_{r4} before Mode 6. When switch S_{r4} is turned on, the voltage across output capacitor C_{o4} is applied across the secondary of the lower transformer. This causes voltage across the primary of the transformer and hence the current through switch S_3 is diverted to leakage inductor L_{S2}, thereby enabling ZCS turn off of the switch S_3.

This additional duty cycle of the secondary side switches is represented as d_r.

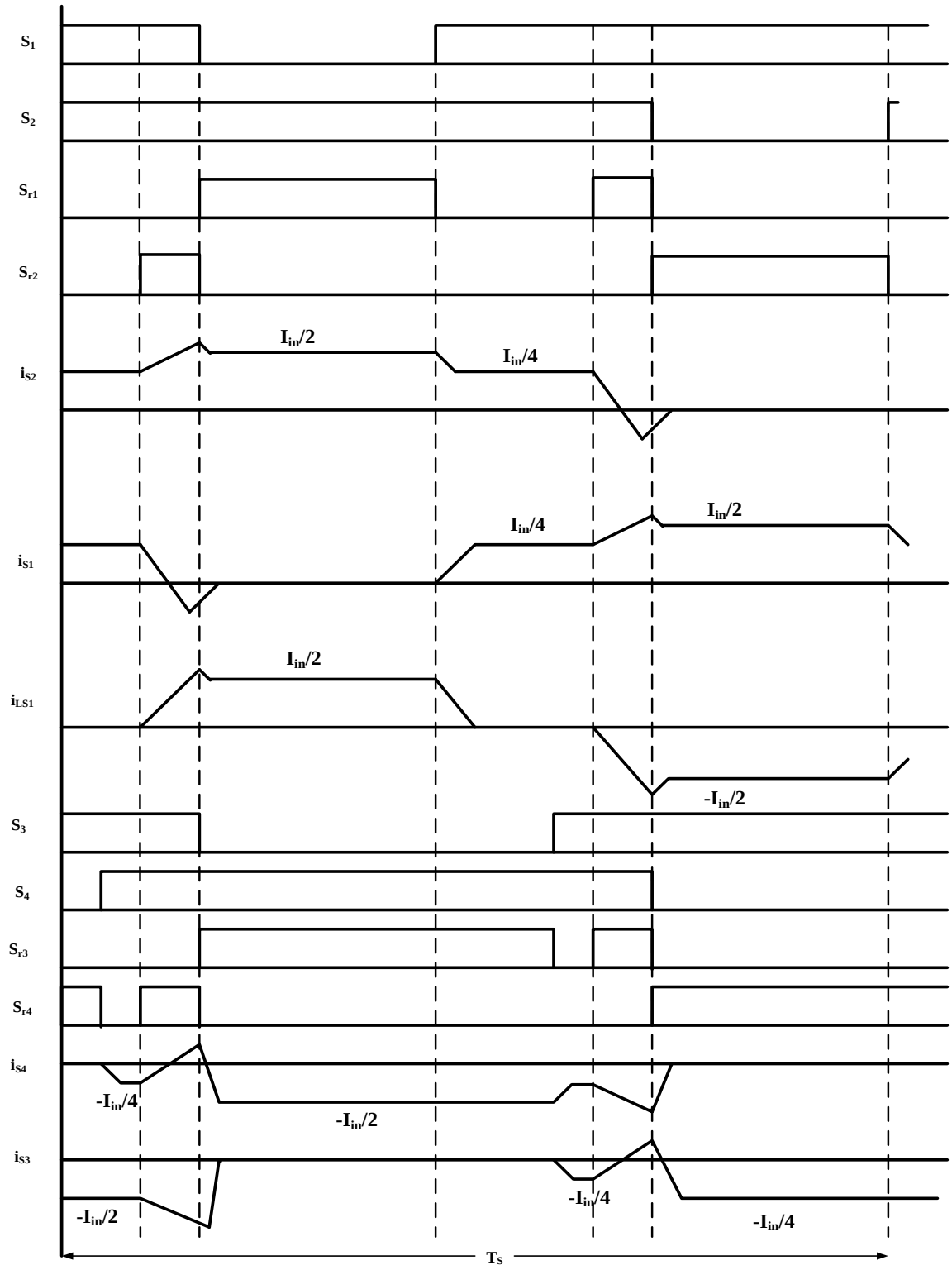

Fig. 28: Timing diagram of the inverter during one switching cycle for positive half cycle of load.

2.3 Generation of switching signals

The sinusoidal reference has a dc-offset of 64% to maintain the duty ratio above 50% for all the primary-side switches of both the modules, at all times. Thus the duty ratio of the primary-side switches varies between 50% and 78%. For Module 1, under hard-switched condition, the sinusoidal reference is compared with a trailing-edge carrier-signal to generate switching signal for primary-side switch S_1. Thus the duty ratio of the primary-side switches varies between 50% and 78%. The complimentary signal of S_1 is the switching signal for S_{r1}. The carrier-signal for switches S_2 and S_{r2} is time displaced in comparison to the carrier signal for switches S_1 and S_{r1}. For Module 2, the sinusoidal reference is phase sifted by 180º to generate switching signals for S_3, S_4, S_{r3} and S_{r4}.

For Module 1, under soft-switched condition, the sinusoidal reference is compared with a trailing-edge carrier-signal to generate switching signal for primary-side switch S_1. The complimentary signal of S_1 is added with a pulse train information for soft-switching to generate the switching signal for S_{r1}. The pulse train information for soft-switching is generated by fixing the turn off time of the primary-side switches using trailing-edge carrier-signals. The carrier-signal for switches S_2 and S_{r2} is time displaced in comparison to the carrier signal for switches S_1 and S_{r1}. For Module 2, the sinusoidal reference is phase sifted by 180º to generate switching signals for S_3, S_4, S_{r3} and S_{r4}, similar to the hard-switched condition.

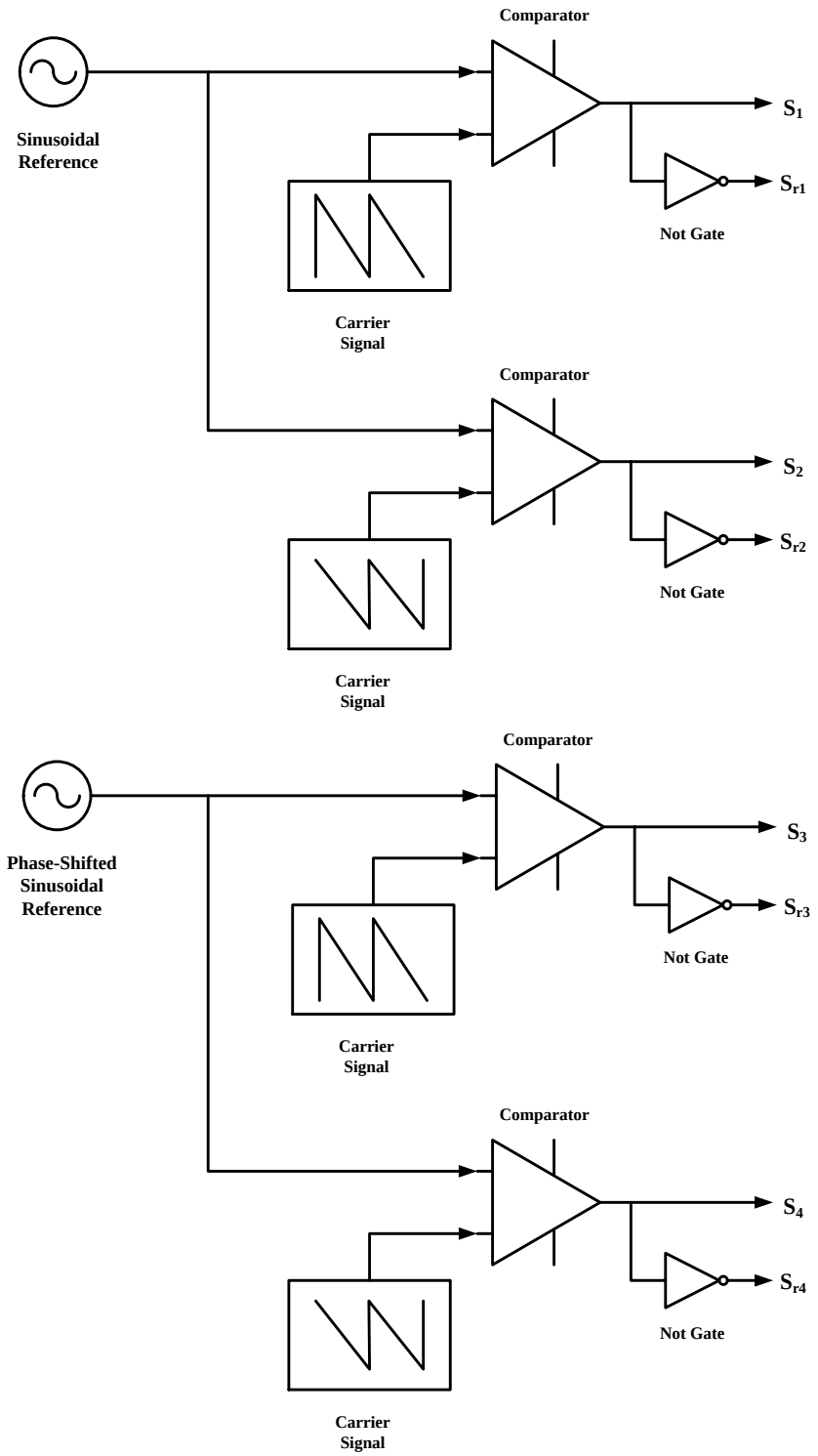

Fig. 29: Generation of switching signals under hard-switched condition.

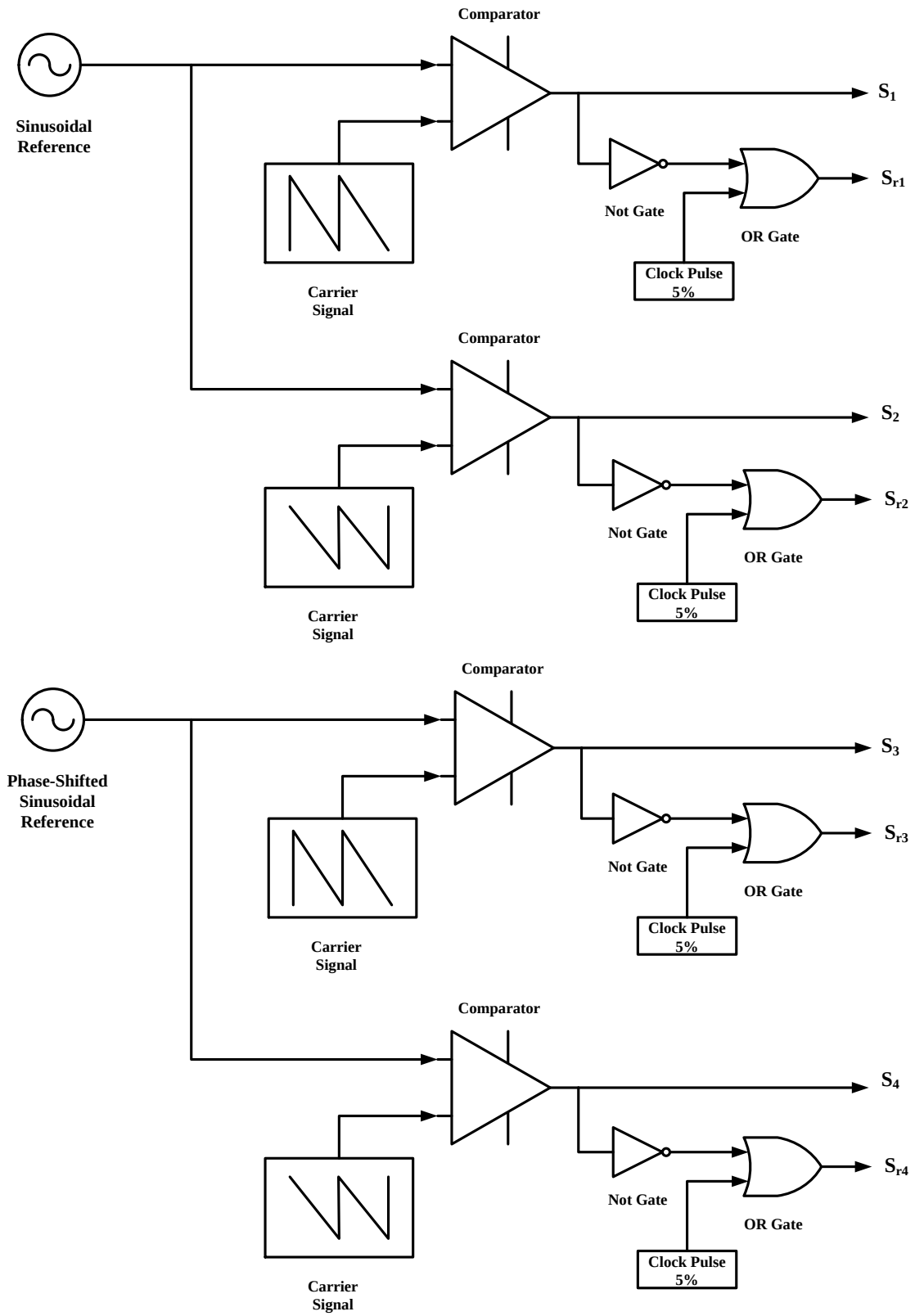

Fig. 30: Generation of switching signals under soft-switched condition.

3. DESIGN OF THE INVERTER AND RESULTS

The power stage specifications of the differential inverter are as follows:

- Input Voltage (V_{PV}): 36 V
- Root-Mean-Square (RMS) Output Voltage (V_{orms}): 120 V
- Output Power (P_o): 500 W
- Switching Frequency (f_s): 100 kHz

The lower limit of the duty ratios of the two modules, d_1 and d_2 is 0.5 to avoid a condition of inconsistency in the currents through the input inductors. For further analysis, the constant offset D is fixed at 0.64 and the upper and lower limits of d_1 and d_2 vary between 0.5 and 0.78.

The key factors that influence the design of the inverter are:

- Cost: The following aspects of the design of the inverter determine the cost of the inverter:
  - The component count- The number of power devices, magnetics, and capacitors. The inverter has a reduced component count since it does not require any auxiliary devices to achieve soft switching in the devices. The secondary side switches, which are mandatory to establish bidirectionality, also take care of the soft switching.
  - Size of the magnetics- Size of the core and the number of windings.
  - Type of components.
  - Complexity of the topology.
- Power Density: Higher power density is governed by the following aspects of the design:
  - Size of the components- The size of the transformer; inductor and output capacitors determine the power density of the system. The current and voltage through the transformer are bipolar, with a zero average which reduces the size

of the cores of both the transformers. The scope for the integration of the magnetics is an additional design advantage for the power density of the inverter.

- The component count.

- Efficiency: The following are the major factors that account for the losses in the inverter:
  - Conduction losses in the primary-side and secondary-side power devices.
  - Switching losses in the primary-side and secondary-side power devices.
  - Core loss in the input inductors and transformers
  - Winding losses in the magnetics.
  - Losses due to Equivalent Series Resistance (ESR).
- Reliability: The following aspects of the design of the inverter determine the reliability of the inverter:
  - The amount of stress that the devices are subjected to, affects the reliability of the inverter. The primary-side devices are affected due to difference in the energy between the input inductors and the leakage inductance.
  - The dV/dt and di/dt stresses in the power devices also affect the reliability of the inverter.

3.1 <u>Input Inductors</u>

The PV cell supplies maximum output power when its output voltage and current are constant. The dc-link inductor acts as an intermediate energy storage element in a current-source inverter. The inductor in the current-source inverter can be considered similar to a capacitor in a voltage-source inverter while choosing the size of the inductor. Increasing the size of the dc-link energy storage increases the cost, size and weight of the magnetics. The lower limit of the size of the magnetics is determined by the maximum allowable photovoltaic

current ripple such that the average photovoltaic output power reduction is limited to a reasonable amount.

The design of the input inductors for the current-source inverters has important trade-off with regard to the size. The larger the input inductors, the lower the current ripple and hence the photovoltaic average power loss. The input inductors in both the modules are identical. The average energy stored in the inductors is given by the following equation:

$$\boldsymbol{E_L = {}^{1}/_{2}\, L i_L{}^{2}} \qquad \textbf{(3.1)}$$

where i_L is the current through the input inductor.

Larger energy storage (lower current ripple) ensures lower average PV power loss. But larger the input inductor, the size and losses associated with the inductor also increases. Fig. 31 shows various values of input inductors as a function of input current ripple and size (number of windings for a given wire dimension). The optimum value of input inductor is chosen as 500 μH.

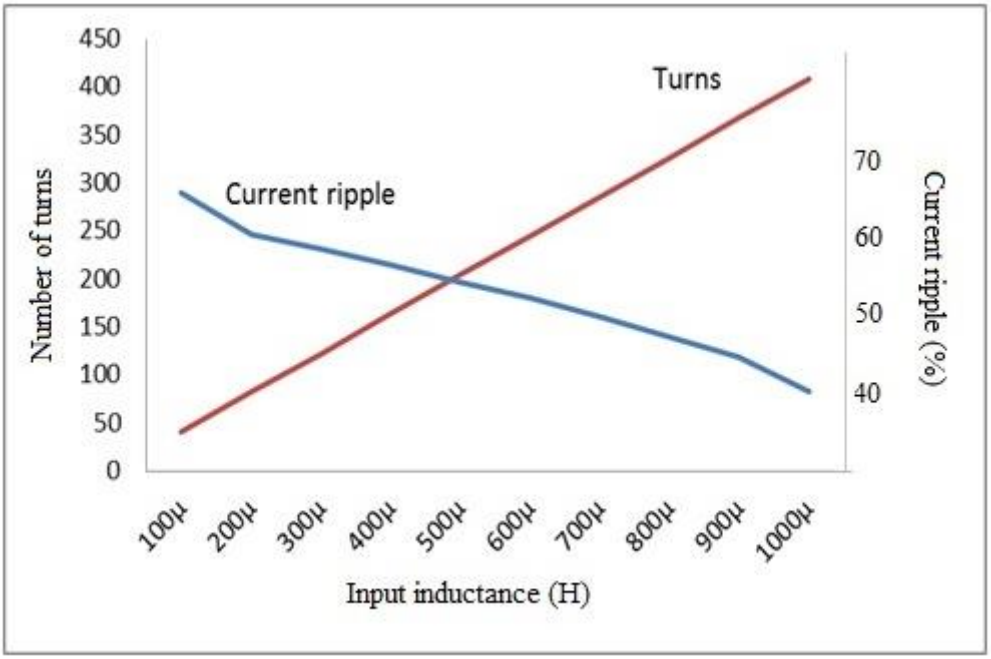

Fig. 31: Input inductor versus input current ripple versus number of turns in the input inductors (The part number of core used for calculation is STX1060M1 1033 C5).

3.2 <u>Primary-Side Switches</u>

The primary-side switches S_1, S_2, S_3 and S_4 of both the modules are operated in a sinusoidal manner with a duty ratio range of 50-100% having a constant dc offset. The duty ratios of the primary-side switches are given by the following equations:

$$\boldsymbol{d_1 = D + D'\sin(\omega t)} \tag{3.2}$$

$$\boldsymbol{d_2 = D - D'\sin(\omega t)} \tag{3.3}$$

where D is the constant dc offset in the duty ratios.

For the analysis, the dc offset D is fixed at 0.64 and the upper and lower limits of d_1 and d_2 vary between 0.5 and 0.78. The maximum voltage across the primary-side switches in both the modules is given by the following equations:

$$\boldsymbol{V_{sw1} = \frac{V_{o1}}{2n}} \tag{3.4}$$

$$\boldsymbol{V_{sw2} = \frac{V_{o2}}{2n}} \tag{3.5}$$

where, V_{o1} and V_{o2} are the output voltages at Module 1 and Module 2 respectively. The current through the primary-side switches in both the modules is given by the following the equations:

$$\boldsymbol{i_{s1} = \frac{i_{in}}{2} + i_{Ls1}} \tag{3.6}$$

$$\boldsymbol{i_{s2} = \frac{i_{in}}{2} + i_{Ls1}} \tag{3.7}$$

$$\boldsymbol{i_{s3} = \frac{i_{in}}{2} + i_{Ls2}} \tag{3.8}$$

$$\boldsymbol{i_{s4} = \frac{i_{in}}{2} + i_{Ls2}} \tag{3.9}$$

where i_{Ls1}, i_{Ls2} are the currents though the leakage inductances and i_{in} is the current input to the inverter. Fig. 32 shows the current through the primary-side switch during one switching cycle sunder hard-switching condition. The turn-on time of the switches during one switching cycle can be divided into three intervals for the ease of the analysis, namely T_I, T_{II} and T_{III}. Thus, the duty ratio, d_1 (or d_2) of the primary-side switches can be represented as the following equation:

$$T_{ON} = T_I + T_{II} + T_{III} \quad \textbf{(3.10)}$$

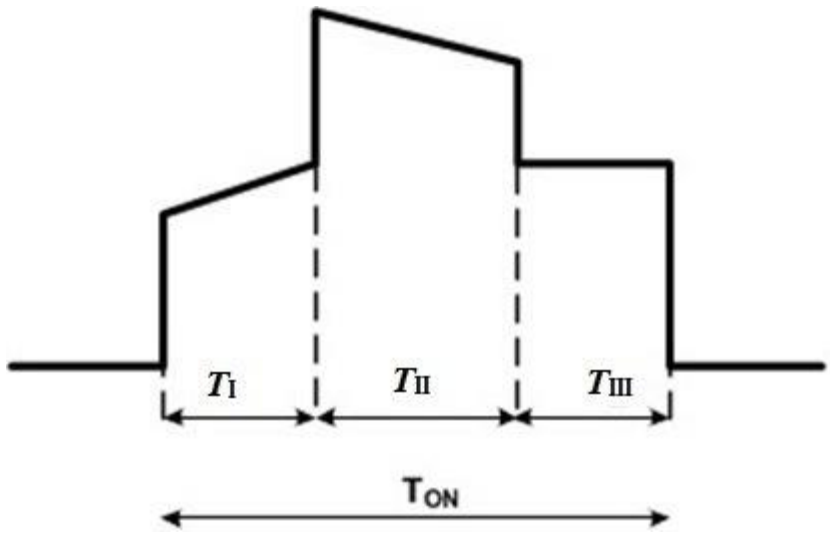

Fig. 32: Current through a primary-side switch.

The switches are modulated such that

$$(1 - T_{ON}) = T_{II} \quad \textbf{(3.11)}$$

Some important factors that govern the selection of a semiconductor device are the maximum voltage across the switch, the conduction and switching losses, and the switch capacitance. The conduction loss is the energy lost in the switch during the on-state and it depends on the voltage across the switch and the current through it. The power loss associated with a semiconductor device during conduction is given by the following equation:

$$\boldsymbol{P_{cond,loss} = \frac{1}{T_{SW}} \int_0^{T_{SW}} r_{on} i_{sw}(t)^2]\ dt} \tag{3.12}$$

$$\boldsymbol{P_{cond,loss} = r_{on} i_{sw,rms}^2} \tag{3.13}$$

where r_{on} is the on-state resistance of the switch, T_{SW} is the switching period, $i_{sw}(t)$ is the instantaneous value of the current through the switch and $i_{sw,rms}$ is the rms value of the current through the switch.

The RMS current of any one of the primary-side switches in Module 1 and Module 2 are derived as follows

$$I_{sw,rms,Primary} = \sqrt{\frac{1}{T_{sw}}[\int_0^{T_{ON}} (I_{sw})^2 dt + \int_{T_{ON}}^{T_{OFF}} (I_{sw})^2 dt]}$$

Between the time interval T_{ON} to T_{OFF}, the switch current is 0. The time interval between 0 to T_{ON} is divided into three intervals (equation 3.10). Between the time interval 0 and T_I, the current through the switch is half the input current to the particular module. The switch current between time interval T_I and T_{II} is $(\frac{i_{in1}}{2} + i_{LS1})$. The switch current between intervals T_{II} and T_{III} is half the input current to the particular module. Further,

$$d_I = \frac{T_I}{T_{sw}}$$

$$d_{II} = \frac{T_{II}}{T_{sw}}$$

$$d_{III} = \frac{T_{III}}{T_{sw}}$$

Substituting these; the rms switch current through each primary switch in each module is obtained as follows:

$$\boldsymbol{i_{sw,rms,Primary1}} = \sqrt{(\frac{\boldsymbol{i_{in1}}}{\boldsymbol{2}})^{\boldsymbol{2}}\boldsymbol{d_{III}} + \boldsymbol{i_{Ls1}}(\boldsymbol{i_{Ls1}} + \boldsymbol{i_{in1}})[\boldsymbol{d_{II}} - \boldsymbol{d_{I}}]} \quad \textbf{(3.14)}$$

$$\boldsymbol{i_{sw,rms,Primary2}} = \sqrt{(\frac{\boldsymbol{i_{in2}}}{\boldsymbol{2}})^{\boldsymbol{2}}\boldsymbol{d_{III}} + \boldsymbol{i_{Ls2}}(\boldsymbol{i_{Ls2}} + \boldsymbol{i_{in2}})[\boldsymbol{d_{II}} - \boldsymbol{d_{I}}]} \quad \textbf{(3.15)}$$

where, $i_{\boldsymbol{sw},rms,Primary1}$ is the rms switch current through each primary-side switch in Module 1, $i_{Ls\boldsymbol{1}}$ is the current through the leakage inductance of the transformer in Module 1, $i_{\boldsymbol{sw},rms,Primary2}$ is the rms switch current through each primary-side switch in Module 2 and i_{Ls2} is the current through the leakage inductance of the transformer in Module 2.

The chosen switch is IPP200N25N3 G, with an on-state resistance of 20 mΩ, maximum continuous drain current (I_D) of 64 A and drain-source breakdown voltage (V_{DS}) of 250 V. Table 2 shows the theoretical and simulated conduction loss for the primary switches. Fig. 33 shows the conduction loss in all the primary-side switches for both modules for a single IXTP50N25T switch, single IPP200N25N3 G and four IPP200N25N3 G switches in parallel. The switch number IXTP50N25T has a 50 mΩ on-state resistance while the chosen switch IPP200N25N3 G has a 20 mΩ on-state resistance.

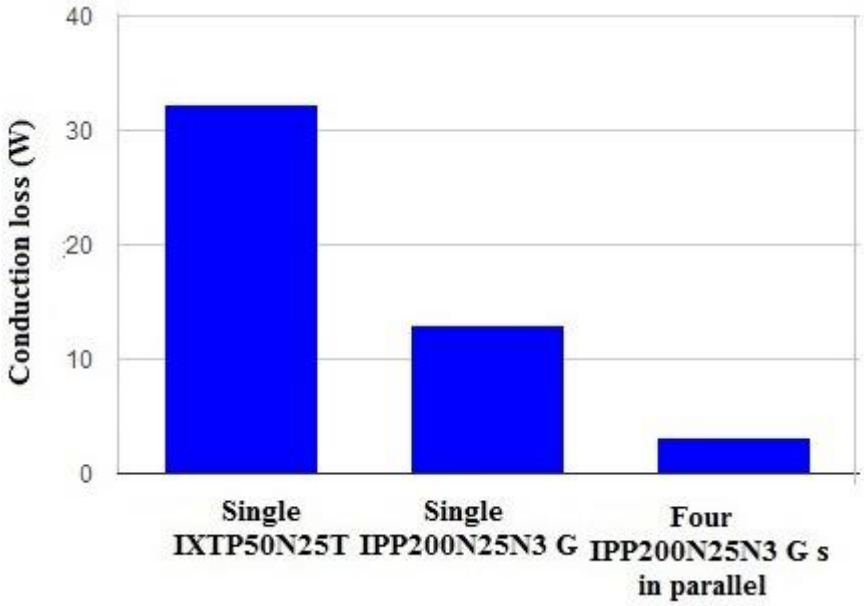

Fig. 33: Conduction loss in the primary-side switches (For a 500 W load and a dc offset in duty ratio of 0.64- Appendix).

Table 2: Theoretical and simulated values of the conduction losses in the primary-side switches (Theoretical projections are obtained using equations 3.14 and 3.15 and simulated losses are calculated for a 500 W inverter with a 0.64 constant dc off set in duty ratio using SABER-Appendix 1 and 2)

R_{DSON} in Ohms	**Theoretical projection of conduction loss per primary switch in Watts**	**Simulated conduction loss per primary switch in Watts**
Single 0.02Ω switch	11.493	12.67
Four 0.02 Ω switches in parallel	2.88	3.17

3.3 Leakage Inductance

When both the primary-side switches in a module are on, the current through the transformer (or leakage inductance) is zero. For all other cases, the current through the leakage inductance is given by the following equations:

$$\boldsymbol{i_{Ls1} = \frac{V_o}{2nL_{s1}}(\Delta t)} \tag{3.16}$$

$$\boldsymbol{i_{Ls2} = \frac{V_o}{2nL_{s2}}(\Delta t)} \tag{3.17}$$

where, L_{S1} and L_{S2} are the leakage inductance of Module 1 and Module 2 respectively and n is the transformers' turns ratio.

The leakage inductance of the transformer must be designed to divert the current through one of the primary-side switches within the additional ZCS duty ratio (d_r) of the secondary-side switches. The lower limit of the leakage inductance is primarily influenced by the ZCS duty ratio and the load. The difference in the energies between the input inductors and the leakage inductance restricts the use of a higher value of leakage inductance. The leakage inductance of individual modules is given by the following equation:

$$\boldsymbol{L_s = \frac{V_o d_r}{n i_{in1} f_s}} \tag{3.18}$$

where, n is the transformer turns ratio, i_{in1} (i_{in2}) is the input current through Module 1 (Module 2), f_s is the switching frequency of the inverter, V_o is the output voltage and d_r is the soft-switching duty ratio. From the above equation, it can be seen that the leakage inductance affects the soft-switching duty ratio (d_r) and Fig. 34 shows the leakage inductance as a function of the soft-switching range. A leakage inductance of 1 μH is chosen for the analysis of the inverter.

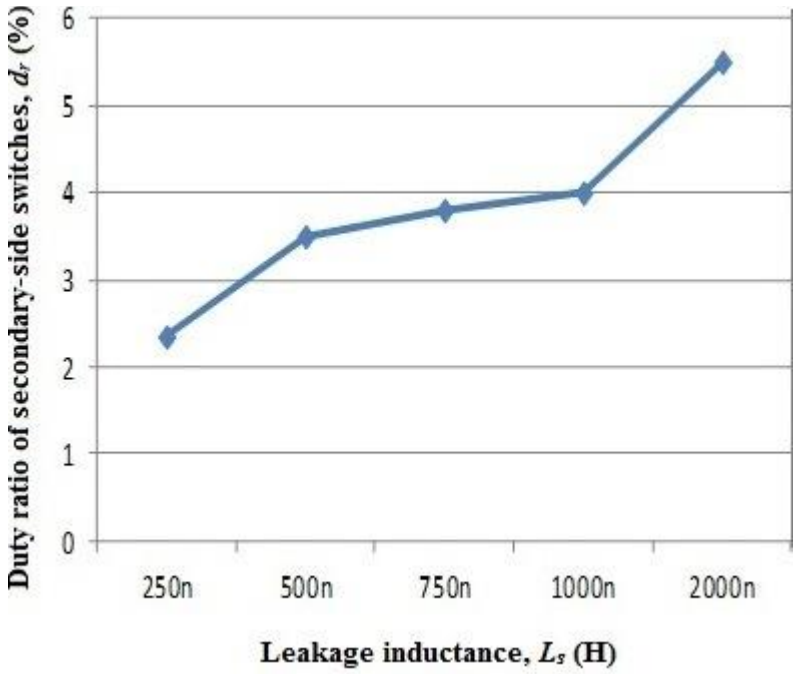

Fig. 34: Duty ratio of secondary-side switches, d_r in percentage as a function of leakage inductance, L_S in Henry (For a 500 W load, Appendix: soft-switching topology).

3.4 Transformer

Apart from providing a galvanic isolation to the source from the load, the transformer also affects two aspects of the inverter. The transformer's turns ratio influences the conduction losses in the switches and the THD of the output. A higher turns ratio in the transformer reduces the voltage across the switches on the primary side, thereby eliminating the need for higher voltage switches. This reduces the on-state resistance of the primary-side switches, thereby bringing down the conduction losses on the primary-side, where the switches are turned on for a longer duration when compared to those at the secondary-side. On the contrary higher turns ratio results in higher switch current and also increased THD at the load, apart

from increasing the size of the magnetics and the transformer losses. One of the major advantages of this topology is that the transformer sees a bipolar voltage and current whose average is zero, thereby reducing the size of the transformer. Fig. 36 shows the conduction losses in primary-side switches as a function of transformer turns ratio. As the turns ratio increases the loss in the device also increase. From Figs. 35 and 36, an optimum value of *n* is found to be 2.

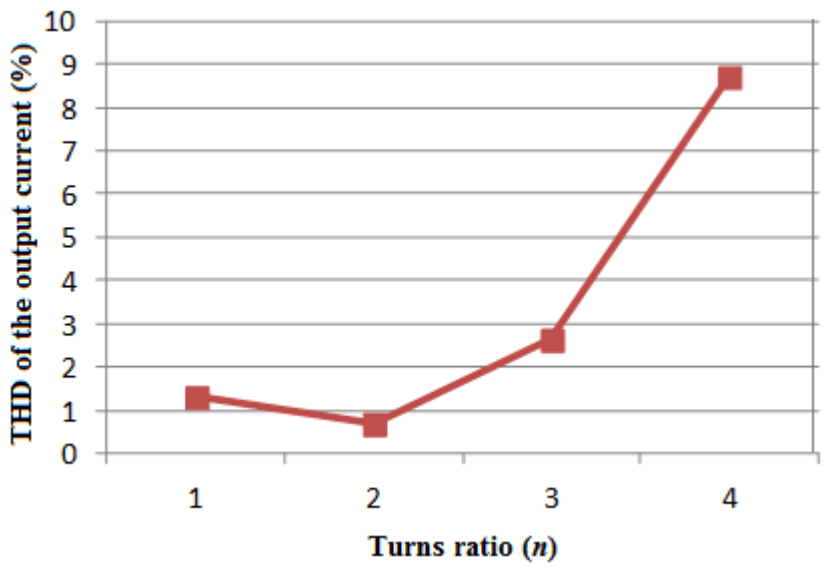

Fig. 35: THD of the output current in percentage versus transformer turns ratio, *n* (For a 500 W load).

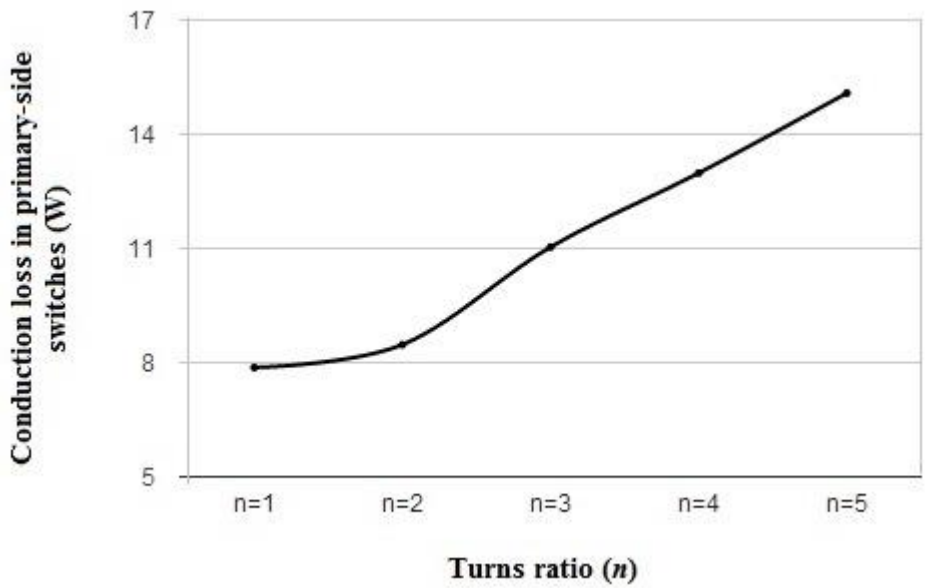

Fig. 36: Conduction losses in a single primary-side switch as a function of the transformer turns-ratio for a 500 W load under soft-switching conditions. (Each switch is a single chosen switch having an on-state resistance of 0.02 Ohms).

3.5 Secondary-Side Switches

The secondary-side switches are operated complementarily to the primary-side switches. When the modules are operated as dc/dc converters, the secondary switches are only turned on during the turn off of the primary-side switches (to aid the ZCS of the primary-side switches), whereas in the inverter operation there is considerable conduction loss in the secondary-side switches, since they are turned on for a longer duration. Maximum voltage across the secondary-side switches is V_o. Fig. 37 shows the current through a secondary-side switch during one switching cycle under hard-switched condition. The RMS current of any one of the secondary-side switches in Module 1 and Module 2 are derived as follows

$$I_{sw,rms,Secondary} = \sqrt{\frac{1}{T_{sw}}\left[\int_0^{T_{ON}} (I_{sw})^2 dt + \int_{T_{ON}}^{T_{OFF}} (I_{sw})^2 dt\right]}$$

Between the time interval T_{ON} to T_{OFF}, the switch current is 0. Between the time interval 0 and T_{ON}, the current through the switch is $\frac{i_{LS}}{n}$. Further,

$$T_{ON,sec} = 1 - T_{ON,pri}$$

where, $T_{ON,pri}$ is the time for which any primary-side switch is turned on and $T_{ON,sec}$ is the time for which it's complimentary switch is turned on. Solving further, the RMS current through any secondary-side switch is obtained as follows:

$$\boldsymbol{i_{rms,Secondary} = \sqrt{(\frac{i_{Ls}}{n})^2[1 - d_1]}} \qquad \textbf{(3.19)}$$

where, i_{Ls} is the current through the leakage inductance of the transformer in any module and d_1 (or d_2) is the duty ratio of the Module 1 (or Module 2).

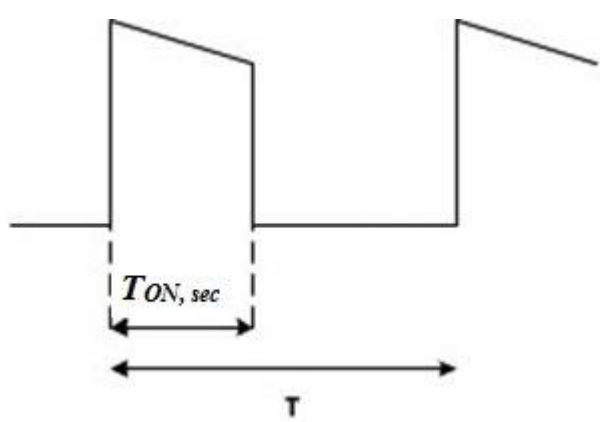

Fig. 37: Current through a secondary-side switch during one switching cycle.

The chosen switch is STY60NM50, with an on-state resistance of 45 mΩ and drain-source breakdown voltage (V_{DS}) of 500 V. Table 3 shows the theoretical and simulated conduction loss for the secondary-side switches. Fig. 38 shows the conduction loss in all the secondary-side

switches for both modules for a switch (IXFB100N50P) with on-state resistance 50 mΩ, single STY60NM50 switch and two STY60NM50 switches in parallel.

Table 3 Theoretical and simulated values of the conduction losses in the secondary-side switches (Theoretical projections are obtained using equation 3.19 and simulated losses are calculated for a 500 W inverter with a 0.64 constant dc off set in duty ratio using SABER- Appendix).

R_{DSON} in Ohms	**Theoretical projection of conduction loss per secondary-side switch in Watts**	**Simulated conduction loss per secondary-side switch in Watts**
Single 0.045Ω switch	2.12	2.6
Two switches in parallel	1.06	1.3

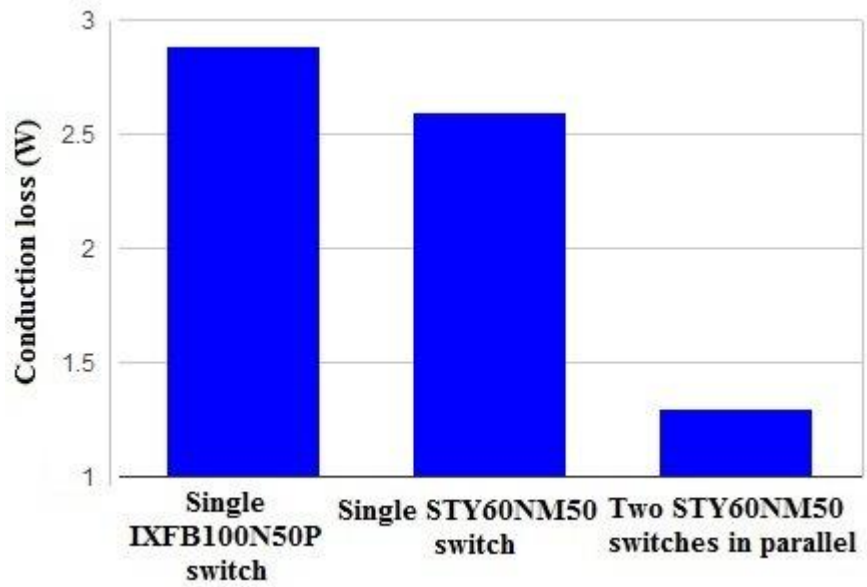

Fig. 38: Conduction loss in the secondary-side switches (For a 500 W load and a dc offset in duty ratio of 0.64- Appendix).

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3.6 Output Capacitors

The voltage across the output capacitances is given by the following equations:

$$V_{Co1} = V_{Co2} = \frac{V_{o1}}{2} \tag{3.20}$$

$$V_{Co3} = V_{Co4} = \frac{V_{o2}}{2} \tag{3.21}$$

where V_{o1} and V_{o2} are the output voltages of the individual modules. Output capacitors are chosen to balance the Total Harmonic Distortion (THD) of the load current as well as aid the control strategy by not forming a low impedance path for the high-frequency components. A larger capacitor mitigates higher-order harmonics at the output. But, a very large output

capacitor provides a low impedance path for the fundamental frequency component. For a 500-W load, Table 4 shows the impedances offered by different values of capacitors in open loop for various orders of harmonics. X_c represents the impedance offered by the output capacitor and *n* represents the fundamental-frequency, 60 Hz. Fig. 39 shows the rms output voltage of the inverter as a function of the output capacitor.

Table 4: Impedances offered by different values of capacitors, for various orders of harmonics of the inverter for a 500 W load (Appendix).

C_o in μF	**X_c at *n* (Ω)**	**X_c at 3*n* (Ω)**	**X_c at 5*n* (Ω)**	**X_c at 7*n* (Ω)**
10	265.2	88.4	53.1	37.9
25	106.1	35.6	21	15.2
50	53	17.7	10.6	7.6
100	26.5	8.8	5.3	3.7

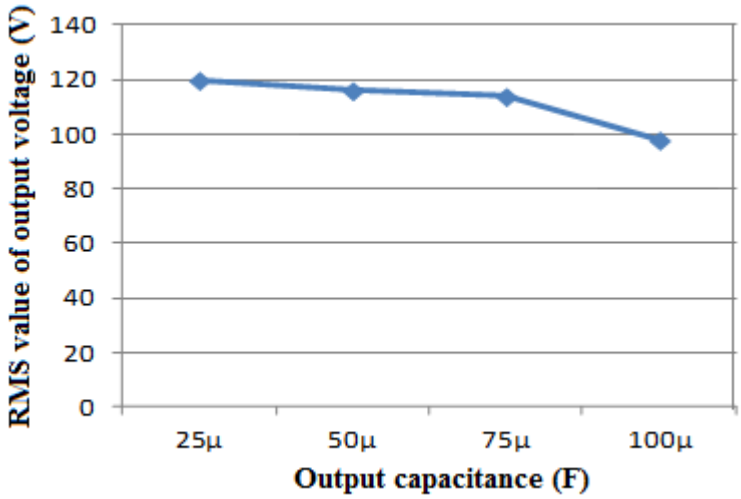

Fig. 39: Output voltage versus output capacitance of the inverter for a 500 W load (Appendix).

3.7 Switching Losses

Switching losses refer to the energy losses that occur during the switching transient as the conducting semiconductor device is changed from on to off state or vice versa. These losses depend on the voltage across the switch during the switching transient, the current through the switch during the transient and the time taken to move from one state to another (or the switching time). The energy associated with the turning on of a switch is given by the following equation:

$$\boldsymbol{E_{on} = \int_{0}^{T_{ri}+T_{fv}} V_{DS}(t) i_D(t) dt} \qquad \textbf{(3.22)}$$

where $V_{DS}(t)$ is the instantaneous value of the drain-source voltage of the switch, $i_D(t)$ is the drain current of the switch, T_{ri} is the time taken for the current to rise from zero to i_D and T_{fv} is

the time taken for the voltage to drop from V_{DS} to zero. The energy associated with the turning off of a switch is given by the following equation:

$$\boldsymbol{E_{off}} = \int_{0}^{T_{rv}+T_{fi}} \boldsymbol{V_{DS}(t) i_D(t) dt} \tag{3.23}$$

where T_{rv} is the time taken for the voltage to rise from zero to V_{DS} and T_{fi} is the time taken for the current to drop from I_D to zero. The power loss during the switching of the devices is given by the following equation:

$$\boldsymbol{P_{sw} = (E_{on} + E_{off}) f_s} \tag{3.24}$$

Where, f_s is the switching frequency of the inverter. Fig. 44 shows the estimated switching losses in all the primary-side switches and the secondary-side devices in both the modules.

3.8 <u>Control Strategy</u>

The THD in the load current exceeds the acceptable limit of 5% when the switches are modulated by sinusoidal Pulse Width Modulation (PWM). To reduce the THD of the load current, a harmonic compensation control is implemented using a Proportional Resonant (PR) controller. The traditional Proportional-Integral (PI) controllers are simple to implement and have a robust performance, but they provide infinite gain only at zero frequencies and limited gain at higher frequencies. This makes the tracking of a sinusoidal reference unsatisfactory. The synchronous-frame controllers, on the other hand, are complex and require transformation from stationary frame AC quantity to rotating frame DC quantities and then design the control strategy. The control strategy, thus developed has to be transformed back into the stationary-frame for implementation. This can increase inaccuracies due to multiple transformations, which are

difficult to apply for single-phase systems. On the contrary, PR controllers provide infinite gain in a narrow bandwidth that is centered at the resonance frequency, thereby eliminating the steady-state error at that particular frequency. The PR controller with harmonic compensators implements infinite gain at the desired frequencies for various orders of harmonics to reduce the harmonic distortions in the voltage or current signals. It is advantageous over the traditional PI controller in regulating sinusoidal signals because of the following reasons:

- It removes steady-state error in the single-phase systems in case of sinusoidal reference signals.
- It reduces the need for a coupling or a feed forward block.
- It yields an easier tuning of the system.
- It has a better rejection capability.

Thus, a PR controller that introduces a higher gain at a selected resonant frequency is implemented to eliminate the higher order harmonics and the steady-state error at that frequency. The PR controller is represented as

$$\boldsymbol{G(s) = K_p + \frac{k_o s}{[s^2 + (n^2\omega^2)]}} \qquad \textbf{(3.25)}$$

where ω represents the line or fundamental (n=1) frequency and n (=3, 5,..) represents the higher-order harmonics. ω is given by the following equation:

$$\omega = 2\pi n * 60$$

For n = 1, the feedback voltage is compared with a reference 60-Hz sinusoidal voltage and the error is passed through a PR controller, which is tuned at the line frequency. The current command of this voltage loop is compared with a differential-current feedback and passed through a PR controller which is tuned at the fundamental frequency. The differential current is synthesized by taking the difference of the input currents (i_{in1} and i_{n2}) of Modules 1 and 2. To

mitigate the higher-order (odd) harmonics (i.e., n = 3, 5,..), separate control loops are implemented that emulate the structure of the fundamental-frequency control loop. However, for the harmonics compensation, the voltage reference is set to 0 and the PR controller is tuned at a frequency that matches the harmonic frequency. The perturbation outputs of the fundamental and high-order harmonic controllers are added to a dc offset such that the duty cycle of the (primary-side) inverter switches do not fall below 0.5. This duty-cycle signal and a 180º phase-shifted signal of the same are then used to generate the pulse trains for the switches S_1 and S_2 and S_3 and S_4, respectively. The signals for the secondary-side switches S_{r1} and S_{r2} are generated by complementing the binary switching signals of primary-side switches S_1 and S_2 respectively, and then adding to the pulse train information (d_r) for achieving soft-switching. . The signals for the secondary-side switches S_{r3} and S_{r4} are generated by complementing the binary switching signals of primary-side switches S_3 and S_4 respectively, and then adding to the pulse train information (d_r) for achieving soft-switching. Fig. 40 represents the implementation of this control strategy.

The above explained control scheme has lower transient response and is tedious to implement due to the presence of multiple voltage and current loops. Thus, the differential-current feedback is compared with zero current reference for higher-order harmonics directly eliminating the need for multiple PR blocks for higher-order harmonics. Fig. 41 represents the implementation of this scheme. The control scheme is implemented without and with the proportional gain for the inner loop of the fundamental frequency. A proportional gain may be added to the resonant compensator to increase the response of the system. But this introduces a steady-state error in the system due to increased k_p. The transfer function of a PR compensator is given by the following relation:

$$G(s) = k_p + \frac{k_o s}{[s^2 + (n^2\omega^2)]}$$

where k_p is the proportional gain. As k_p increases, the THD of the load current increases above 5% for lower turns ratio of the transformer.

Alternatively, the differential-current feedback can also be compared with the current command of the voltage loop of the fundamental frequency, which is given in Fig. 42. This strategy is effective for higher turns-ratio of the transformer.

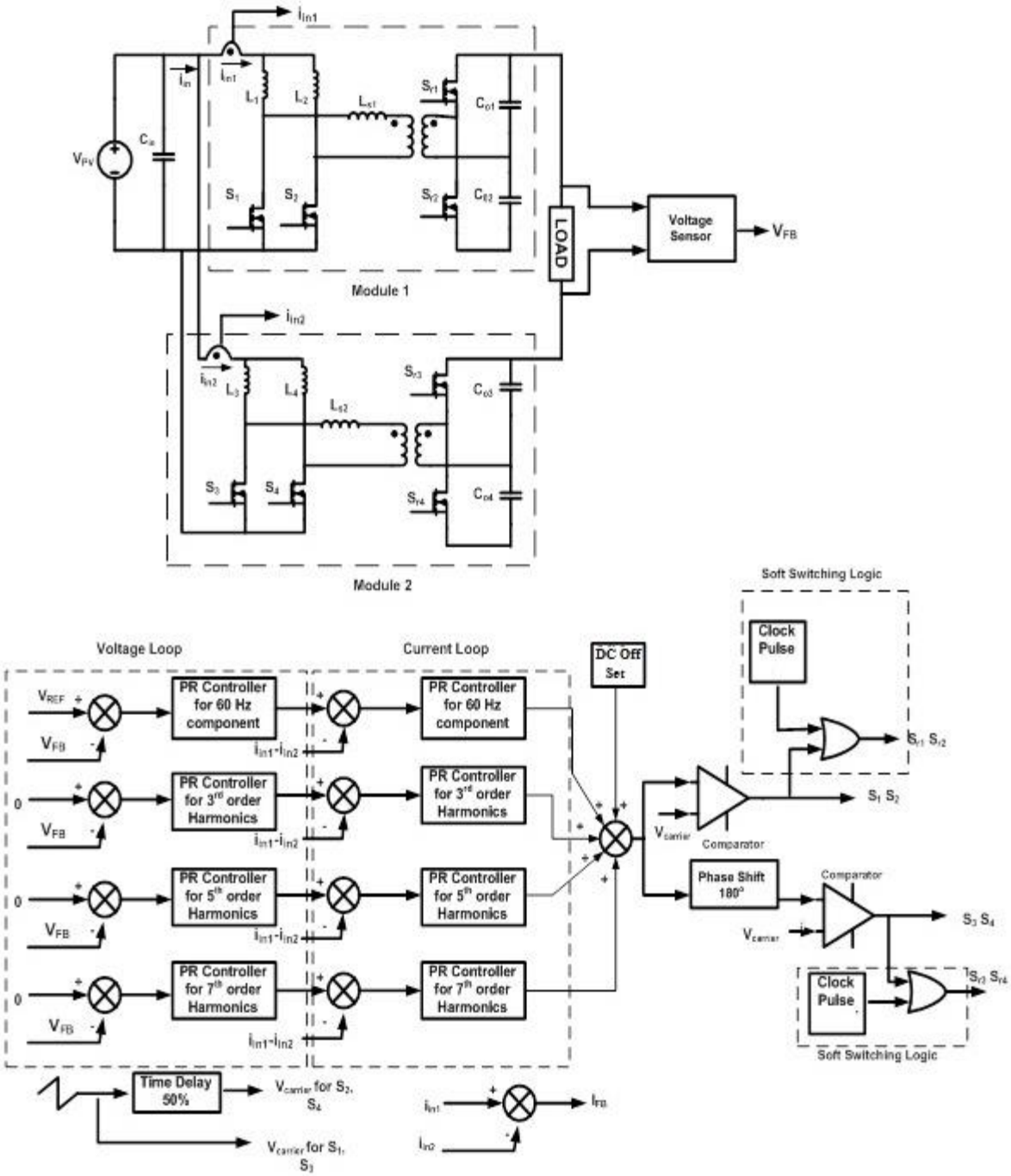

Fig. 40: Implementation of the control strategy-1.

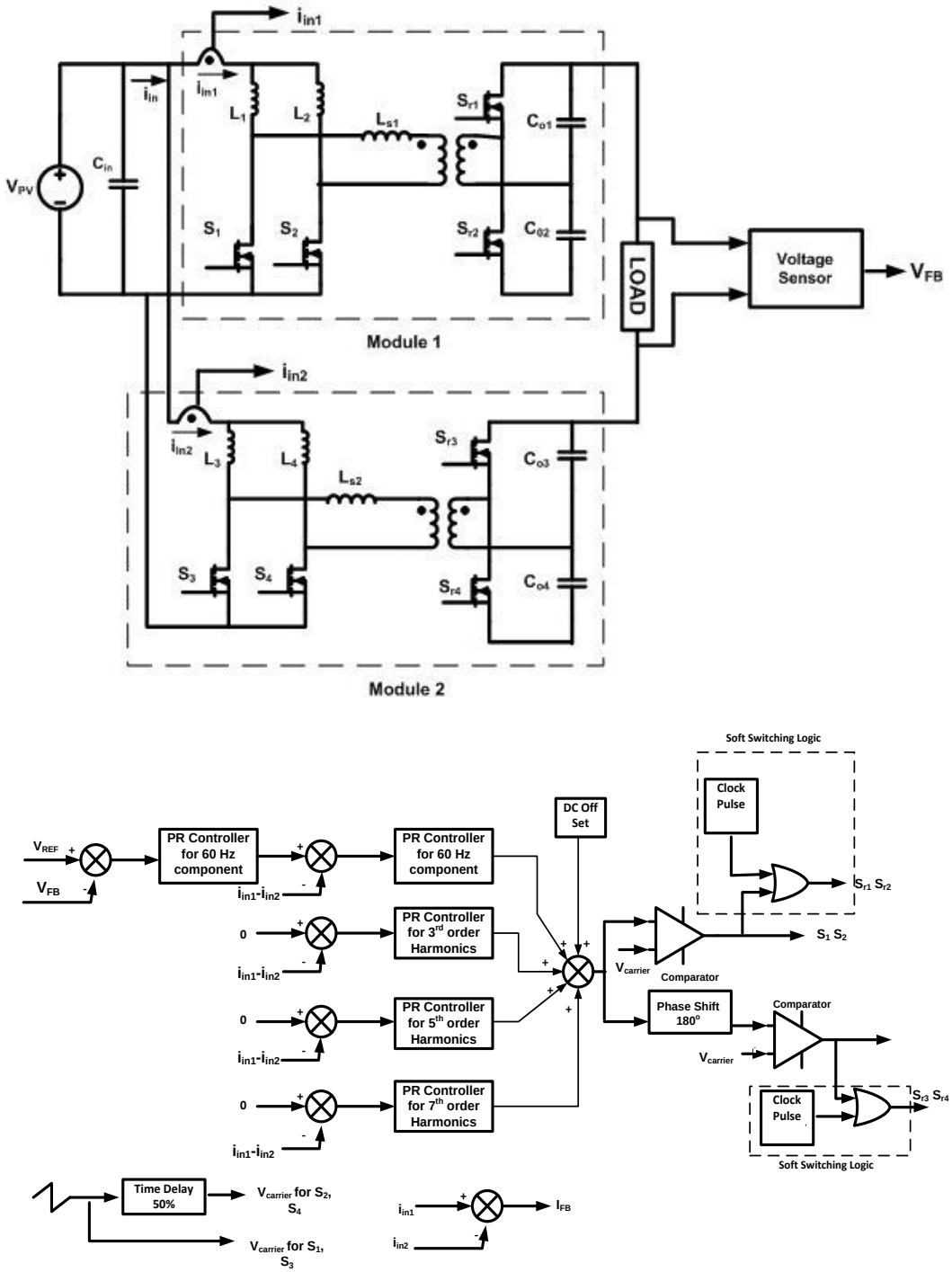

Fig. 41: Implementation of the revised control strategy-2.

Table 5: The number of turns for all the chosen values of the magnetic components of the inverter (The part number of core used for calculation is STX1060M1 1033 C5. For number of turns calculation, refer to Appendix).

COMPONENT	DIAMETER OF WIRE (mm)	NUMBER OF TURNS
Input inductors	0.9	204
Transformer primary	0.5	110
Transformer secondary	0.7	219

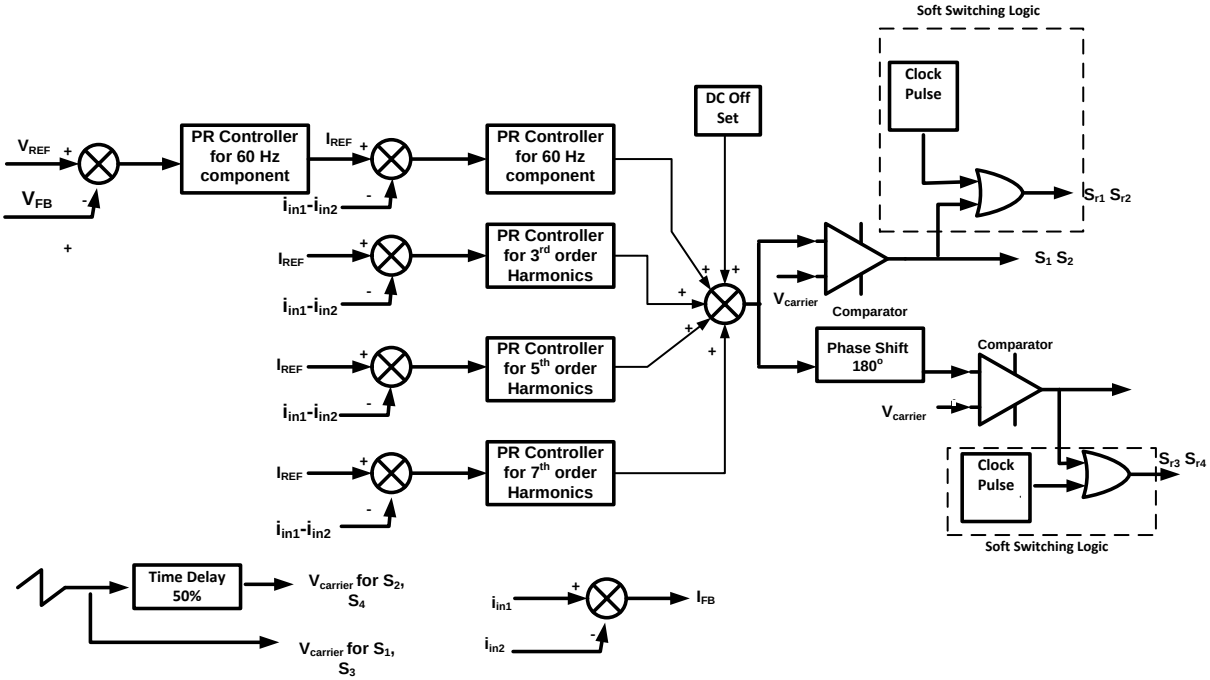

Fig. 42: Schematic of alternative control strategy-3.

Fig. 43 shows the total conduction losses in all the semiconductor devices in the inverter while Fig. 44 shows the switching losses in the switches in the inverter. Fig. 45 represents the soft-switching duty-ratio as a function of load in Watts. Fig. 46 shows the THD of the load current as a function of the output capacitor under closed-loop conditions. Figs. 47 and 48 indicate the THD of the load current as a function of transformer turns-ratio for closed-loop control strategy 2 and 3 respectively. When control strategy-3 is used, that is; when the current command of the voltage loop of the fundamental frequency is used as a reference for the differential current feedback, the THD for higher turns ratio (n=4) is lower than the THD for lower turns ratio. Whereas, for control strategy-2, lower THD can be attained even with lower turns ratio of transformer (n=2), since the inner loop uses a zero reference to drive the differential input current for higher-order harmonics to zero. Thus control strategy-2 is chosen over the strategy-3. As stated, higher the turns ratio, lower the THD of the load current.

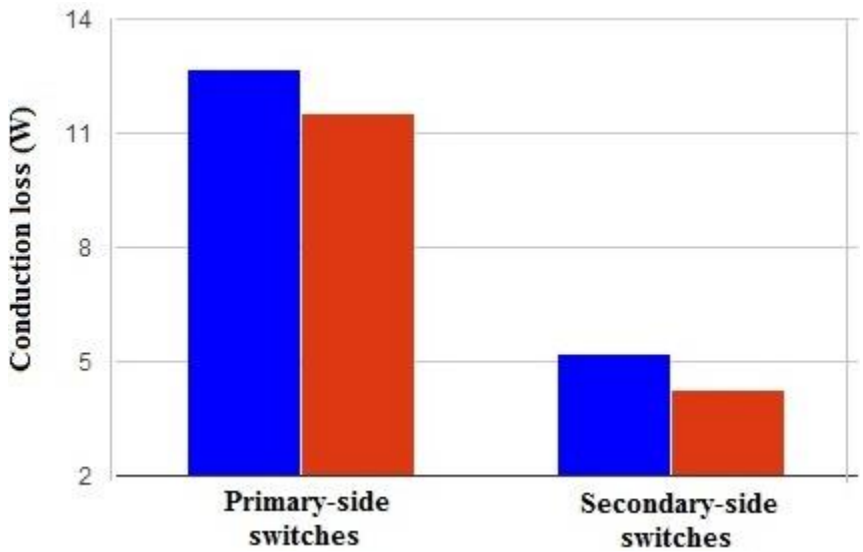

Fig. 43: Conduction loss in all of the switches (simulated and projected values) (For a 500 W load and a dc offset in duty ratio of 0.64). Projected values were calculated using equations 3.14, 3.15 and 3.19. The chosen primary-side switch is IPP200N25N3 G and the chosen secondary-side switch is STY60NM50. The simulated values were generated for a 500 W inverter using SABER (refer Appendix)

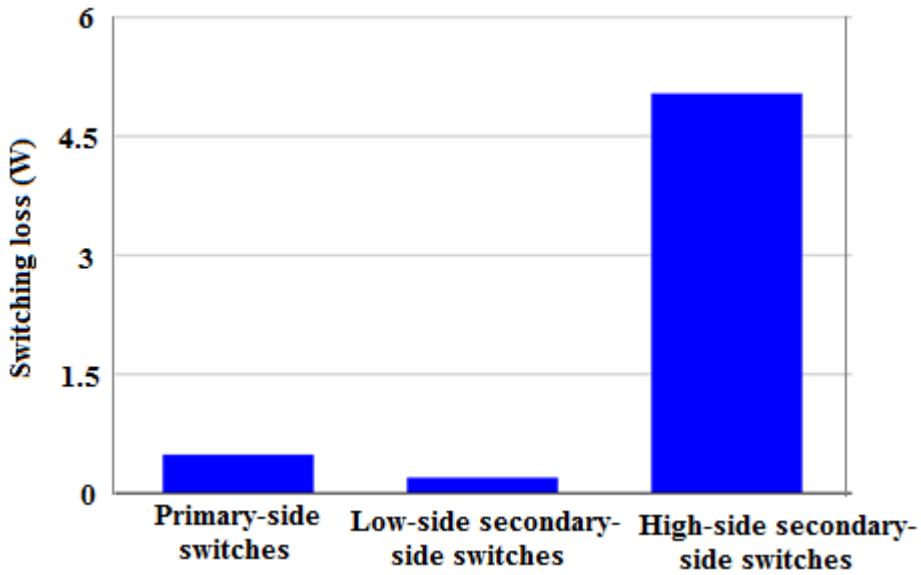

Fig. 44: Estimated switching losses for a switching frequency of 100 kHz (For a 500 W load and a dc offset in duty ratio of 0.64). Projected values were calculated using equations 3.14, 3.15 and 3.19. The chosen primary-side switch is IPP200N25N3 G and the chosen secondary-side switch is STY60NM50. The simulated values were generated for a 500 W inverter using SABER (refer Appendix).

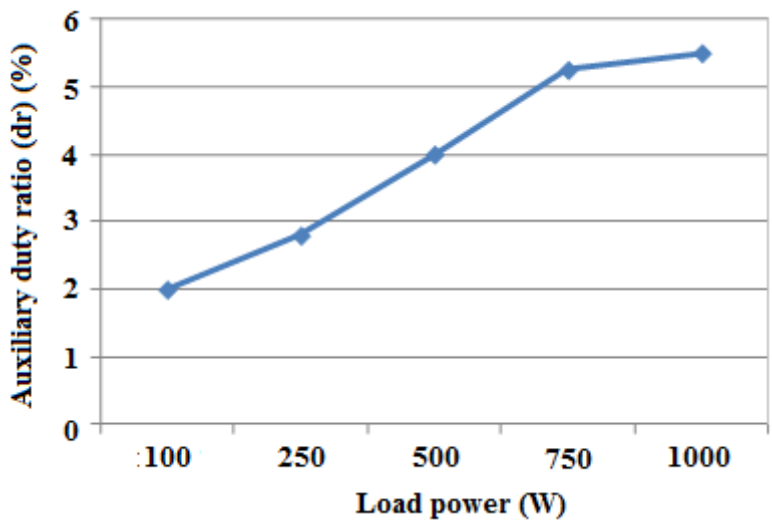

Fig. 45: Auxiliary duty ratio (d_r) in percentage versus Load power in Watts (Simulations performed using Saber- Appendix). The auxiliary duty ratio for each load power is fixed by the maximum time required for a primary-side switch's current to fall below zero. For a 500 W load, Module 1 requires 5% auxiliary duty ratio during the maximum point of the positive load current and does not require any auxiliary duty ratio for minimum point of the negative load current, whereas, Module 2 requires 5% auxiliary duty ratio during the maximum point of the negative load current and does not require any auxiliary duty ratio for minimum point of the positive load current.

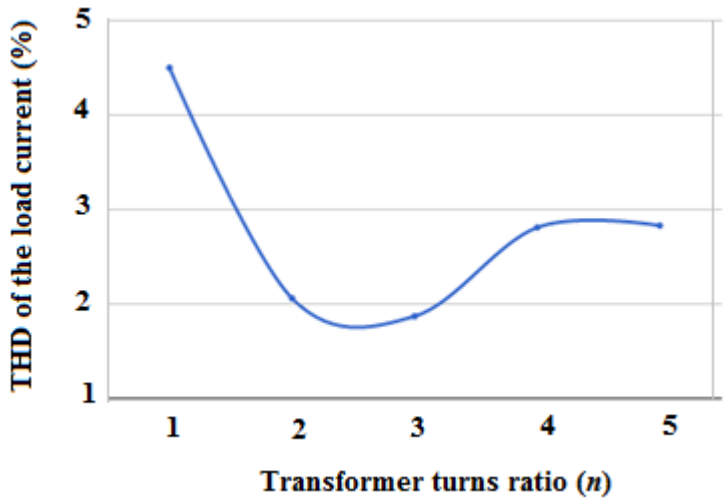

Fig. 46: THD of the load current versus transformer turns ratio for a fixed value of k_p (for control strategy -2: with a reference of zero for the current loop).

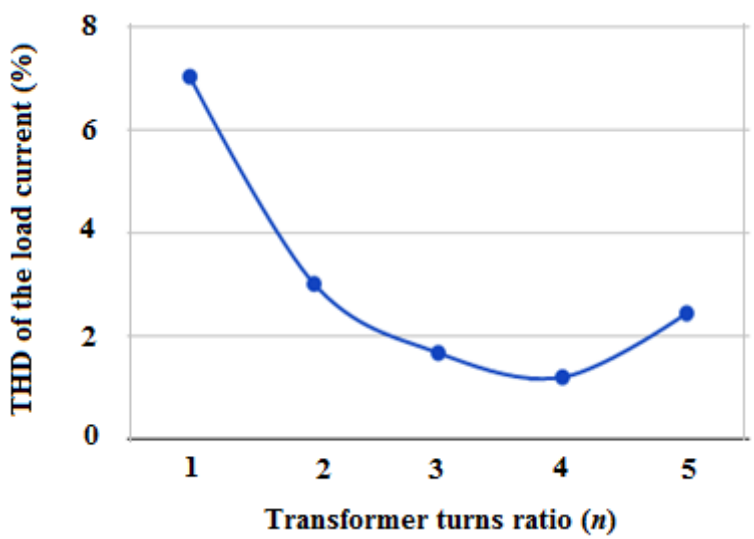

Fig. 47: THD of the load current versus transformer turns ratio (for control strategy-3).

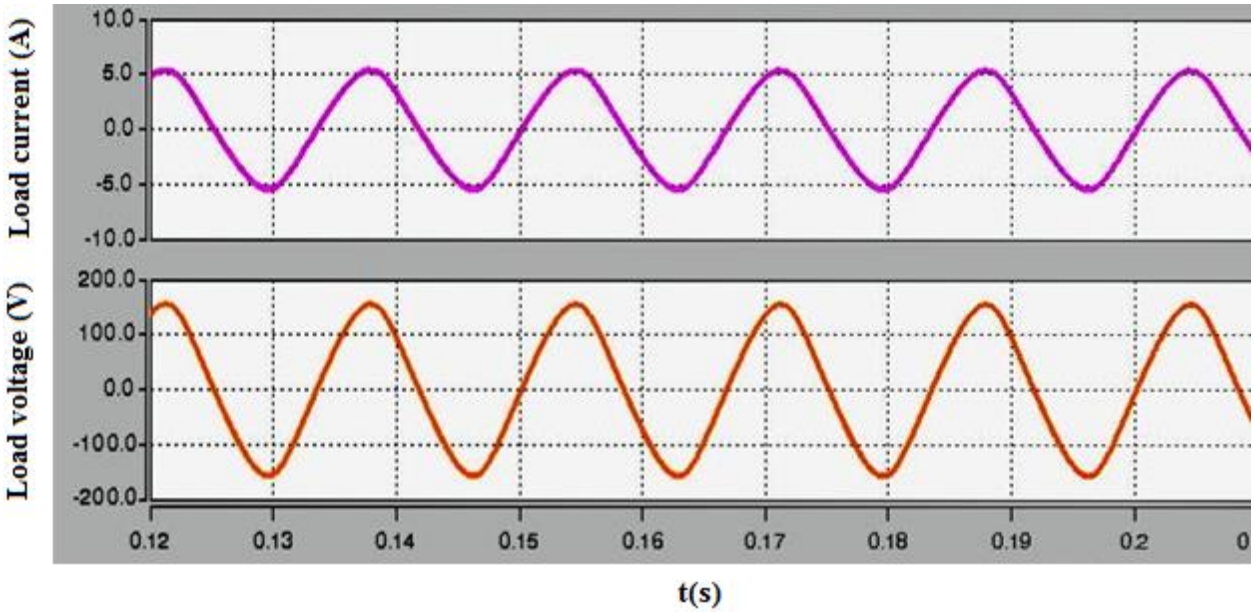

Fig. 48: Output current and voltage of the inverter under hard-switched condition.

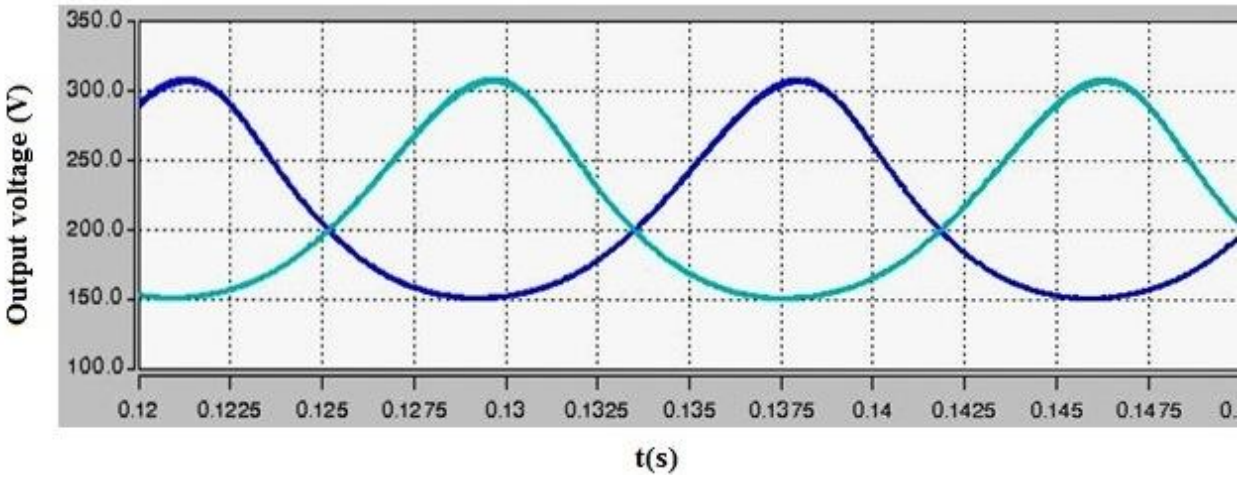

Fig. 49: Output voltage of the individual modules under hard-switched condition.

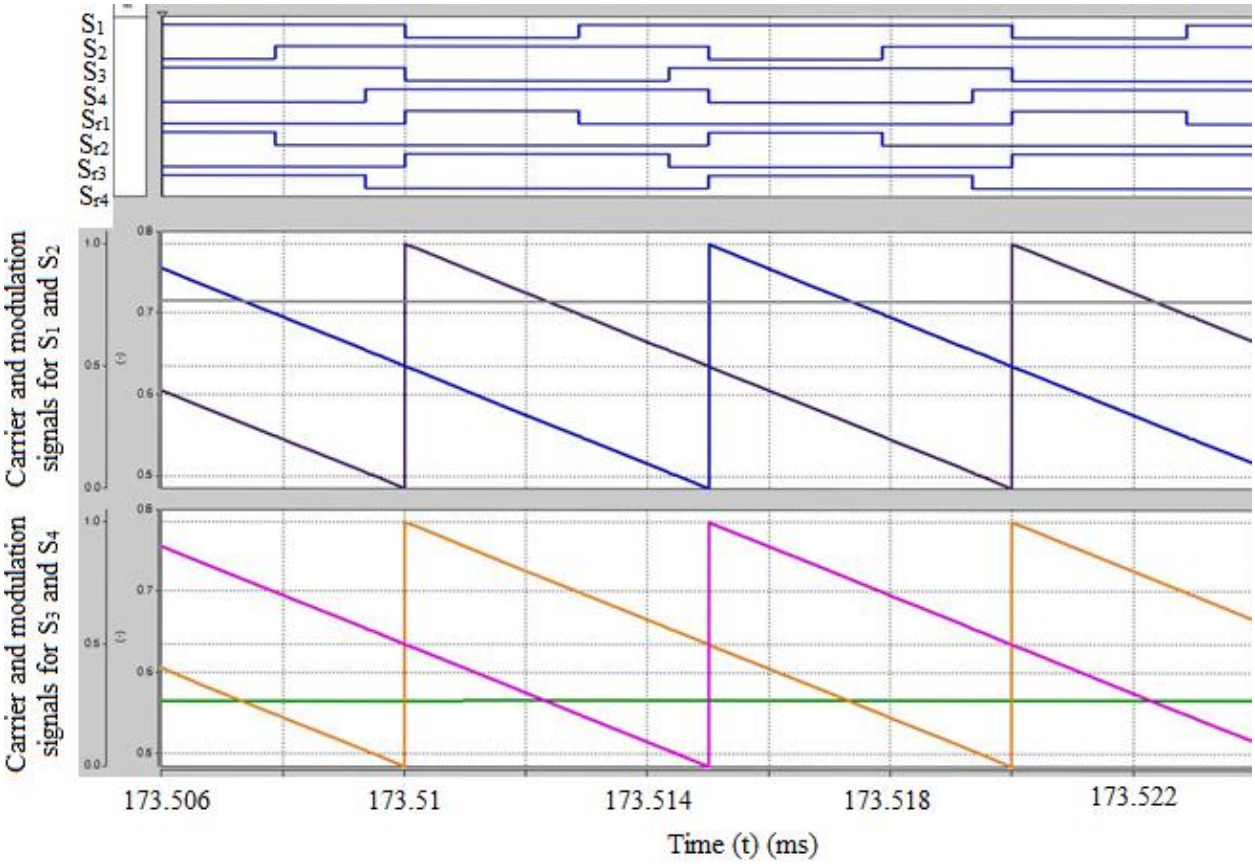

Fig. 50: (Top 4 traces): Gating signals for switches S_1, S_2, S_3, and S_4. (Next 4 traces): Gating signals for switches S_{r1}, S_{r2}, S_{r3}, S_{r4} signals. (Second trace from bottom): Phase–shifted carrier and modulation signals that generate gating pulses for switches S_1 and S_2. (Bottom trace) Phase–shifted carrier and modulation signals that generate gating pulses for switches S_3 and S_4 signals-under hard-switched conditions.

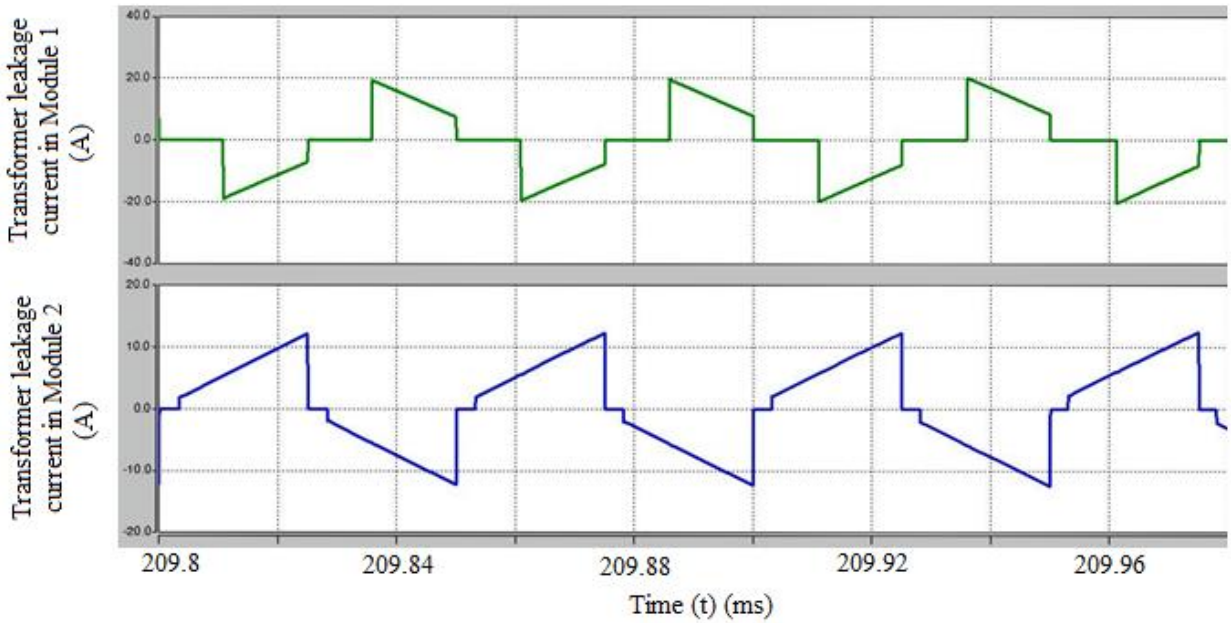

Fig. 51: Currents through the leakage inductance of the transformers of both the modules under hard-switching condition.

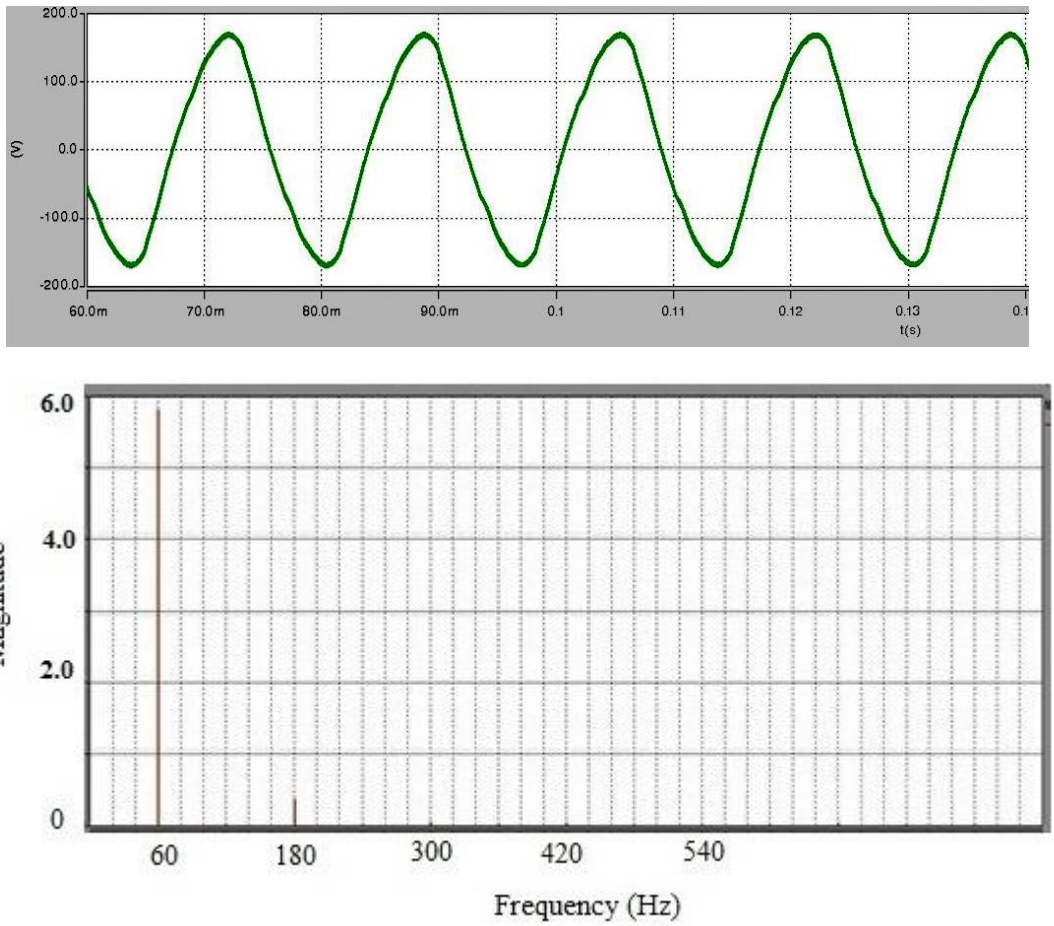

Fig. 52: Output voltage (above) and FFT of load current (below) of the inverter operating in open loop condition under soft-switched conditions.

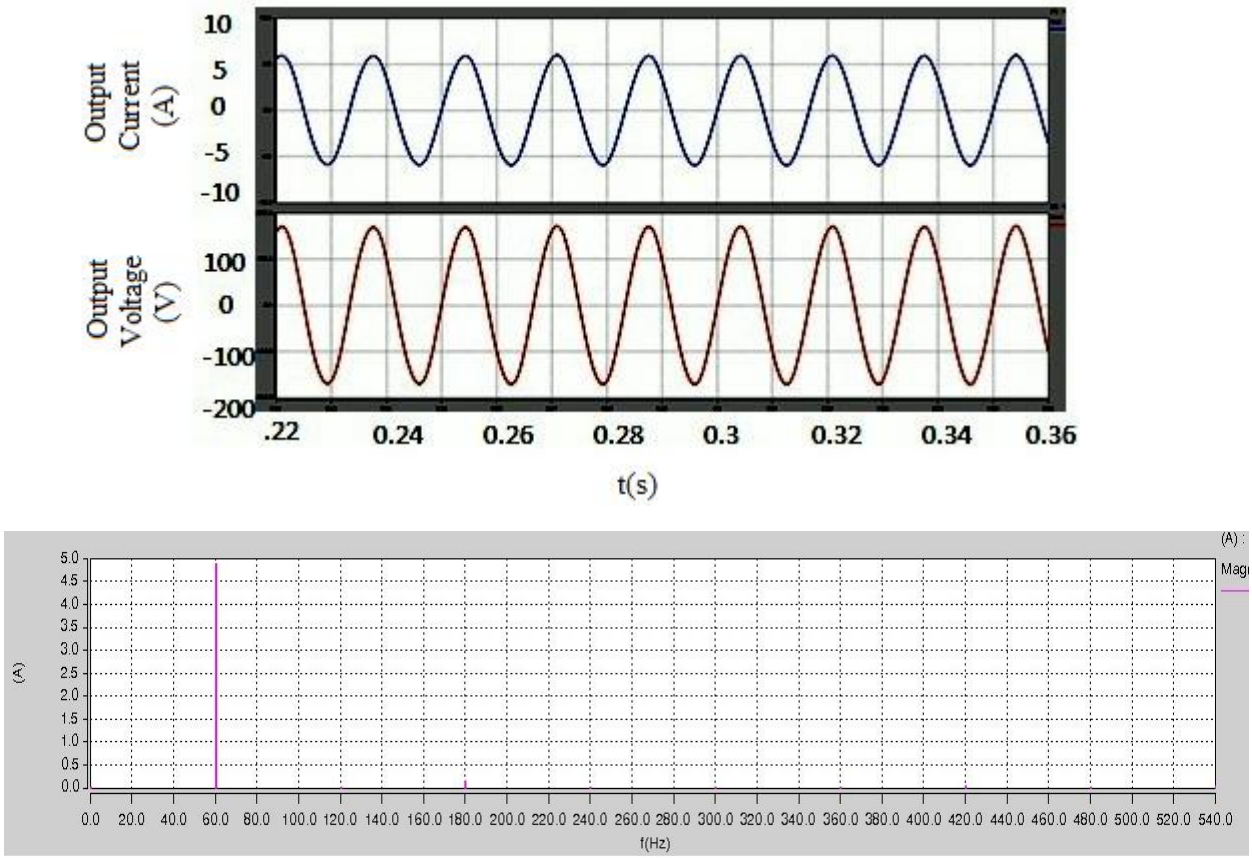

Fig. 53: Output voltage (below), load current (middle) and THD of the load current (below) of the inverter under soft-switched conditions in closed-loop operation.

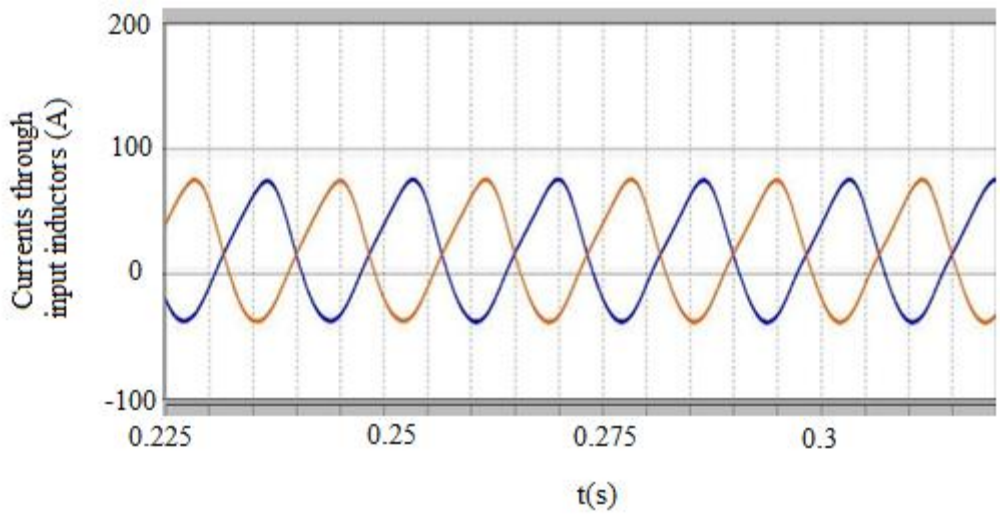

Fig. 54: Currents through input inductors L_1 and L_3.

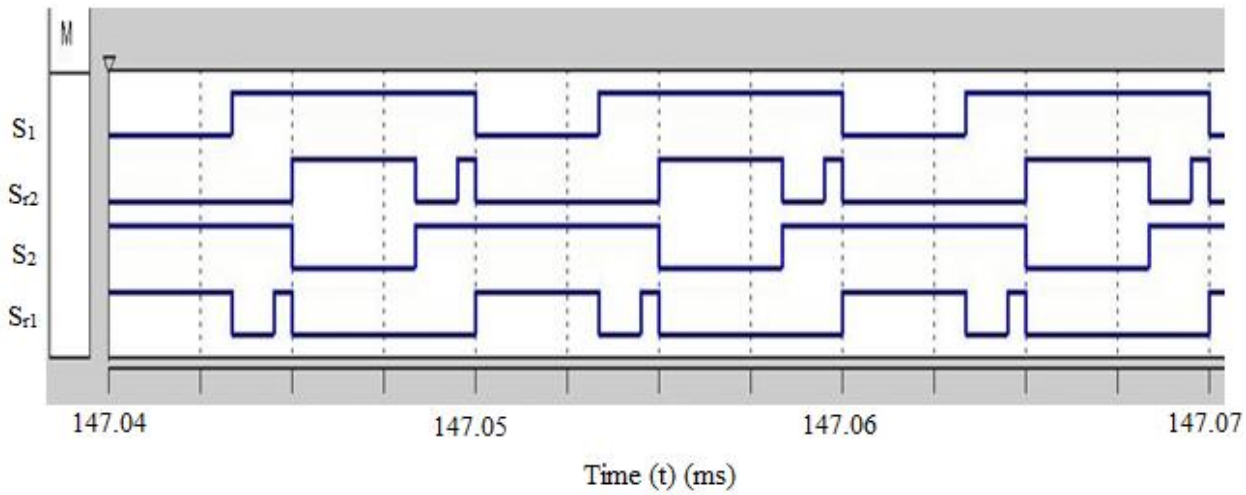

Fig. 55: Gate signals of switches S_1, S_{r2}, S_2, S_{r1} from the top under soft-switched condition.

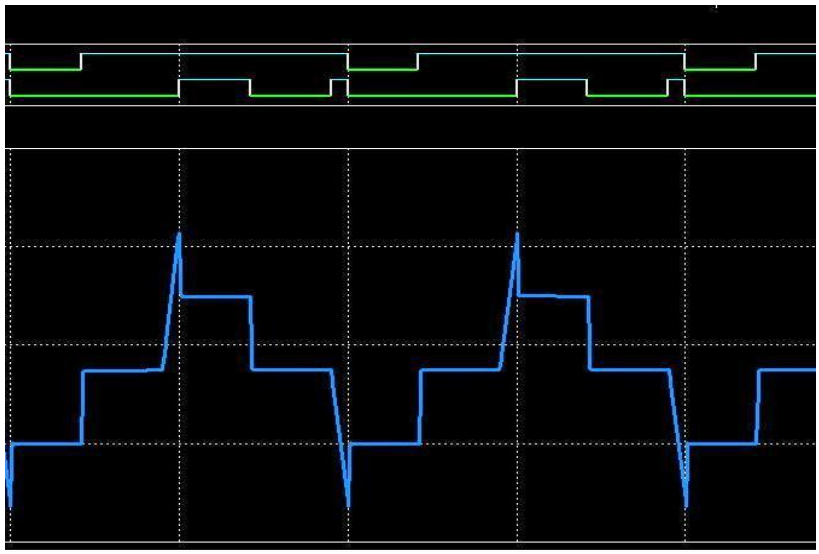

Fig. 56: Gate signals through S_1 and S_{r2} and current through S_1.

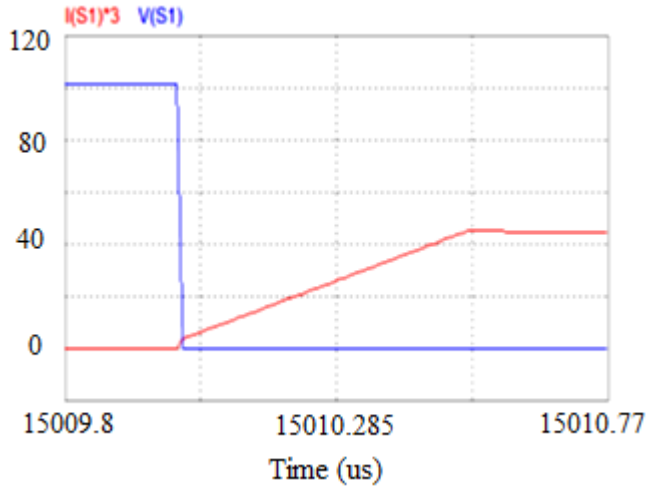

Fig. 57: Zero-current turn-on of S_1 (waveforms are scaled for clarity).

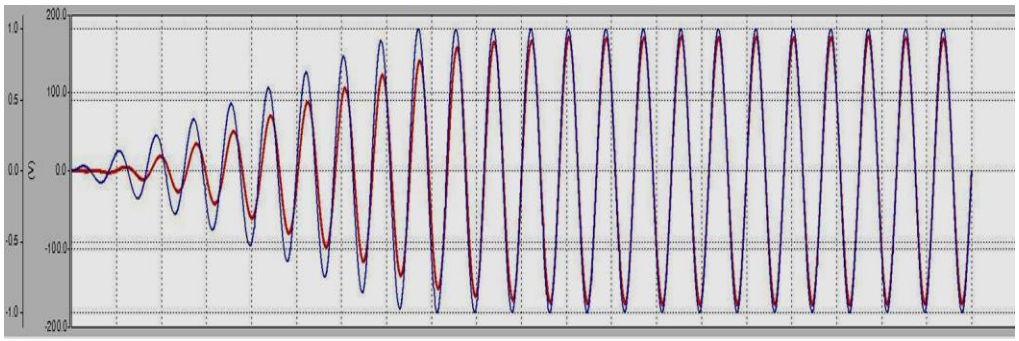

Fig. 58: Comparison of the output voltage under closed loop condition and the reference voltage signal.

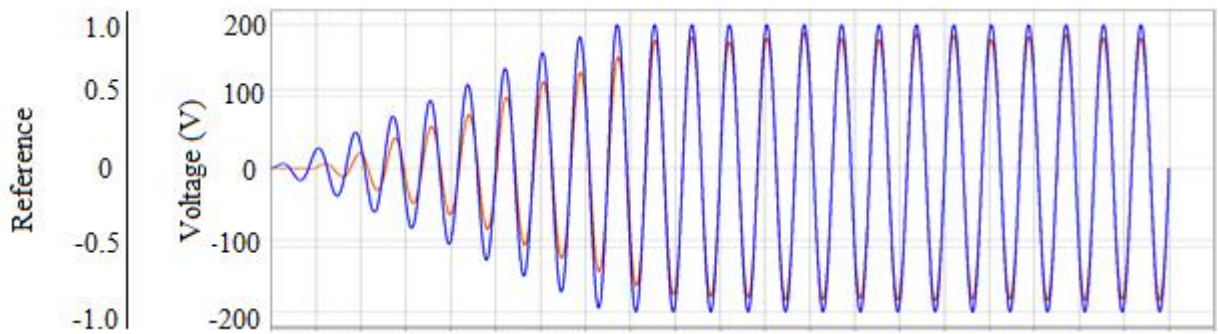

Fig. 59: Comparison of the output voltage under zero-reference closed loop scheme (without proportional gain) and the reference voltage signal.

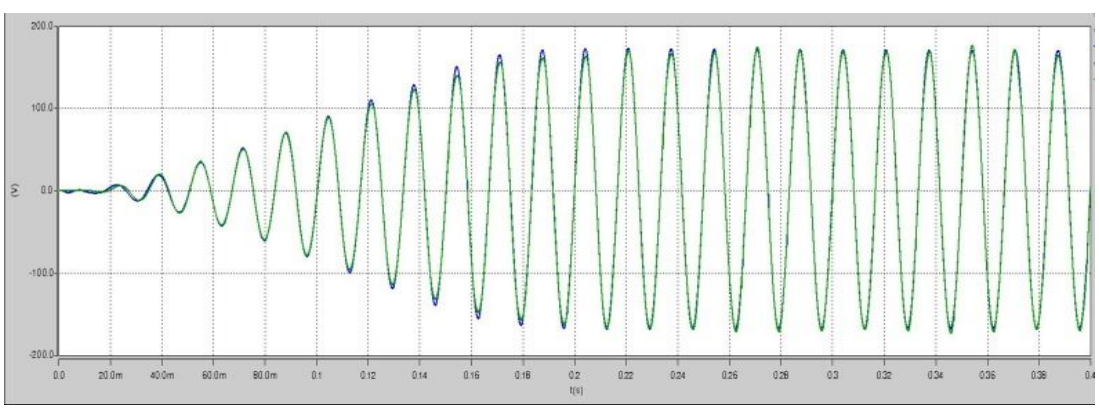

Fig. 60: Comparison of the load voltage with and without proportional gain (blue trace- with proportional gain and green trace- without proportional gain).

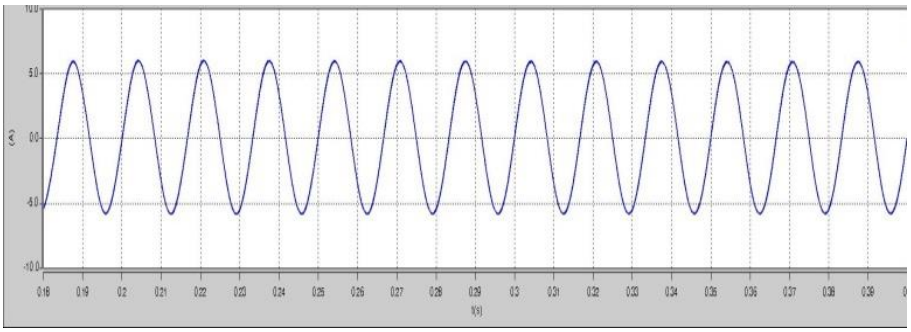

Fig. 61: Load current (with proportional gain and zero-reference).

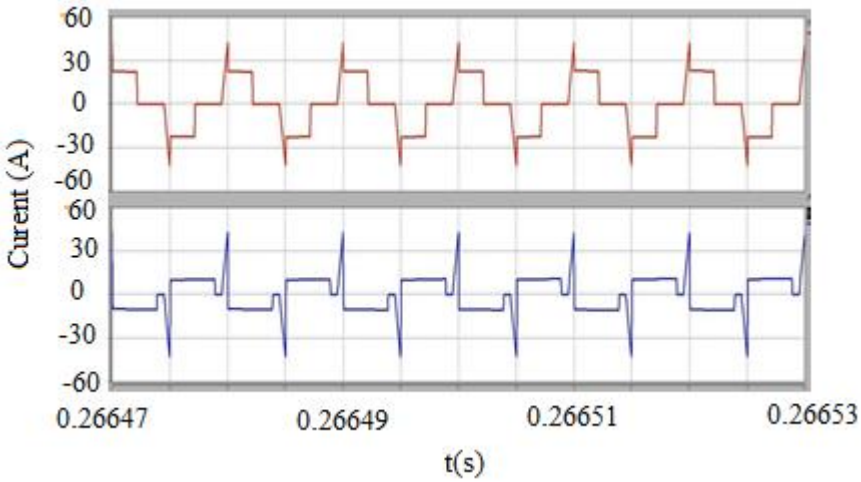

Fig. 62: Current through the leakage inductance (Module1- above and Module2- below) of the two modules during positive half-cycle of the load voltage.

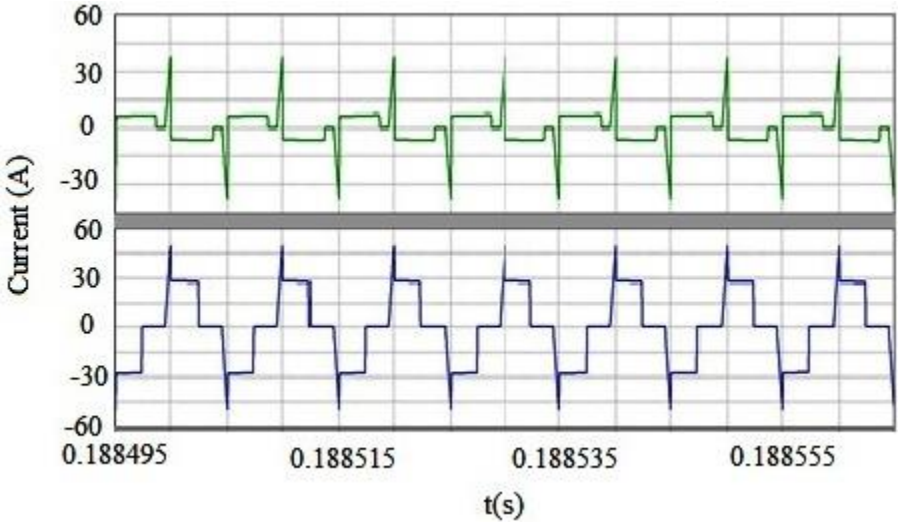

Fig. 63: Current through the leakage inductance (Module1- above and Module2- below) of the two modules during negative half-cycle of the load voltage.

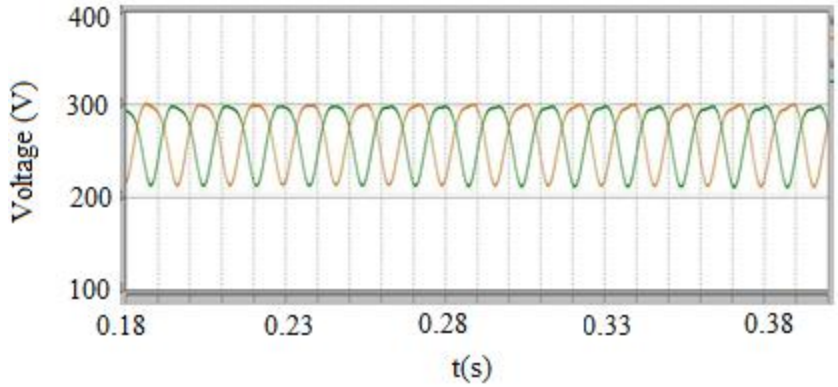

Fig. 64: Voltages of the output capacitors of both the modules.

APPENDIX

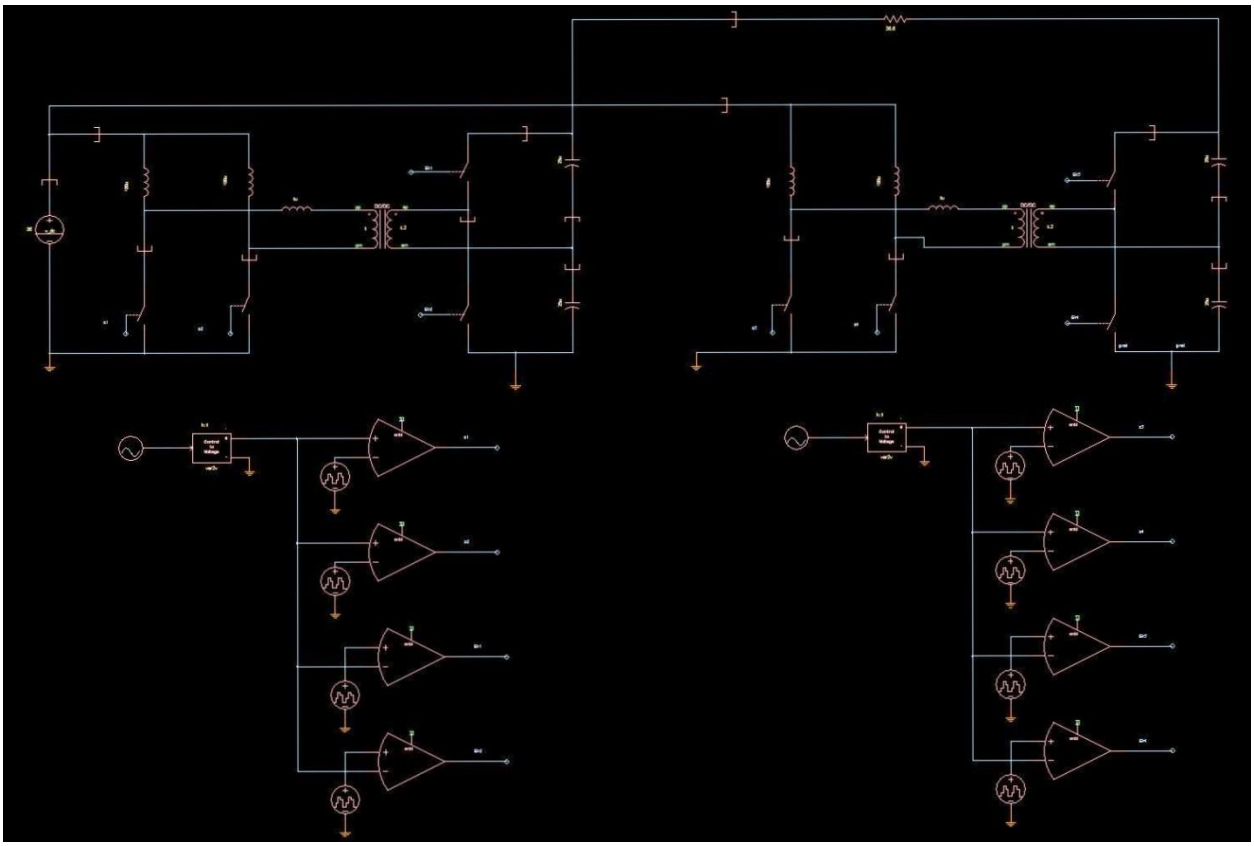

Fig. 65: Schematic of the hard-switched topology- Open loop in Saber.

APPENDIX (Continued)

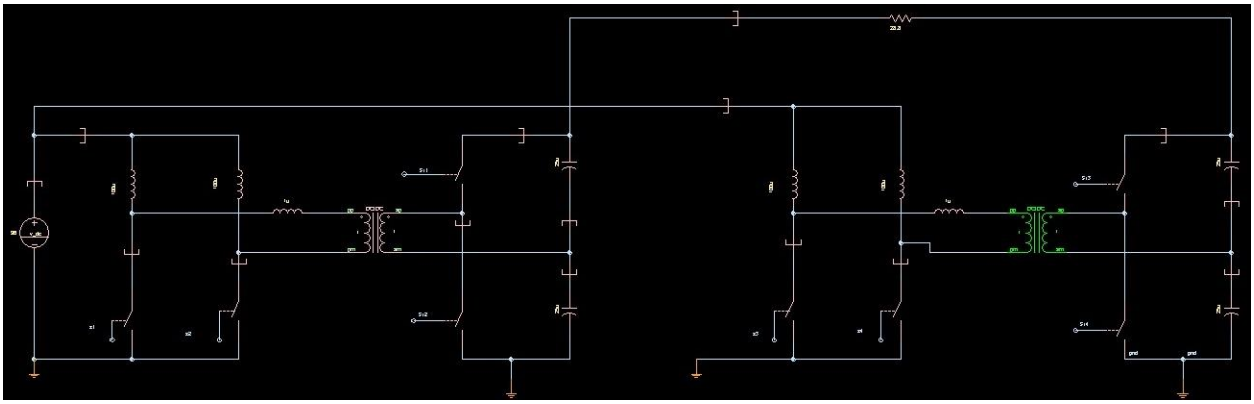

Fig. 66: Modules of the inverter (Zoomed in view).

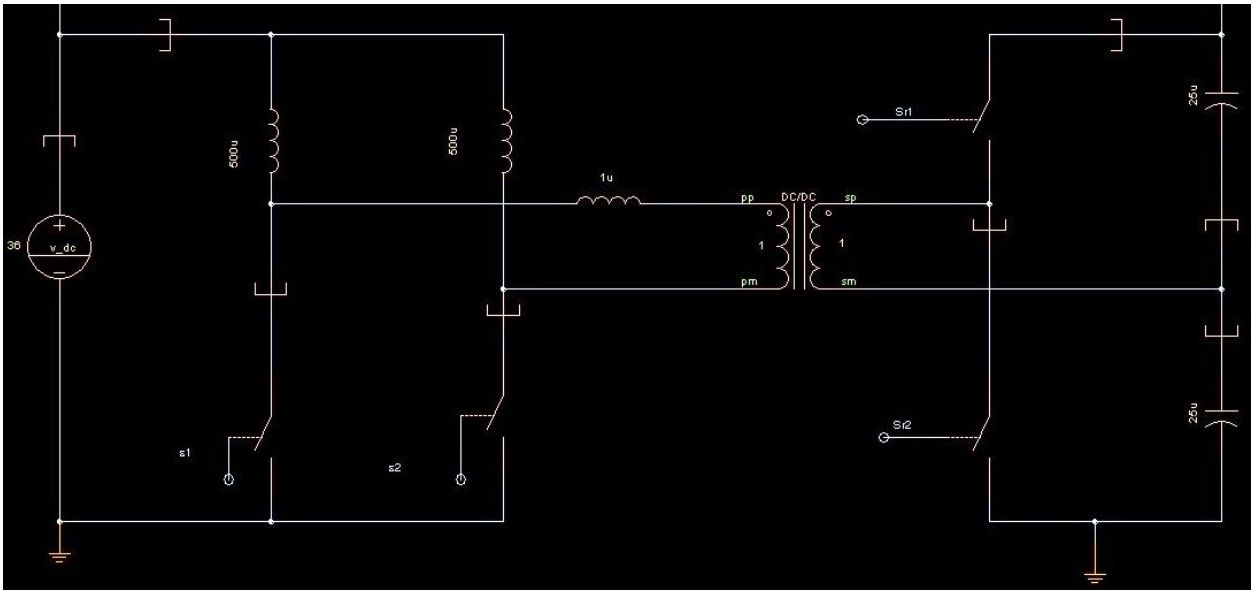

Fig. 67: Single module of the inverter (Zoomed in view).

APPENDIX (Continued)

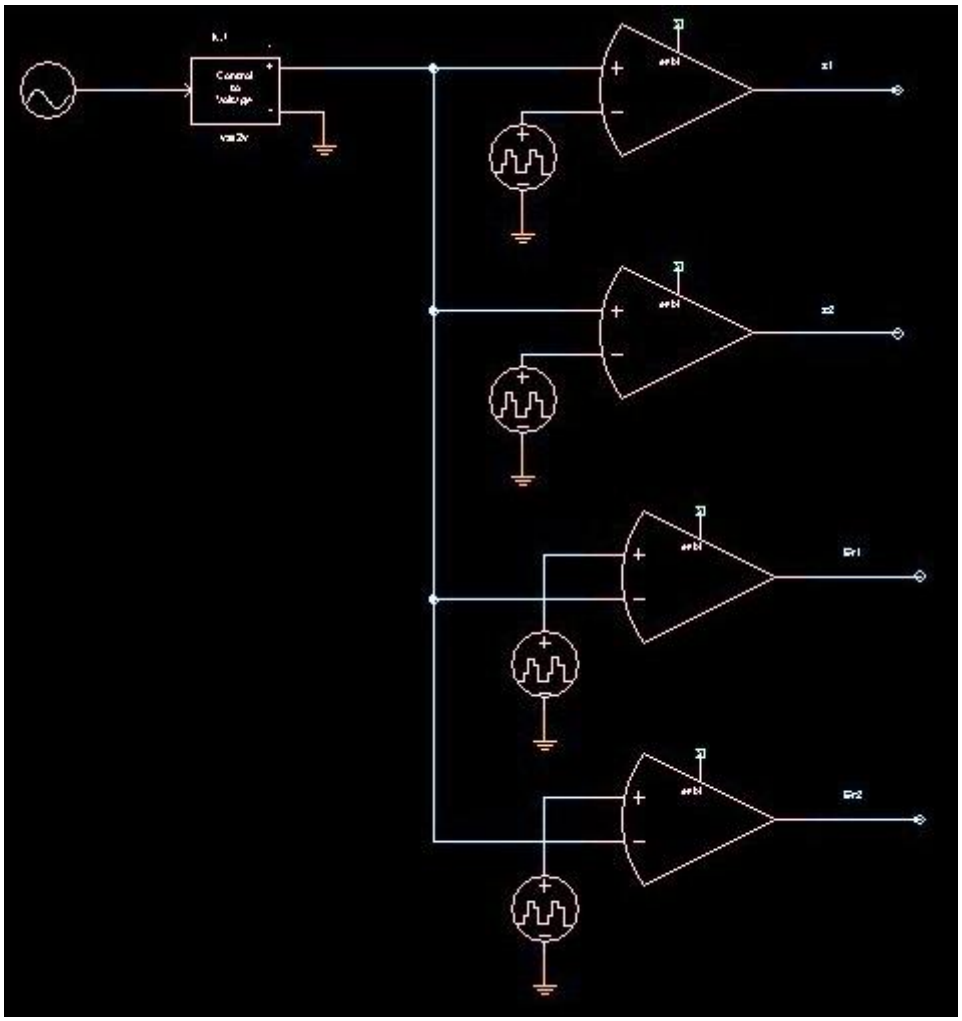

Fig. 68: Generation of switching signals under hard-switched condition (Zoomed in view).

APPENDIX (Continued)

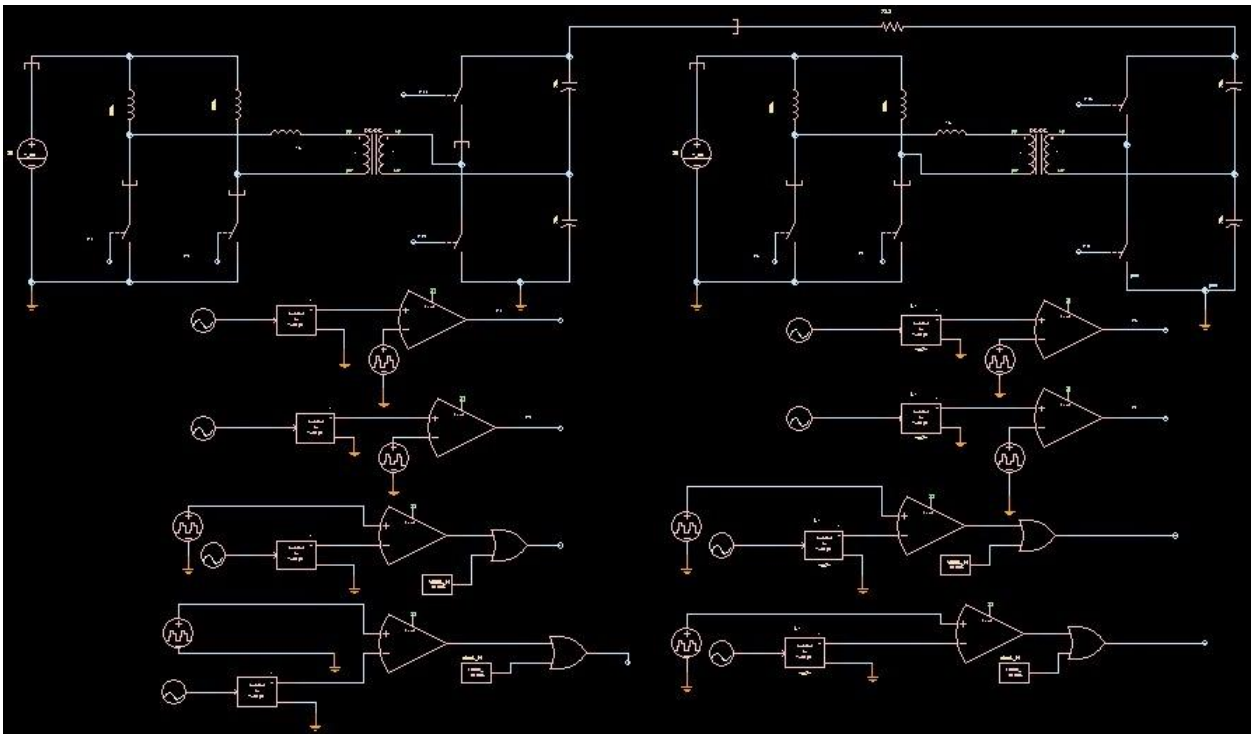

Fig. 69: Schematic of the soft-switched topology- Open loop in Saber.

APPENDIX (Continued)

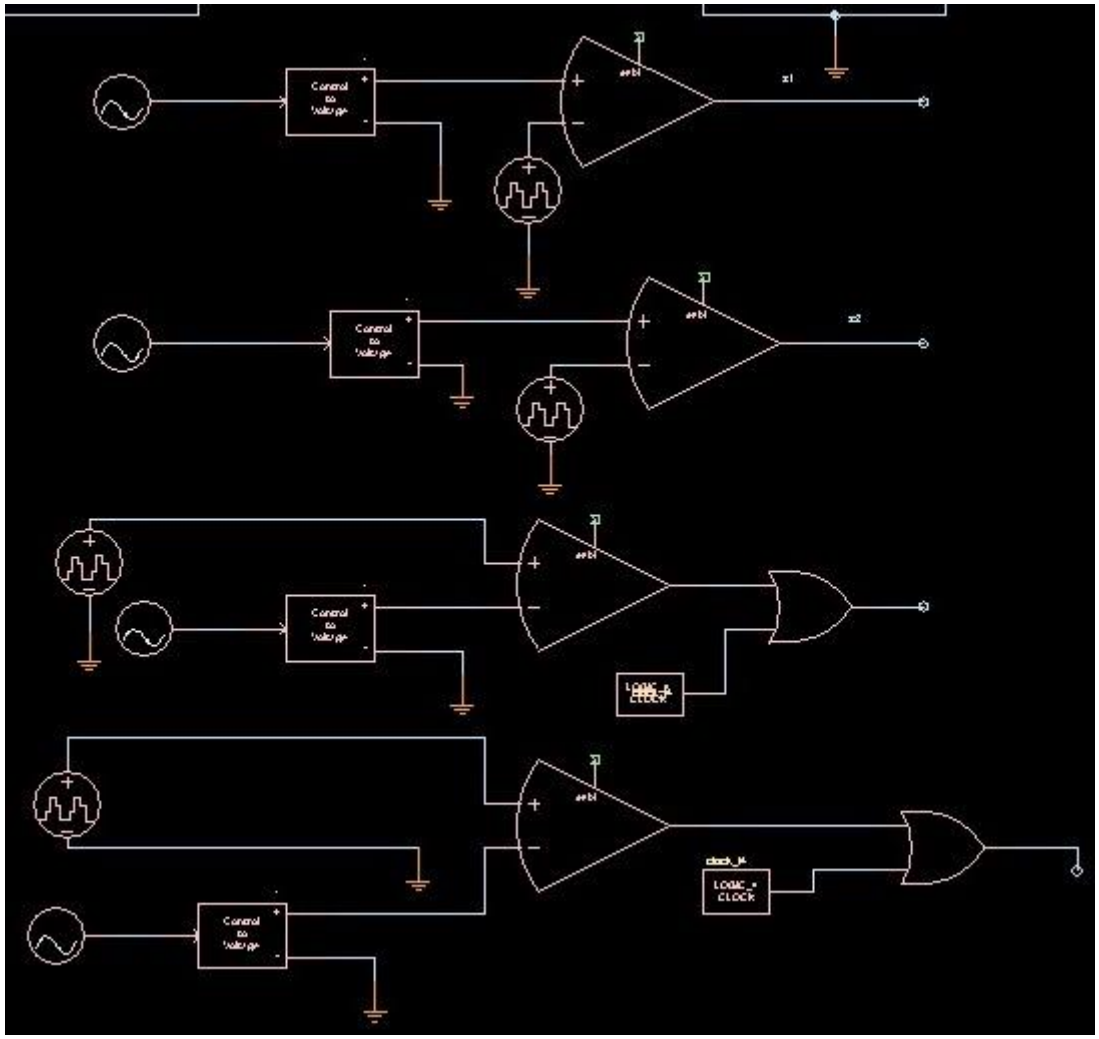

Fig. 70: Generation of switching signals under soft-switched condition (Zoomed in view).

APPENDIX (Continued)

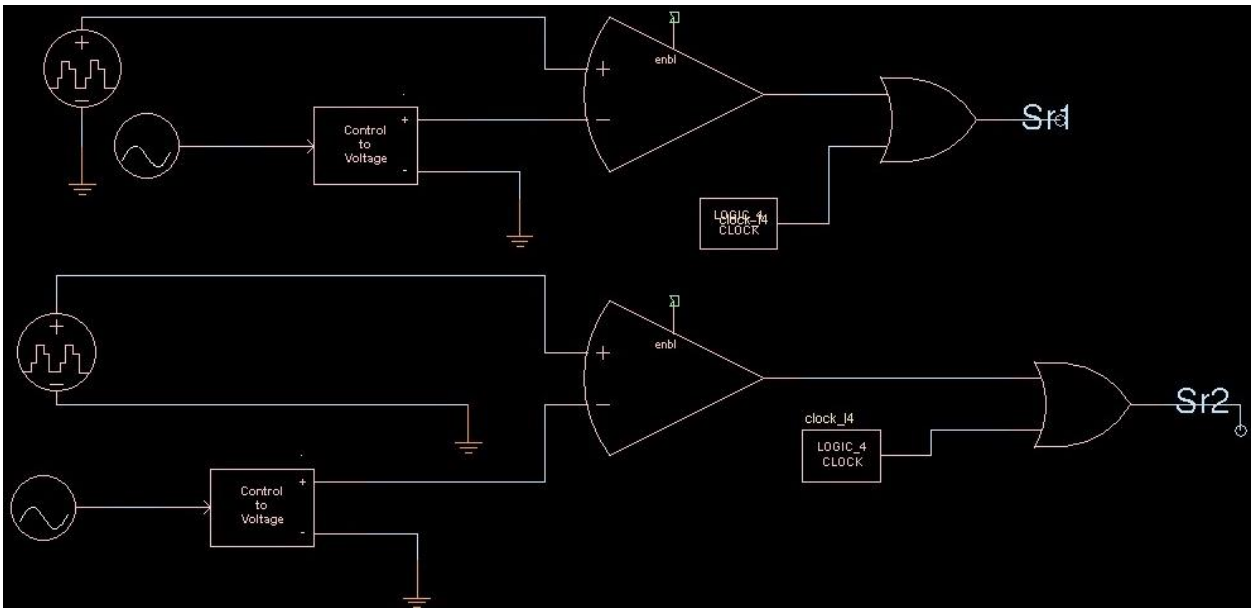

Fig. 71: Generation of switching signals for secondary-side switches in a single module under soft-switched condition (Zoomed in view).

APPENDIX (Continued)

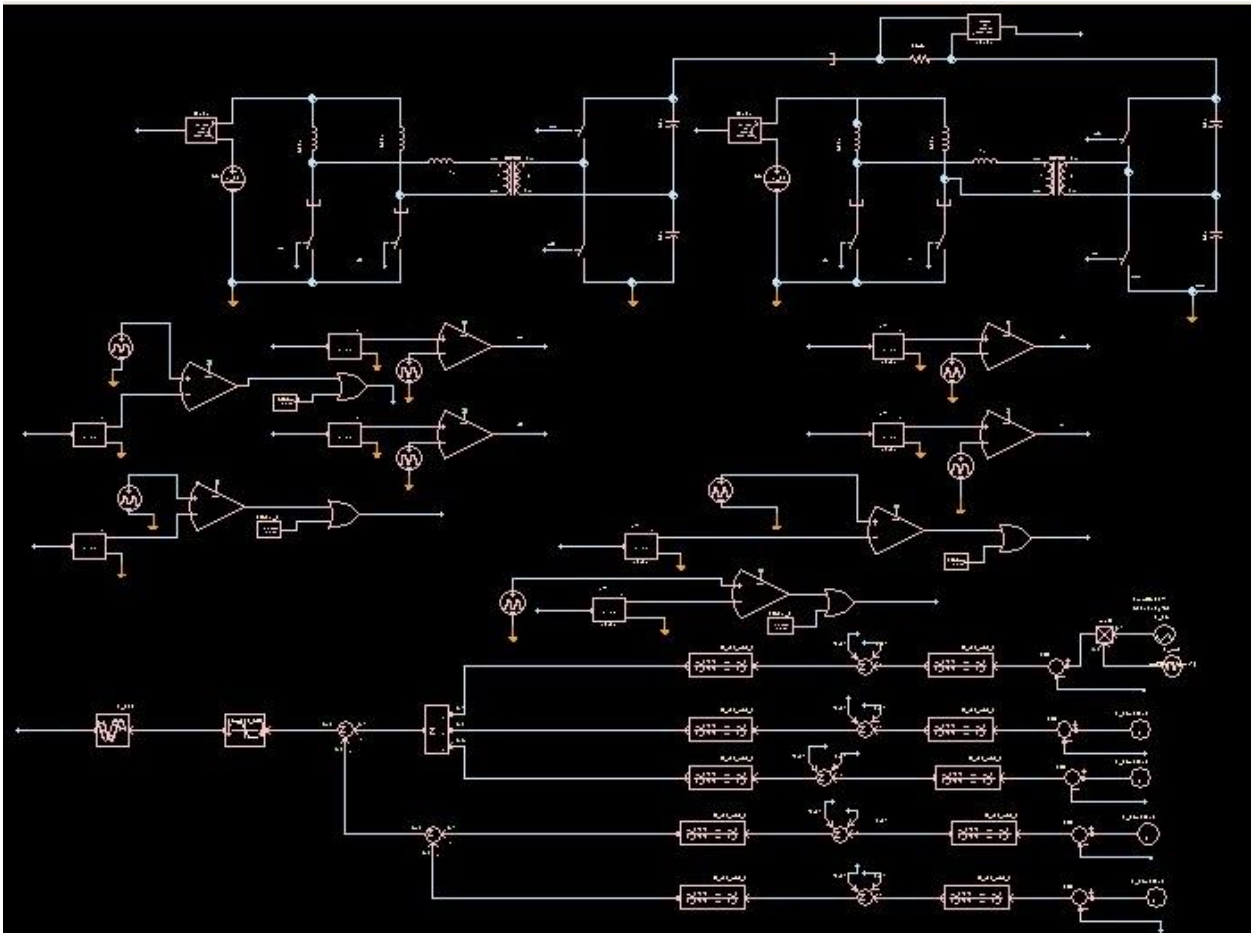

Fig. 72: Schematic of the differential inverter- Control strategy 1 in Saber.

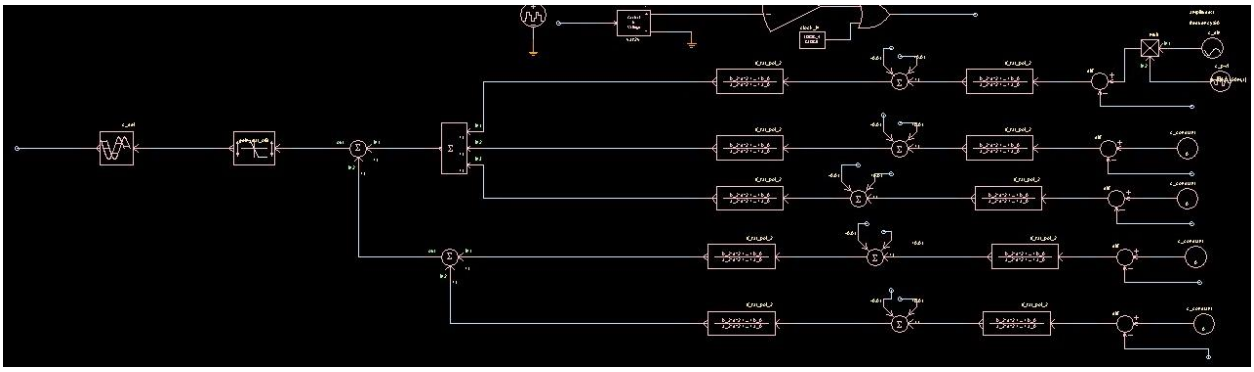

Fig. 73: Schematic of the PR controller- Control strategy 1 (Zoomed in view).

APPENDIX (Continued)

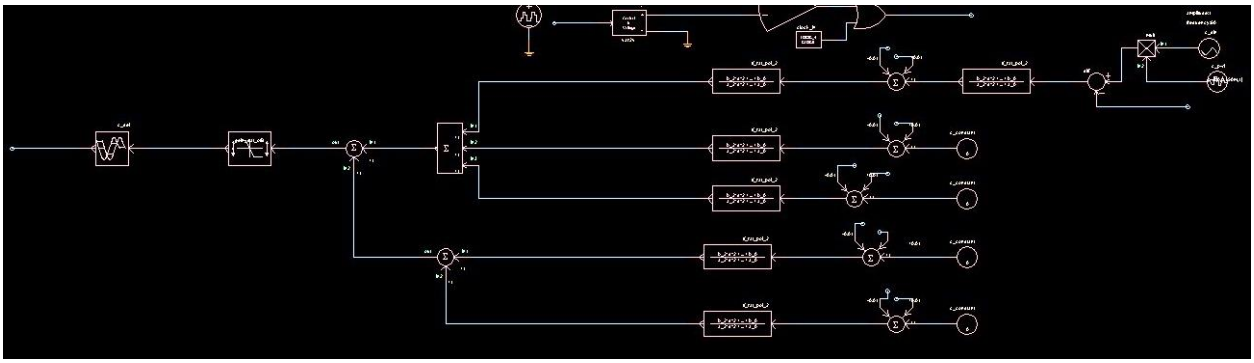

Fig. 74: Schematic of the PR controller- Control strategy 1 (Zoomed in view).

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