Design of a Frequency Counter for Mass-sensing Film-Bulk Acoustic Resonators

BY

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THESIS

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To my grandfather,

the best man I've ever known.

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LIST OF ABBREVIATIONS

PM	Particulate Matter
FBAR	Film Bulk Acoustic Resonator
MEMS	Microelectromechanical Systems
RF	Radio Frequency
AC	Alternate Current
DC	Direct Current
RTXO	Room Temperature Crystal Oscillator
TCXO	Temperature Compensated Crystal Oscillator
OCXO	Over Controlled Crystal Oscillator
IC	Integrated Circuit
DBM	Double-Balanced Mixer

SUMMARY

Particulate matter (PM) is a kind of air-borne pollutant to which smog, diesel exhaust, dust and smoke belong. Fine particle ($PM_{2.5}$) pollution is especially damaging to our health. Due to their small size these particles can lodge into the alveoli by deeply penetrating into our respiratory system, contributing to several health problems such as reduced lung functionality, bronchitis, and heart attacks. While there is increasing demand for $PM_{2.5}$ monitoring, the prevailing equipment is fairly bulky and expensive, which limits the possibilities for widespread, fine granularity sensing. Portable PM sensors are needed to allow for better identification of pollution sources, health awareness, and pollution control. In order to achieve this goal a MEMS air-microfluidic sensor is used, which measures the concentration of the particulates by the rate of the frequency shift of a mass-loaded film bulk acoustic resonator (FBAR). As particles are deposited onto the exposed surface of the resonator, the additional mass lowers its resonant frequency[1]. The main goal of this dissertation thesis is to design and realize a very low power portable RF frequency counter which operates with the MEMS air-microfluidic sensor in order to correctly measure the concentrations of airborne PM. The whole design is realized on a PCB board and it is specifically designed for small form factor and low power so that it can be seamlessly integrated with a mobile device such as a smartphone or a laptop.

CHAPTER 1

INTRODUCTION

The goal of this dissertation thesis is to design a portable, low cost frequency counter which can operate at very low power with an input signal coming from a FBAR resonator which senses PM in the atmosphere. Nowadays, higher spatial density monitoring is needed due to the increasing awareness of the negative health impacts of PM. Commercially available PM sensors are expensive and have a large form factor, which does not allow integration into a portable device designed to perform personal PM exposure level monitoring. The MEMS PM sensor developed by Paprotny et al.[1] is about two orders of magnitude smaller than any commercially available PM sensor: this enables easy integration into a portable platform for personal $PM_{2.5}$ monitoring. The schematic drawing of Figure 1 shows the functions of our MEMS PM sensor. The main goal of the air channels (shown in dark grey) is to separate the airflow into two airflows, one containing particles with aerodynamic diameter smaller than 2.5 μm (fine particles) and the other one containing particles with a larger aerodynamic diameter (coarse particles). This is achieved since air enters into the channels through the inlet (a), then the inertial size separator (b) (also called VI) divides particles by size. The coarse particles are ejected through the exhaust (d), while fine particles are removed from the airstream by thermophoresis and deposited on the exposed surface of a mass-sensing FBAR (c). The concentration of $PM_{2.5}$ particles in the airstream can be inferred by the rate of change in the resonant frequency of the FBAR: this is

made possible by the fact that the $PM_{2.5}$ concentration in the airstream is proportional to the rate of particle deposition onto the FBAR.

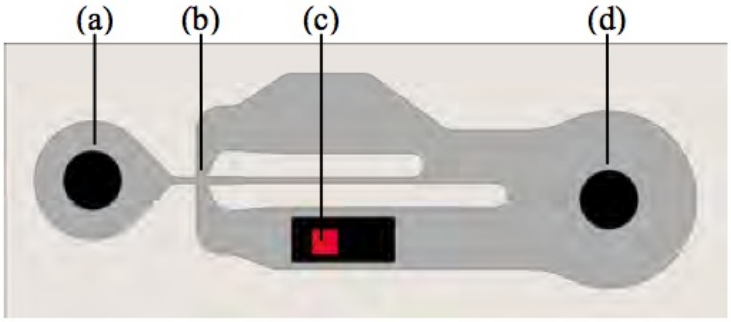

Figure 1. Schematic drawing (top view) of the air-microfluidic channels of our MEMS PM sensor. The channels are shown in dark grey, while the through-wafer holes are in black [1].

The signal coming from the PM sensor has been measured to have a central frequency of about 611 MHz, with output power -5 dBm. This frequency is subjected to change when the FBAR is mass-loaded and it senses $PM_{2.5}$ particulates in the environment. What we are interested in is to measure this frequency shift, which will tell us what is the pollution rate of change with respect to time in the environment under test. In order to achieve this goal we need to design a frequency counter, whose task is to collect frequency measurements of the PM sensor signal. The collected data will be sent to a laptop, in order to be analyzed and visualized

on a graphical display. Since the frequency coming from the sensor is centered around 611 MHz, a direct frequency counting is not feasible with cheap and low-power ICs because these circuits cannot work at such high frequency. In order to perform a high frequency measurement it is necessary to have a RF down-conversion front-end which must be placed between the PM sensor and the actual frequency counter. Doing so, the bandwidth of a cheap and low-power frequency counter can be extended to a much higher one and the signal can be easily counted. The overall FBAR frequency monitor block diagram is shown in Figure 2.

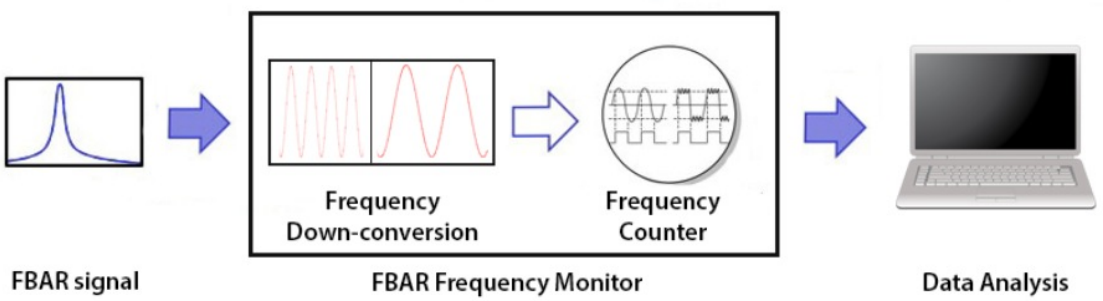

Figure 2. Block diagram of FBAR frequency monitor.

As we can see, the FBAR frequency monitor is composed of two main blocks: the first one is the front-end which reduces the input signal's frequency, while the second one is a

standard frequency counter. Our design must be low cost and low power, therefore the main device used to count the frequency is a microcontroller. As we all know, microcontrollers are devices that cannot work with signals much higher than 20 MHz, thus if we want to work with higher frequencies we need to find out a down-conversion method for reducing the input signal's frequency in order to keep it within the operating range. Hence, the main goal is to find a technique that lets us reduce the input frequency without losing the information carried by the signal and resulting in the minimum possible loss in resolution and accuracy. For this work, two popular down-conversion techniques have been implemented and tested in the final devices: *prescaling* and *heterodyne conversion*. Prescaling is a technique that involves dividing the frequency of a signal by means of a *prescaler*, which can be found as an integrated circuit (IC). Heterodyne conversion is a more complex technique that makes use of a *mixer* in order to take the sum and the difference of two input frequencies: the first input frequency is the frequency to be counted, while the second one is provided by a stable and high quality local oscillator. By choosing the appropriate frequency for the local oscillator, one can down-convert the RF input signal frequency within the operating range of the actual frequency counter. We will highlight the strengths and weaknesses of the two down-conversion methods described above, with focus on comparing them in order to find the best solution for our specific application. The design space will be explored in order to find the solution that meets the desired power-constraints without losing accuracy and resolution, keeping the price as low as possible in order for the device to be affordable for the average consumer.

CHAPTER 2

FREQUENCY COUNTER BASICS

RF frequency counters and timers are digital electronic devices which measure the frequency of a RF input signal. They operate by counting the number of events within a well known period or by measuring a period by counting the number of some precisely timed events. A very stable quartz crystal oscillator is usually used to generate the time periods within which events are counted, or the precisely timed events. Nowadays it is possible to find simple frequency counters, designed with state-of-the-art digital components, that can measure frequencies up to 500 MHz by exploiting a direct counting approach[4]. In the following sections we are going to analyze and compare the two main counting techniques, which are called *direct counting* and *reciprocal counting*.

2.1 Direct Frequency Counter

The direct frequency counter exploits a *direct counting* approach in order to perform related frequency measurements. The direct counting approach is the simplest one and it was the first to be ever used for commercial counters. The frequency f of periodic signals can be expressed as in Equation 2.1:

$$f = \frac{n}{t} \tag{2.1}$$

where n represents the number of cycles of the periodic signal that occur in the time interval t. Usually t is set to 1 second so that the frequency can be expressed in *cycles per second*, or *Hertz*

(Hz). More generally, the frequency of a signal is measured by counting a number of cycles and dividing it by the time interval during which the measurement has been performed. The basic block diagram of a frequency counter in direct counting configuration is shown in Figure 3.

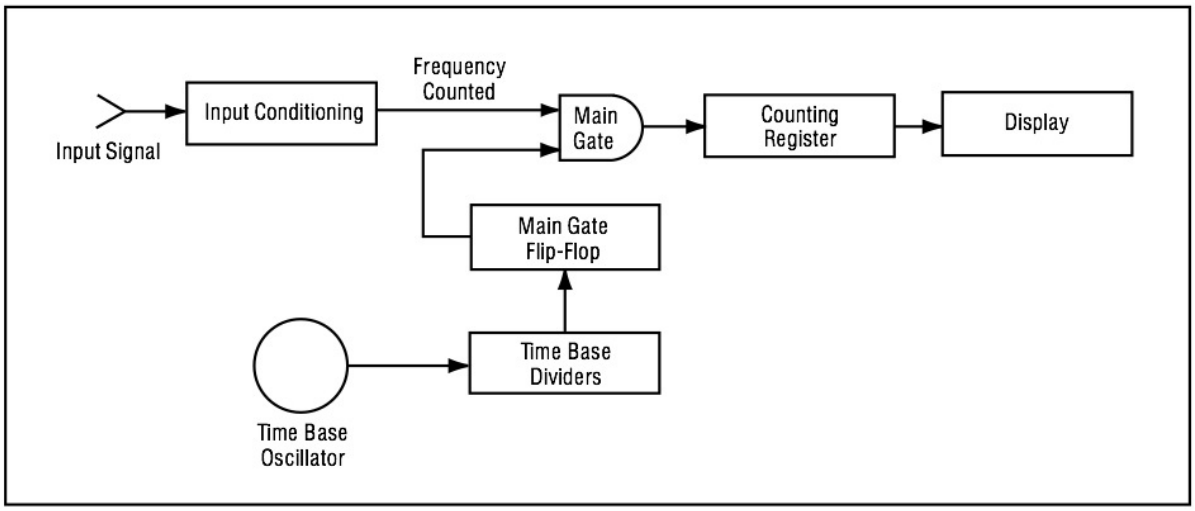

Figure 3. Basic block diagram of a frequency counter [5].

Within the conventional frequency counter we can observe several main blocks:

- *Input Conditioning*: The input signal is initially converted into a digital square wave representation in order to be compatible with the counter's internal digital circuitry. This is usually achieved by means of a Schmitt trigger circuit to avoid the generation of spurious

pulses due to noise in the input signal. Trigger levels and sensitivity are controlled within this section.

- *Time Base*: From equation Equation 2.1 it is possible to show that the accuracy and resolution of a frequency measurement is strictly related on the accuracy in which the gate time t is generated. For this reason, commercially available counters make use of a very precise crystal oscillator as the Time Base element[5]. Many low cost instruments can be used with a higher quality external oscillator for improved performance, while expensive high quality instruments may be provided with an oven controlled crystal oscillator (OCXO), which is way more precise and expensive than a standard XO.
- *Time Base Dividers and Flip-Flop*: The Gate Time enabling signal for the Main Gate is generated by dividing the Time Base oscillator signal using the Time Base Dividers and then feeding it into a flip-flop. The time t of equation Equation 2.1 corresponds to the Gate Time. Common gate times are 0.01, 0.1, 1, and 10 seconds. Shorter Gate Times let output data to be refreshed faster, the drawback is that the counting accuracy is decreased.
- *Main Gate*: The precisely generated Gate Time signal is fed into one input of the Main Gate, while the input signal coming from the input conditioning section is fed into the second input. The resultant output from the Main Gate is a pulse train which last for a precise amount of time equal to the Gate Time itself, so that pulses are counted by the Counting Register during the time the Main Gate is kept open by the Gate Time signal.

- *Counting Register*: The input signal frequency is computed by taking the value stored into the Counting Register and dividing it by the selected Gate Time. For instance, if value stored in the Counting Register is 50000 and the Gate Time is 1 s, then the measured input signal frequency is 50000 Hz. The counted frequency can be visualized on a display or sent to another electronic device for further data manipulations.[5]

2.2 Input Considerations

The input conditioning stage usually consists of some basic blocks such as an attenuator, an amplifier and a Schmitt trigger as shown in Figure 4. The attenuator and the amplifier are employed in order to fully exploit the available dynamic range, while The Schmitt trigger is employed to convert the input signal from an analog representation into a digital one compatible with the counter's internal digital circuitry. There are many critical aspects to take into account in order to properly condition the input signal, what follows next is a description of the problems that may appear and the solution to solve them.

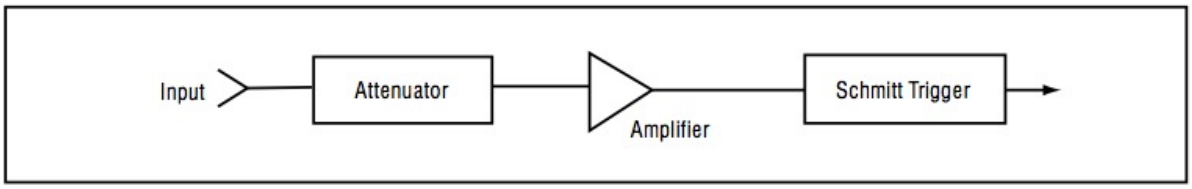

Figure 4. Major elements of a counter's input circuitry [5].

- *AC-DC Coupling*: Signals with a DC content can be counted only if some kind of AC coupling is provided in the input conditioning section. The effect of AC coupling is clearly shown in Figure 5.

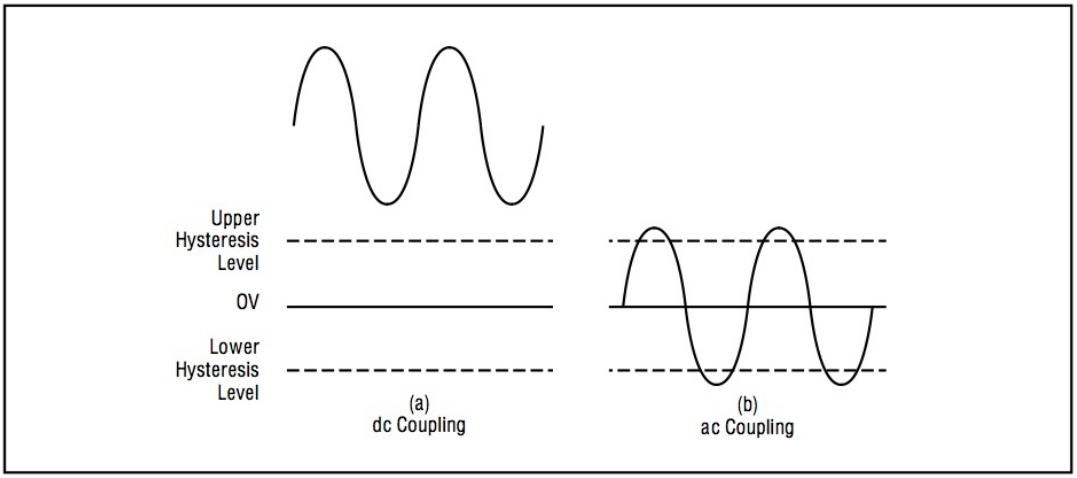

Figure 5. AC coupling is used to remove the DC content of the input signal, if present [5].

- *Sensitivity*: The counter's sensitivity is defined as the minimum voltage that the input signal must reach in order to be counted. The sensitivity is determined by the input impedance, the amplifier gain and the amplitude of the Schmitt trigger hysteresis window. The input sensitivity must be carefully optimized during the design process because noise

on the input signal can cause false triggering if the the front end is highly sensitive. The effect of having a hysteresis level is shown in Figure 6.

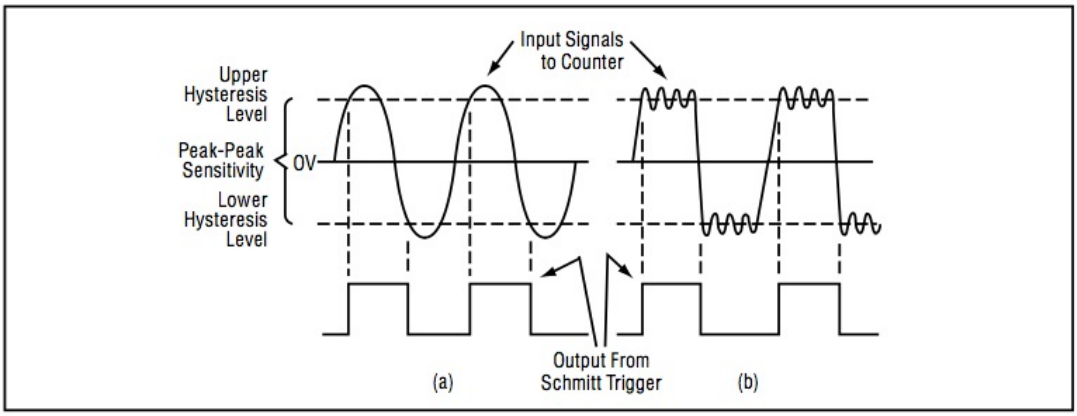

Figure 6. The signal is counted if and only if it crosses both boundaries of the hysteresis window. In this way, any noise present on the input signal cannot cause false triggering [5].

- *Dynamic Range*: The dynamic range can be defined as the linear operating range of the input amplifier. A highly linear input amplifier is not needed since we are not interested in the waveform itself but only in its frequency. With a well designed amplifier it is not a problem to exceed the dynamic range since no false counts will take place. However, exceeding the dynamic range is not good practice since, in case of input impedance drop, the amplifier response speed could decrease due to saturation effects. Input protection

is usually provided in order to do not exceed the damaging level of the input amplifier. Conventional protection often are not enough in case of fast transients on a 50Ω input, therefore several commercial counters are equipped with high speed fuses in order to provide further protection.

- *Attenuators*: The dynamic range of the input should not be exceeded, for this reason attenuators are provided for large level signals. Standard step attenuators with fixed values such as X1, X10 and X100 are usually employed for wide dynamic range inputs, even though it is also possible to find counters with variable attenuators on low dynamic range input because of their capability of variably attenuating noisy signals in order to generate an optimal signal amplitude while minimizing noise.
- *Input Impedance*: A 1MΩ input impedance with a sensitivity of 25 mV to 50 mV is usually preferred for frequencies up to 10 MHz because sources connected to the input will not be loaded and the 35 pF shunt capacity will have small effect. On the other hand, a 50Ω impedance input with low shunt capacity is preferred for frequencies beyond 10 MHz because the shunt capacity of high impedance inputs rapidly reduces the input impedance beyond this frequency. A sensitivity from 20 mV to 25 mV is usually employed with 50Ω inputs in order to avoid noise and related problems.

2.3 Time Base Oscillator Considerations

The time base oscillator represents the source of the precise gate time t as defined in Equation 2.1. Virtually every modern frequency counter employs a quartz crystal as the oscillating element because of its good performance/price ratio. A quartz crystal oscillator can be modeled

with an equivalent electrical circuit, as shown in Figure 7. The physical properties of the crystal determine the values of R_1, C_1, L_1, and C_0. In order to obtain a tuned circuit, an external variable capacitance is typically added. The frequency of a crystal oscillator is temperature sensitive because of the L, C and R elements.

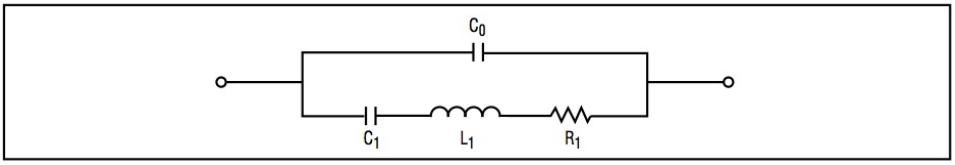

Figure 7. Equivalent circuit of the crystal [5].

Three main families of crystal oscillators are available:

- *Room Temperature Crystal Oscillator (RTXO)*: these oscillators have the highest frequency change over temperature. Pretty good stabilities can be achieved by choosing a proper crystal cut during the manufacturing process. Typical high quality RTXO may have a stability over temperature of about 2.5 parts per million (ppm) in the range from 0°C to 50°C.
- *Temperature Compensated Crystal Oscillator (TCXO)*: A cheap and effective method to compensate for frequency changes due to temperature variation is to add some external capacitance or passive component to the tuned circuit, with opposite temperature coef-

ficient with respect to the internal one. A typical high quality TCXO offers an order of magnitude improvement in frequency stability with respect to a RTXO, with a frequency stability of 0.5 ppm over 0°C to 50°C.

- *Oven Controlled Crystal Oscillator (OCXO)*: in this type of oscillator, the crystal is embedded in an oven which actively compensates for temperature variations in the environment surrounding the crystal. A typical frequency stability for a high quality OCXO may be around 0.007 ppm over 0°C to 50°C. An OCXO may take 24 hours or more after turn-on to achieve its specified stability, however most high-end counters employing an OCXO have a feature that allows the oven to be powered whenever the power line is connected even if the counter is not turned on. In this way it possible to avoid the need for the warm-up phase and retrace. This is the most precise, expensive and power hungry type of crystal oscillator, therefore it can be found only on very high-end counters.

The accuracy of the oscillator frequency can be affected by additional factors other than temperature variations, which can be defined as follows:

- *Effect of Line Voltage Variations*: any variation in the power supply voltage causes a variation in the oscillator frequency. The stability with respect to line voltage variation is typically expressed within 10% of line voltage variation. High quality voltage regulators are usually incorporated in the counter in order to reduce this kind of error, however very high line voltage stability is not needed since the frequency error due to line voltage variation is always smaller compared to the one due to temperature variation.

- *Aging Rate or Long Term Stability*: aging is a cumulative frequency drift due to the change of the physical properties of the crystal with respect to time, as shown in Figure 8, which is usually specified in terms of frequency change per month since temperature and other effects would mask the amount of aging over shorter time periods. The higher the quality of the crystal used, the lower the effect of aging.[5].
- *Short Term Stability*: it is related to random frequency changes and phase fluctuations present in the oscillator signal. Any specification of short term stability must include the averaging or measurement time involved since it is spectrally related. The effect of this noise is inversely proportional to the averaging (or measuring) time, so that the larger the measuring time the lower the noise.[5].

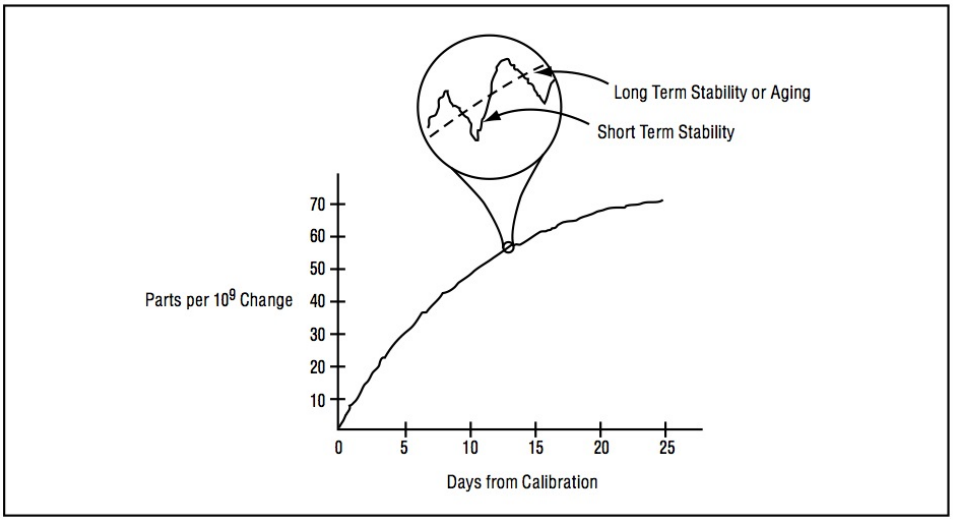

Figure 8. Effect of aging on frequency stability [5].

TABLE I

TYPICAL ERRORS SPECIFICATIONS OF THE FOUR TYPES OF OSCILLATORS

	RTXO	TCXO	Switching OCXO	Proportional OCXO
Temperature (0°C - 50°C)	$< 2.5 \cdot 10^{-6}$	$< 5 \cdot 10^{-7}$	$< 1 \cdot 10^{-7}$	$< 7 \cdot 10^{-9}$
Line Voltage (10% change)	$< 1 \cdot 10^{-7}$	$< 5 \cdot 10^{-8}$	$< 1 \cdot 10^{-9}$	$< 1 \cdot 10^{-10}$
Aging	$< 3 \cdot 10^{-7}/mo$	$< 1 \cdot 10^{-7}/mo$	$< 1 \cdot 10^{-7}/mo$	$< 1.5 \cdot 10^{-8}/mo$ or $< 5 \cdot 10^{-10}/day$
Short Term (1 sec avg.)	$< 2 \cdot 10^{-9}$ rms	$< 1 \cdot 10^{-9}$ rms	$< 5 \cdot 10^{-10}$ rms	$< 1 \cdot 10^{-11}$ rms

All the oscillator characteristics described before are summarized in Table I, they are collected by considering typical specifications of high quality commercially available oscillators. The total time base oscillator error is computed by adding together all these individual sources of error. However, the frequency deviation due to time base error is only one of the several sources of error for a frequency counter, which are going to be described in the following section.

2.4 Frequency Measurement Error Analysis

The first source of measurement error is represented by the propagation delay of the physical main gate, also called *switching time*: the time window in which the main gate is open is affected by the swithcing time. This error is often referred to as *switching error*. It is clear that the switching error will be significant only if the switching time is significantly large compared to the period of the highest frequency that must be counted. While the switching error can be

minimized by allowing longer times, we still have other relevant sources of errors. The most relevant sources of measurement error for a frequency counter can be summarized into the following four categories:

- *Quantization Error*: Any electronic counter has a ± 1 count ambiguity in the least significant digit. This ambiguity occurs because the internal clock frequency and the input signal are not coherent between each other, as shown in Figure 9. In other words, the quantization error represents the minimum input frequency change detectable by the counter. The quantization error can be expressed as:

$$Q_{err} = \frac{1}{t_m}\ Hz \tag{2.2}$$

  Where t_m represents the gate time. A longer gate time results in a smaller quantization error. This also represents the *resolution* of the system.

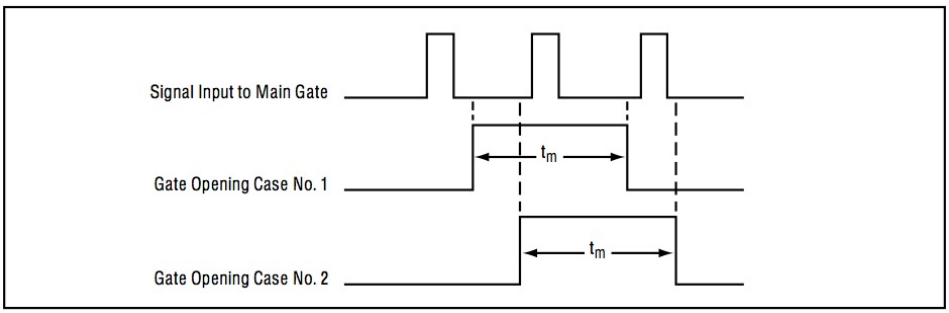

Figure 9. The same gate time t_m may provide different readings because the input signal is not synchronized with the main gate signal [5].

- *Time Base Error*: Any difference between the actual time base frequency and its nominal one induces a measurement error, which is the due to the cumulative effect of all the individual time base errors described in Section 2.3 and it is expressed in parts per million (ppm).

The overall frequency measurement error (FM_e) can be expressed as the sum of the quantization error (C_e) and the time base error factor (TBF_e):

$$FM_e = \pm C_e \pm TBF_e \ [Hz] \tag{2.3}$$

The relative frequency measurement error due to ± 1 count ambiguity for a 1 second gate time can be therefore expressed as:

$$\frac{\Delta f}{f} = \frac{\pm 1}{f_{in}} \tag{2.4}$$

Where f_{in} represents the frequency of the input signal. From Equation 2.4 it's easy to show that the relative frequency measurement error due to ± 1 count becomes smaller for high input signal frequencies. For instance, if we consider a 10 MHz input signal we can compute the relative frequency measurement error due to ± 1 count ambiguity for a 1 second gate time, which comes out to be:

$$\frac{\Delta f}{f} = \frac{\pm 1}{f_{in}} = \frac{\pm 1}{10 \cdot 10^6} = \pm 1 \cdot 10^{-7} \tag{2.5}$$

For the purpose of this example we can assume a time base error of 1 ppm, i.e. $TB_e = \pm(1{\cdot}10^{-6})$. If we consider again a 10 MHz input signal then the measurement error introduced by the time base will be:

$$TBF_e = TB_e \cdot f_{in} = \pm(1 \cdot 10^{-6}) \cdot 10^7 \ Hz = \pm 10 \ Hz \tag{2.6}$$

In this particular case we get that the ± 1 quantization error is masked by the time base error, which is one order of magnitude bigger. If the input frequency would be below 1 MHz then the ± 1 count error would become dominant over the time base error[5].

CHAPTER 3

DOWN-CONVERSIONS TECHNIQUES

The upper limit on the frequency bandwidth of a counter is determined by the speed of the digital logic employed in the design. The designer of frequency counters must look for some kind of down-conversion techniques if it is necessary to extend the range of his counter beyond the available 500 MHz range. It is possible to find state-of-the-art commercial counters that work with very sophisticate down-conversion techniques, high-speed digital devices and extremely precise time base oscillators. Some of them can work with frequencies up to 40 GHz, giving resolutions up to 12 digits thanks to interpolation and mathematical analysis based on statistical models[4]. The main issue is that they are designed to work in a laboratory's environment, therefore they are not portable, consume a huge amount of power and are very expensive. This not a problem if the user can afford one and it is possible to connect the instrument to a main power supply, however it becomes not feasible if the main goal is to work with a cheap device that must be USB or battery-powered for low power applications. In the following sections we are going through the details of two main down-conversion techniques, which are called *prescaling* and *heterodyne conversion*. Both of them have been implemented and tested on our final devices. The PCB designs and experimental results are shown in Chapter 4 and Chapter 5, respectively.

3.1 Prescaling

The speed of the main gate switches and the counting registers represent an upper limit on the accuracy of a frequency measurement at high input frequencies. The simplest possible technique that is employed in order to increase the bandwidth of a frequency counter is called *prescaling*, which is simply implemented by adding a *prescaler* (also called frequency divider) in the input signal path. The prescaler is an electronic device used to divide the frequency of a high frequency signal by a factor N, thus reducing its frequency to a lower one . Modern prescalers can operate in the GHz range[6][7], obviously the upper limit in frequency that a counter can reach will be the maximum frequency at which the prescaler can operate. In a frequency counter the prescaler may condition the input signal before applying it to the main gate, as shown in Figure 10. The prescaler can also be placed before the input conditioning stage.

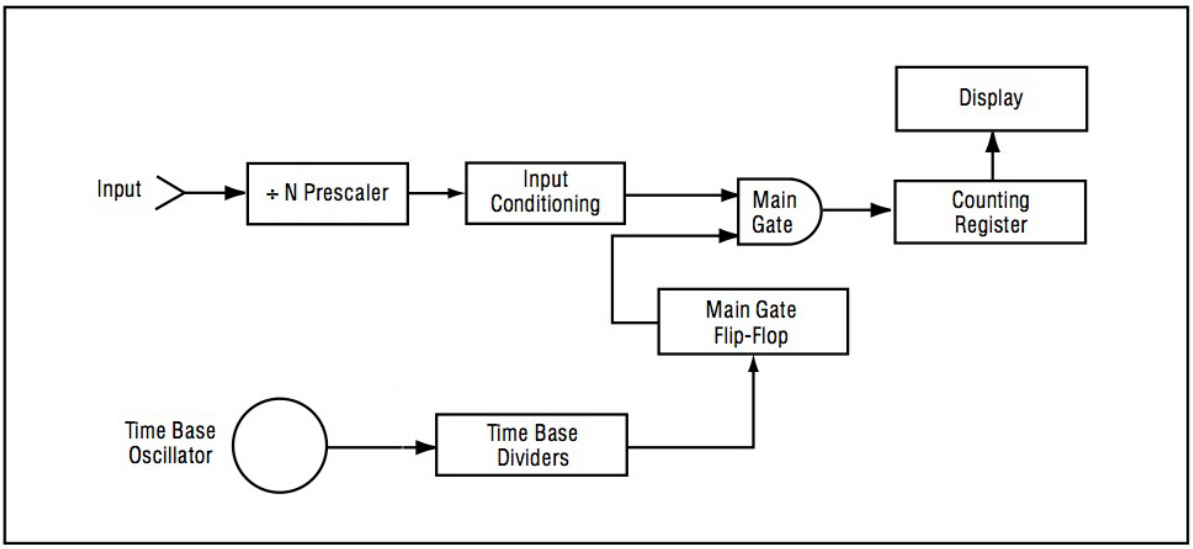

Figure 10. Block diagram of prescaling counters [5].

Typical modern prescaler are designed with division factors in powers of 2, usually going from 2 up to 256. With a prescaler, the frequency response of a counter can be easily increased by a factor N. However, the gate time must be N times longer in order for the counting register to accumulate the same number of counts that would be accumulated in a counter without any prescaler in the front-end. Therefore, prescaling involves a tradeoff: a slower and cheaper internal digital logic can be used, at the expense of an additional device (i.e. the prescaler) and a slower frequency measurement[5]. For instance, assume to use a direct frequency counter as shown in Figure 3. For a 1 second gate time, the quantization error will be ± 1 Hz. If a

modulo-64 prescaler is placed before the counter, the quantization error for the same gate time will be ±64 Hz. In order to get a ±1 Hz quantization error with a modulo-64 prescaler we need a gate time of 64 seconds.

3.1.1 Prescaler Topologies

A Johnson counter is an easy and popular implementation of a 1:2 prescaler[8]. As shown in Figure 11, two D-latches are coupled in a loop and clocked by inverse clocks.

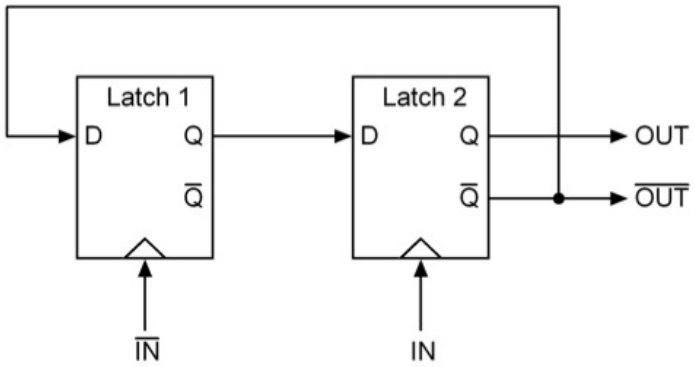

Figure 11. Johnson counter, 1:2 prescaler [7].

When IN goes low the signal $\overline{OUT}$ is being transferred to the output of the first latch, and transferred further to OUT when IN goes high again. This is shown in the timing diagram of Figure 12. OUT inverts every time IN goes high, and thus the frequency is divided by two. Figure 13 shows a 1:3 prescaler circuit utilizing two flip-flops and an AND gate. Both flip-flops

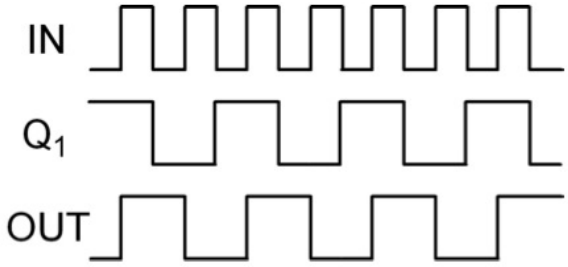

Figure 12. Timing diagram for Johnson counter [7].

are being clocked at the rising edge of IN. The following logic function is obtained:

$$\overline{Q_2}(n+1) = \overline{Q_1(n)\overline{Q_2}(n)} = \overline{\overline{Q_2}(n-1)\overline{Q_2}(n)} = Q_2(n-1) + Q_2(n) \tag{3.1}$$

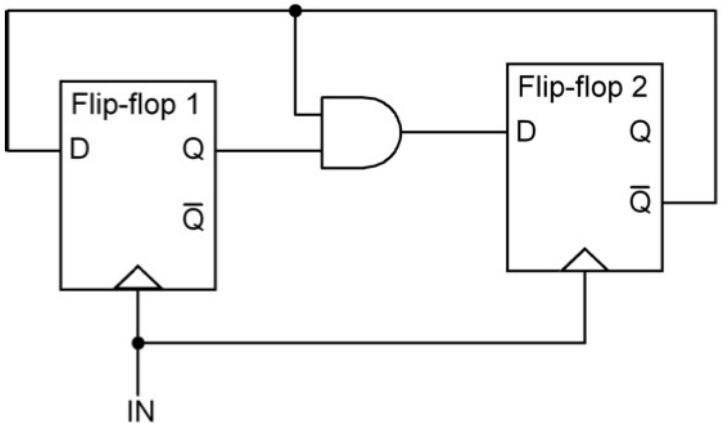

Figure 13. 1:3 prescaler [7].

As can be seen from the timing diagram of Figure 14, the circuit swallows one extra period of the input signal per output period compared to the Johnson counter.

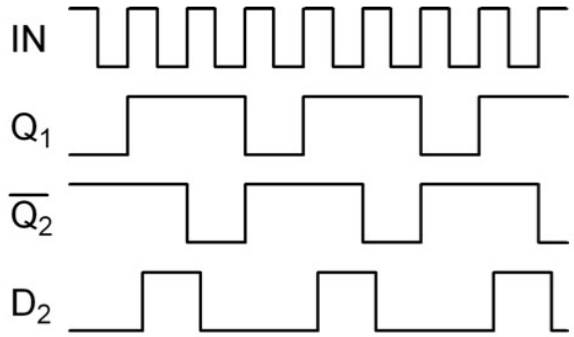

Figure 14. Timing diagram for 1:3 prescaler [7].

It is also possible to combine the two previous topologies in a new one which lets the user to chose between a 1:2 and a 1:3 prescaler. This is called a dual-modulus prescaler[9] and it is shown in Figure 15. This circuit divides the frequency of the input signal by either 2 or 3, depending on the logic state of the control signal M. When M is low the output of the OR-gate will be controlled directly by Q_1, and the circuit will operate in the same way as the previously described 1:3 circuit. When M is set to high the output of the OR-gate will be high independent of the output of the first flip-flop, thus the output of the first AND-gate follows $\overline{Q_2}$. On every rising edge of IN, $\overline{Q_2}$ will be inverted, and thus the frequency is divided by 2.

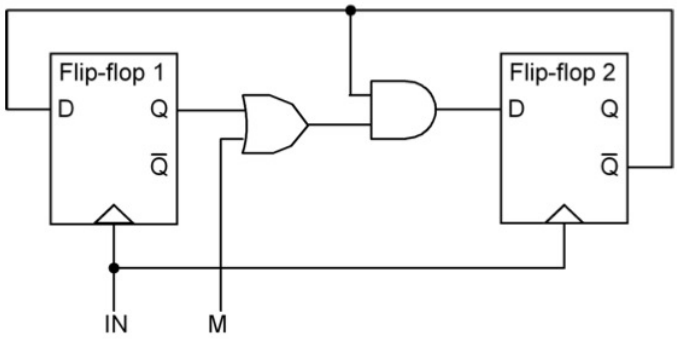

Figure 15. Modulo-2/3 dual-modulus prescaler circuit [7].

By cascading two or more dual-modulus prescalers one can obtain a multi-modulus prescaler. An example of how this can be done is shown in Figure 16. The circuit consists of two of the modulo-2/3 circuits described above coupled in series. The modulus control signals are binary weighted, so the period of the output signal will be as shown in Equation 3.2, the resulting prescaler can divide on moduli ranging from 4 to 7.

$$T_{OUT_2} = T_{IN} \cdot (2^2 + 2^1 \cdot M_1 + 2^0 \cdot M_0) \tag{3.2}$$

To achieve this there is an OR-gate on the M input of the first prescaler which allows this circuit to work in 1:3 mode only once per OUT_2 period. Note that it is the inverses of the modulus control signals that are applied at the inputs, in order to achieve the given function

for the output period since the cells that are used divide by 2 when $M = 1$ is applied and by 3 when $M = 0$ is applied.

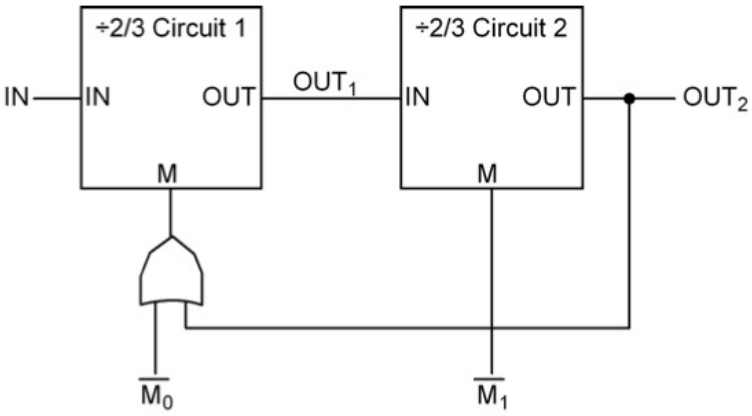

Figure 16. Modulo-4/5/6/7 2-bits prescaler circuit [7].

A timing diagram for this circuit in 1:5 mode is shown in Figure 17 ($M_1M_0 = 01$). This circuit can easily be extended to a n-bits prescaler by cascading n modulo-2/3 prescalers and gating the modulus control signal for each of them through an OR-gate together with the OUT signal from all the following modulo-2/3 prescaler circuits[7].

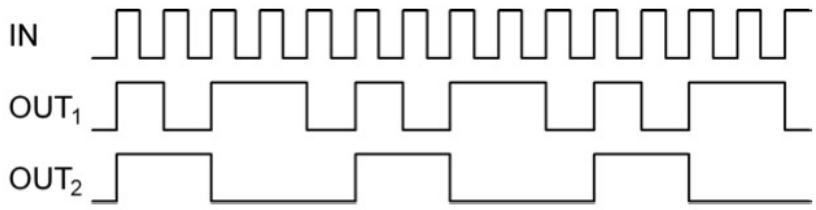

Figure 17. Timing diagram for modulo-4/5/6/7 prescaler in 1:5 mode [7].

3.2 Heterodyne Conversion

Heterodyning is a radio signal processing technique in which a new frequency is generated by mixing two frequencies[10][11][12]. With this technique, usually employed in demodulation and modulation of radio and microwave signals, it is possible to shift the harmonic content of a signal into a completely new frequency range, thus getting an output signal at a higher or lower frequency but without losing the information carried by the input signal[11]. In its simplest form, two frequencies are combined in a nonlinear device such as a diode, a transistor or a vacuum tube, usually called a *mixer*[12]. Figure 18 shows the block diagram of a frequency counter that exploits the heterodyne down-conversion technique.

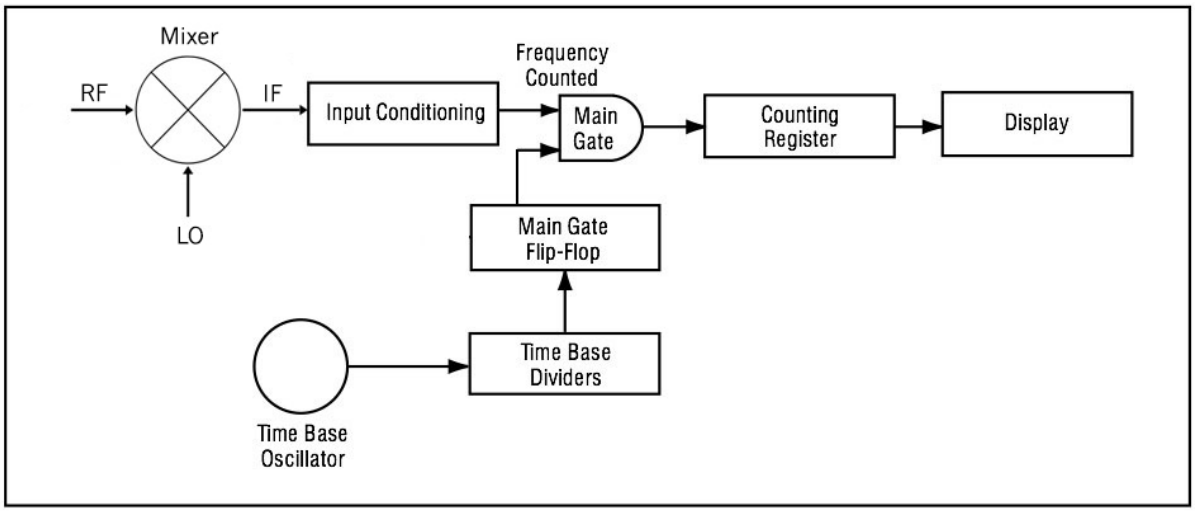

Figure 18. Block diagram of the heterodyne down-converting counters.

Figure 19 shows the basic diagram of an ideal mixer. A mixer has two input ports, which are called Radio Frequency (RF) and Local Oscillator (LO), and one output port called Intermediate Frequency (IF). In frequency counters, one of the two input frequencies of the mixer is provided by a high-stability local oscillator signal, while the other one is of course the signal whose frequency must be counted.

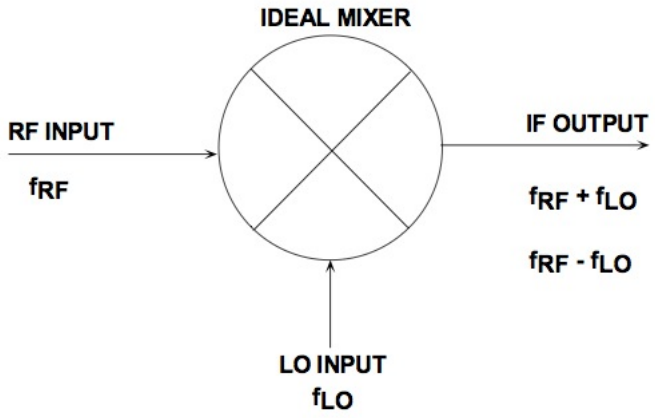

Figure 19. The mixing process.

The task of a mixer is to take the signal coming into the port RF and to mix it with the one coming into the port LO, thus producing an IF output signal. The frequency of the signal IF consists of both the sum and the difference between the two input frequencies[13], as shown in Equation 3.3.

$$f_{IF} = f_{RF} \pm f_{IF} \tag{3.3}$$

Typically, a square wave signal or a sinusoidal continuous wave (CW) signal is used to drive the LO port, depending on the particular application. The LO signal can be seen as the gate of the mixer, i.e. the mixer is active when the LO signal has a large voltage and not active when LO has a small voltage. It is possible to use the RF port either as an input or an output, depending on the mixer mode of operation. We are talking about *down-conversion* if the desired output

frequency is lower than the input one: in this case, the RF represents the second input and IF is the output. This is exactly how we desire the mixer to perform in a heterodyne frequency counter. It is also possible to use the mixer in a *up-conversion* configuration, where the output frequency is higher than the input one. In this case, IF is used as the second input and RF is the output. Figure 20 shows a spectral representation of down-conversion and up-conversion. The mixer's symbol identifies which is the input frequency. In down-conversion the input is RF, which is combined with LO, while in up-conversion the input is IF, which combined with LO provides the output up-converted frequency RF. The dashed arrow indicates in which direction the input frequency is shifted.

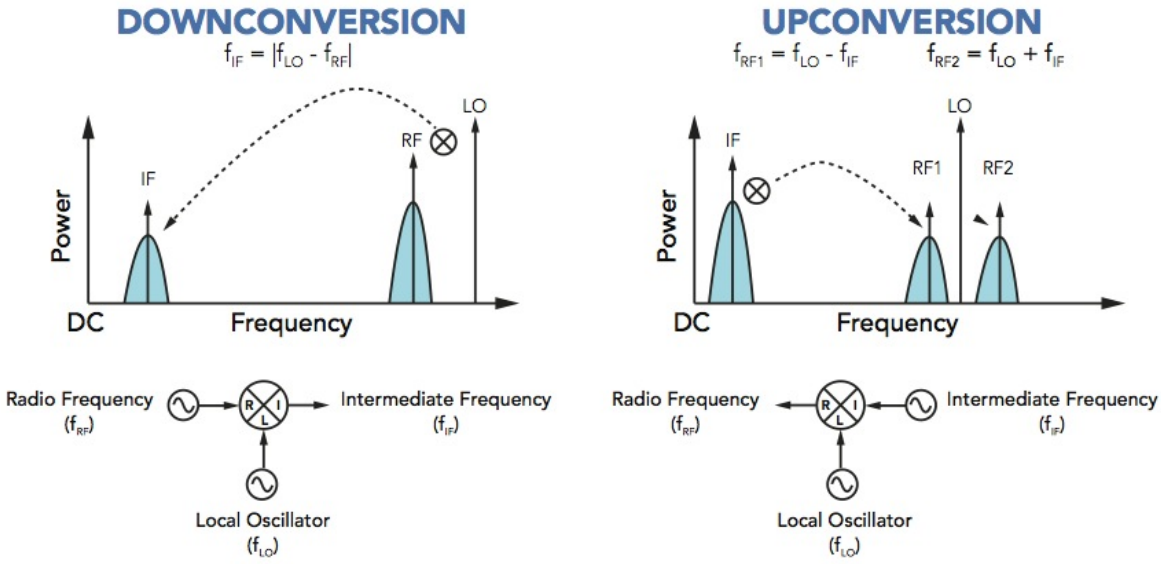

Figure 20. Definition of down-conversion and up-conversion [14].

As we can see from Figure 20, RF and IF have broad spectra since they are information bearing signals. When a down-frequency conversion is performed, all the information carried by RF is translated to the IF output. It is clear that mixers must be carefully designed in order to perform frequency transformations without distorting the original information carried by the input signal[14]. The strength of this technique is that there is no loss in resolution and very small loss in accuracy if the local oscillator has a very high stability, therefore an accurate frequency measurement can be obtained even when the input frequency is reduced

by a big factor. Modern mixers are designed by employing Schottky diodes, GaAs FETs, BJTs and CMOS transistors. Schottky diodes are used for high performance applications while CMOS and FETs are used in high volume applications because of their lower cost and higher density[14].

3.2.1 Passive Mixers

Passive mixers typically use Schottky diodes as nonlinear elements, or FETs as passive switches. The most common form of mixer is represented by a single diode, where both the LO and RF signals are applied at the anode. The LO must be a strong signal that forces the diode to be open or closed, thus chopping the small signal RF. Real diodes posses some amount of turn-on transition time, moreover the diode transconductance is modulated by the RF signal (even if the RF signal is very small). Because of these issues, additional mixing products appear at the mixer output, which are called *spurs*[14]. A real diode produces all possible harmonic mixing components, both odd and even, as shown in Equation 3.4.

$$f_{IF} = Nf_{LO} \pm Mf_{RF} \ (N \ and \ M \ are \ all \ integers) \tag{3.4}$$

We are only interested in a single output frequency (i.e. N = M = 1) therefore te existence of all the other harmonics represents a problem. For this reason, modern high-performance mixers are designed by making use of circuit simmetry in order to create *balance*. A basic scheme of a double-balanced mixer (DBM)[13] is shown in Figure 21, which is simply a diode ring.

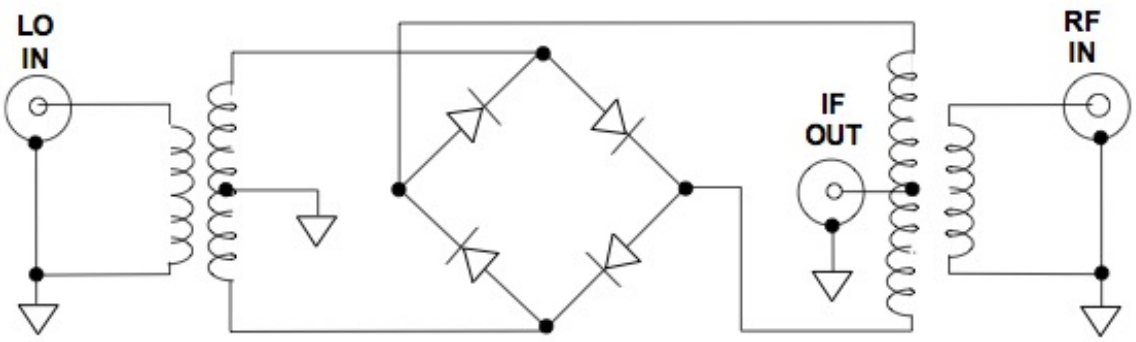

Figure 21. Double-balanced diode-ring mixer.

The principle of operation is exactly the same as before, where the LO signal switches the diodes ON and OFF while the RF signal is alternately sent through the diodes. DBM are commercially available as surface-mount packages, with embedded diodes and transformers[15]. Real-world DBMs reduce nearly 75% of all spurs, since only odd N and odd M harmonics reach the IF port. Hence, a balanced mixer offers several advantages like very good isolation among all ports, high conversion efficiency, common mode signal rejection and cancellation of most intermodulation products[14]. The drawback is that passive mixers don't provide any gain, instead they show a conversion loss of about 7 dB. This loss is due to the internal resistance of the diodes, port impedance mismatches and the 3 dB wasted in filtering out the undesired output frequencies[15]. DBMs can work up to 8 GHz and beyond by using Schottky diodes, therefore they are suitable for very high performance applications.

3.2.2 Active Mixers

The diode-ring mixer is not suitable for fabrication using integrated circuit technologies. The diodes can be replaced by four transistors, which can essentially perform the same switching function[16]. This is the basis of the Gilbert cell circuit[17], which basic scheme is shown in Figure 22.

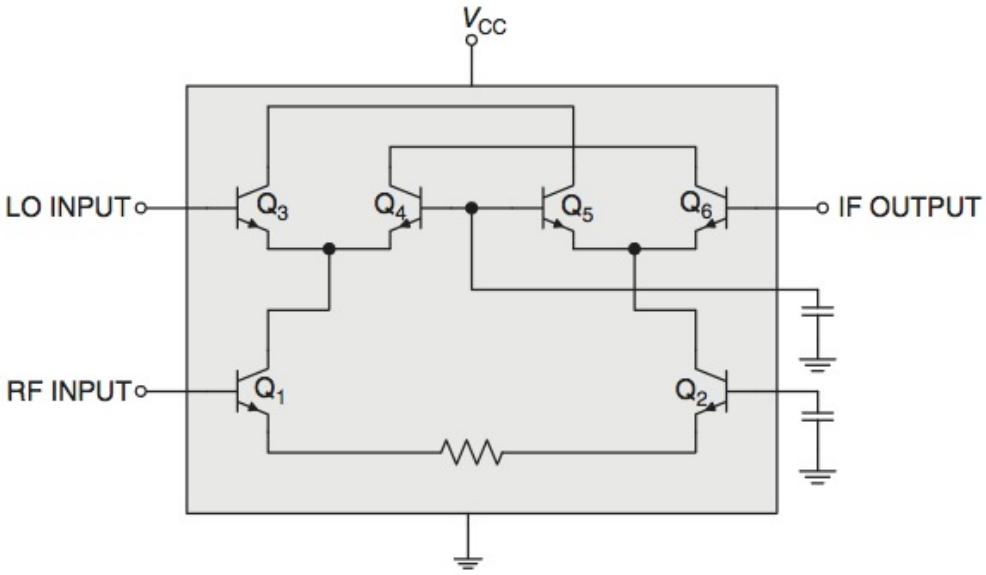

Figure 22. A simplified depiction of a Gilbert cell integrated mixer.

The RF signal is fed into the base of Q1, while the LO signal is input into the base of Q3. The LO signal forces Q3 and Q6 in ON/OFF state while Q4 and Q5 are always turned ON. This causes the mixing of RF and LO thus generating the output IF[17]. The strong LO signal forces the transistors to operate in their nonlinear region while the small RF signal operates within their linear region. The devices of choice for Gilbert cells can be BJTs, CMOS and GaAs FETs[13], which allow these kind of mixers to be monolithically fabricated and packaged into very small surface-mount ICs. Gilbert cells commonly work with RF frequencies up to 5.8 GHz and IF up to 2 GHz. Active mixers offer many advantages over passive mixers: they provide conversion gain instead of insertion loss, require less LO drive power, are less sensitive to port terminations (i.e., the LO input typically does not require an external buffer amplifier and the IF does not require a di-plexer), have better LO-to-IF isolation and produce less spurs. The drawback is that they have a poor IP3, a higher Noise Figure (NF) and the need of a power supply voltage and a series blocking capacitor at the RF, IF, and LO ports to remove DC components[15].

3.2.3 Mixer Performance Metrics

Commercial mixers are characterized by a set of parameters which may have different importance depending on the specific applications in which they are used. The performance of a mixer cannot be judged by just looking at its specifications, the system designer must take care of every single parameter in order to understand if the mixer is suitable for performing the required task. For instance, active mixers provide gain between the RF and IF ports, while passive mixers don't. Passive mixers and active mixers also have different power requirement

for the LO port. Moreover, some mixers have a higher dynamic range than other, which means that they can operate in linear region for higher input power levels. The main mixer metrics are listed below.

- *Conversion loss*: it can be expressed as the power level difference between the input RF signal and the output IF signal, as shown in the following equation:

$$CL = P_{RF} - P_{IF} \tag{3.5}$$

  where P_{RF} and P_{IF} are in dBm and CL is in dB. Conversion loss is the benchmark mixer metric because it correlates closely with other metrics like isolation and 1 dB compression[14].

  Active mixers have an internal amplifier in one or more of the three signal paths, when the amplifier is in the RF or IF path, it generally provides IF output power that is greater than the RF input power. Therefore, *conversion gain* is specified instead of conversion loss[18].

- *1 dB compression*: the conversion loss of a mixer is constant when the mixer works in linear region, regardless of the RF input power. This implies that if the RF power level is increased by 1 dB then also the IF power level will increase by 1 dB. This linear relationship between the RF and IF power levels does not hold anymore if the RF power level grows above a certain threshold. Hence, the 1 dB compression point can be defined as the RF power level needed in order to increase the conversion loss by 1 dB from its ideal

value. This situation is clearly shown in Figure 23. The 1 dB compression point represents the upper limit of the dynamic range and it is a measure of the mixer's linearity[14].

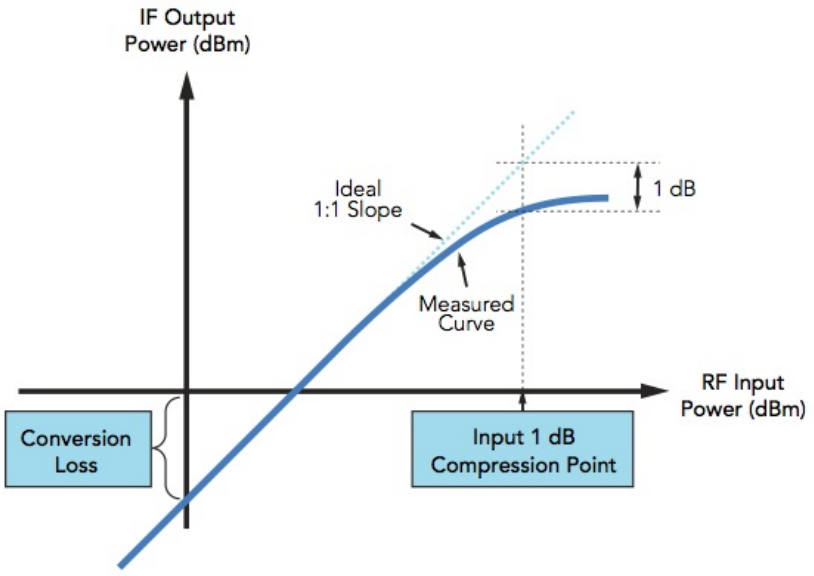

Figure 23. Graphical representation of 1 dB compression point [14].

- *Isolation*: it can be mathematically expressed as the power level difference between the input signal power on one port and the leaked power measured on another port. For instance, let's assume to apply a signal with a known frequency and power at the LO

port and to measure the power at the RF port at that frequency, then the isolation can be computed as in Equation 3.6 and it is expressed in dB.

$$P_{ISO\ (L-R)} = P_{IN\ @LO} - P_{OUT\ @RF} \tag{3.6}$$

There are three types of isolation, which are called LO-RF, LO-IF and RF-IF[14]. LO-RF isolation indicates the power leakage from the LO to the RF port: this is critical for down-conversion applications because the LO power could leak into the RF port, thus interfering with the RF amplifier or causing cross-channel interferences. LO-IF isolation indicates the power leakage from the LO into the IF port. If there is poor LO-IF isolation it is possible that the LO frequency contaminate the IF circuitry when their frequencies are close each other. Moreover, poor LO-IF isolation may cause problems in the conversion loss flatness. The last isolation metric is the RF-IF, which is not a main concern of system designers because the RF and IF powers are usually some orders of magnitude smaller than the LO power.

- *Noise Figure (NF)*: it can be expressed as the difference in dB between the noise power level at the input of the mixer and the one at the output. If the mixer is driven with a proper LO power level then the NF can be approximated by the conversion loss[15]. When talking about mixers, the noise figure denotes the lower bound in the dynamic range. For this reason it is extremely important to choose a mixer with the lowest possible conversion loss for low power applications[18].

- *Multi-tone intermodulation distortion (IMD)*: it is a form of common-mode mixing that appears when two or more harmonics enter the RF port and mix with each other and the LO signal, thus creating some distortion at the IF output. Multi-tone IMD can be a problem if the interference harmonics fall within the IF bandwidth of the receiver. This represents a theoretical upper limit on the receiver's dynamic range[18]. For instance, assume that two closely spaced signals f_{RF1} and f_{RF2} enters the RF port and nonlinearly inter modulate with f_{LO}. The relationship between the input frequencies and the third-order harmonics at the IF port are shown in Equation 3.7 and Equation 3.8:

$$Interference_1 = 2f_{RF1} - f_{RF2} - f_{LO} \tag{3.7}$$

$$Interference_2 = 2f_{RF2} - f_{RF1} - f_{LO} \tag{3.8}$$

  These interference harmonics overlap with the desired down-converted signal in frequency domain. Hence, the SNR of the output signal is degraded because no filtering can separate the interference harmonics from the desired one[14].

- *Intercept point*: the figure of merit for multi-tone performance is referred as *two-tone IMD*, or more simply by the acronym IP3. Fundamental mixing tones (i.e. $M = 1$ and $N = 1$ in Equation 3.4) grow with a 1:1 slope with respect to the RF input power, while higher order RF harmonics grow by a M:1 slope. The interference harmonics shown in Equation 3.7 and Equation 3.8 grow by a 3:1 slope, this the reason why they are called *third-order IMD products*. The situation is clearly depicted in Figure 24. The IP3 is the

point at which the input power line (with 1:1 slope) intersects the interference line (with 3:1 slope). The IP3 is a theoretical extrapolated point since a real mixer would compress before the two lines actually cross each other. However, the impact of third-order IMD products can affect the performance of a system even when the RF power level is below the 1 dB compression point[14]. For this reason it is possible to conclude that a higher IP3 level indicates a better quality mixer.

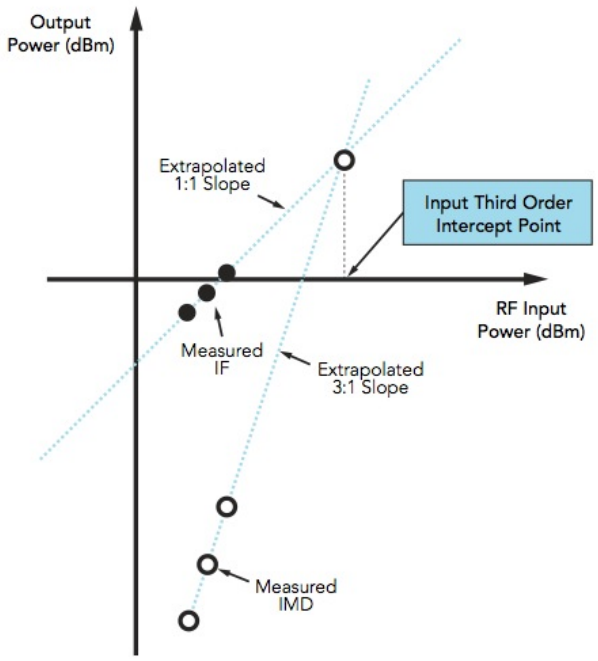

Figure 24. Graphical representation to derive input third order intercept point [14].

CHAPTER 4

FBAR FREQUENCY MONITOR DESIGN

In this chapter we are going through the details of designing a low power microcontroller-based frequency counter. First we are going to analyze the overall system's functionality, then we will go through the different sections in order to have an accurate description of what is the role of each component in the design. At the end we will analyze the PCB layouts and their components in order to understand how the design will be finally implemented on a real electronic board. The PCB layout has been carried out in CadSoft EAGLE PCB Design Software (v6.6.0).

4.1 Overall System's Functionality

The basic block diagram of the frequency counter is shown in Figure 25. We can identify and define the following functional blocks:

- *RF front-end*: The front-end section is the most challenging section of the whole system. Its role is to take a RF high frequency input signal coming from the PM sensor (in the order of 611 MHz) and reduce its frequency so that the microcontroller is able to work with the new frequency. The frequency limitation is not only dependent on the maximum frequency that the input pins of the microcontroller can handle, but also on the maximum frequency at which the input conditioning stage can operate. In order to get reliable frequency measurements we want the microcontroller to work with frequencies lower than

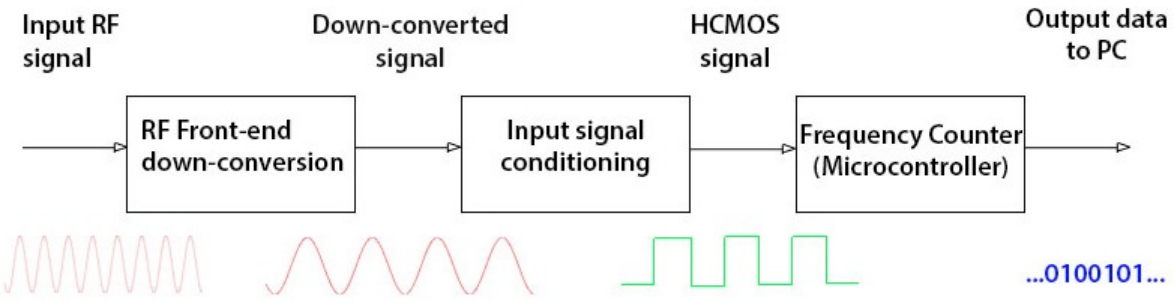

Figure 25. Block diagram of the frequency counter system.

20 MHz. This is when the down-conversion electronics come into play because the input frequency must be reduced by 580 MHz or even more, without distorting or losing the fundamental information contained in the original signal, i.e. its harmonic content.

- *Input conditioning*: The input conditioning section has the task to convert the analog input signal to a digital one so that the new voltage levels are compatible with the operating voltages of the microcontroller's input pins. What we need is a CMOS level signal in the range 0 to VCC, where VCC is the power supply voltage of the microcontroller. This is achieved by means of a *comparator* used in a *zero-cross detector* configuration. More simply, when the input signal's voltage goes above 0 then the comparator outputs a signal at a voltage VCC, when the input signal goes below 0 then the comparator outputs a signal at voltage 0. It's important to notice that the input signal must be AC coupled

in order for the comparator to properly work. We will discuss the details of the input conditioning block in Section 4.3.

- *Microcontroller section*: This is the computational core of the whole system. The microcontroller has multiple tasks: it performs the frequency counting of the input signal, it outputs data to a computer via UART protocol and it is responsible for the power management of the whole system. Minimum power consumption is achieved using low-power features embedded in the microcontroller and by implementing a smart power management for all the ICs present in the system. The power management is driven by the operation of the frequency counter, in the sense that every IC is powered up when it is strictly necessary, while it is placed in stand-by mode when not needed in order to minimize power consumption. The microcontroller itself enters *Deep Sleep mode* when it is not performing any frequency measurement and it is waken up only when a measurement has to be performed.

The microcontroller has been set to work as a direct frequency counter. The choice has been made because of limitations in the maximum clock frequency at which the microcontroller can work with an external oscillator. As we already discussed in Section **??**, reciprocal counters are the best choice for measuring frequencies lower than the time base frequency, and work best for low frequency measurement. In this case, the input frequency that we are going to measure can go up to 17 MHz, which is higher (or too much close) to the external time base frequency. In conclusion, the direct counting approach is the most effective and simple to implement technique. The PCB layout for the two devices is shown in Figure 27 and Figure 26.

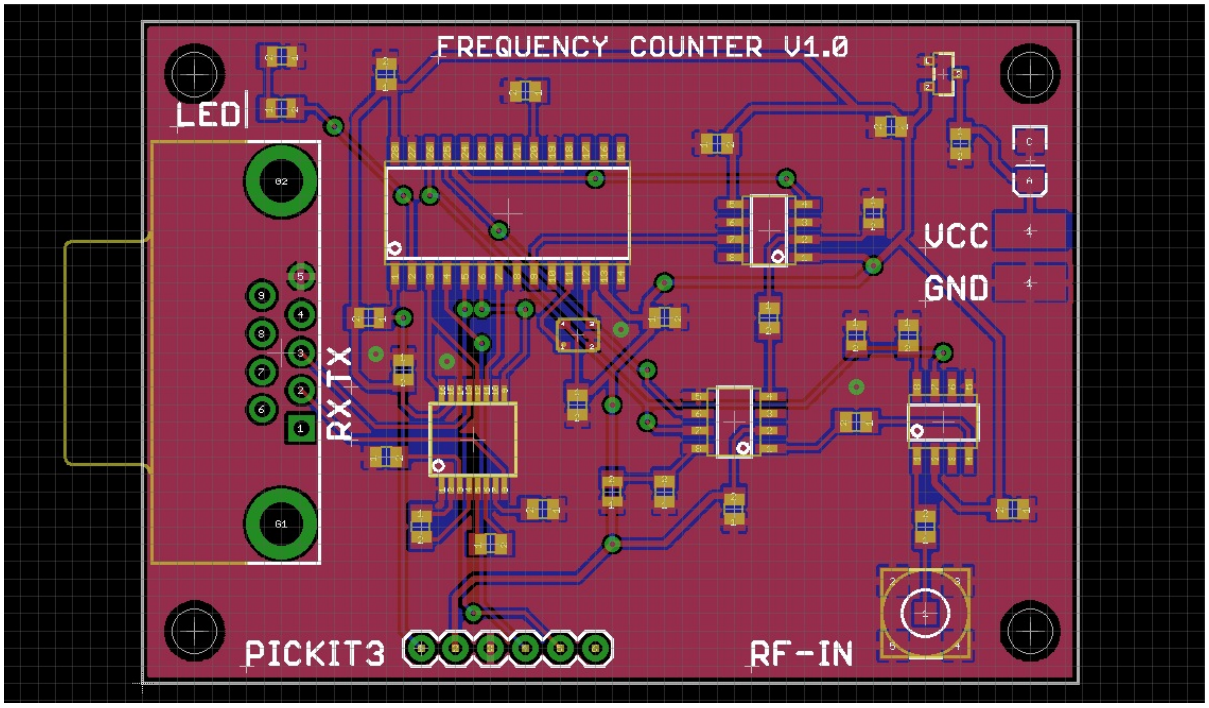

Figure 26. PCB layout of the frequency counter with down-converting prescaler.

The designed devices have been implemented on standard 2-layers PCBs with FR-4 substrate, 0.062 inches thickness and 1 oz copper plate.

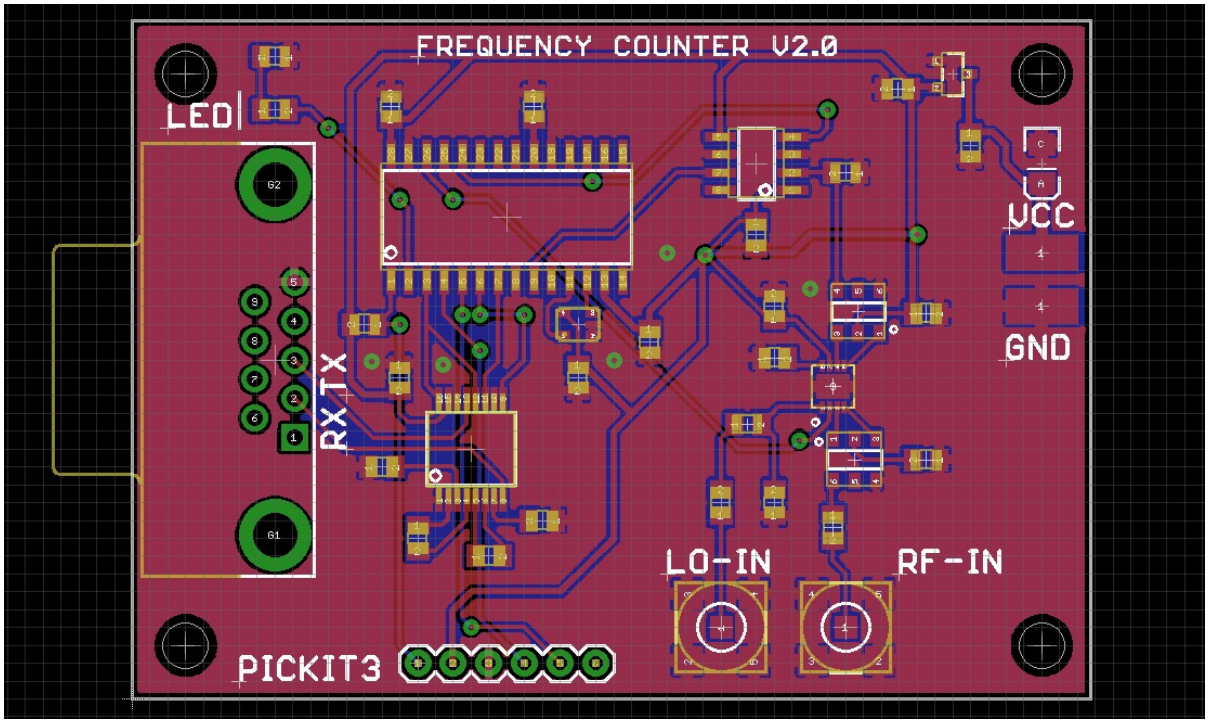

Figure 27. PCB layout of the frequency counter with down-converting mixer.

4.2 Microcontroller Section

The microcontroller and all its related components are shown in the schematic of Figure 28, while the PCB layout is shown in Figure 30. Figure 29 and Figure 31 show the power supply section with the 3.3V voltage regulator that feeds the whole system. The chosen microcontroller for this design is the PIC24FJ64GB002, a 16-bit MCU Flash microcontroller manufactured by Microchip Technology Inc®.

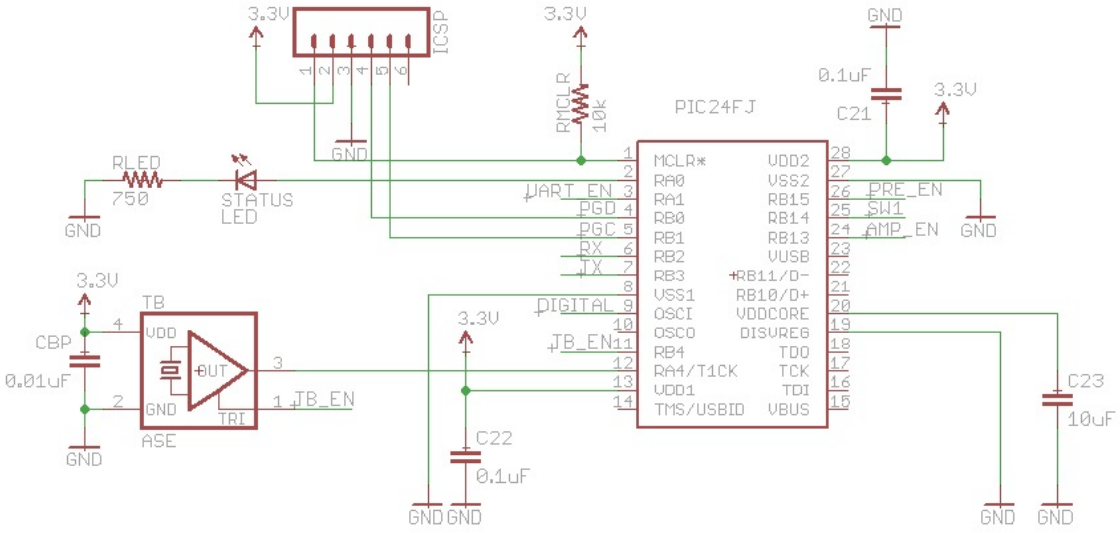

Figure 28. Microcontroller section schematic.

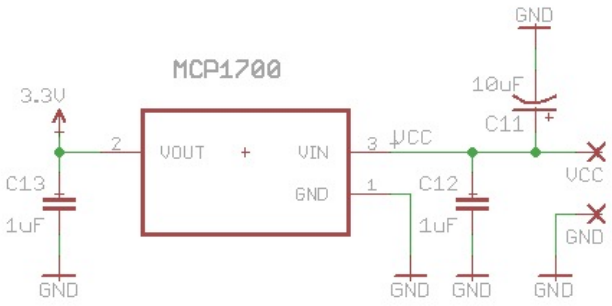

Figure 29. Power supply section schematic.

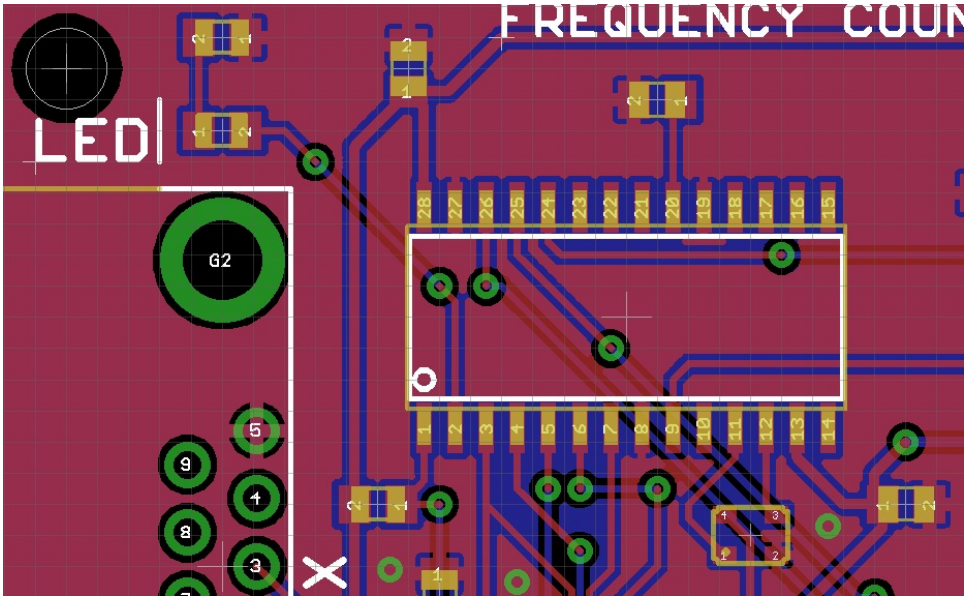

Figure 30. Microcontroller PCB layout.

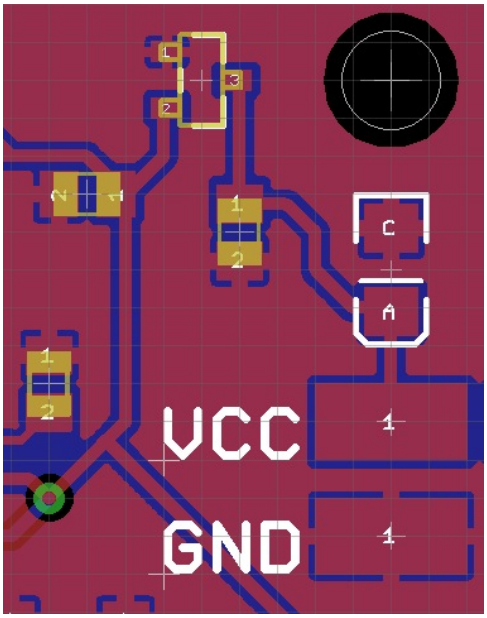

Figure 31. Power supply PCB layout.

The schematics of Figure 28 and Figure 29 show all the basic connections and components that the PIC needs in order to properly work:

- The ICSP header, used for connecting the programmer to the microcontroller (the programmer is a PICKit3 manufactured by Microchip Technology Inc®).
- The MCP1700, a CMOS LDO voltage regulator able to deliver up to 250 mA of current while drawing a 1.6 μA quiescent current. The maximum input voltage is specified at 6.0V, therefore it represents a good device for battery-powered systems. In our design the MCP1700 provides the power to the whole system, with an output voltage of 3.3V. The

power supply is provided by a battery pack situated under the board, which contains 3 AA batteries for a total input voltage of 4.5V.

- The ASTX-H11, a TCXO manufactured by Abracon Corporation®, is used as the accurate Time Base for the frequency measurement. This TCXO has been chosen for it's good price and availability, as well as high frequency stability, low power consumption (maximum 4 mA of supply current) and small SMD form factor. It has a HCMOS output which makes it perfectly suitable for this kind of applications. Another very useful characteristic of this is TCXO is the ability to put it into *Tri-State mode*, which allows the output port to assume a high impedance state, thus removing the output from the circuit. In Tri-State mode the power consumption is reduced to a minimum.
- The Status LED is used to signal to the user when a frequency measurement is being performed. For instance, if a frequency measurement is set to last 1 second then the LED will be on for 1 second, and it will be turned off as long as the PIC runs in sleep mode. If there is no input signal or the input signal's amplitude is lower than the sensitivity of the counter, the Status LED will remain powered on to signal to the user that the measurement cannot be performed because of a problem with the input signal.

Although the PIC is provided with several peripherals, we are only interested in few of them which are three timers and the UART module. The PIC24F is provided with five 16-bit timers called TMR1, TMR2, TMR3, TMR4 and TMR5. We are not going to use TMR4 and TMR5, therefore they will be disabled as well as all the other unused peripherals. The TMR1 module is a 16-bit timer that can operate in three modes: Timer, Synchronous Counter and Asynchronous

Counter. What we are interested in is the third mode of operation, which is the Asynchronous Counter. TMR1 is set to count rising edge events on the pin number 13, which is called T1CK. As we can see from Figure 28, the Time Base's output is connected to T1CK. It's clear that TMR1 will be responsible for generating the accurate gate time during which the frequency measurement will be performed. The gate time is controlled via interrupts, and it is defined by the user. TMR1 is provided with a period register called PR1, as we can see in Figure 32, which is used to set the value at which we want TMR1 to overflow. A comparator is present

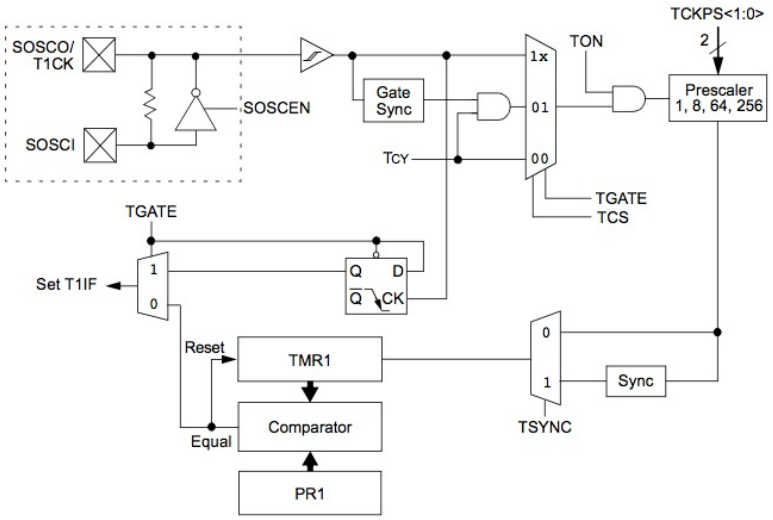

Figure 32. 16-bit Timer1 module block diagram.

between TMR1 and PRD1, the comparator is used to signal when TMR1 overflows by means

of a control bit called T1IF. This is one of the bits present in the *interrupt controller register map*: if interrupts are enabled for TMR1 and T1IF is set then an interrupt will be raised when TMR1 overflows. In other words, we exploit the interrupt routine in order to understand when the measurement is over. Moreover, TMR1 is provided with a modulo-1/8/64/256 prescaler, which is used to reduce the input clock frequency coming into the TMR1 module.

In order to set a desired gate time it's necessary to take into account the clock frequency and perform an easy computation. The value to put into PRD1 is computed by means of Equation 4.1:

$$PRD1 = \frac{t_g \cdot f_{CLK}}{Prescaler\ Value} \tag{4.1}$$

Where f_{CLK} is the frequency of TMR1's source clock (which in our case is the ASTX-H11), t_g is the desired gate time expressed in seconds and $Prescaler\ Value$ is the division factor of the prescaler associated to TMR1. In our design we are using a 16 MHz TCXO as a source clock for TMR1, and the prescaler is set to modulo-256. If we want a gate time of 1 second then the value to put into PRD1 will be:

$$PRD1 = \frac{1 \cdot 16 \cdot 10^6}{256} = 62500 \tag{4.2}$$

Once we set $PRD1 = 62500$ then TMR1 will overflow when it reaches the value 62500. This is going to happen after 1 second from when TMR1 is started, since we decided that our gate

time is $t_g = 1\ s$. The upper-bound in the time base's frequency is given by the maximum value that TMR1 can reach multiplied by the maximum prescaler's divide ratio:

$$f_{TB_{max}} = (2^{16} - 1) \cdot 256 = 16.77696\ MHz \tag{4.3}$$

Hence, no oscillator faster than 16.77696 MHz can be used for this design. The lower the external clock frequency, the higher gate time we can get. For instance, a 8 MHz time base will let us generate gate times up to 2 seconds, or even longer gate times for lower clock frequencies. The other modules we are interested in are TMR2 and TMR3, which are 16-bit registers that can be combined together in order to be used as a single 32-bit timer, called TMR2/3. When used in 32-bit configuration they can operate in three modes: 32-bit timer or 32-bit synchronous counter. We are interested in the third mode of operation, which is the 32-bit synchronous counter. The block diagram of TMR2/3 is shown in Figure 33. TMR2/3 has the fundamental task of counting our input frequency, which is of course the down-converted signal coming from the input conditioning section. Since TMR2/3 can only operate as a synchronous counter, i.e. it can only count the internal clock cycle and no external one, the input signal must be given to a clock port of the PIC, which in this case is the OSCI port at pin 9, as shown in Figure 28. This implies that the input signal is used as a clock source for our system but, as we will see later, this doesn't affect code execution since no instructions are executed while the microcontroller is performing the frequency measurement. The period register PRD2/3 has the exact same functionality as PRD1 for TMR1. In this case we want TMR2/3 to overflow

when it reaches the maximum possible value, even though overflow will never happen since the maximum value that a 32-bit counter can reach is $2^{32} = 4294967296$, which would represent a frequency of about 4.3 GHz.

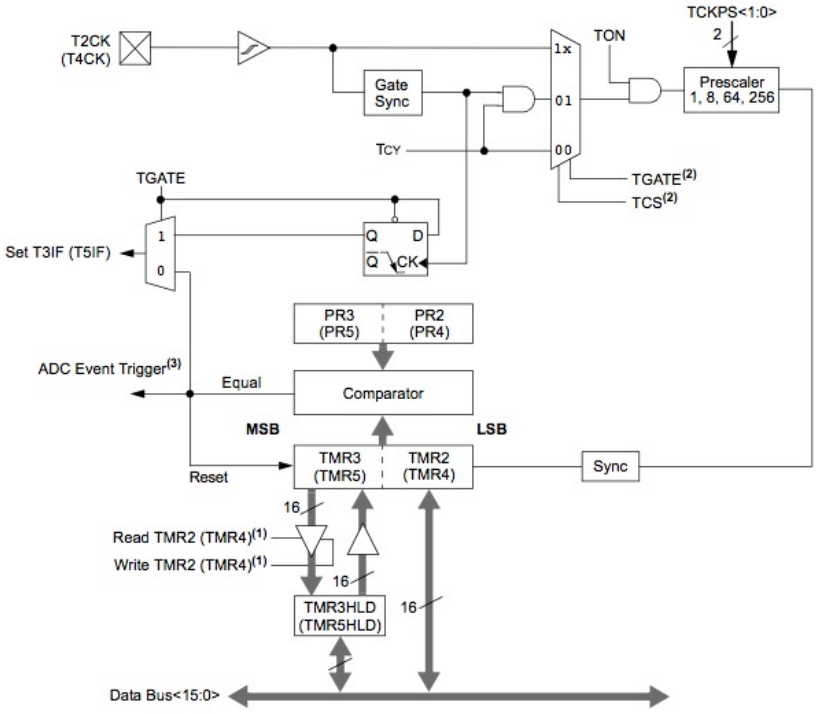

Figure 33. 32-bit Timer2/3 module block diagram.

The last important thing to discuss about TMR2/3 is that the instruction cycle for a PIC24F is 2 clock cycles, therefore the system operating frequency is $F_{cy} = F_{osc}/2$. This implies that

TMR2/3 will count the input frequency divided by 2. This is the same of having a modulo-2 prescaler in the input signal's path. As a consequence, the resolution of a measurement decreases by a factor of 2 for the same gate time, i.e. from ±1 Hz down to ±2 Hz for a 1 second gate time. This has to be carefully taken into account in the design stage, for instance let's assume that we are using a modulo-64 prescaler in order to down-convert the RF input signal; the resulting resolution for a 1 second gate time will be ±64 Hz, as we discussed in Section 3.1, but since the signal is further divided by 2 than the final resolution will be ±128 Hz. The work-around for bringing the resolution back to its original value consists in doubling the measurement time. This is not strictly needed if the final resolution is acceptable by the user's point of view. We will discuss the tradeoff between resolution and power consumption in Chapter 6.

4.3 Input Conditioning Stage

In order to translate the voltage levels of the input signal to the CMOS level needed by the input pin of the PIC we make use of a *comparator*. The simplest form of a comparator is a high-gain differential amplifier which is not used with negative feedback. A comparator can be made with an op-amp, which can go into positive or negative saturation depending on the difference of the two input voltages. Hence, the basic function of a comparator is to determine which one of its own two inputs has the larger voltage. Even if the two inputs differ by a fraction of a mV, the comparator will always go into saturation because its open-loop gain typically exceeds 100000. A comparator can be implemented by emploiyng an ordinary op-amp or a particular IC specifically designed to be used as a comparator, with very fast response. The output circuit

of a comparator is more flexible than the one of an op-amp because usually comparators have an open-collector output with grounded emitter, while op-amps use a push-pull output stage to swing between the supply voltages. It is enough to provide the output of the comparator with a pull-up resistor, connected to an external voltage, in order to get an output swing from V_{DD} to ground. The basic comparator is shown in Figure 34.

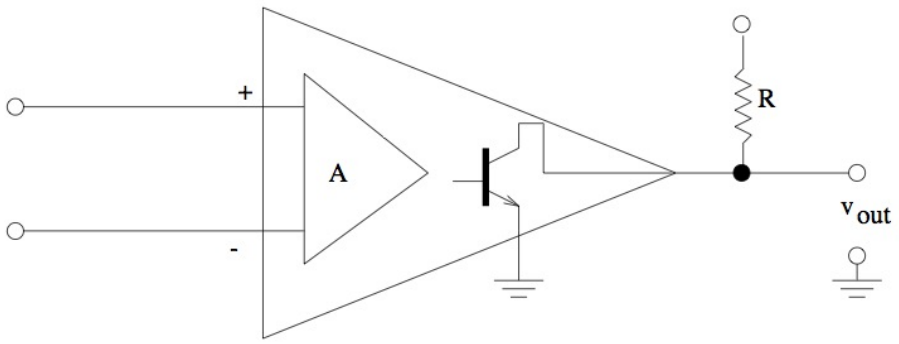

Figure 34. Basic comparator model.

If $v-$ is connected to ground and the input signal is applied to $v+$ then the output swings from V_{DD} to ground when the input signal goes negative. In this case the comparator converts an analog input signal into a digital output. This is equivalent to a 1-bit analog to digital converter (A/D or ADC). The external pull-up resistor completes the comparator's output circuit

by providing a load resistor to the collector of the output transistor. The value of the resistor is not critical because the output operates as a saturated switch, therefore values between a few hundreds of ohms and a few thousands of ohms are typical. Small values improve the immunity to noise and the switching speed, at the expense of a higher power dissipation. Comparators are never used with negative feedback because they are not stable in this configuration. Usually comparator circuits employ positive feedback in order to ensure that only the two extreme output states are utilized and nothing in between. Moreover, without negative feedback there is no need to do compensation, i.e. there is more gain at high frequency, which translates in a faster response. Finally, it is possible to optimize comparators for speed at the expense of linearity.

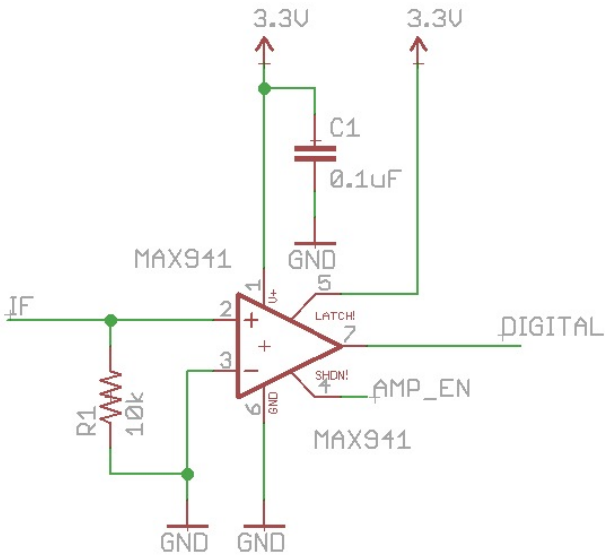

Figure 35. MAX941 in non-inverting comparator configuration.

Comparators, like op-amps, are readily available as ICs chips such as the MAX941 that we used in our design. The MAX941 is used as a non-inverting comparator and its schematic is shown in Figure 35. As we can see, the power supply goes from $V_{DD} = 3.3V$ to ground. This means that the digital output will swing from 0 to 3.3V.

The MAX941 contains a current-driven output stage, as shown in the model of Figure 36. This device is suited for direct interface with CMOS or TTL logic because its output pulls to within 0.4V of either supply rail without the need of an external pull-up resistor.

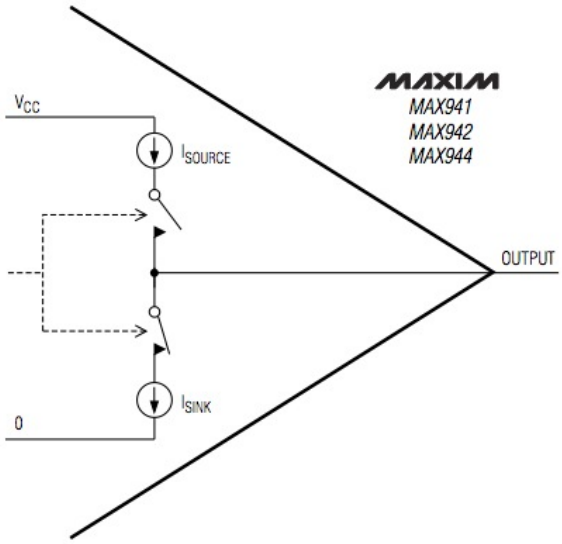

Figure 36. MAX941 output stage circuitry.

The MAX941 is provided with an internal hysteresis, which ensures a glitch-free output switching even with noisy or slow input signals. The hysteresis window is shown in Figure 37, where the V_{TRIP} points represents the boundaries of the differential input voltage required in order for the output of the comparator to change state.

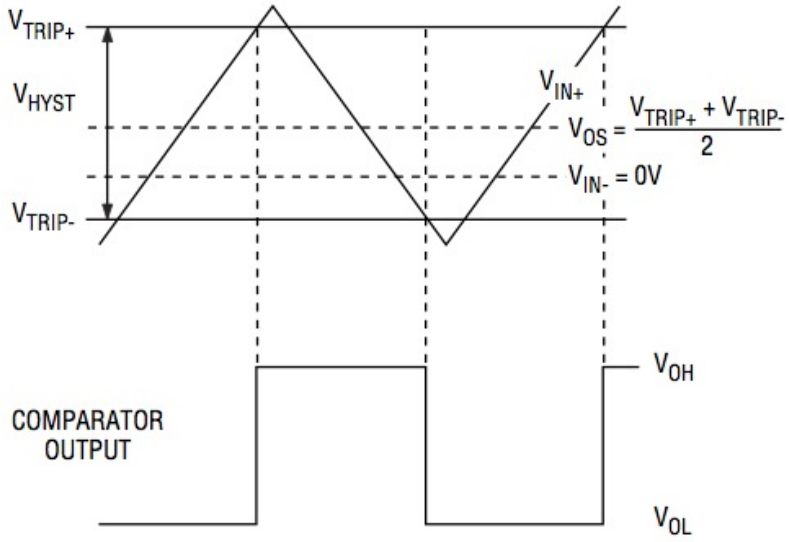

Figure 37. MAX941 input and output waveforms, with hysteresis.

The width of the hysteresis windows can be expressed as the difference between the upper and lower V_{TRIP} points. V_{OS} represents the center of the hysteresis zone. The typical value for V_{TRIP} is 1mV. This is very useful because we don't want the comparator to trigger on noise if there is no input signal coming from the RF front-end section. If the input signal's amplitude is too small or if there's no input signal, the frequency counter simply get stuck and the status LED will remain on in order to signal to the user that the measurement can't be performed because of the absence of a valid input signal.

The PCB layout for the MAX941 comparator is shown in Figure 38, where pin 2 is the input

and pin 7 is the output which is fed to the PIC24F. Pin 4 is the shut-down signal, which is driven by the microcontroller.

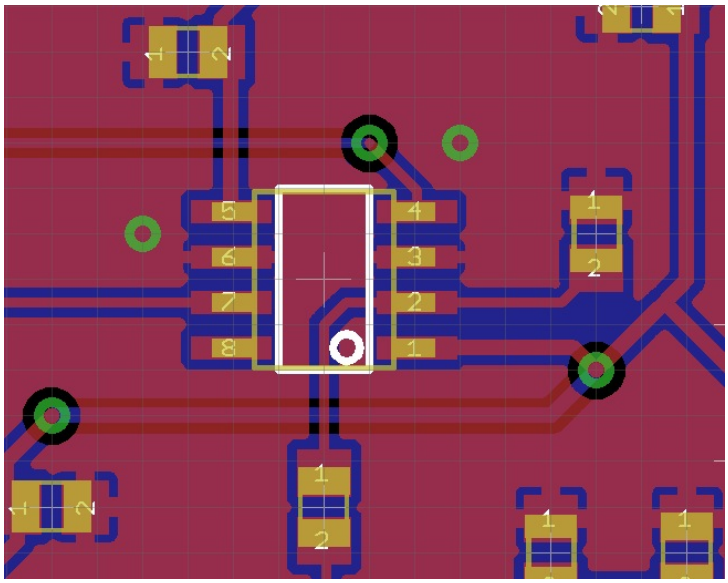

Figure 38. MAX941 PCB layout.

4.4 UART-RS232 Section

UART stands for Universal Asynchronous Receiver Transmitter, it is a hardware device used to translate data between a parallel representation to an asynchronous serial one, or viceversa. Most modern computers employ a serial port that makes use of standard protocol known as RS-232, which is a specific type of UART that sends out data at voltages different from the usual

TTL levels. PIC24F microcontrollers usually have 2 UART modules called UART1 and UART2. These two modules are controlled by several registers such as the UxBRG, the UxMODE and the UxSTA. The UxBRG establishes the baud rate of the communication by means of a clock prescaler. The UxMODE is used to turn the module ON and OFF. The UxSTA is the status register, which can be used to check all the current conditions of the module. A data buffer for both transmission and reception is also present. It is possible to load up to 4 bytes of data in the transmission buffer, that will be sent one at a time by the module. Also the receiver buffer is 4 bytes in size. The hardest part is establishing the timing. The first thing to figure out is the instruction clock frequency F_{CY} before proceeding. In the PIC24F family, F_{CY} is equal to the system's clock frequency divided by 2, as already explained in Section 4.2. Once F_{CY} has been computed, the register called UxBRG has to be updated in order to determine the correct baud rate for the UART module. It is possible to set the module in high speed or standard speed mode. For this particular application we can safely use the module in standard speed mode by clearing the BRGH bit of the UxMODE register. The UxBRG value must be computed using Equation 4.4 for standard speed mode:

$$BRGx = \frac{F_{CY}}{16 \cdot Baud\ Rate} - 1 \tag{4.4}$$

In our design we have have a clock frequency of $F_{osc} = 8\ MHz$ provided by the internal FRC oscillator, with no PPL, and no clock divide. The Baud Rate has been chosen to be 9600, therefore the content of the BRGx register is computed as in Equation 4.6:

$$F_{cy} = \frac{F_{osc}}{2} = \frac{8 \cdot 10^6}{2} = 4 \cdot 10^6 \ Hz \tag{4.5}$$

$$BRGx = \frac{4 \cdot 10^6}{16 \cdot 9600} - 1 = 25.04 \simeq 25 \tag{4.6}$$

The value is rounded to 25 because the register UxBRG works with integers only. It doesn't make any significant difference because the value of 25 only means that the timing will be off by a small amount, not enough to consistently get an error.

Now we are going through the configuration of some of the bits in the UxSTA status register, which controls transmission and reception. The UTXISEL bits control how an interrupt is handled during transmission. UTXISET is set to binary 10 because we want interrupts to signal when the transmission is completed, and that the buffer is empty. Moreover we need to control how the PIC24F will notify when a byte has been received. This is possible by means of the URXISEL bits. By setting the URXISEL bits to binary 00 is it possible to process a value as soon as it is received by the PIC24F: this results in an interrupt each time a character is received. In order to avoid transmission errors and to be completely sure that the PIC has sent out all the data before entering Deep Sleep, we must wait that the Transmit Shift Register is empty. This is signaled by the TMRT bit: we know that the Transmit Shift Register is empty when TMRT is set to 0 by the PIC. The UTXBF bit indicates whether an empty spot is present or not in the transmission buffer: we need to wait for it to be set to 1 by the PIC24F before proceeding in sending out a new data. For what concerns reception, we set URXISEL to raise an interrupt each time a byte is received. The interrupt is raised when the receive interrupt

flag bit (IFS0.U1RXIF) is set to 1 by the PIC24F. Finally, the TXEN bit is used to turn the transmission ON and OFF.

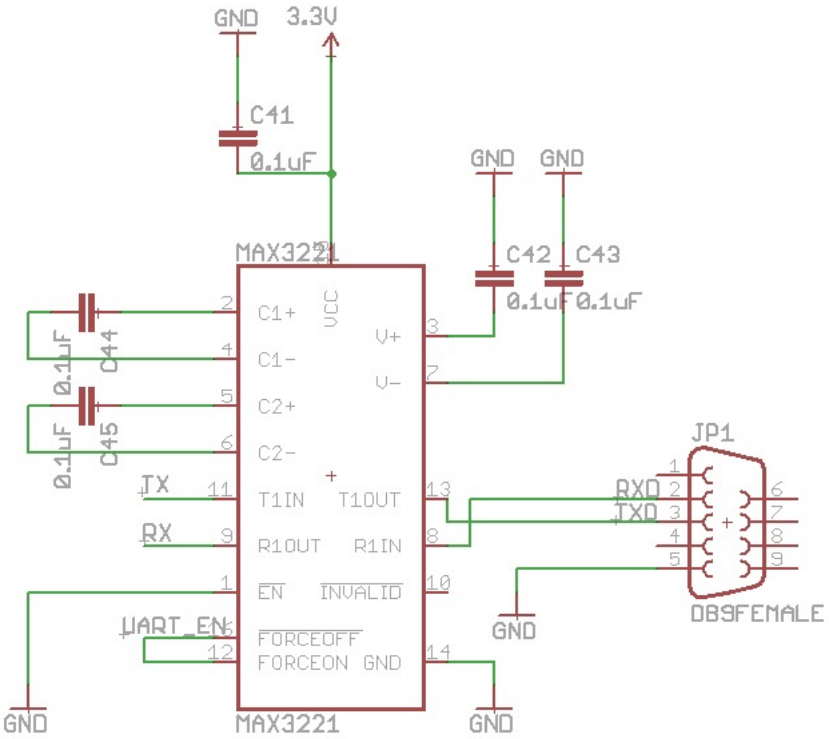

Figure 39. Typical operating circuit with MAX3221 transceiver.

The schematics for the UART-RS232 section is shown in Figure 39. This MAX3221 IC uses four 0.1μF capacitors (C42, C43, C44, C45) to operate. C41 is a decoupling capacitor for the power supply that must be placed as close as possible to VCC and GND pins of the IC.

JP1 is simply the DB9 connector, in our case the female version is mounted on the PCB. The UART_EN signal is used to power or shut-down the MAX3221 IC and it is controlled by the PIC, it is connected to pin 3 (RA1). The lines T1IN and R1OUT are respectively connected to pins 6 (RB2) and 7 (RB3) on the PIC, thus RB2 acts as a receiver and RB3 as a transmitter. Finally, T1OUT and R1IN pins from the MAX3221 are respectively connected to pin 3 (TXD) and pin 2 (RXD) of the DB9 connector.

The PCB layout for the MAX3221, as well as the DB9 connector, is shown in Figure 40.

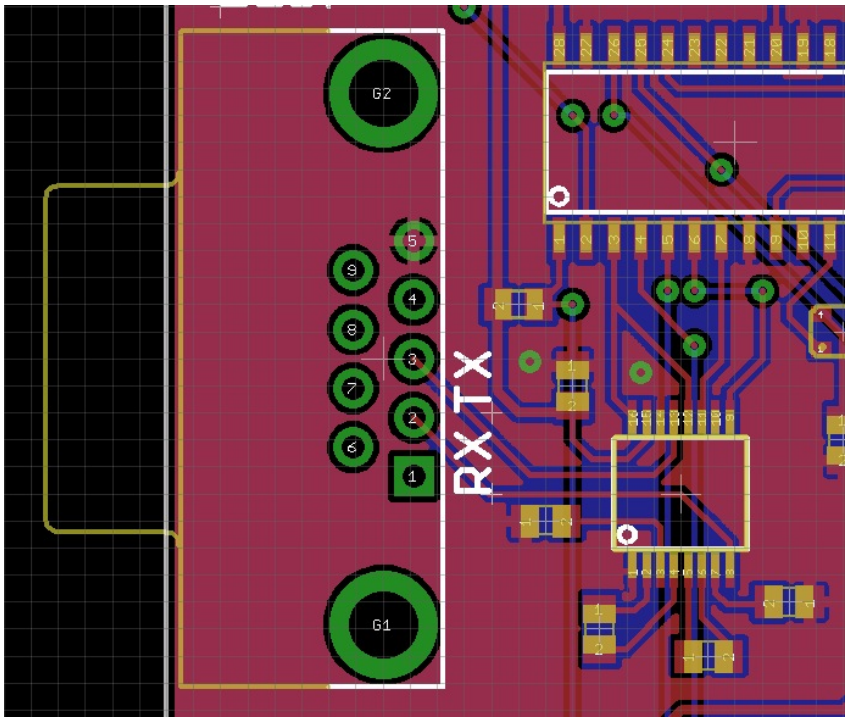

Figure 40. MAX3221 PCB layout.

4.5 Prescaler Front-End Section

The prescaler front-end section has been designed in two different ways, the first design implements a single MC12080 5V prescaler as shown in the schematic of Figure 41, while the second design implements two MC12093 3.3V prescalers in cascade configuration as shown in the schematic of Figure 42. Both the MC12080 and the MC12093 are manufactured by ON Semiconductor®.

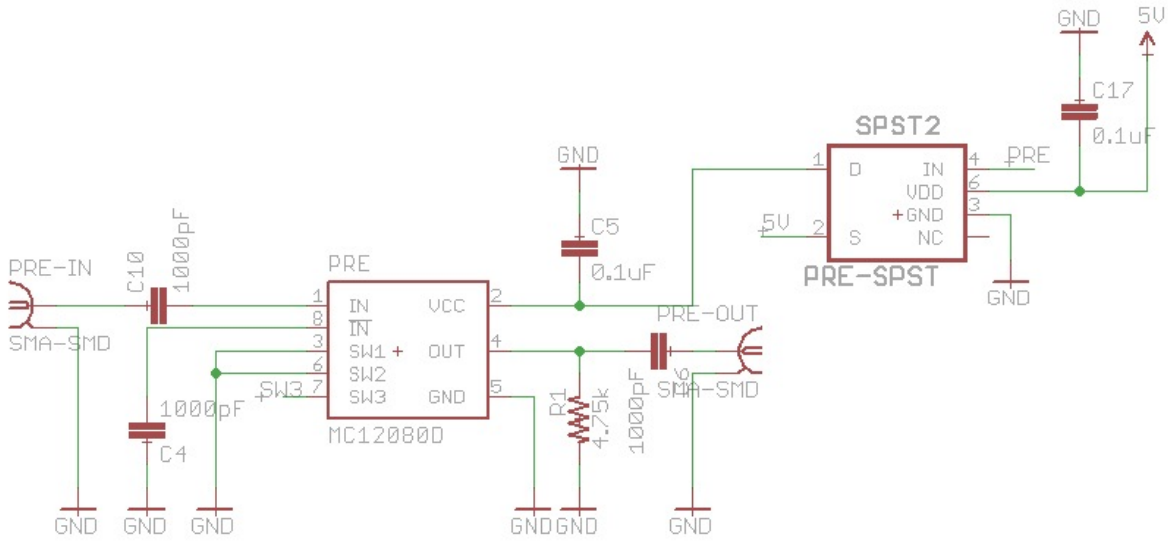

Figure 41. Typical operating circuit with MC12080 prescaler.

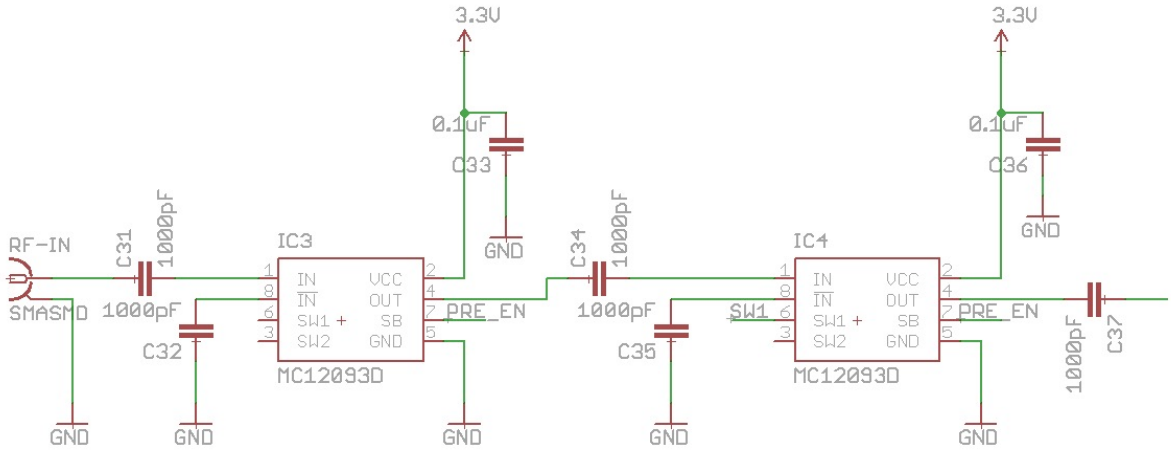

Figure 42. Composite prescaler made with two MC12093 ICs in cascade configuration.

The MC12080 is a single modulus prescaler with different divide ratios equal to 1:10, 1:20, 1:40 and 1:80 for low power frequency division of input signals up to 1.1 GHz. The control pins SW1, SW2 and SW3 select the desired divide ratio between 1:10, 1:20, 1:40 and 1:80.

The MC12093 is a single modulus prescaler for low power frequency division of input signals up to 1.1 GHz. The control input pins SW1 and SW2 select the required divide ratio between 1:2, 1:4 and 1:8. The IC is also provided with a stand-by feature that disables the prescaler in order to reduce current drain down to 50 μA when the standby pin SB is driven at a LOW logic level.

The choice of passing from a 5V prescaler to a 3.3V one is due to the fact that the control

signals for the prescalers have logical high equal to V_{DD}, hence in order to drive the control signals of the 5V prescaler we need a digital signal at 5V level. The microcontroller operates at 3.3V and its digital pins are able to generate signals at voltage level up to 3.3V, thus making the integration between the PIC24F and the MC12080 more difficult with respect to the MC12093. The drawback is that two prescalers are required because a single MC12093 has a maximum divide ratio equal to 1:8, but our design requires a minimum divide ratio equal to 1:32 in order to down-convert a 611 MHz input signal to a one with a frequency lower than 20 MHz. The two prescalers in series let the user to choose between divide ratio of 1:4, 1:8, 1:16, 1:32 and 1:64. As we said, we need a divide ratio at least equal to 1:32 or 1:64, therefore all the other ratios are ignored and some control ports are simply left open because they are not used.

Let's analyze the schematics in detail. The MC12080 shown in Figure 41 needs 1000pF AC coupling capacitors at the input ports (IN, and $\overline{IN}$) and the output port (OUT). C5 is a bypass capacitor for the power supply, while R_1 is an external load resistor required to terminate the output. The data-sheet suggests to use a 3.3kΩ resistor in order to get 1.1mA output current at divide ratio 1:40, or a 6.2kΩ resistor to get 0.57mA at divide ratio 1:80. The chosen value is 4.75kΩ, which is simply the average between the two. It has ben chosen to be the average because the prescaler can be used either in 1:40 or 1:80 mode and with a 4.75kΩ resistor we get slightly less current at 1:40 and slightly more current at 1:80, which is a nice tradeoff and it doesn't compromise the prescaler's operation. The logic control signals to select the divide ratios are shown in Table II. We only need 1:40 and 1:80, therefore SW1 and SW3 are hard-wired to ground and SW3 is externally driven. The MC12080 is not equipped with an enable

TABLE II

FUNCTION TABLE FOR MC12080

SW1	SW2	SW3	Divide ratio
L	L	L	1:80
L	L	H	1:40
L	H	L	1:40
L	H	H	1:20
H	L	L	1:40
H	L	H	1:20
H	H	L	1:20
H	H	H	1:10

or stand-by port, therefore an ADG802 SPST switch by Analog Devices has been added to design in order to switch off the prescaler when required. The switch is normally open and it needs a logic high level signal at the port IN to be closed. The input signal is the 5V V_{DD} and it is connected to the Source port (S) while the output signal is the 5V power supply for the prescaler, connected to the Drain port (D). The control signal for the IN port is called PRE_EN and it is provided by the microcontroller's pin 26 (RB15) as shown in Figure 28. The minimum voltage level to drive the IN port high is 2V. The MC12093 shown in Figure 42 also needs 1000pF AC coupling capacitors at the input ports (IN and $\overline{IN}$) and the output port (OUT). No external load resistor is required, therefore the output from the first prescaler is directly connected to the input port of the second one. Again, C33 and C36 are power supply's bypass capacitors. The MC12093 is equipped with a stand-by port that lets the user to put

TABLE III

FUNCTION TABLE FOR MC12093

SW1	SW2	Divide ratio
L	L	1:8
H	L	1:4
L	H	1:4
H	H	1:2

the IC in stand-by when the SB port is driven with a logical low level. Obviously, the SB port is controlled by the microcontroller and it is driven with the PRE_EN signal. The logic control signals to select the divide ratios are shown in Table III. The first prescaler is fixed to a divide ratio of 1:8, therefore SW1 and SW2 are left unconnected. The second prescaler can toggle between 1:4 and 1:8 in order to get an overall divide ratio of 1:32 and 1:64, respectively. On the second prescaler, SW2 is left unconnected and SW1 is connected to pin 25 (RB14) of the microcontroller. The layout for the 5V prescaler is shown in Figure 43, while for the 3.3V one is shown in Figure 44.

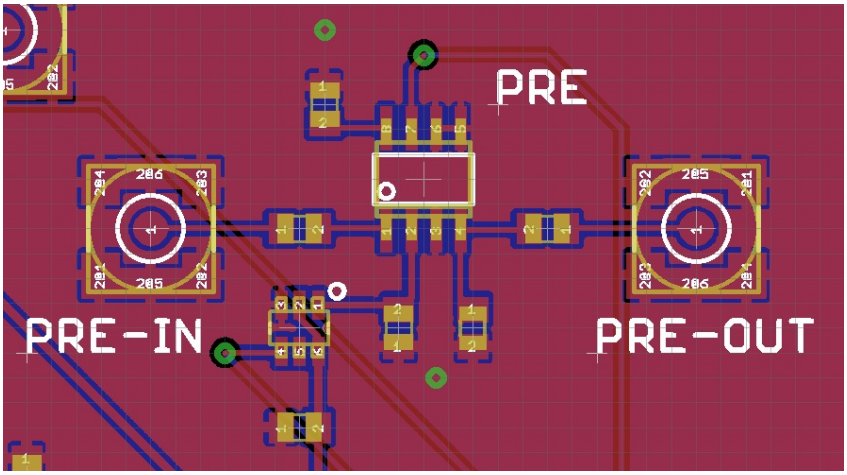

Figure 43. PCB layout for MC12080 prescaler.

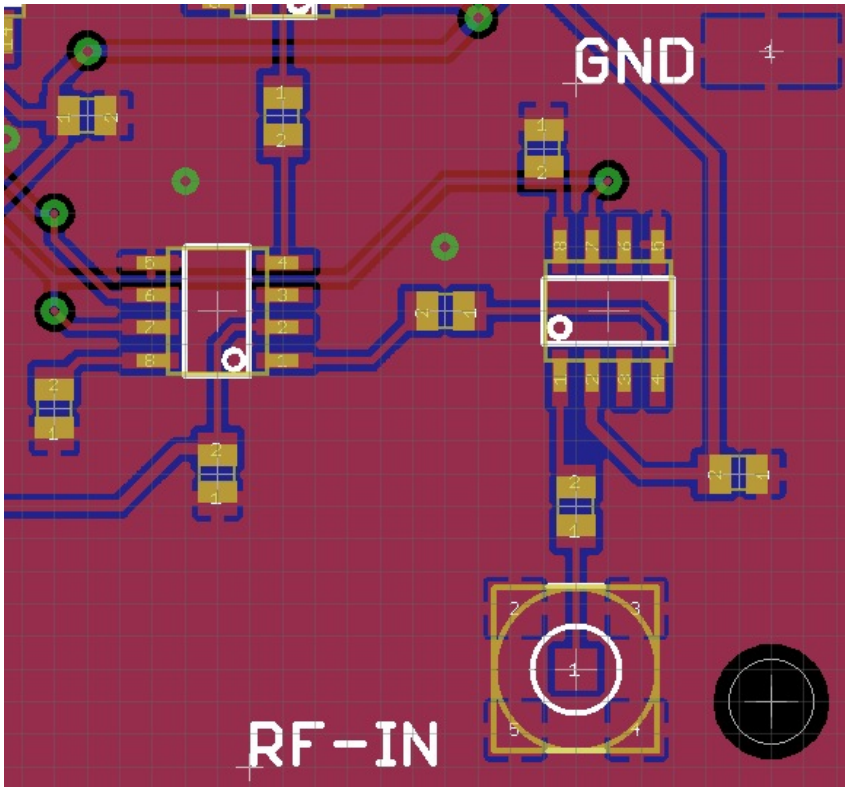

Figure 44. PCB layout for MC12093 prescaler.

4.6 Mixer Front-End Section

The mixer front-end section, as well as the prescaler front-end, has been designed in two different ways. Both designs exploit active mixers instead of passive ones. This is due to the fact that active mixers have a conversion gain rather than a conversion loss, they can be found as very small and cheap ICs that consume small power and they can work with lower LO level with respect to passive mixers. As we discussed in Section 3.2.2 and 3.2.3, active mixers

have a lower IP3 level and higher NF with respect to passive mixers, therefore they have a lower input linearity. However, we are not interested in having a highly linear device for this particular application, therefore IP3 and NF can be sacrificed for a cheaper device which also offers a conversion gain. The first design implements a LT5522 5V active mixer as shown in the schematic of Figure 45, while the second design implements a LT5560 3.3V active mixer as shown in the schematic of Figure 46. Both mixers are manufactured by Linear Technology®.

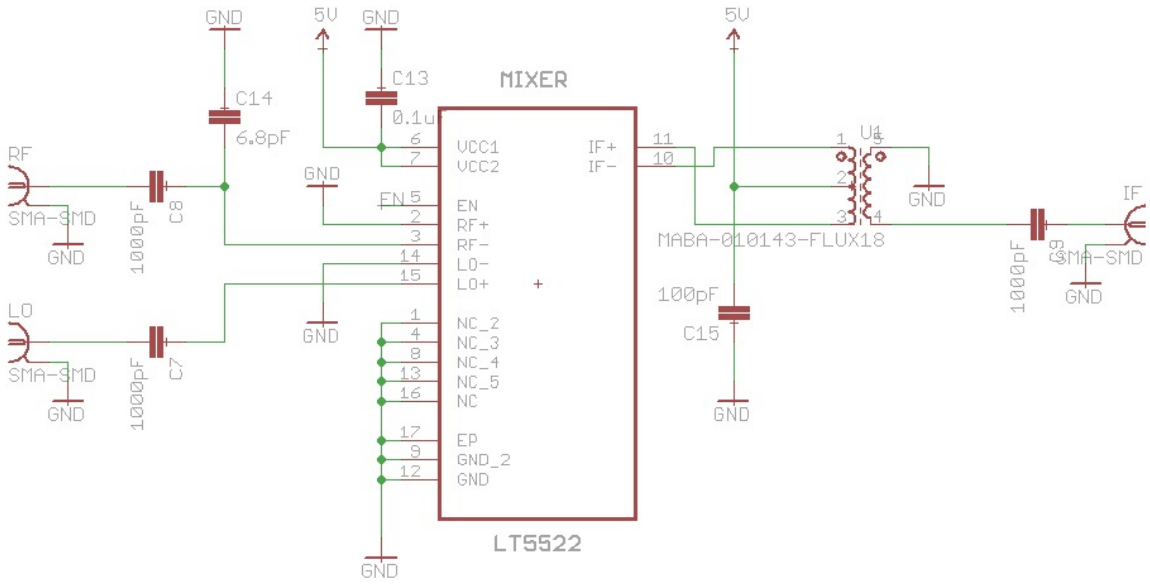

Figure 45. Schematic for down-converting application (1MHz-20MHz IF) with LT5522.

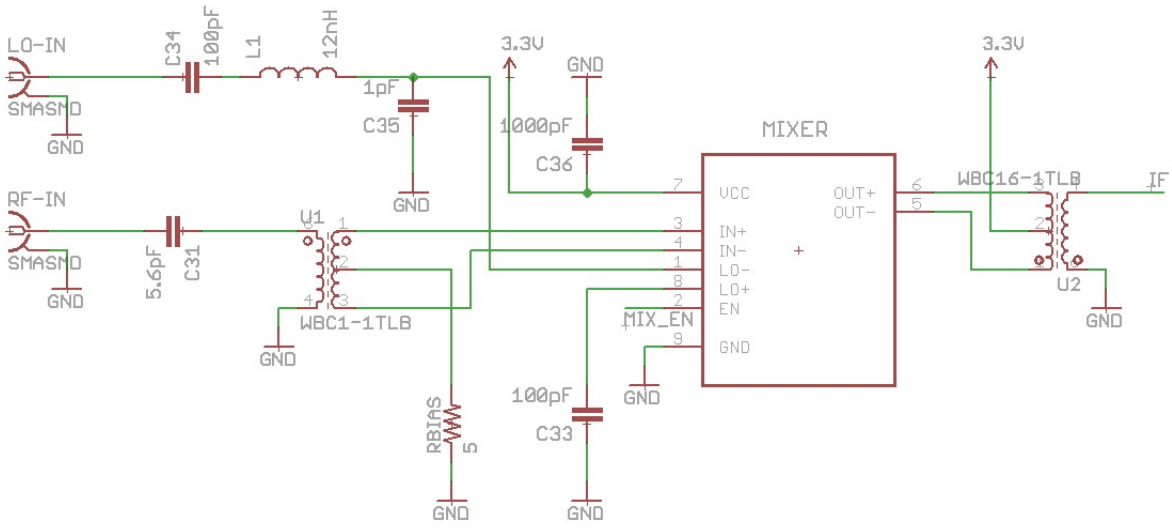

Figure 46. Schematic for down-converting application (1MHz-20MHz IF) with LT5560.

The LT5522 has been used and tested in the prototype version of the frequency counter, however the final device has been designed with the LT5560 because of its lower operating voltage and much lower power consumption. The LT5560 can work with frequencies up to 4 GHz and it is made of an active double-balanced mixer, a common-base input buffer amplifier and bias/enable circuits. The power supply current of this mixer can be tuned in order to find the right trade-off between IIP3 performance and DC current: it can be simply adjusted by the proper choice of an external resistor and it ranges from 4mA to approximately 13.5mA. The LT5560 mixer draws a significantly lower power supply current with respect to the LT5522,

this is the main reason that pushed us to change the mixer for the final design. The drawback is that it requires more passive components and two transformers instead of one, in order to perform impedance matching. The LT5560 represents a better solution because of its very low power consumption and lower operating voltage, which makes the integration easier with a 3.3V system such as the PIC24F. Impedance matching of inputs and output ports of the LT5560 is explained in the following pages.

- *RF input port*: Figure 47 shows a simplified schematic of the RF port and an example topology for the external impedance matching circuit. Each input pin (indicated as pin 3 and 4) sources up to 6mA of DC current, which can be reduced by adding the resistor R1. The center-tap of a transformer provides the DC ground path, as shown. In order to get a 600 MHz match we can avoid to use the inductors L1 and L2 and we can put C1 in series with the input port rather than shunt to the transformer. Figure 46 shows our implementation, with a 5.6pF ceramic capacitor (C31) in series with the primary of a 1:1 transformer. C31 also acts as an AC-coupling capacitor. The 1:1 transformer chosen for this design is a WBC1-1TLB manufactured by Coilcraft®.

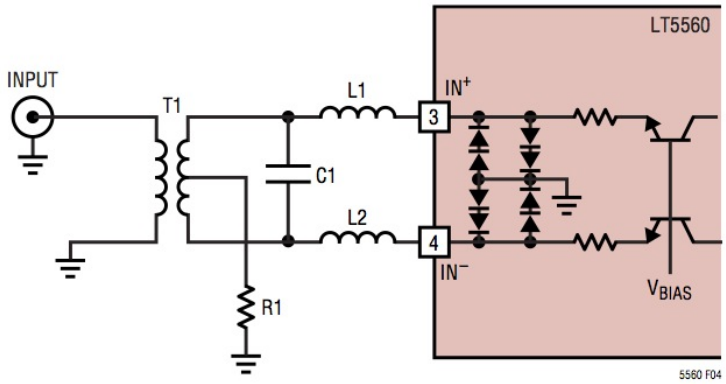

Figure 47. RF input schematic for LT5560 [20].

- *LO input port*: Figure 48 shows a simplified schematic for the LO input port. The LO input pins drive the bases of the mixer transistors, while the internal 1kΩ bias resistors, in parallel with the 200Ω resistor across the inputs, result in a net input DC resistance of approximately 180Ω. An internally generated voltage at approximately 1V below V_{DD} provide the biasing to the pins. External DC blocking capacitors are required.

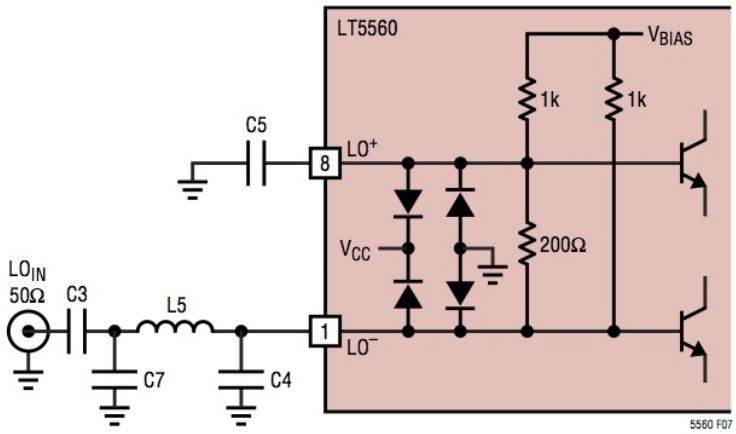

Figure 48. LO input schematic for LT5560 [20].

The recommended values by the LT5560 data-sheet for a 590-890 MHz match at the LO port are: $C4 = 1\text{pF}$, $L5 = 12\text{nH}$, $C3 = C5 = 100\text{pF}$. $C7$ is not used. $C3$ and $C5$ are AC-coupling capacitors.

- *IF output port*: Figure 49 shows a simplified schematic of the output circuit. Pins 5 and 6 are connected to the collectors of the mixer transistors. These differential outputs have been combined externally through a transformer, which also provides supply voltage bias through its center-tap.

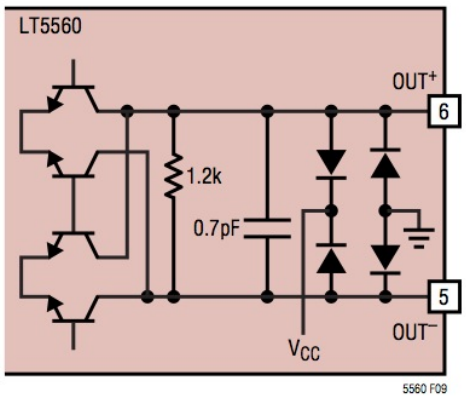

Figure 49. IF output schematic for LT5560 [20].

Figure Figure 50 shows an equivalent small-signal model for the output. The output impedance can be modeled with a 0.7pF capacitor in parallel with a 1.2kΩ resistor. The 0.7nH series bondwire inductances can be ignored for low frequency applications.

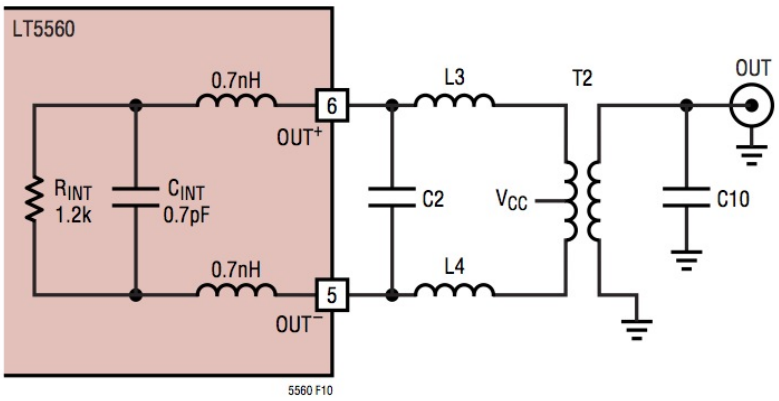

Figure 50. IF output small-signal model with external matching for LT5560 [20].

A 16:1 transformer connected across the output pins 5 and 6 provides impedance transformation and single-ended 50Ω output for IF frequencies below 140MHz. The data-sheet recommends to use a WBC16-1TLB 16:1 transformer, manufactured by Coilcraft®, as shown in Figure 46. The IF pins are biased at the 3.3V supply voltage through the center-tap of the transformer. No other matching is required.

- *Adjustable supply current*: the power supply current has been tuned by properly choosing the resistor R1 value, which is connected between the center-tap of the input transformer and ground. Figure 51 shows how the supply current changes with respect to the value of R1[20]. The performance vs current of a 900MHz down-converting mixer, as given by the data-sheet, is plotted in Figure 52[20].

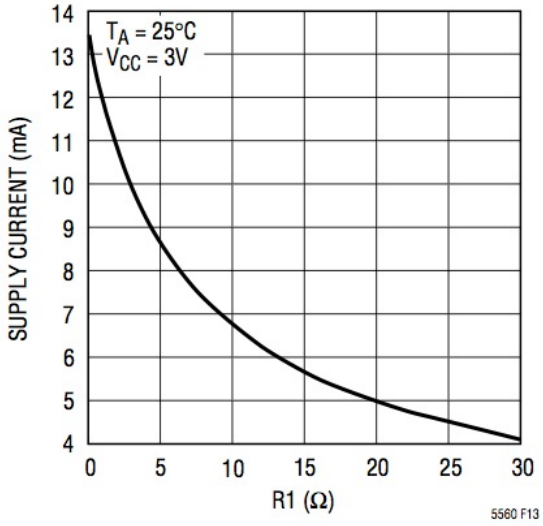

Figure 51. Typical supply current vs. R1 value [20].

The chosen value for R1 is 5.1Ω, which defines a power supply current of about 8.7mA. Resistor R1 is defined as R_{BIAS} in Figure 46. We wanted to chose a supply current close to the one at which the mixer has been characterized. As we can see from Figure 52, the performance is poor for a power supply current lower than 6mA, while it is very good for 10mA. Hence, 8.7mA represents a good tradeoff because higher performance and high linearity are not the our main requirements.

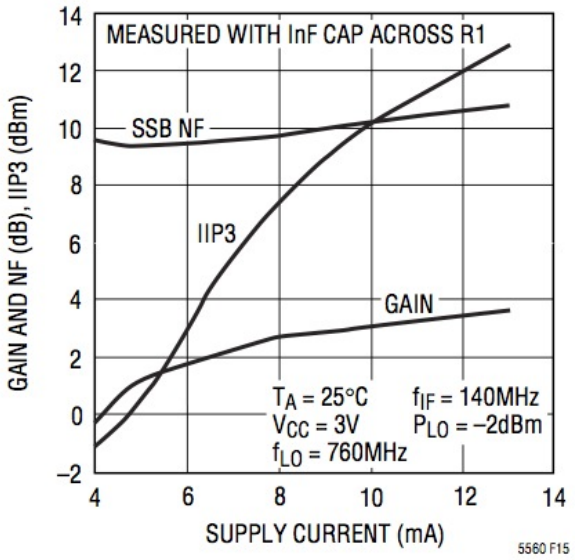

Figure 52. 900MHz down-converting mixer gain, noise figure and IIP3 vs. supply current [20].

The PCB layouts for the LT5522 and the LT5560 are shown in fig Figure 53 and Figure 54, respectively.

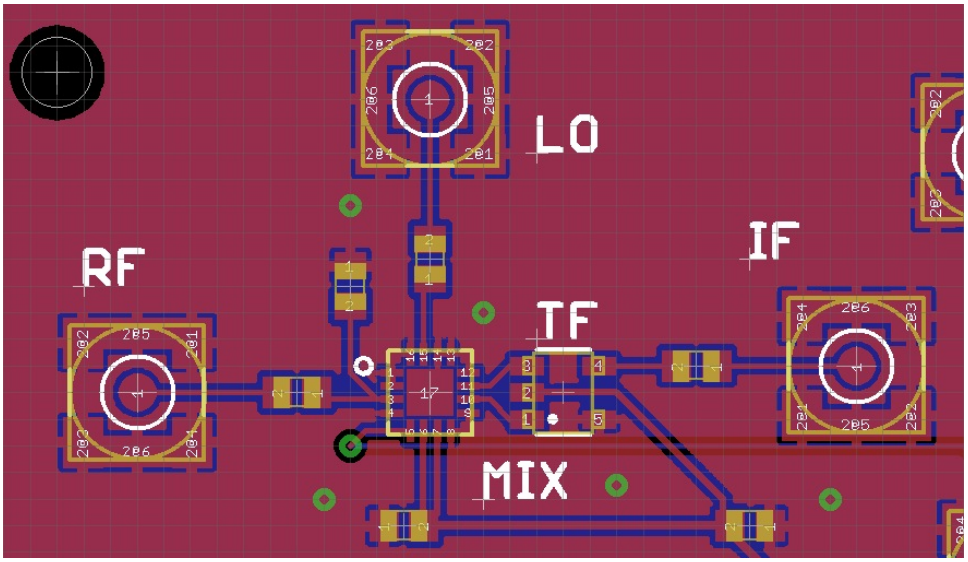

Figure 53. PCB layout for LT5522 mixer.

Notice that no LO oscillator has been placed on the PCBs, instead only a SMA connector is provided for the LO port. In order to down-convert the 611 MHz PM sensor signal to a signal lower than 20 MHz we would need a LO oscillator able to generate a very high frequency such as 600 MHz. These kind of oscillators draw high power supply current and are very expensive. Moreover, the LO oscillator must be very stable in order to get a reliable frequency measurement with heterodyne conversion, otherwise we would lose all the advantages of having a frequency shift with no loss in information. Commercial high frequency XO and TCXO oscillators are available with several temperature stabilities, spanning from ±1ppm up to ±100ppm. One possible alternative solution is to use the designed heterodyne frequency counter combined with

a high-end RF signal generator such as the one used for tests in our laboratory, the Agilent N9310A. This will provide the user with a very high resolution, at the expense of portability.

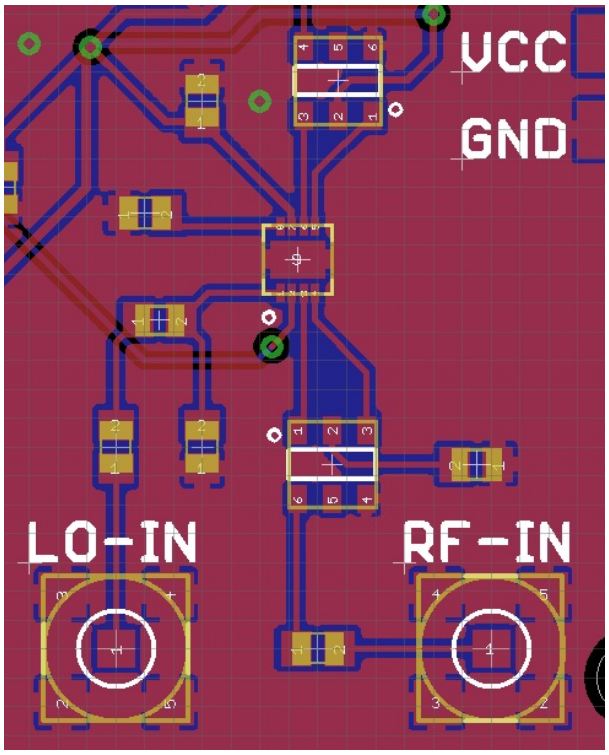

Figure 54. PCB layout for LT5560 mixer.

4.7 Power Management

The operation of the system is designed with particular focus on reducing power consumption while achieving best possible resolution. In order to achieve the lowest possible power

consumption it is necessary to carefully choose the ICs to integrate into the system but also to implement a proper power management in order to use them only when their operation is necessary and to power them down when they are not useful. Each of these ICs is equipped either with an enable or a stand-by port, making their power supply status very easy to control for the microcontroller by means of its digital I/O pins. As a result, the MAX3221 is powered only when a UART communication has to take place, while the ASTX-H11 oscillator together with the MAX941 comparator and the LT5560 mixer/MC12093 prescaler are powered only when a frequency measurement has to be performed. Table IV shows the ICs used in the final designs. Power supply current in stand-by and run mode is shown for each of them, as indicated on their datasheets.

TABLE IV

POWER SUPPLY CURRENT FOR DIFFERENT ICS.

Component	Stand-by current (min - max)	Run-time current (min - max)
ASTX-H11	NA - 15 μA	2 mA - 4.8 mA
MAX941	12 μA - 60 μA	380 μA - 600 μA
MAX3221	1 μA - 10 μA	0.3 mA - 1 mA
LT5560	0.1 μA - 10 μA	4 mA - 13.4 mA
MC12093	120 μA - 200 μA	3 mA - 4.5 mA
LED	0 - 0	NA - 2 mA
PIC24F	0.6 μA - 1.5 μA (Deep Sleep, LPRC) 44 μA - 60 μA (Idle, LPRC) 0.75 mA - 0.95 mA (Idle, FRC @ 8 MHz)	57 μA - 125 μA (LPRC) 2.9 mA - 4.2 mA (FRC @ 8 MHz)

The PIC24F is put into Idle mode when a frequency measurement is being performed and in Deep Sleep mode when the measurement and the communication with the PC has successfully completed. Figure 55 shows how the average power supply current consumption is affected with this kind of approach.

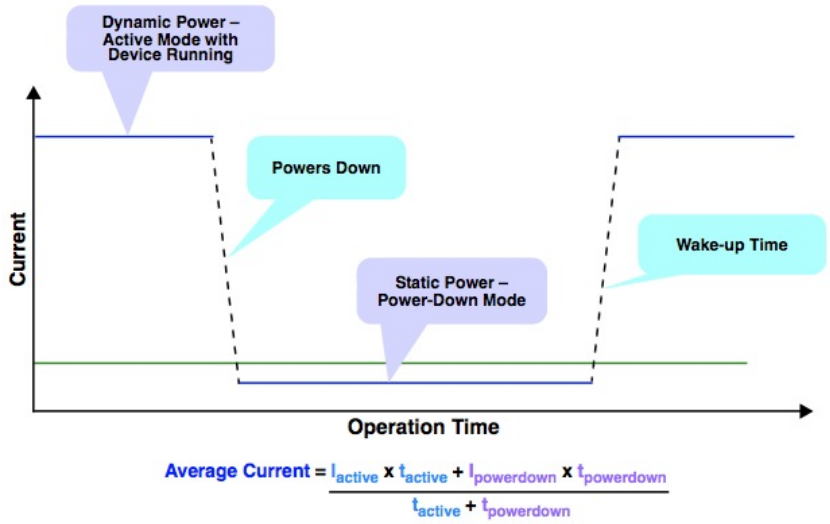

Figure 55. Power management effect on average power supply current consumption.

Idle mode suspends the CPU and code execution while allowing peripheral modules to continue operation. This is where the frequency measurement takes place, because the CPU is halted while TMR1 and TMR2/3 keep working, thus the power consumption will be only due to the switching action of the transistor inside these threes registers. In Deep Sleep mode the core, all peripherals (except RTCC and Deep Sleep Watchdog Timer DSWDT) are shut down for current savings. The DSWDT runs when the PIC is in Deep Sleep mode. For this project we used the LPRC oscillator in order to get lowest possible current consumption when driving the DSWDT. Entering Deep Sleep mode is controlled via software while exiting is triggered by DSWDT time-out. Deep Sleep time is selectable by the user by means of some

dedicated configurations bits, and it ranges from 2.1 ms up to 25.7 days. During our tests we experimented with Deep Sleep times from 2.1 up to 540 seconds. Sleep times longer than 10 minutes are completely meaningless for this particular application.

The maximum current drawn by the prescaling counter during a frequency measurement is about 13 mA, while for the heterodyne counter (without on-chip LO oscillator) is about 14 mA. However, the mixer also needs an on-chip LO oscillator if we want to build a portable device, therefore the current drawn by a LO oscillator must be added for getting the final results. A very high quality oscillator, as the ASGTX manufactured by Abracon Corporation®[22], has a typical power supply current of 50 mA. Hence, in order to find the overall current consumption of the heterodyne counter, we collected current consumption data from our device (which doesn't embed a LO oscillator) and we added the typical current consumption of the ASGTX to compute the overall average current consumption. The simulation has been run in Matlab®. The current consumption achieved during deep sleep mode can be expressed as the sum of all the stand-by currents drawn by all the devices mounted on the PCB. We can compute a best and worst case current consumption for the heterodyne counter as follows, using the data stored in Table IV:

$$I_{DS_{BEST}} = (15 + 12 + 1 + 0.1 + 0.6)\ \mu A = 28.7\ \mu A \tag{4.7}$$

$$I_{DS_{WORST}} = (15 + 60 + 10 + 10 + 1.5)\ \mu A = 96.5\ \mu A \tag{4.8}$$

While for the prescaling counter we get:

$$I_{DS_{BEST}} = (15 + 12 + 1 + 120 + 0.6)\ \mu A = 148.6\ \mu A \tag{4.9}$$

$$I_{DS_{WORST}} = (15 + 60 + 10 + 200 + 1.5)\ \mu A = 286.5\ \mu A \tag{4.10}$$

The deep sleep current is negligible compared to the run-time current, especially for the heterodyne counter. Notice that it is extremely unlikely that all the components draw the maximum possible current during stand-by mode, hence the worst case scenarios of Equation 4.8 and Equation 4.10 is unlikely to happen.

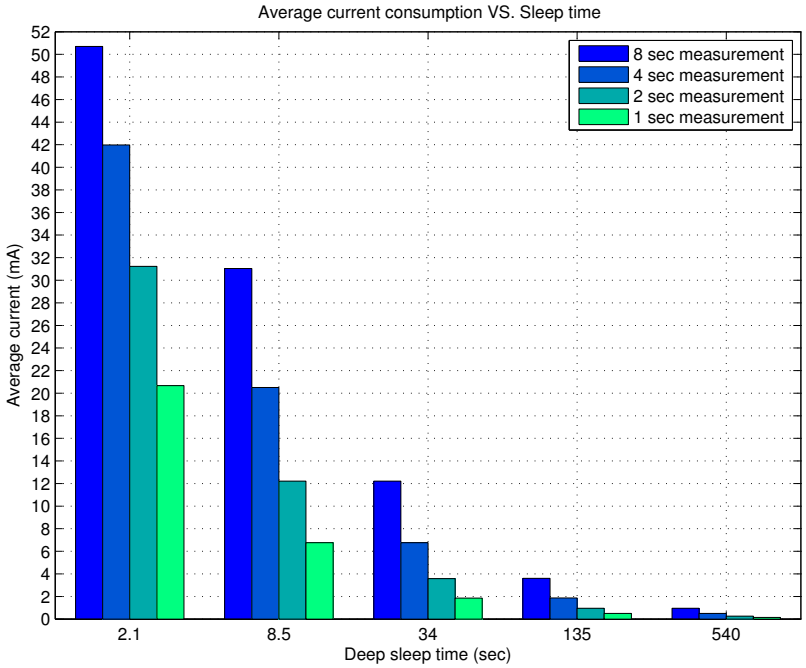

Figure 56. Average current consumption VS. deep sleep time simulation, for heterodyne counter.

The plots of Figure 57 and Figure 56 show the average power supply current with respect to the sleep time and the measuring time. It's important to notice how fast the average power supply current decreases for increasing sleep time, but even more important is to notice how faster it decreases for decreasing gate time. The combination of long sleep time and short gate time is the key for getting the lowest possible current consumption.

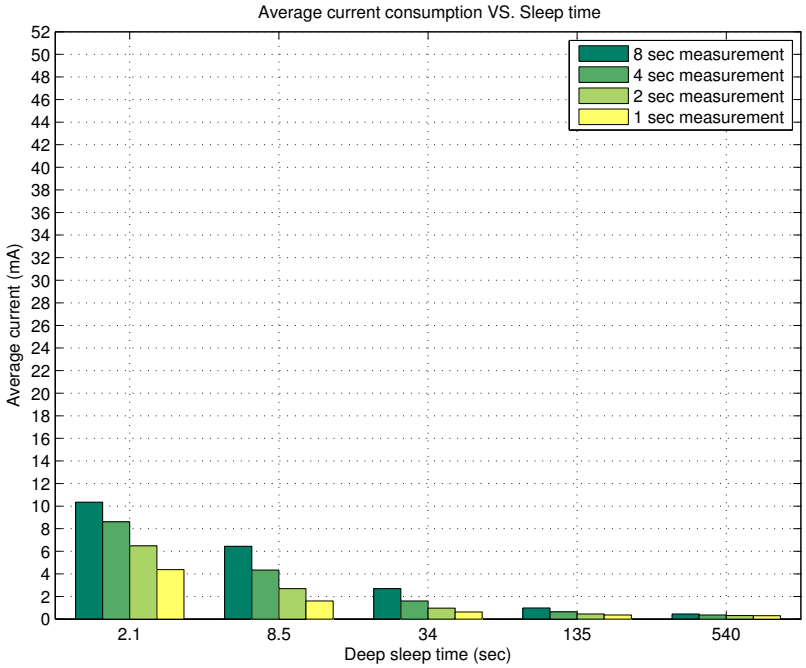

Figure 57. Average current consumption VS. deep sleep time simulation, for prescaling counter.

The drawback of a shorter gate time is of course a degradation in resolution. Table V shows resolutions for different gate times, both for the prescaling and the heterodyne counter. The higher the gate time the better the resolution, at the expense of a higher current consumption. Remember that all these values are computed assuming negligible time base and LO oscillator errors.

TABLE V

RESOLUTIONS FOR DIFFERENT DEVICES AND GATE TIMES

Gate time	Resolution with mixer	Resolution with prescaler
8 sec	±0.25 Hz	±16 Hz
4 sec	±0.5 Hz	±32 Hz
2 sec	±1 Hz	±64 Hz
1 sec	±2 Hz	±128 Hz

The choice of the gate time is not trivial, it is strongly dependent on the final application. In this case, the frequency counter must work with a FBAR which senses particulate matter in the air. If we want a rough approximation of how the pollution changes in time we may decide to have a shorter gate time, i.e. a lower current consumption, because resolution is not the main concern. If a very precise measurement has to be perform, then a longer gate time is needed at the expense of a higher current consumption. Also the choice for the sleep time is application-dependent. This choice could be driven by the required number of measurements that the device must perform in a given amount of time. If we need to collect few data we may go for longer sleep times, saving a considerably amount of power. If instead we need a high number of samples than a shorter sleep time is right the way to go. In Table VI we can find

an approximation of how many samples the device can retrieve every hour, based on different sleep and gate times. These value are approximated because the overhead due to the C code run-time and the UART communication time is not taken into account, thus the final number of samples/hour will be slightly less than the declared one. These numbers are only meant to provide the reader with an idea on how the sleep time could be chosen for a real-world application.

TABLE VI

NUMBER OF MEASUREMENTS PER HOUR, BASED ON SLEEP TIME AND MEASURING TIME

1 sec	2 sec	4 sec	8 sec	Sleep time (s)
1161	878	590	356	2.1
379	342	288	218	8.5
102	100	94	85	34
26	26	25	25	135
6	6	6	6	540

The frequency measurement takes place in several different steps, which are meant in order for the whole system to draw the minimum possible amount of current.

1. Wake microcontroller up from Deep Sleep mode, select internal low power RC oscillator as initial clock for the PIC24F.
2. Setup input and output pins and turn all unused peripherals off, except for TMR1, TMR2/3 and the UART1 module.
3. Turn the external Time Base ON, as well as the LED, the comparator and the mixer/prescaler (depending on which device is considered).
4. Switch system's clock to the external down-converted signal.
5. Start TMR1 and TMR2/3 together, the frequency measurement *starts* here.
6. Put the microcontroller in Idle mode. The measurement *is being performed* here.
7. Interrupt is raised and frequency measurement *stops*. Stop TMR1 and TMR2/3.
8. Switch system's clock to internal low power RC oscillator.
9. Switch all external peripherals OFF.
10. Read frequency value from TMR2/3 and save it in a global variable.
11. Apply calibration curve to the retrieved data.
12. Switch system's clock to internal 8 MHz RC oscillator.
13. Send data to PC via UART.

14. Put microcontroller in Deep Sleep mode. Repeat from step 1 after deep sleep time has elapsed.

CHAPTER 5

EXPERIMENTAL DATA AND VERIFICATION

5.1 Errors And Calibration

As we observed in Chapter 1, the time base plays a fundamental role in the accuracy and resolution of a frequency counter. There are two critical parameters to take into account for the time base, which are the frequency stability and the jitter, or phase noise. The frequency stability indicates how much the oscillating frequency will deviate from the nominal value, based on parameters such as the temperature, the aging, the variation of the supply voltage and the load. The frequency stability specifications of the ASTX-H11 TCXO used in our design are shown in Figure 58[21].

Frequency Stability Δf/f0 vs Tolerance (@+25℃)	-2.0	-----	+2.0	ppm
vs Temperature (ref. to +25℃)	-2.5	-----	+2.5	
vs Supply Voltage Change (Vdd±5%)	-0.2	-----	+0.2	
vs Load Change (ZL±10%)	-0.2	-----	+0.2	
vs Aging (first year @+25℃)	-1.0	-----	+1.0	

Figure 58. Frequency stability specifications for the Abracon ASTX-H11 [21].

As we can see, the biggest deviation from the nominal frequency is due to temperature variations. Let's analyze how the frequency stability may affect a frequency measurement. The chosen oscillator works at a frequency $f_{TB} = 16$ MHz. As we have seen in Section 4.2, the signal coming from the external TCXO is fed into the pin T1CK, which drives TMR1. The input frequency in pin T1CK is divided by the embedded prescaler in TMR1, i.e. it is divided by 256. Hence, the frequency at which TMR1 will work is:

$$f_{INT} = \frac{f_{TB}}{256} = \frac{16000000}{256} = 62500\ Hz \tag{5.1}$$

Since the temperature frequency stability is declared as ±2.5 ppm, then the maximum and minimum frequency at which TMR1 will work is:

$$f_{INT_{MAX}} = \frac{16000000 + (16000000 \cdot 2.5 \cdot 10^{-6})}{256} = 62500.15625\ Hz \tag{5.2}$$

$$f_{INT_{MIN}} = \frac{16000000 - (16000000 \cdot 2.5 \cdot 10^{-6})}{256} = 62499.84375\ Hz \tag{5.3}$$

Assuming a standard nominal gate time of 1 second we can compute how this gate time deviates from its nominal value based on the change of frequency of the external TCXO. In order to get a 1 second gate time with a 62.5 kHz frequency, the period register PRD1 of TMR1 is set to 62500, so that when TMR1 reaches that value then an interrupt is raised. The maximum

and minimum gate times can be computed by dividing the the value stored in PRD1 by the maximum and minimum operating frequency, as shown in Equation 5.4 and Equation 5.5:

$$t_{G_{MAX}} = \frac{PRD1}{f_{INT_{MAX}}} = \frac{62500}{62500.15625} = 0.9999975\ s \tag{5.4}$$

$$t_{G_{MIN}} = \frac{PRD1}{f_{INT_{MIN}}} = \frac{62500}{62499.84375} = 1.0000025\ s \tag{5.5}$$

As we can see, the gate time may deviate from its nominal value by a factor of $\pm 2.5\ \mu s$. This kind of gate time error can introduce a maximum frequency measurement error of ± 2.5 Hz for a 1 MHz measurement, and a ± 42.5 Hz error for a 17 MHz measurement.

Another possible cause of time base error is the jitter, or phase noise. In fact, if the jitter is too large then the measurement will last for a too long or too short period with respect the nominal value. The ASTX-H11 TCXO has been chosen for its very low phase noise, which is specified as -130 dBc @1kHz offset and -158 dBc @100kHz offset. The corresponding period jitter is about 0.2ps RMS. The maximum input frequency accepted by this counter is 17 MHz, which corresponds to a minimum period of:

$$t_{MIN} = \frac{1}{17000000} = 58.82\ ns \tag{5.6}$$

It's clear that the jitter introduces no error because the period jitter is several orders of magnitude smaller than the minimum period that the frequency counter will handle.

The last source of error is represented by the PIC24F instruction cycle delay. There is a certain

delay in the C code routine between the time when TMR1 raises its interrupt to when TMR2/3 is finally stopped and therefore the measurement is complete.

The overall error, which is the sum of the time base error and the instruction cycle delay, is very easy to correct in software because it is constant. For instance, for 1 MHz measurement we may find an error of +22 Hz. Knowing that the input frequency is divided by 2 into the PIC24F, the resolution will be ±2 Hz for a 1 second measurement. Hence, the error will be $(+22 \pm 2)$ Hz, resulting in a measurement of (1000022 ± 2) Hz. Assuming a good quality time base, if the measurement is repeated several times then the measured value will always be (1000022 ± 2) Hz. It is enough to perform a calibration procedure that consists in subtracting 22 Hz from the measured value to get a final value of (1000000 ± 2) Hz. Figure 59 shows the curve representing the error, measured on the actual devices. On the x-axis we find the nominal input frequency, while on the y-axis the error from the nominal value is represented, in Hz.

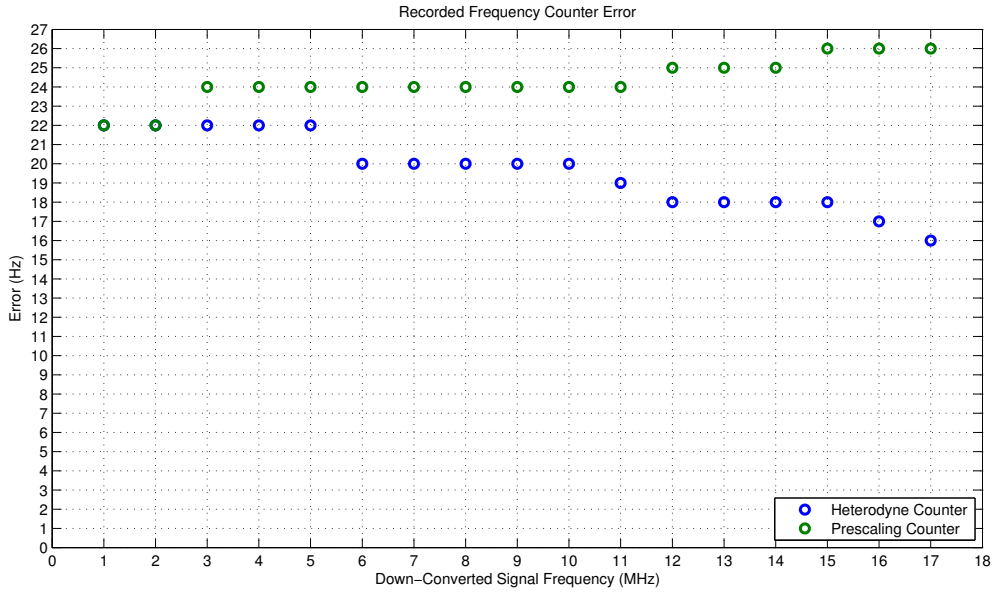

Figure 59. Recored FBAR frequency monitor error. The plot shows the error for a 1 second measurement, averaged over 10 measurements.

The calibration must be performed with a very stable and precise reference, which in our case is an Agilent N9310A. The output from the RF generator must be fed directly into the input of the MAX941 comparator, so that it will emulate a down-converted signal coming from the RF front-end section. The procedure for calibration is very standard: some known frequencies are generated in order to be counted by the frequency counter, the difference between the nominal value and the measured one represents the error that must be corrected via software. In order

to do that, a look-up table is implemented in the C code of the microcontroller. This look-up table will store all the errors for different frequencies. Every time a measurement has been performed, the program finds out what is the error for that particular frequency thanks to the value stored in the look-up table, and it will compensate for this error by performing a simple arithmetical subtraction. Hence, the final output value will be a calibrated version of the one measured in the beginning. Notice that the calibration will not affect the resolution but only the accuracy of the measurement. The resolution will still be dependent on other factors such as the gate time and the divide ratio applied to the input frequency. The calibration has been performed for input frequencies from 1 MHz up to 17 MHz, with steps of 1 MHz. Reducing the step's size may increase accuracy, but since the error grows slowly with growing input frequency, it may be not necessary to apply a calibration with a very small step's size.

5.2 Input Sensitivity And Frequency Bandwidth

Input sensitivity defines the dynamic range of the frequency counter. The dynamic range can be expressed as the difference between the maximum and the minimum RF power than can be applied to the system:

$$DR = P_{RF_{max}} - P_{RF_{min}} \tag{5.7}$$

If the input power exceeds one of these two boundaries, the frequency counter is not guaranteed to work. As a consequence, the frequency measurement can return a not reliable value or the device could even stop working or brake if the input power becomes too high. The frequency

bandwidth can be defined as the difference between the maximum and minimum frequencies at which the device may operate:

$$\Delta f = f_{RF_{max}} - f_{RF_{min}} \tag{5.8}$$

Dynamic range and bandwidth are two fundamentals parameter for evaluating the performance of a frequency counter. The main goal of this design is to extend the bandwidth of the frequency counter using a RF front-end able to down-convert the input signal frequency. Without any RF front-end, the input signal would be directly applied to the comparator. In this case, the bandwidth and the sensitivity of the frequency counter would correspond to the bandwidth and sensitivity of the comparator. When a mixer or a prescaler is added in front of the comparator then the bandwidth and sensitivity change, based on the characteristics of the device added in the RF path. In order to test the sensitivity of the mixer we set a LO frequency of 600 MHz with a power of -2dB, which is indicated as typical LO power in the LT5560's datasheet. The LO signal is provided by an Agilent N9310A RF generator. The input sensitivity with the mixer front-end has been tested using RF frequencies ranging from 601 MHz (giving $IF = 1$ MHz) up to 617 MHz (giving $IF = 17$ MHz, i.e. the upper bandwidth limit of the direct frequency counter). The datasheet of the LT5560 mixer reports that the absolute maximum rating for the RF power must be +10dB, this is the reason why no higher RF power has been tested.

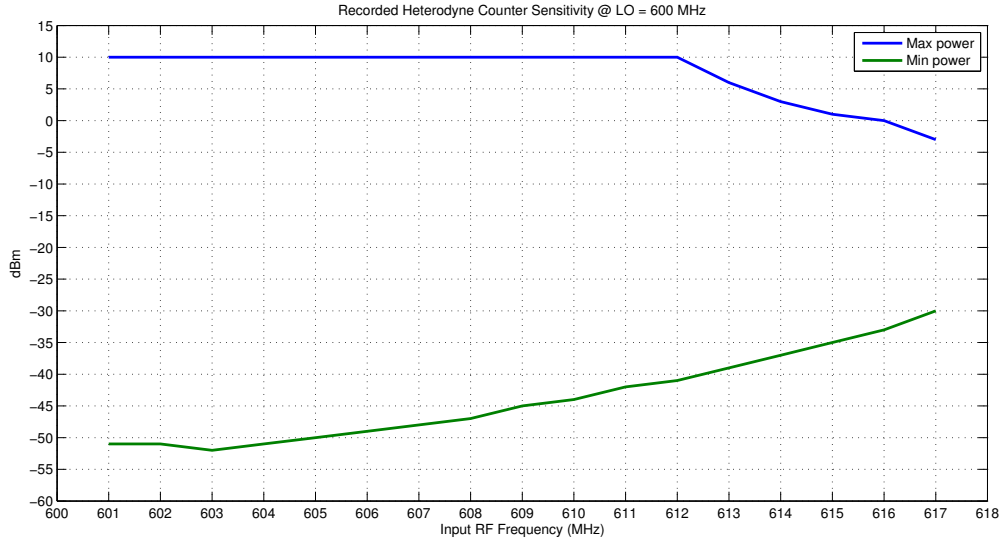

Figure 60. Recorded input sensitivity for heterodyne counter @ LO = 600 MHz.

It's easy to notice from the plot in Figure 60 that the higher the difference between the RF and the LO frequencies (i.e. the higher the IF frequency), the lower the dynamic range is. Using a mixer front-end we don't expand the frequency counter's bandwidth, instead we simply shift its operating frequency range. The shift is determined by the LO signal. By selecting the right LO frequency it is possible to measure much higher frequencies than the direct counter's maximum one, even though the bandwidth never changes. In this case, the whole design has been carried out with the goal of measuring a signal coming from the PM sensor, which is centered at about 611 MHz. Using a LO signal at 600 MHz it's possible to shift the 611 MHz

signal down to 11 MHz, which is within the bandwidth of the direct counter. Moreover, The conversion gain offered by this active mixer improves the input sensitivity in the lower range.

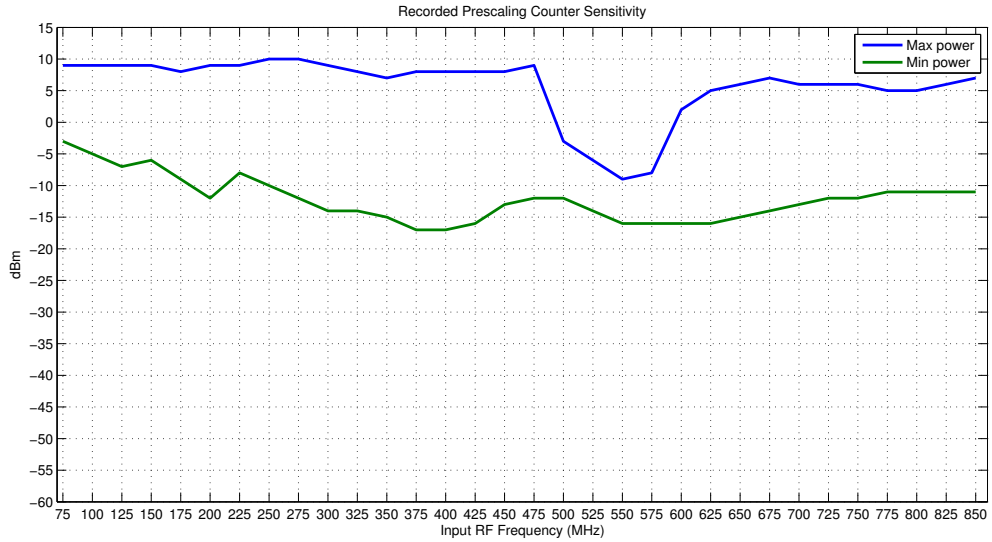

Figure 61. Recorded input sensitivity for prescaling counter.

For what concerns the prescaler, input frequencies from 75 MHz up to 850 MHz have been tested, using a divide ratio of 64. Those are the minimum and maximum frequencies at which the prescaler front-end has been verified to be properly working. The actual minimum frequency seen by the comparator is $75000000/64 = 1171875$ Hz, while the maximum one is

850000000/64 = 13281250 Hz. These two frequencies sit within the bandwidth of the direct counter. The drop of dynamic range from 500 up to 575 MHz is due to parasitic effects of the PCB and resonances in the passive components. The bandwidth of the frequency counter is both shifted and expanded using a prescaler, while the sensitivity is reduced in the whole range. We can conclude that both devices have enough dynamic range and bandwidth for counting the PM sensor signal, which has been measured to have a power of -5 dBm and a central frequency of 611 MHz.

CHAPTER 6

PRESCALING COUNTER VS. HETERODYNE COUNTER COMPARISON

The prescaling and the heterodyne counters have their own advantages and disadvantages, therefore choosing one solution over the other requires some knowledge of what the final application will be. As we observed in Section 4.7, current consumption differs significantly if a prescaler rather than a mixer is used as the down-converting element. The main reason behind this difference in current consumption consists in the fact that the mixer requires a high frequency LO oscillator in order to work, which is the more power hungry component of the whole design. Figure 57 and Figure 56 clearly show the difference in average power supply current consumption. The average current consumption becomes comparable only for very high sleep times, however if a high number of samples per hour is needed, then the heterodyne counter will significantly draw more current with respect to the prescaling counter. The other element to take into account is of course the resolution. The mixer front-end does not degrade the resolution (assuming that the LO oscillator is a good quality one and therefore has a tight stability), while the prescaler front-end introduces a considerable loss in resolution, which must be compensated by increasing the gate time. A longer gate time implies a higher average current consumption. Table VII summarizes all the different specifications of the two front-ends, highlighting resolution and average current consumption. The average current consumption is expressed in terms of maximum and minimum, i.e. for 1 second gate time and 8 seconds gate

time. At this point, we could split the choice between the two front-ends by considering how many samples per hour are needed. In case we don't need a high number of samples, choosing the prescaler and using a gate time of 8 seconds can provide a resolution of ±16 Hz with an average current consumption of 2.7 mA for a 34 seconds sleep time. With this setup we are able to collect about 85 measurements per hour. The second scenario is that we want a higher number of samples, therefore using a mixer with a 1 second gate time can provide a ±2 Hz resolution with an average current consumption of 6.7 mA for a 8.5s seconds sleep time. With this setup it's possible to collect about 342 measurements per hour.

The dynamic range is higher for the heterodyne counter, as shown in Figure 60 and Figure 61. However, the signal coming from the PM sensor has a power of about -5 dBm, therefore the difference in dynamic range does not influence the final decision. The last factor to be taken into account when deciding which front-end to adopt is the overall cost for the components. Table VII shows a production cost estimation, which doesn't take into account the price for fabricating the actual PCB. The price of the PCB is a common denominator between the two devices, hence in order to understand their price difference we only need to analyze the different price for buying all the components. As we can see, the heterodyne counter is 3 times more expensive if we want to build a single device, while it's about 2.3 times more expensive if we want to build 1000 devices. The higher resolution of the heterodyne counter comes at the expense of a higher current consumption and a higher production cost.

TABLE VII

HETERODYNE VS. PRESCALING COUNTER SPECIFICATIONS COMPARISON

	Mixer	Prescaler
1s gate time resolution	±2 Hz	±128 Hz
2s gate time resolution	±1 Hz	±64 Hz
4s gate time resolution	±0.5 Hz	±32 Hz
8s gate time resolution	±0.25 Hz	±16 Hz
Avg. current for 2.1s sleep time	21 - 51 mA	4 - 10 mA
Avg. current for 8.5s sleep time	7 - 31 mA	2 - 6 mA
Avg. current for 34s sleep time	2 - 12 mA	0.6 - 3 mA
Avg. current for 135s sleep time	0.5 - 4 mA	0.4 - 1 mA
Avg. current for 540s sleep time	0.15 - 0.9 mA	0.3 - 0.45 mA
Dynamic range @ 611 MHz	-42 to +10 dBm	-16 to +5 dBm
Components cost for 1 board	108 USD	36 USD
Components cost for 10 board	92 USD	30 USD
Components cost for 100 board	54 USD	25 USD
Components cost for 1000 board	51 USD	22 USD

The low-end sensitivity of the prototype PM sensors is about 2 $\mu g/m^3$ with 10 minutes integration time[1], which corresponds to a negative frequency drift of about 50 Hz over 10 minutes. What we need is a frequency monitor able to provide a resolution higher than ±50 Hz. Since the integration time lasts for 10 minutes, we could decide to take one frequency measurement every 540 seconds (9 minutes). Considering this scenario we can find one possible design solution, shown in Table VIII.

TABLE VIII

DESIGN SOLUTION 1

	Prescaling Counter
4s gate time resolution	±32 Hz
Avg. current for 540s sleep time	0.4 mA
Components cost for 1000 boards	22 USD

For the next generation sensor, the integration time is expected to be reduced by an order of magnitude, so that the frequency drift will be reduced to about 5 Hz per minute. In this case we need a frequency monitor able to provide a resolution higher than ±5 Hz. Since the

integration time lasts for 1 minutes, we could decide to take one frequency measurement every 34 seconds. Considering this scenario we can find another possible design solution, shown in Table IX.

TABLE IX

DESIGN SOLUTION 2

	Heterodyne Counter
1s gate time resolution	±2 Hz
Avg. current for 34s sleep time	4 mA
Components cost for 1000 boards	51 USD

The current drawn by the PM sensor itself is about 200 mA, while its production cost for a high volume of pieces is expected to be 50 USD per each. The current drawn by the FBAR frequency monitor is negligible compared to the one drawn by the sensor. Finally, we can state that the design constraints are represented by the desired resolution, sleep time and cost.

CHAPTER 7

CONCLUSIONS

The goal of this work is to design a portable, low cost FBAR frequency monitor which can operate at very low power with an input signal coming from a PM sensor. This frequency of this signal is subjected to change when the FBAR is mass-loaded and it senses $PM_{2.5}$ particulates in the environment. What we are interested in is to measure this frequency shift, which will tell us what is the pollution rate of change with respect to time in the environment under test. In order to achieve this goal we need to design a frequency counter, whose task is to collect frequency measurements of the PM sensor signal. The collected data will be sent to a laptop, in order to be analyzed and visualized on a graphical display. Since our design must be low cost and low power, the main device used to count the frequency has been chosen to be a microcontroller. The scheme used for counting the frequency has been chosen to be the direct frequency counting rather than the reciprocal one, because the reciprocal counter works best with frequencies much lower than the time base frequency. In our case, the input frequency would be too much close the time base frequency, making a reciprocal frequency measurement much less reliable than a direct one. As we all know, microcontrollers are devices that cannot deal with signals much higher than 20 MHz, thus if we want to measure much higher frequencies in the RF range, we need to choose a proper down-conversion method for reducing the input signal frequency in order to keep it within the operating range of the microcontroller with minimum loss in resolution and without adding any kind of noise, distortion or undesired harmonic content

that would affect the measurement accuracy. Hence, the main goal is to find which technique allows us to reduce the input frequency without losing the information carried by the signal and resulting in the minimum possible loss in resolution and accuracy. For the purpose of this work, two popular techniques have been implemented, which are the prescaling and the heterodyne conversion. As we observed throughout the previous chapters, the prescaling approach is a much lower cost solution which works at low power and can easily reach resolution as good as ±16 Hz. The heterodyne conversion, which makes use of a mixer and a LO oscillator, can provide much higher resolution, even below 1 Hz, at the expense of a higher average current consumption and higher production cost. In Chapter 6 we compared every specification of the two down-converting counters and we summarized everything in Table VII. As we observed, the final choice is dependent on many factors, but the most important ones are the cost, the resolution and how many measurements per hour we want to get.

If cost is not the main constraint, it is clear that a heterodyne counter is the best choice: it provides a higher resolution and, with the proper choice of gate time and sleep time, almost the same current consumption as the prescaling. Whereas, if a lower cost and lower performance device is desired, the prescaler may be the desired choice because of its much lower cost. As we already said, there is no right or wrong choice. This work is intended to provide the reader with a deep knowledge of all the benefits and drawbacks of the two designs. The final choice can be made and tuned by using all the elements provided in this work.

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