Design and Optimization of GaN-Based Power Semiconductor Transistors

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THESIS

Submitted as partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Chicago, 2017

Chicago, Illinois

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To My Parents and Girlfriend, Adriana Macias

ACKNOWLEDGEMENTS

There are many people I have encountered in my studies that have been fundamental to the success of this thesis. First, I would like to express my gratitude toward my advisor, Dr. Lucy Shi. She has been a constant source of support, guidance and inspiration. Her utmost patience, understanding and confidence have been instrumental for me and completion of this thesis would not have been possible without her. I also thank Dr. Michael Stroscio and Dr. Vitali Metlushko for being on both my committee and excellent instructors in both undergraduate and graduate courses, shaping my education.

I would also like to thank all the staff at Argonne's Center for Nanoscale Materials but most notably Dr. Ralu Divan and Liliana Stan. They have been a great source of knowledge, encouragement and examples. I would also like to thank Ralu for being on my committee.

Dr. Antonio DiVenere and Dr. Seyoung An who have helped me tremendously at UIC working at the Nanotechnology Core Facility. Dr. Seyoung An who has shown me a different perspective of cleanroom tools and learning from him has been truly a pleasure and Dr. Antonio DiVenere for both being on my committee and for all the long helpful discussions we have had.

I am also extremely grateful to the folks at NXP semiconductors especially Dr. Bruce Green and Dr. Karen Moore. I sincerely appreciate all their advice and support throughout my graduate career. They have truly kept me on track with my research progress.

I would also like to thank my fellow labmates for all their help and discussions: Chenjie Tang, Nathaniel Nicandro and Xiaowei Wang, as well as all the graduate assistants at NCF, whom I've worked with: Khodr Maamari, Jacek Lechowicz, Tejumade Durowade, Tara Foroozan and Nick Anderson. They have kept me sane throughout graduate studies and I have appreciated all the time spent together.

ACKNOWLEDGMENTS (continued)

I would also like to thank all the staff at Cornell's NanoScale Science and Technology Facility, especially Mike Skvarla. During my early years as a graduate student, he was patient enough with me to teach me about work in the cleanroom.

Also on the list is all the helpful administrative staff at UIC's ECE department: Mona Hurt, Ala Wroblewski, Tina Alvarado, Erica Plys, Martha Salinas, Evelyn Reyes, Beverley Miller and Mihai Bora.

Lastly, I am extremely grateful for the love, support and guidance from all my family and my girlfriend. They have been with me through it all; through the dark and low times as well as the happy best times.

AC

CONTRIBUTIONS OF AUTHORS

Chapter 3 is published in Elsevier (Solid State Electronics) having co-authors of my advisor. Chapter 4 and Chapter 5 are both published in AIP Publishing LLC (Journal of Vacuum Science & Technology B and Journal of Vacuum Science & Technology A, respectively) having co-authors consisting of Liliana Stan, Ralu Divan and my advisor. In both cases, Liliana Stan helped me with the deposition of the various insulators using atomic layer deposition and x-ray diffraction measurements and Ralu Divan assisted with other fabrication aspects including electron beam lithography and dry-etching. However, all figures and writing in these letters are originally my own. Permission for re-use of Chapters 3, 4 and 5 are all located in Appendix C under C.1, C.2 and C.3, respectively. All other chapters in this thesis is un-published work.

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LIST OF ABBREVIATIONS

AC	Alternating Current
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BOE	Buffered Oxide Etch
CV	Capacitance-Voltage
DC	Direct Current
EBL	Electron Beam Lithography
FET	Field Effect Transistor
HEMT	High Electron Mobility Transistor
HV	High Voltage
ICP-RIE	Inductively Coupled Reactive Ion Etching
MBE	Molecular Beam Epitaxy
MIS	Metal Insulator Semiconductor
MISHCAP	Metal Insulator Semiconductor Heterojunction Capacitor
MISHFET	Metal Insulator Semiconductor Heterojunction Field Effect Transistor
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
PDA	Post Deposition Anneal
PECVD	Plasma Enhanced Chemical Vapor Deposition
PM	Protection Module
PR	Photo Resist
PVD	Physical Vapor Deposition
RF	Radio Frequency
RIE	Reactive Ion Etching
RPM	Remote Pulse Unit
RTA	Rapid Thermal Anneal
RTP	Rapid Thermal Processing
SCS	Semiconductor Characterization System
SEM	Scanning Electron Microscopy
SMU	Source Measure Unit
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
XRR	X-Ray Reflectance

SUMMARY

Gallium Nitride, a viable candidate to advance current technology in high-voltage and high frequency transistors, has seen a boom in research advancements within the last couple of decades. However, compared to Si-based transistors, fabrication processing technology is still in its infancy. Key areas in the metal insulator semiconductor heterojunction field effect transistors (MISHFET) are still inhibiting demonstration of GaN's theoretical limits in terms of transistor performance. In this dissertation, I tackle several topics concerning the MISHFET structure to improve transistor electrical performance.

Through fabrication and testing of design-conscious GaN-based devices, I study various aspects in the MISHFET structure. I begin by optimizing the metal-semiconductor contact, rather the ohmic contact. Realizing a low-contact resistance process is delicately dependent a wide array of processing conditions. I delve into various promising techniques such as recessed-contacts, gold-free processing and metal thicknesses dependency. Moreover, contacts on both AlGaN/GaN and InAlN/GaN were studied. The lowest contact resistance achieved here showed a minimum contact resistance of 0.14 Ω·mm and 0.17 Ω·mm on AlGaN/GaN and InAlN/GaN substrates, respectively.

Next, I study various high-κ insulators in the metal-insulator-semiconductor structure. The insulator's quality may be a severe bottleneck for transistors. Criteria such as excess leakage current and high interfacial defect densities can seriously degrade device performance in both RF operation and breakdown voltage. Thus, I investigate several insulators on GaN and correlate device performance metrics with insulator qualities. By tuning the elemental composition of the insulators, we can control and improve several key factors concerning insulating materials. Overall, I found that HfO_2-based insulators provide lowest insulator/semiconductor interface

defects within the insulators studied here, however, these films are generally electrically leaky. By creating ternary insulators such as $HfAlO_x$, an AlGaN/GaN transistor demonstrated ultra-low leakage on the order of 10^{-12} A/mm.

Lastly, a technique to improve off-state breakdown voltage of an InAlN/GaN transistor was also briefly experimentally verified. By capping the transistor with an insulator with defined qualities, breakdown voltage was improved by more than 400 % of a normally-on InAlN/GaN transistor, compared to the un-passivated device.

1. INTRODUCTION

1.1. Overview of GaN-Technology

During the mid-20th century investigation of solid-state electronics, many semiconducting materials were under intense research to use for the promising newly discovered transistor at Bell Laboratories[1]. However, due abundancy of Silicon and the ability to grow a high-quality oxide (SiO_2), Silicon led the transistor revolution into the 21st century. Silicon, however, is reaching its theoretical limitations in terms of speed, power density and applications. III-V semiconductors have been researched since the discovery of GaAs in the early 1950s but have been severely limited due to poor material synthesis techniques. Within the recent decades with the developments of Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE), the quality of compound semiconductors has drastically improved and thus is becoming a serious candidate to replace Silicon technology.

Gallium Nitride (GaN) is a wide and direct bandgap semiconductor. Moreover, nitrides exhibit strong spontaneous and piezoelectric polarization charges, thus, by growing a stress-inducing 'doped' barrier layer on GaN, a high concentration of electrons (sheet charges) are accumulated at the GaN surface. The high density of electrons at the GaN surface are referred to as the 2-Dimensional Electron Gas (2DEG). The 2DEG, thereby, can be used as a highly conducting channel that may be manipulated by external electric fields. The heterojunction such as described is not the first time the world has seen it. AlGaAs/GaAs HEMT transistors operate under similar principles. However, the GaAs system relies on piezoelectric polarization only to induce a 2DEG while GaN systems have the additional spontaneous charges. Moreover, GaN's wide bandgap (3.4 eV) properties allow for more robust applications which require high-power.

One of the major demands in highly efficient solid state electronics include ‘clean’ energy Electric Vehicles (EV). The large power handling requirements EV’s exhibit require semiconductors with wide bandgaps such as SiC or GaN [2]. SiC is currently dominating the market mainly due to the ability to grow larger single crystal wafers, however, GaN having a slightly larger critical field breakdown and much higher electron mobility is surely a serious contender. Besides high power applications, the ability to form a high-mobility 2DEG with GaN heterojunctions makes it an attractive material for fast switching applications such as power amplifiers in Long Term Evolution (LTE) wireless communication networks [3]. Furthermore, the advantageous wide bandgap nature creates electronics that can be used outer space where background radiation easily damages Si-based electronics [4]. Lastly, GaN enabled the invention of the blue LED which was awarded the 2014 Nobel Prize in Physics [5]. Nonetheless, there are countless applications for GaN-material where it excels performance making it a highly robust and serious contender to replace Si-technology.

So you may ask yourself, ‘Since GaN seems like such a great material, why hasn’t it dominated the market yet?’. Well, GaN does not come without its’ caveats. From the synthesis of GaN single-crystal wafers, the process becomes extremely costly. To date, a 2” single-crystal GaN wafer costs $2,500 while it’s possible to purchase a 4” Si-wafer for a mere $15. Ohmic contact formation is a very complex process as well. Typical ohmic contacts require a multi-layered metal stack of Ti/Al/Ni/Au followed by a high temperature alloying to induce ohmic behavior. There are several problems with the current process. 1. The complexity of the metal stacks in terms of relative thicknesses may be cumbersome. 2. For GaN to be accepted in current Si-fabrication facilities, gold must not be present. 3. Any high temperature processing should be avoided to minimize processing complexity and prevent any damage to high-temperature sensitive

structures. and 4. Contact resistance should be as minimal as possible. In essence, there is much research necessary on the ohmic contacts formation for GaN. Typical GaN transistors are normally-on devices, meaning a negative gate voltage must be applied to 'turn off' the device. To reduce electrical circuits configuration complexities, transistors in the normally-off regime would be preferred. Unlike the high-quality oxide found in SiO_2/Si systems, GaN does not have the same advantages. Typically, high defect densities are found for insulators on GaN. Lastly, current GaN-based devices are far from reaching theoretical breakdown voltage performance. In summary, there is much work required to further improve and mature GaN processing for it to dominate the semiconductor markets.

In this dissertation, I tackle most of these issues through several experiments except for GaN growth. While I mostly focused on insulators on GaN during my graduate career, I will also go into detail on ohmic contacts, normally-off approaches, and high voltage performance.

1.2. Organization of Chapters

I have organized the chapters based on transistor fabrication hierarchy. Although all steps in a fabrication process are important, key issues involved in the process include ohmic contact formation for source/drain electrodes, gate insulation/passivation in the metal-insulator-semiconductor structure and device passivation/encapsulation. In Chapter 2, I delve into techniques to improve metal contacts on GaN. I spent a lot of effort into optimizing the process here since 'good' metal contacts are of utmost importance for optimal transistor performance. Chapters 3, 4 and 5 discusses several aspects of gate insulators. I discuss several important parameters concerning dielectrics such as temperature stability, band offsets, interface trapped charge, etc. Lastly, Chapter 6 discusses a technique studied by Chenjie Tang, and shown experimentally here, to improve 3-terminal off-state breakdown voltage of a type of GaN transistor. Each chapter discussed here stands on its' own and may be read separately from the rest.

1.3. Introduction to Ohmic Contacts

Ohmic contacts on compound semiconductors such as GaAs or GaN require a complex process to induce ohmic behavior. Metal-semiconductor junctions may act one of two ways. The first is rectifying, which is when the contact exhibits diode-like current conduction, namely schottky contact. The other is non-rectifying, or ohmic, when the junction can conduct current in forward or reverse directions. Typical ohmic contacts on GaN requires a process as follows. 1. Multi-layered metal stack deposition of Titanium, Aluminum, Molybdenum (or Nickel), and Gold. 2. High temperature rapid thermal annealing between 800° to 860° for 30 seconds in Nitrogen gas ambient. The purpose of the first two metals, Ti and Al, are required to form successful contact to the semiconductor. When depositing these metals, it is important to choose the optimal respective thicknesses and ratio of thickness. The 3rd metal, either Mo or Ni, is used as a diffusion barrier layer between Au and Al. It is believed that during the high temperature processing, these two material intermix to form Al-Au 'blobs' causing the rough surface morphology seen on ohmic contacts. The 4th metal, typically a noble metal such as Au, is used for electrical contact either by probes or wire bonding. After deposition of the metals, a high temperature rapid thermal annealing is required to induce ohmic behavior. This is an utmost critical process dependent on temperature, time and ambient gas. Typical processing requires at least 800° C for 15-30 seconds in nitrogen gas ambient.

Low ohmic contact resistance is desired to reduce power consumption. Furthermore, large contact resistances degrade the maximum attainable current densities in transistor structures. Other desirable properties include low-temperature contact formation, gold free-technology and low roughness contacts. During the high temperature processing required for the standard stack, inevitably, the 2DEG becomes damaged in the process and thus leads to lower carrier densities

and lower carrier mobility. Moreover, when designing the process flow, one must be wary of any potential damage to the structure during exposure to high-temperature such as gate dielectrics which typically have low-temperature stabilities. Gold-free processing is desirable since no gold is allowed in Silicon fabrication facilities; gold can easily contaminate Silicon-based devices. Thus, for GaN processing to be incorporated in Silicon fabrications facilities, it can't require any gold-processing. Lastly, low-roughness contacts are desired for ultra-scaled devices. During the high temperature annealing, the metal alloying causes rough surface morphology which translates to lateral roughness. When dealing with ultra-scaled devices where source, gate and drain contacts are separated in sub-micron dimensions, the surface roughness may lead unwanted electrical shorts. Careful design and techniques are required to be able to achieve these properties with ohmic contacts.

A common technique to characterize the contact resistance is known as the Transfer Length Model (TLM) or Transmission Line Model. This requires rectangular contacts of width, W, with different spacing between each pad; s_0, s_1, s_2 and so on. The design is depicted in Figure 1. Based on a linear fitting of the measured points, it is possible to extract sheet resistance (R_s [Ω/□]), contact resistance (R_c [Ω·mm]), and specific resistivity (ρ [Ω·cm^2]) by extrapolating to find y-intercept (y_0) , x-intercept (x_0) and the slope (m) and using the following equations:

$$R_s[\Omega/\square] = W \times m$$

$$R_c[\Omega \cdot \text{mm}] = \frac{y_0}{2} \times m$$

$$\rho\ [\Omega \cdot cm^2] = \frac{R_c^2}{R_s}$$

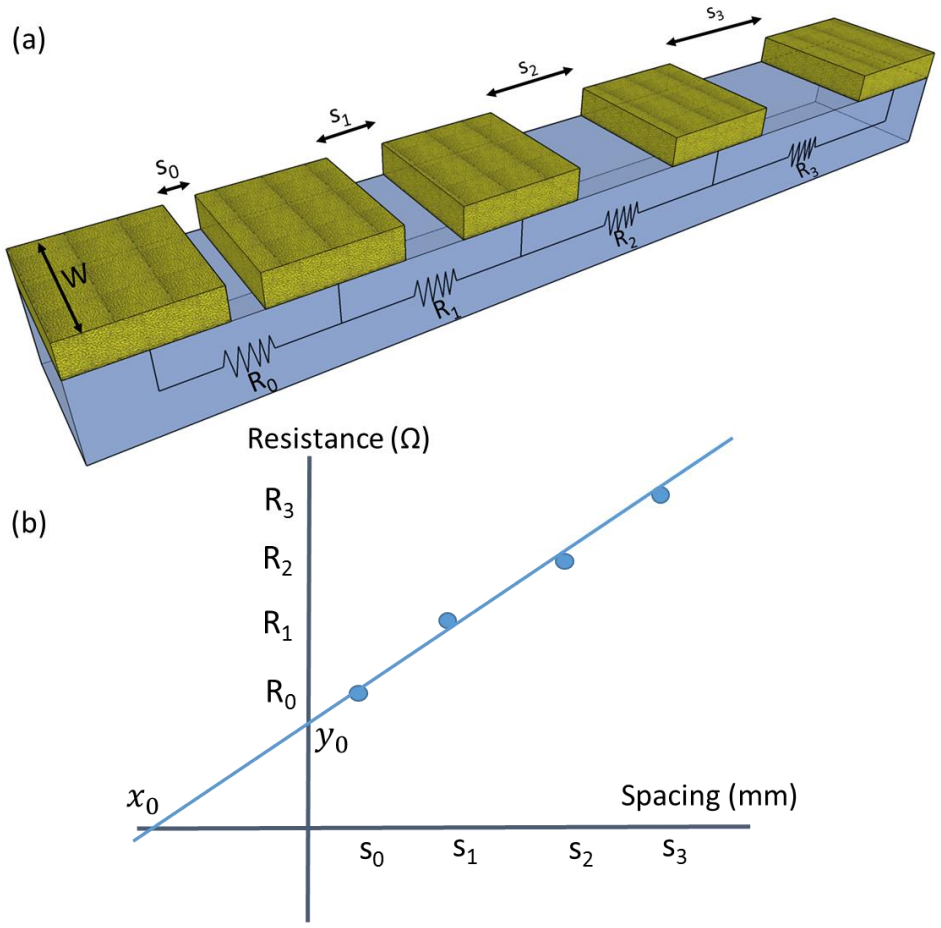


Figure 1 (a) Cross-sectional schematic of TLM rectangular patterns with different spacing and their respective resistances and (b) modeling resistance vs spacing to extract contact resistance.

1.3.1. Literature Review on ohmic contacts

There has been much progress within the research community on ohmic contacts for GaN semiconductors. However, due to the complex process required, there is much room for error and thus there is a large variation on the reported results. The typical ohmic contact stack of Ti/Al/Ni/Au yields contact resistances in the range of 0.7 to 1.0 Ω·mm on AlGaN/GaN. There are many techniques studied to reduce the contact resistance. Processing techniques can be divided into three sections, all of which will be discussed, 1. pre-metallization 2. metal deposition and 3. post metal processing.

1.3.2. Ohmic Contact Pre-Metallization Processing

Pre-metallization processing includes any steps taken before metal-deposition. This includes any plasma exposures using reactive ion etching (RIE) with the aim of lowering resulting contact resistance and reducing the temperature required for ohmic behavior during annealing. $SiCl_4$ has been shown to decrease ohmic contact resistance on both InAlN [6, 7] and AlGaN [8, 9] by creating defects in the semiconductor such as nitrogen vacancies, which act as n-type carriers. For example, as reported in [7], using a low temperature anneal (600° C) for the Ti/Al/Ni/Au stack, the authors compared the contacts with and without RIE treatment which resulted in a contact resistance of 1 and 12 Ω·mm, respectively. However, $SiCl_4$ is not a commonly used gas and so may be unavailable for use in many cleanroom facilities. Thus, there are other reported plasma chemistries used to achieve the same effect. Various reported etching properties are summarized on Table I. Most processes reported utilize a very slow etch rate or no etching in the case of [10] to create the defects necessary for successful ohmic contacts. In many of the reported cases, the authors report a contact resistance < 0.5 Ω·mm, however, low-temperature annealing is not always achieved, or perhaps, not reported.

Table I List of reported reactive ion etching process parameters which may be used for ohmic contact pre-metallization treatment on GaN.

Ref	*Etching Tool*	*Plasma Chemistry*	*Gas Flow Rates (sccm)*	*Process Pressure (mTorr)*	*ICP/RF Power (or Voltage)*	*Etch Rate (Å/min)*	*Substrate*	*Metal Stack*	*Annealing Temperature (C)*	*Contact Resistance (Ω·mm)*
[11]	Samco 200iP ICP-RIE	SiCl4	3	1.9	50/20 W	12.5	GaN and AlGaN	N/A	N/A	N/A
[10]	Samco 200iP ICP-RIE	BCl3 SiCl4	5	1.9	100/0 W	0	GaN(cap)/AlGaN/GaN	Ti/Al/Ni/Au	870°	0.41 0.17
[12]	Oxford PlasmaLab RIE	SiCl4	10	25	0/-300 V	N/A	GaN and AlGaN/GaN	N/A	N/A	N/A
[13]	N/A	Cl2	10	5	60 W/-300 V	6	AlGaN/GaN	Ti/Al/Ni/Au	870°	0.27
[8]	N/A	SiCl4	10	25	0/-100 V to 400V	N/A	AlGaN/GaN	Ti/Al/Mo/Au	850°	0.2
[9]	N/A	SiCl4	N/A	N/A	0/-300 V	N/A	AlGaN/GaN	Mo/Al/Mo/Au	500°	0.11
[6]	N/A	SiCl4	10	25	0/-300 V	N/A	InAlN/GaN	Mo/Al/Mo/Au	650°	0.15
[7]	N/A	SiCl4	N/A	N/A	N/A	N/A	InAlN/GaN	Ti/Al/Ni/Au	600°	1.0

Another elaborate process some researchers have reported using involve completely etching the barrier layer followed by regrowth using molecular beam epitaxy (MBE) of highly doped GaN and finally metallization using a simple structure, such as Ti/Au, with no annealing required. Some of the reported results are listed on Table II. The etching is achieved using a SiO_2 or SiN_x mask to completely etch the barrier layer by RIE. Afterwards, the sample is loading in a MBE system to regrow a highly-doped n-type GaN layer which is highly conductive (regrowth thickness was mentioned to be 40 nm). Next, a bilayer metal stack (e.g. Ti/Au) is deposited and patterned by the lift-off process followed by the removal of the etching mask. There is no high temperature processing required to form the ohmic contact and results in extremely low contact resistances in the range of 0.1 Ω·mm for InAlN/GaN. However, the process is rather complex and requires the costly operation of MBE.

Table II. Comparisons of recent ohmic contact schemes using the regrowth method for InAlN/GaN devices and their resulting contact resistance.

Ref	***Ohmic pre-metallization***	***Ohmic Metal Stack***	***Thermal Annealing Temperature (°C)***	***Contact Resistance (Ω·mm)***
[3]	n+-GaN regrowth	Mo/Au	Non-alloyed	0.1
[14]	n+-GaN regrowth	Ti/Au	Non-alloyed	0.16
[15]	n+-GaN regrowth	Ti/Au	Non-alloyed	0.16
[16]	n+-InGaN regrowth	N/A	N/A	0.13

1.3.3. Ohmic Contact Metal Deposition

After any pre-metallization processing are complete on the ohmic contact step, comes the metal deposition. Typically, metal deposition is accomplished by electron-beam evaporation which is a physical vapor deposition (PVD) process. Although sputtering is also available as an adequate deposition method, patterning of the films may prove to be difficult since the lift-off process is problematic with sputtered films and masked etching is difficult with so many layers present in the ohmic stack.

Design of respective thicknesses and ratio of the metal films are extremely important for low-contact resistance as previously mentioned. However, there are many reported metal stack variations with impressive results. For ease of discussion, I will divide the various contacts into 3 subsections with many results falling into other categories: gold free, complex structures (6 or more layers), and Si or Ge incorporation.

Gold-free contacts typically involve refractory metals (such as Ta, Hf, W) as a capping laying instead of gold. Some report successful results using the standard first two metals Ti/Al, while others report low resistance through some other variation using Ta. Some excellent reports with low contact resistances using gold-free processing is reported in Table III. As discussed previously, the contacts with plasma etching prior to metallization exhibits low temperature annealing required for ohmic behavior. Other contacts listed in the table require the typical high temperature of > 800° C.

Table III List of reported Gold-Free ohmic contacts on GaN semiconductors listed with their respective processing conditions and results.

Ref	*Pre-metallization treatment*	*Substrate*	*Metal Stack*	*Metal Thicknesses (nm)*	*Annealing Conditions*	*Contact Resistance (Ω·mm)*	*Specific Contact Resistance (Ω·cm2)*
[17]	Cl_2-based recess	GaN(cap)/AlGaN/GaN	Ta/Al/Ta	N/A	600°C for 240s in N_2	0.2	N/A
[18]	None	GaN(cap)/AlGaN/GaN	Ta/Si/Ti/Al/Ni/Ta	5/5/20/120/40/30	850°C for 30s in N_2	0.22	$0.78 \cdot 10^{-6}$
[19]	None	AlGaN/GaN	Ta/Si/Ti/Al/Ni/Ta	N/A	800°C for 30s in N_2	0.24	$1.25 \cdot 10^{-6}$
[20]	Recess	GaN(cap)/AlGaN/GaN	Ti/Al/W	60/100/30	870°C for 30s in N_2	0.49	$6.5 \cdot 10^{-6}$
[21]	None	GaN(cap)/AlGaN/GaN	Ti/Al/Ni/Pt	20/100/40/50	975°C for 30s in N_2	0.6	N/A
[22]	Recess	AlGaN/GaN/AlGaN	Ti/Al/TiN	N/A	550°C for 90s in N_2	0.62	N/A
[23]	None	AlGaN/GaN/AlGaN	Ti/Al/W	20/100/20	600°C for 60s in N_2	0.65	N/A
[24]	Cl_2-based recess	GaN(cap)/AlGaN/GaN	Ti/Al/Ti/TiN	30/150/30/50	600°C for 30s in N_2	0.81	N/A
[25]	None	AlGaN/GaN	Ti/Al/W	40/100/60	875°C for 30s in N_2	0.93	N/A
[26]	None	AlGaN/GaN	Ti/Al/Ti/TiN	20/120/45/120	870°C for 45s in N_2	2.1	$35 \cdot 10^{-6}$
[27, 28]	None	InAlN/GaN	Hf/Al/Ta	15/200/20	600°C	0.58	$6.75 \cdot 10^{-6}$
[29]	Cl_2/Ar-based recess	AlGaN/AlN/GaN	Ta/Al/Ta	20/280/100	N/A	.34	N/A
[30]	None	GaN(cap)/AlGaN/GaN	Ta/Al/Ta	10/280/20 10/140/20	550°C for 60s in N_2	.06 .26	N/A N/A
[31]	None	InAlN/AlN/GaN	Ta/Al/Ta	N/A	550°C in N_2	0.64	N/A
[17]	Cl_2-based recessed ohmic	GaN(cap)/AlGaN/GaN	Ta/Al/Ta	3.5/100/10	<600°C for 4min in N_2	0.2	N/A

Besides gold-free ohmic contacts, another method to reduce the contact resistance is by inserting a thin layer of either Si or Ge in the stack. Silicon and Germanium are both n-type dopants for GaN with specific growth conditions. During MOVPE epitaxial growth of n^+-GaN, silane (SiH_4) or the more reactive disilane (Si_2H_6) gases are used to obtain a Si-doped layer. For Ge-doping, GeH_4 gas is commonly used, although it has been shown it is 10 times less efficient doping compared to Silicon [32]. Similar results were shown for MOCVD growth [33]. Since Si and Ge are typical n-type dopants for GaN, inserting these materials in the metal stack may lead to diffusion of carriers into the substrate leading to better ohmic contacts. There have been several structures studied and are summarized on . For some reported technologies, depositing Si or Ge prior to metal stack results in better contacts, while in others, deposition as the second layer shows better results. The following references also consider several other variables such as thicknesses, annealing temperatures and thus, only the best results from each study are tabulated.

Table IV List of ohmic contacts on GaN using either Si or Ge to improve the contact resistance.

Ref	*Pre-metallization treatment*	*Substrate*	*Metal Stack*	*Metal Thickness (nm)*	*Annealing Conditions*	*Contact Resistance (Ω·mm)*	*Specific Contact Resistance ($Ω·cm^2$)*
[18]	None	GaN(cap)/AlGaN/GaN	Ta/Si/Ti/Al/Ni/Ta	5/5/20/120/40/30	850°C for 30s in N_2	0.22	$0.78 \cdot 10^{-6}$
[19]	None	AlGaN/GaN	Ta/Si/Ti/Al/Ni/Ta	N/A	800°C for 30s in N_2	0.24	$1.25 \cdot 10^{-6}$
[34]	Cl_4-based recessed ohmic	Si-doped GaN	Ge/Cu/Ge	N/A	600°C for 60s in N_2 (>400°C ohmic)	N/A	$10 \cdot 10^{-6}$
[19]	None	AlGaN/GaN	Ta/Si/Ti/Al/Ni/Ta	N/A	800°C for 30s in N_2	0.24	$1.25 \cdot 10^{-6}$
[35]	None	InAlN/GaN	Ti/Si/Al/Si/Mo/Au	N/A	850°C for 30s in N_2	0.12	$0.387 \cdot 10^{-6}$
[36]	None	GaN(cap)/AlGaN/AlN/GaN	Si/Ti/Al/Mo/Au	5/20/80/35/50	780°C for 60s in N_2	0.45	N/A
[37]	$SiCl_4$ exposure	AlGaN/GaN	Ti/Si/Al/Si/Mo/Au	15/10/60/10/35/50	850°C for 30s in N_2	0.16	$0.677 \cdot 10^{-6}$
[38]	$SiCl_4$ exposure	AlGaN/GaN	Si/Ti/Al/Mo/Au	5/15/60/35/50	850°C for 30s in N_2	0.31	N/A
[39]	None	n^+AlGaN/AlGaN/GaN	Si/Ti/Al/Cu/Au	3/85/50/80/100	800°C for 30s in N_2	N/A	$38 \cdot 10^{-6}$
[40]	None	GaN(cap)/AlGaN/GaN	Si/Ti/Al/Mo/Au	1/15/90/45/55	800°C for 30s	0.18	$1 \cdot 10^{-6}$
[41]	none	InAlN/GaN	Si/Ti/Al/Ni/Au	2/20/100/40/50	840°C for 15s in N_2	0.30	N/A
	Cl_2-based recessed ohmic				835°C for 15s in N_2	0.34	
		InAlGaN/GaN			860°C for 18s in N_2	0.23	
	none					0.31	
[42]	None	AlGaN/GaN	Si/Ti/Al/Ni/Au	N/A	800°C for 30s	0.23	$1.06 \cdot 10^{-6}$

1.3.4. Ohmic post-metal processing

Lastly, post metal processing is also extremely important to achieve low-contact resistance. As noted earlier, a high temperature annealing is required to induce ohmic behavior and as we have seen in the previous sections, there are several different temperatures research groups have found has worked for them. It is desirable to refrain from any processing with temperatures >870° C as damage to the 2DEG becomes highly unstable, thus limiting its' performance as a transistor. The amount of time the contacts are annealed are also important. Typically, this ranges from 15 s up to 1 or 2 min. Although some researchers have reported a two-step annealing process yields better results [43], more commonly a single step is sufficient and desirable. Lastly, ambient gas during annealing plays a key role as well. Most modern-day rapid thermal annealing systems have the options of N_2, Ar, O_2, forming gas (N_2/H_2) and vacuum as the ambient condition. There are several reports using the first three mentioned gases (N_2, Ar and O_2) but limited information on those using vacuum.

To conclude, there is many variables when developing the process for ohmic contacts on GaN. The most important goals to consider include: low-contact resistance, low-temperature annealing, gold-free technology and 'smooth' surface morphology. The best reports thus far utilize GaN-regrowth using MBE to yield contact resistance as low as 0.1 Ω·mm on InAlN/GaN [3, 14, 15], however, the high cost associated with operation of MBE yields it impractical.

1.4. Introduction to Dielectrics

1.4.1. Background on interface trap density extraction

In the metal-oxide-semiconductor field effect transistor (MOSFET) structure, the oxide layer plays a key role on transistor performance. In the early days of semiconductor research, Silicon dominated the market since it had an excellent ability to grow a highly stable and compatible oxide layer, i.e. SiO_2. Exposure of a clean Silicon lattice to oxygen ambient, either by water vapor or O_2 gas (i.e. wet or dry oxidation), consumes part of the Silicon structure to form SiO_2 compound. This compound is an excellent insulator with the obvious purpose to use in the MOSFET structure. Moreover, the number of defects at the interface between Si-SiO_2 is of excellent quality. However, GaN does not share these qualities, thus, other types of insulators have been widely studied. As researchers began fabricating and measuring GaN-based MISHFETs, they found that the electrical measurements exhibit peculiar negative effects such as current collapse [44], threshold voltage instability and degradation of 2DEG mobility [45]. They attributed these negative effects to the defects at the oxide/semiconductor interface.

But what are defects and how can we measure the 'amount' of defects? Professor Dieter K. Shroder has written an excellent book describing these defects in [46] in Chapter 6. There are 4 types of defect charges in an oxide-semiconductor system, they include fixed, mobile and trapped oxide charges and interface trapped charge. The first three are within the oxide layer and some are mobile while others are fixed. These are primarily caused by growth conditions and impurities in the film. The other type of defects is interface trapped charges, which I focused my most attention to. Focusing on the atomic structure of the oxide/semiconductor layer, at the transition region (i.e. interface) there is a large density of defects present. These defects are cause by a combination of contaminants and dangling bonds (un-liked atoms in the structure). In effect, the

defects present electron/hole trap centers which will negatively influence electrical performance of the device.

There are both qualitative and quantitative methods to probe the traps at the interface. The number of traps is typically reported in amount per unit area per energy ($cm^{-2}eV^{-1}$). These values physically correspond the number of traps in a unit area at a certain energy level within the semiconductor's bandgap. Different levels of energy correspond to different response times of the traps. Shallow traps, i.e. traps close to the band edges, respond quickly to electrical signals which in turn affects high-frequency operations of a device while deep level traps require more time to charge/discharge affecting mostly DC (direct current) operation.

1.4.2. Metal-Insulator-Semiconductor Capacitor

A powerful structure to determine the number of defects present is the Metal-Oxide-Semiconductor (MOS) capacitor. The device layout can be either of a vertical structure (more for Si-based capacitors) where the gate electrode is patterned on top of the oxide on silicon. The back of the wafer is typically used as the semiconductor contact node. The typical structure for Si-based capacitor is shown in Figure 2 as a cross-sectional schematic. In the case of GaN, however, the substrate is typically insulating so the capacitor must be laterally fabricated. The cross-sectional schematic is shown on Figure 3. This structure consists of an outer circular ohmic contact to the semiconductor. The inner portion contains the insulator with a metal circular electrode deposited on top of the oxide to form the Metal-Insulator-Semiconductor Heterostructure (MISH) capacitor, or MISH-Cap. The oxide layer refers to oxidized materials such as SiO_2, Al_2O_3, HfO_2, etc. while insulators is a more general term which includes other insulating materials such as Si_3N_4.

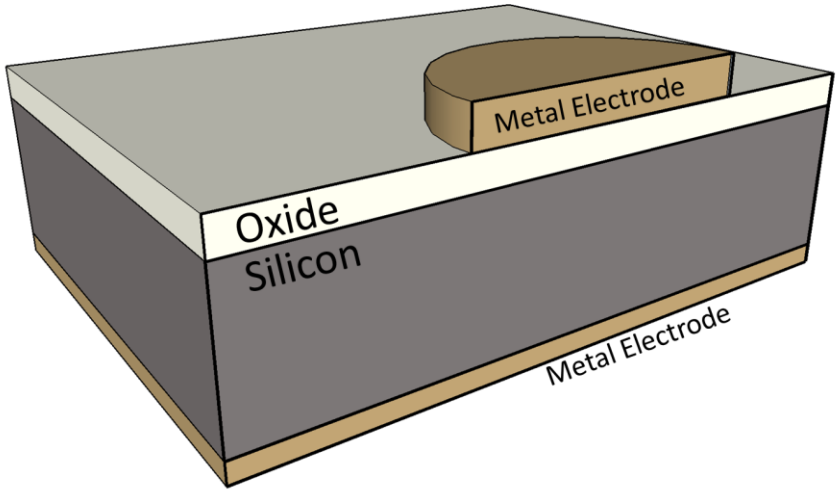


Figure 2 Cross-sectional schematic of a vertical Metal-Oxide-Semiconductor (MOS) capacitor structure typically fabricated for Si-based devices

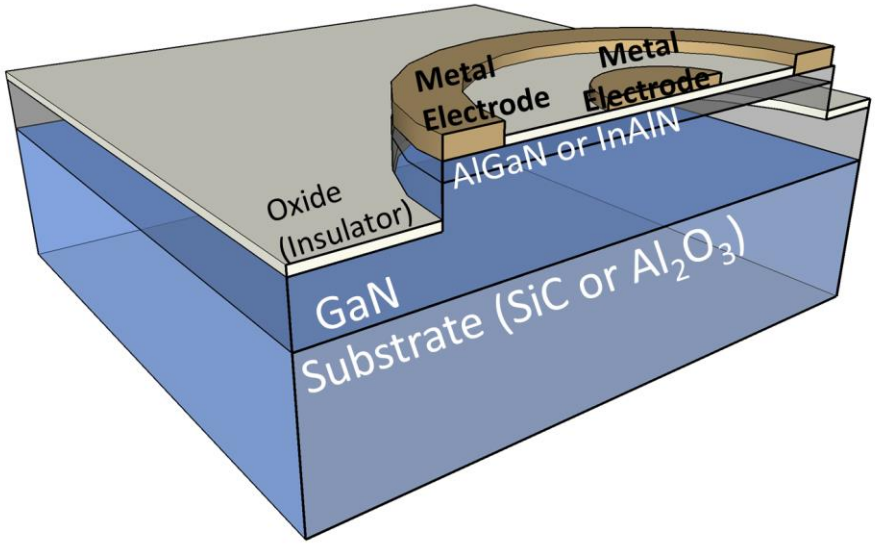


Figure 3 Cross-sectional schematic of a lateral Metal-Oxide (or Insulator)-Semiconductor Heterostructure (MOSH or MISH) capacitor structure typically fabricated for GaN-based devices.

The capacitor allows you to sweep a wide DC voltage bias range while using a small AC-signal at various frequencies to gather many device and process parameters. Again, I refer you to Schroder's book to learn more [46] about the subject as I will cover the interface trap density extraction methods here.

There are several methods applicable to Si-based MOS capacitors utilized to extract interface trap density through *C-V* (capacitance-voltage) sweeps. In a Si MOS capacitor, sweeping the voltage takes you into three regions as shown in Figure 4 (depicted for the low-frequency sweep). The first is accumulation where you accumulate carriers to the oxide/semiconductor interface. At this region, the carriers form a parallel plate capacitor with the oxide being the capacitor's dielectric medium. Here, you can extract parameters such as dielectric constant, oxide defects, oxide strength, etc. As you sweep the voltage, you will encounter a slope in the curve where the capacitance suddenly drops. This corresponds to the depletion region where the majority carriers are quickly repelled by the electric field. After the quick transition, the semiconductor eventually reaches inversion mode when a large amount of minority carriers has replaced the majority carriers in the semiconductor. By manipulating the AC frequency, the sweep can reveal the amount of traps by using various methods such as the Berglund Integral or the Terman Methods [46, 47]. However, methods that apply to Si-based MOS structures, may not apply to GaN because of its' wide-bandgap nature. For GaN-based MISH structures, the curve is much different. Take a HfO_2/AlGaN/GaN MISH structure for example. When sweeping voltage, you encounter a few different regions in the C-V sweep as shown in Figure 4. First, it is the deep depletion region. Instead of finding an inversion region such as in the case of Si-capacitors, the system goes into deep depletion mode since GaN has a very long minority carrier generation time constant due to its' wide bandgap nature. Next, you encounter a slope, the depletion region. Sweeping the voltage

further leads you to the accumulation of carriers at the first interface, the AlGaN/GaN heterostructure 2DEG. At this region, the total capacitance is a series sum of capacitances due to the insulator layer and the barrier layer. Increasing the voltage further, you will encounter a second slope. This increase in capacitance is due to the electron spill-over through the barrier layer and into the insulator/semiconductor interface.

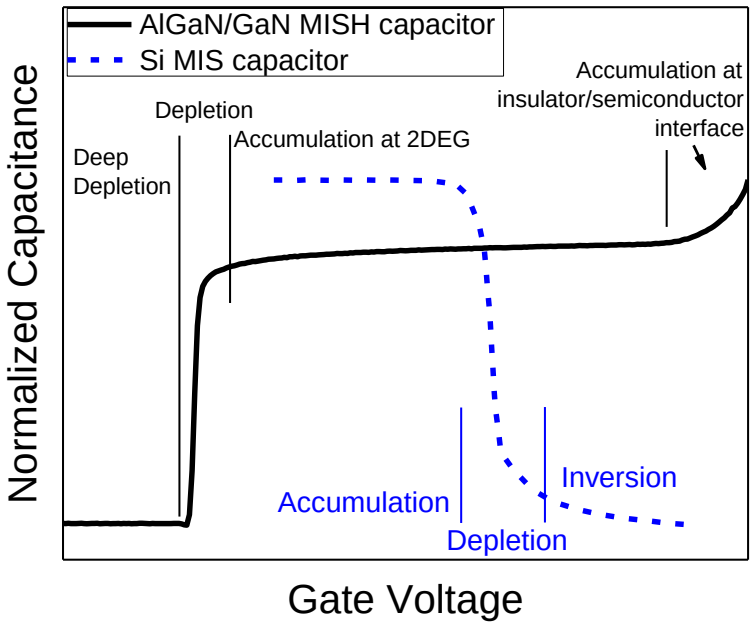


Figure 4 Comparison of a 100 kHz capacitance-voltage sweep of a HfO_2/AlGaN/GaN MISH-capacitor (black curve) with a HfO_2/Si MIS-capacitor (blue curve).

Now, to extract interface trap density in a GaN MISH system, there are a few popular methods. The most straight-forward and simplest method comparers the frequency dispersion in

a C-V sweep [48-50]. The dispersion that is compared is within the 2nd slope on the complete curve; i.e. during the accumulation of carriers at the insulator/semiconductor interface. Based on the onset voltage shift in the 2nd slope, Dit values can be calculated for an averaged energy range (E_{avg}) using the following equations:

$$D_{it} = \left(\frac{\varepsilon_0 \kappa}{t_{ox}}\right)\left(\frac{1}{q}\right)\left(\frac{\Delta \mathrm{V}}{\Delta E}\right) = C_{ox}\left(\frac{1}{q}\right)\left(\frac{\Delta \mathrm{V}}{\Delta E}\right)$$

$$\Delta E = kTln(\frac{f_i}{f_{i+1}})$$

where q is the elemental electron charge, $\Delta \mathrm{V}$ is the measured voltage hysteresis between two different frequency sweeps, ΔE is the corresponding trap energy difference based on the measurement frequencies f_i and f_{i+1}, k is Boltzmann's constant, and T is measurement temperature. Next, the average activation energy of the traps can be calculated using:

$$E_{avg} = E_i + \frac{\Delta E}{2}$$

$$E_i = kTln\left(\frac{\sigma_c N_C v}{2\pi f_i}\right)$$

where E_i is the trap activation energy at frequency f_i, σ_c is the interface traps capture cross section, N_C is the effective density of states in the barrier conduction band, and v is the thermal velocity of electrons in GaN. There are several limitations, however, with this simplistic approach. Foremost, this method only gives you an average value within a wide activation energy range so there is no idea on the distribution of traps within the bandgap. Secondly, this method is best for slow-responding traps (traps a few kT eV away from the band edges), corresponding to AC-frequencies < 100 kHz.

To get a better picture of the distribution of traps within the bandgap, there is another popular approach called the conduction method and the steps are summarized in Appendix D.2.

The conductance method, on the other hand, retrieves trap density by varying frequency and measuring the capacitance and conductance of the capacitor. The traps with time constants lower than 1/ω will not respond to the signal while those with larger time constants will contribute to the measured conductance. From this concept, it is possible to extract trap time constant and trap density. Based on frequency dependent C-V measurements, the conductance is fitted to the following model:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau}\ln[1 + (\omega\tau)^2]$$

where G_p is the conductance, ω is the radial frequency, Dit is the trap density, τ is the trap state time constant, and q is the elementary charge. Once the trap state time constant are fitted, trap state energy level as a function of trap time constant can be calculated using the following equation:

$$E_T = kTln(\sigma N_C v_t \tau)$$

where σ is the capture cross section, N_c is the density of states in the conduction band, v_t is the thermal velocity, E_T is the trap state energy below the conduction band, k is Boltzmann's constant, and T is temperature. Once the above information is gathered, it is possible to plot trap density as a function of energy. This method typically only measures trap density in about 0.25 eV below the conduction band. Comparing it to the C-V frequency dispersion method, conductance reveals trap distribution within the bandgap. This method is best for fast-traps, i.e. shallow traps within a few kT eV away from the band edge. To get more information from deeper level traps, some form of external stimuli is necessary to generate minority carriers. One viable option is by measuring at the conductance at different temperatures. Cooling the device below 25° C would reveal traps closer to the band edges while increasing the temperature would stimulate deep-level traps, thereby obtaining a better trap distribution within the bandgap. Figure 5 shows

the activation energy range that is revealed using the temperature-variation conduction method. As we can see, this method reveals more information on trap distribution, but the bandgap of GaN is 3.4 eV and this method only reveals a fraction of the bandgap. So, what about mid-gap level states? Increasing the temperature further can improve the range but should be avoided considering the high temperature may cause irreversible damage to the device. Thus, another method is required.

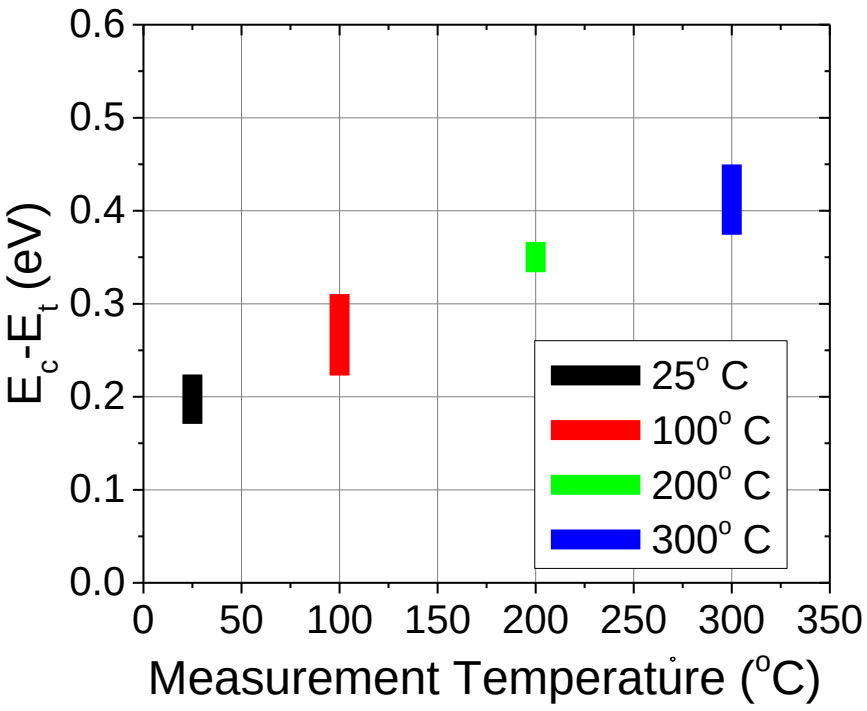


Figure 5 Interface trap density activation energy distribution profile within AlGaN bandgap revealed using temperature-varied conductance method.

Another type of external stimuli that may be applied is photons. A popular method using this approach is called photo-assisted C-V method. Photo-assisted C-V method relies on a photon source to generate carriers to fill traps within the band gap [51-55]. Comparing a post-illuminated C-V curve to a sweep done in the dark will reveal a hysteresis. Based on this hysteresis, it is possible to calculate interface trap density within the photon's energy range. This method is an excellent way to estimate near-midgap interface states.

The process is as follows: sweep voltage from accumulation to depletion in the dark. At depletion, shine photons on the sample with energy less than the band gap for a moment in order to ionize the interface states. Turn off the light and sweep back to accumulation in the dark. This measurement will produce a hysteresis in the C-V curves. Based on this hysteresis, one can calculate average interface trap density within the energy of the photon source used with the following equation:

$$D_{it} = \frac{C_{Total} * \Delta V}{q * \Delta hv}$$

Where C_{Total} is the series capacitance of the dielectric layer and the barrier layer, ΔV is the hysteresis voltage, q is the charge of the electron and Δhv is the energy of the photon. Since only the average trap density within the energy range of the photon source is calculated, a variety of light sources (wavelengths) will yield more detailed results. For example, using a light source with band-pass filters 1.26 (984 nm) <= hv <=2.43 eV (510 nm) would be sufficient to reveal traps 1 to 2 eV from the conduction band edge of AlGaN [51].

In summary, there are several techniques utilized to measure interface trap densities of insulators on GaN materials. More attention in the extraction method is required for wide-bandgap materials such as GaN to reveal an accurate trap distribution. C-V frequency dispersion is a 'rough' analysis technique to estimate the average trap densities. Conductance method is a more

refined technique to reveal trap distribution within a limited drain. Lastly, utilizing heat or photon-assisted methods allows for probing of deep-level traps. A U-shaped distribution of interface trap charges within the band-gap is expected [46] with highest trap density close to the conduction/valence band edges.

1.4.3. High-κ Dielectrics

In the previous section, we covered methods to measure interface trap densities of insulators on GaN. Now, we will review several materials reported in literature and what makes an insulator adequate. There are countless materials researches have studied to use as an insulator for transistors but there are a few key properties to aim for. First off, one of the most important parameters is the dielectric constant, or relative permittivity, often symbolized as κ. This value is a property of a material and represents the ability to maintain an electric field. In a metal-insulator-semiconductor (MIS) structure, the value is directly proportional to the capacitance seen at the gate as shown in the following equation:

$$C = \frac{\kappa \varepsilon_0 A}{t_{insulator}}$$

where C is the gate capacitance, κ is the dielectric constant of the insulator, ε_0 is the permittivity of vacuum, A is the area of the gate and $t_{insulator}$ is the thickness of the insulator layer. Depending on the application, a high-κ material is often desired. In the case of ultra-scaled Si-CMOS in Intel's Core i7 processors, for example, a high-κ material such as HfO_2 is desirable to maintain a low Equivalent Oxide Thickness (EOT). However, in the case of GaN MISHFETs, a high-κ insulator is desirable to maintain maximum channel control, increase AC transconductance [56] and minimize threshold voltage shift [57]. This property is often material dependent but it can vary due to growth conditions, crystallinity and stoichiometry.

Another important property is the bandgap of the insulator. It is important to have a large bandgap to be able to maintain adequate conduction and valence band offsets to the semiconductor, thereby reducing the probability of leakage current. Silicon has a very small bandgap of 1.12 eV, so it is very easy to find compatible insulator with wide enough band offsets, such as SiO_2 (which has bandgap of 9 eV) or Si_3N_4 (bandgap of 4 eV). However, in the case of GaN (bandgap of 3.4

eV), the selection become extremely limited. To make matters worse, insulator's bandgaps are typically inversely proportional to the dielectric constants so there is often a trade-off associated.

One of the target markets for GaN-transistors is high-power electronics. Thus, the device must be able to handle large electric fields without breakdown. This also includes the insulator breakdown strength, often termed dielectric strength. The dielectric strength of a material is often given in [MV/cm] units. Typical gate insulation layers are on the order of 10's of nanometers, thus, the insulator must have a large breakdown strength > 4 MV/cm to prevent premature breakdown of the device.

Beyond electrical performance metrics for insulators, there are also some material aspects to consider. It has been repeatedly shown that polycrystalline or crystalline insulators exhibit higher leakage current than their amorphous counterparts [58, 59]. They found that the grains provide a leakage path, thereby increasing the power consumption of the device on the gate side. Thus, it is preferred to maintain amorphous structure for the insulator. However, this can prove to be difficult for some materials. It is possible to induce polycrystalline structures during growth/deposition of the film or by any high-temperature processing of the device. For some materials, the transformation can be as low as 370° C, for TiO_2 [60], or as high as 900° C, for Al_2O_3 [61]. Thus, careful design of process flow must consider this.

Lastly, a highly important aspect, which we covered in the last section, is the interface traps/defects. It is desirable to maintain a low interface trap density to reduce electrical performance degradation. This can be dependent on either processing, material deposition/growth technique, or the material itself. Before depositing the insulator, it is important to prep that GaN surface to reduce the number of defects present [62, 63]. There are several techniques reported in literature to accomplish that such as ozone cleaning [62], hydrofluoric acid (HF) dip [64],

hydrochloric acid (HCl) dip [65], etc. [66]. Deposition technique can vary such as sputtering, chemical vapor deposition, oxidation or, the more popular, atomic layer deposition. Atomic layer deposition is a highly conformal process which gives you precise control down to one atomic layer of deposition at a time [67]. ALD typically may result in much better film quality than the other deposition techniques. Table V lists the more commonly used insulators on GaN and their extracted interface trap densities. HfO_2 and Al_2O_3 are commonly used for gate insulation due to their relatively high dielectric constant, large temperature stability and low defect densities on GaN.

Table V List of various insulators deposited on GaN-materials and their respective extracted interface trap densities. Listed, is also the D_{it} extraction technique.

Structure	***Characterization Method***	***Interfacial Trap Density ($cm^{-2}eV^{-1}$)***	***Ref.***
Al_2O_3/GaN	Terman	$(5\text{-}8)\cdot10^{11}$	[68]
HfO_2/GaN	Terman	$(7\text{-}11)\cdot10^{11}$	[68]
HfO_2/ Al_2O_3/GaN	Terman	$(5\text{-}10)\cdot10^{11}$	[68]
Al_2O_3/AlGaN	Photo-assisted *C-V*	$(4\text{-}50)\cdot10^{12}$	[53]
Al_2O_3/AlGaN	Photo-assisted *C-V*	$(7\text{-}10)\cdot10^{11}$	[51]
Al_2O_3/AlGaN	Photo-assisted *C-V*	$(1\text{-}3)\cdot10^{12}$	[52]
AlN/AlGaN	Conductance	$(5\text{-}25)\cdot10^{12}$	[69]
Al_2O_3/AlGaN	Conductance	$(0.3\text{-}10)\cdot10^{11}$	[70]
Al_2O_3/AlGaN	Conductance	$(2\text{-}15)\cdot10^{11}$	[71]
Al_2O_3/AlGaN	Conductance	$(2\text{-}23)\cdot 10^{12}$	[72]
Al_2O_3/InAlN	Capacitance-time transients	$3\cdot10^{13}$	[73]
ZrO_2/InAlN	Capacitance-time transients	$1\cdot10^{13}$	[73]

To summarize, an ideal insulator for gate dielectric should exhibit the following properties: large bandgap to maintain large conduction/valence band offsets to GaN, high temperature stability to maintain amorphous structure, high dielectric constant to maintain maximum channel control (transconductance), large breakdown strength and low defect densities.

1.4.4. Atomic Layer Deposition Basics

Atomic layer deposition is a popular method used to deposit high-quality insulators. Typical setups require at least two precursors: the metal source such as Tetrakis(dimethylamido)hafnium (TDMAHf) used for Hf and an oxidizer source such as H_2O vapor. The sample is loaded in a high-vacuum chamber and heated to an appropriate temperature, typically between 100° to 300° C. The heater source may be either a hot-wall chamber, a chuck-heater or a combination of both. A carrier gas, such as N_2, is used to flood the chamber with the metal-precursor using fast (milliseconds) pulsing valves. The material saturates the surfaces in a conformal and self-limiting matter everywhere in the chamber. Thereafter, the carrier gas is used to purge the chamber to remove excess material. Next, water vapor is pulsed into the system to form the HfO_2 compound and by-products. The by-products are then purged from the system completing one full ALD cycle. This cycle is typically ≈1 Å thick, thus to achieve the final desired thickness, the cycles are repeated. Since ALD is a very slow process compared to other deposition methods such as sputtering, films thicker than 75 nm, although possible, are not practical to deposit.

2. OHMIC CONTACT OPTIMIZATION

An optimized ohmic contact on GaN is necessary to improve transistor performance and reduce power consumption. Thus, much effort was directed towards optimizing the recipe. We first started with verifying the deposition rates of the materials using Nanotechnology Core Facility's Varian Electron-Beam Evaporation system. The materials of interest were as follows: Si, Ti, Al, Ni, Au, Hf, Ta, Mo. Physical vapor deposition systems are often equipped with a quartz crystal microbalance, also known as the crystal monitor, directed in the line-of-sight of the source material. The crystal monitor senses the material deposited by monitoring the resonant frequency, which changes with accumulated material. To accurately determine the thickness, three parameters are required: Density, Z-ratio, and tooling factor. Density of the metal is a material parameter given in g/cm^3 and Z-ratio corresponds to the acoustic impedance of the material, both are tabulated values easily found on the internet. Tooling factor, however, depends on the tool-set up (i.e. where samples are loaded, where the crystal monitor is located, process pressure). To verify (and calibrate for some newer metals) the deposition on the system, I did several test runs to determine the tooling factor for each material. I first had some pre-patterned Si-test samples prepared for metal-liftoff process. Next, I deposited several tens of nanometers of material and measured the thickness after lift-off using either atomic force microscopy (AFM) or using a stylus Profilometer. Afterwards, tooling factor becomes updated using the following equation:

$$TF_{updated} = TF_{initial} \frac{t_{expected}}{t_{actual}}$$

It is important to accurately determine deposition to insure reproducibility. In Table VI, I show the initial deposition test run of each material with the updated tooling factor. After several test runs, under 'Final Test Run', I list the final updated tooling factor based on accurate deposition rate measured.

Table VI Deposition rate calibration on the Varian E-Beam evaporator.

			1st Test Run				***Final Test Run***		
Metal	Density (g/cm^3)	Z-Ratio	Initial Tooling Factor (%)	Target Thickness (Å)	Actual Thickness (Å)	Updated Tooling Factor (%)	Target Thickness (Å)	Actual Thickness (Å)	Updated Tooling Factor (%)
Al	2.70	1.08	129	400	506	164	2800	2440	143
Au	19.3	0.381	179	100	90	161	-	-	-
Hf	13.09	0.36	180	300	406	243	-	-	-
Mo	10.2	0.257	100	300	690	230	900	949	198
Ni	8.91	0.331	-	-	-	-	-	-	-
Si	2.32	0.712	180	200	288	259	200	188	243
Ta	16.6	0.262	185	251	367	270	200	197	272
Ti	4.50	0.628	170	300	317	179	100	90	161

2.1. Titanium/Aluminum for Ohmic Contacts

After determining deposition rates of each material, we began by first optimizing the Ti:Al ratio and thicknesses in the standard stack Ti/Al/Mo/Au. We used AlGaN/GaN substrates for this process patterned by lift-off process and dipped in buffered oxide etch (BOE) 20:1 for 30 s followed by deionized water rinse and N_2 blow drying prior to metallization. We held the Mo and Au thicknesses constant at 45 and 55 nm, respectively. For the Ti and Al, we tested two different ratios, 1:5 and 1:6 with various thicknesses as shown on Table VII.

Table VII List of the two different Ti:Al ratios used (1:5 and 1:6) and the tested respective thicknesses for ohmic contacts using the Ti/Al/Mo/Au standard stack.

	1:5 Ratio	***1:6 Ratio***
Ti/Al Thickness (nm)	25/125	10/60
	30/150	15/90
	35/175	20/120

Next, we held annealing conditions constant for all the samples and annealed at 800° C in N_2 ambient for 30 s. The best measured contact resistances are shown in Figure 6. I found that a ratio of 1:6 showed the best results throughout the whole measured thicknesses range. Moreover, using a Ti/Al thickness of 15/90 nm showed the lowest contact resistance of ≈ 1.5 Ω·mm.

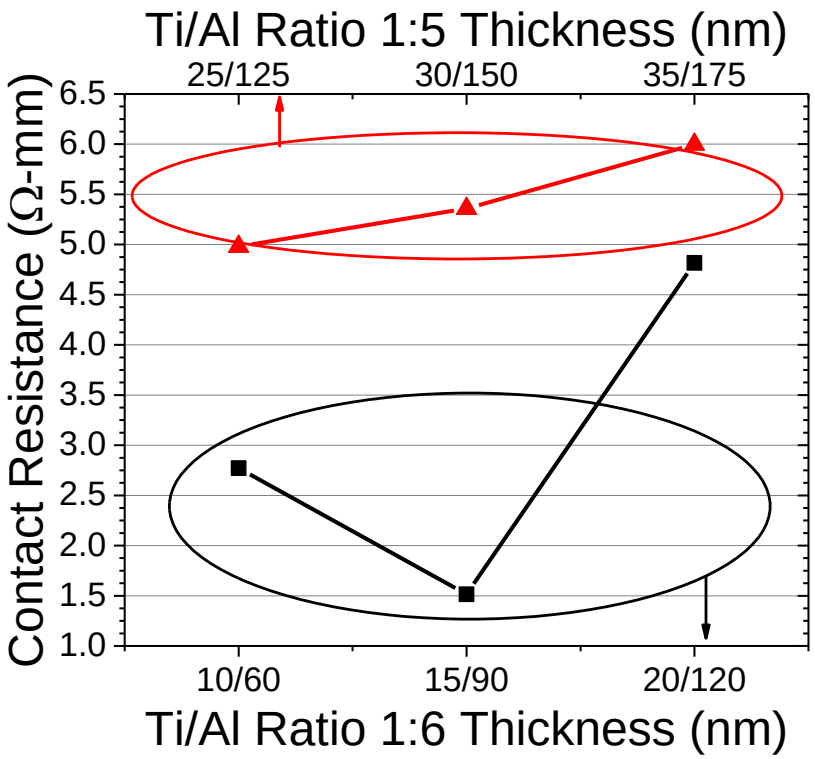


Figure 6 Optimizing the Ti:Al ratio and thicknesses. All samples were annealed under the same conditions and the best measured contact resistances are shown.

The next step was to determine the optimal annealing temperature using the Ti/Al/Mo/Au (15/90/45/55 nm) stack. The three variables during annealing were temperature, time and ambient. We varied the former from 750° to 850° C while keeping the time and ambient constant for 30 s in N_2, respectively. As shown in Figure 7, the best results were found for an annealing at 800° C.

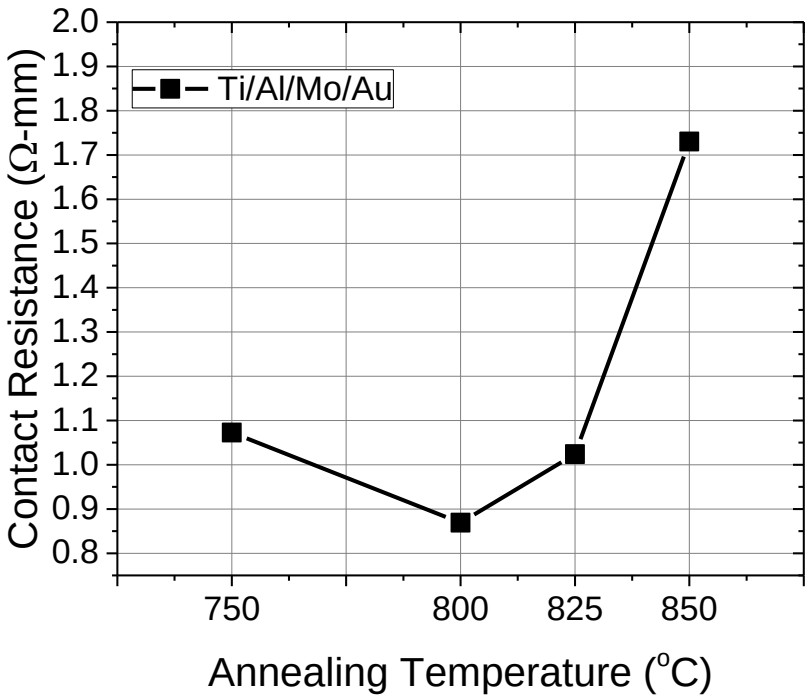


Figure 7 Optimizing the annealing temperature for the Ti/Al/Mo/Au ohmic contact scheme. Annealing temperature was varied while time and ambient were held constant for 30 s in N_2, respectively.

We found that the contact resistance using Ti/Al/Mo/Au was rather high and inconsistent. Thus, we studied which diffusion barrier layer (3rd layer in the stack) exhibits better contact resistances, either Ni or Mo, two of the more popular choices. We found that using Ni instead of Mo consistently showed lower contact resistances both annealed at 800° C for 30 s in N_2 ambient. For the Ti/Al/Mo/Au (15/90/45/55 nm) stack, we previously found a contact resistance of 0.87 Ω·mm but when we replaced Mo with Ni, the contact resistance decreased to 0.75 Ω·mm. I believe the contact resistance is lower and more consistent using Ni because deposition of the Mo material

exposes the substrate to high-temperatures due to it having a high-melting point. However, perhaps a system which has better substrate heat dissipation will yield different results.

2.2. Silicon in Ti/Al/Ni/Au Stack

At this point, we have optimized the standard ohmic contact processing using the following parameters: pre-patterned AlGaN/GaN substrates for lift-off, BOE 20:1 dip for 30 s followed by DI rinse, metallization of Ti/Al/Ni/Au (15/90/45/55 nm) and annealed at 800° C for 30 s in N_2 ambient to obtain a contact resistance of 0.75 Ω·mm. However, this value is commonly reported. So I studied methods to further reduce this value. Depositing Si in the standard stack has shown promising results, however, there is many variations reported in literature. We studied inserting Si either as the first layer in the stack (Si/Ti/Al/Ni/Au) or the second layer (Ti/Si/Al/Ni/Au). We also determined if using 2 nm or 1 nm of Si yields better results. We purchased Si-source material from Materion and is un-doped high resistivity Silicon of 99.999% purity. The Varian e-beam evaporator system only has 4 pockets available, so we needed to break vacuum in the process to replace a crucible. We opened the chamber quickly after depositing Ti since it had largest heat of formation of its' oxide. We first tested using 2 nm of Si as the first layer, i.e. Si/Ti/Al/Ni/Au (2/15/90/45/55 nm). For this case, we varied the annealing temperature and annealing time as shown in Figure 8. We found the optimal temperature was 825° C and the optimal time 15 s. From this run, the lowest contact resistance was 0.75 Ω·mm, no difference compared to the standard stack without the Si-layer.

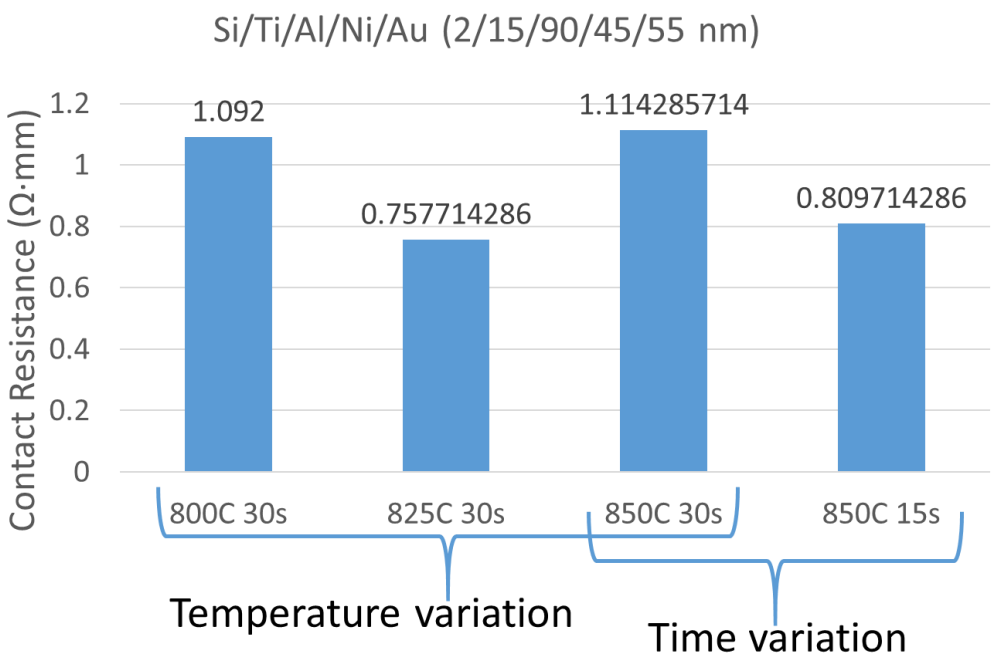


Figure 8 Optimizing the Si/Ti/Al/Ni/Au (2/15/90/45/55 nm) ohmic contact annealing conditions on AlGaN/GaN.

Instead of using 2 nm of Si, we decreased the thickness to 1 nm since we had high contact resistances. Next, we tried using Si as the second layer in the stack, i.e. Ti/Si/Al/Ni/Au (15/1/90/45/55 nm). We compared annealing for 15 s and 30 s from 800° to 850° C and the results are plotted on Figure 9. For both times used, 825° C showed the minimum contact resistance, however, 15 seconds showed the lowest of the two at 0.72 Ω·mm, the best so far.

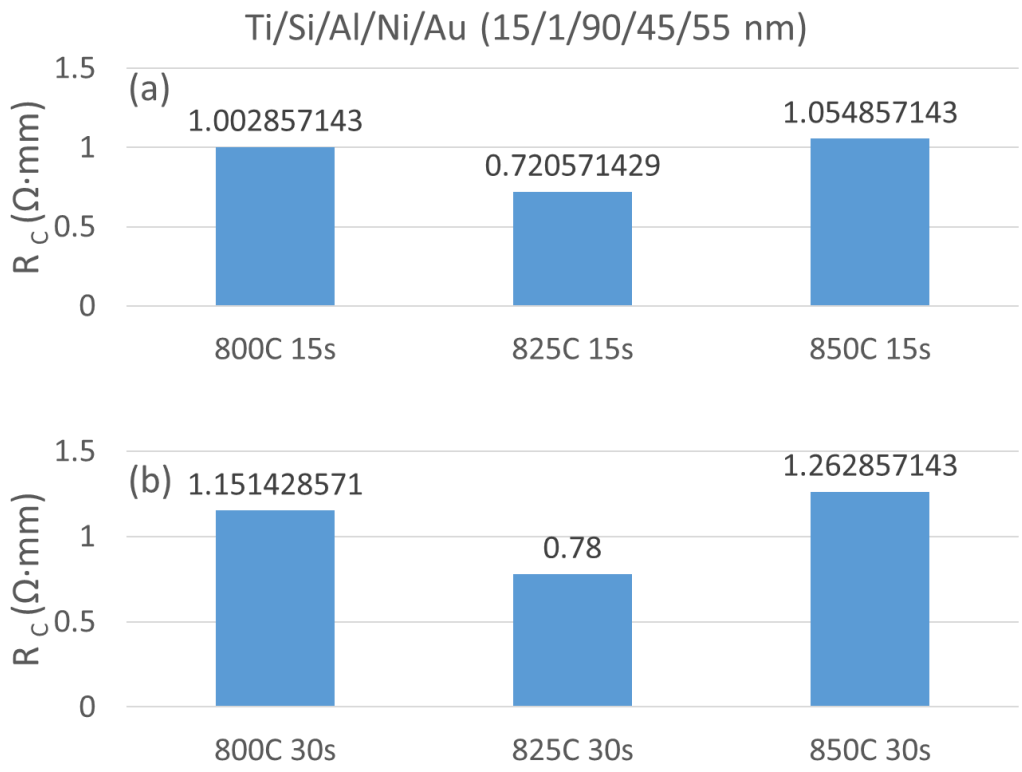


Figure 9 Optimizing the Ti/Si/Al/Ni/Au (15/2/90/45/55 nm) ohmic contact annealing conditions on AlGaN/GaN.

Lastly, I was curious to revisit Si as the first layer but this time, use 1 nm instead of 2 nm of Si, i.e. Si/Ti/Al/Ni/Au (1/15/90/45/55 nm). Since I previously found an optimized temperature of 825° C, I varied the annealing time using a wider range; from 5 seconds to 30 seconds. The results are shown on Figure 10. The trend exhibits lower contact resistance with increasing annealing time. The contacts annealed at 825° C for 30 s in N_2 exhibited very low contact resistance of 0.22 Ω·mm on AlGaN/GaN. To summarize, the results are shown on Table VIII.

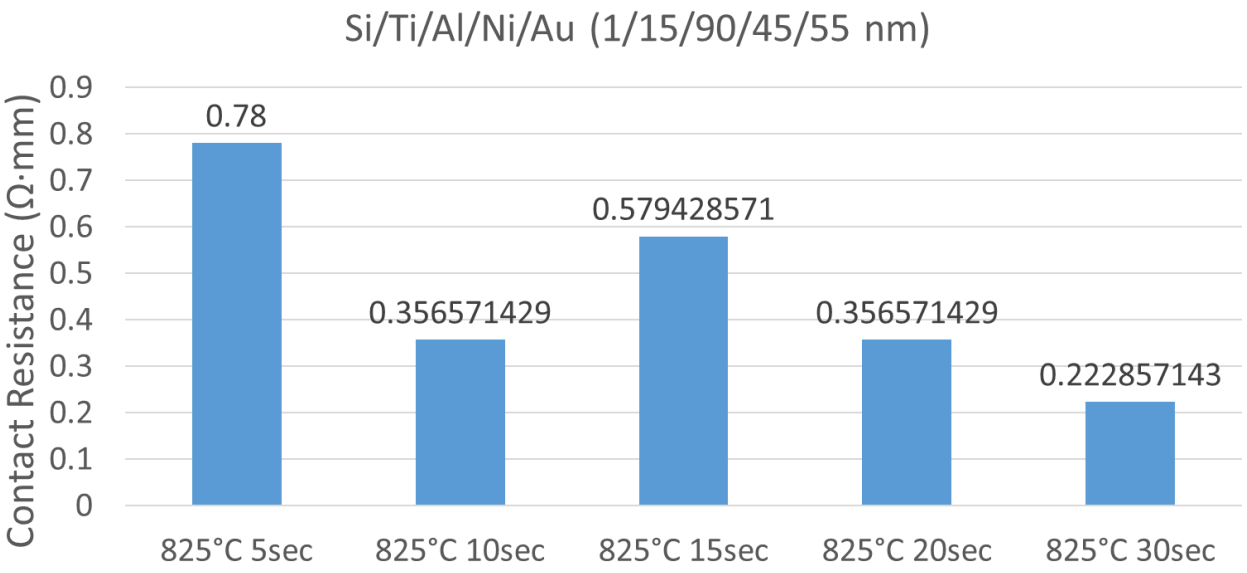


Figure 10 Optimizing the Si/Ti/Al/Ni/Au (2/15/90/45/55 nm) ohmic contact annealing conditions on AlGaN/GaN.

Table VIII Summary of lowest contact resistances measured using a thin layer of Si in the standard stack Ti/Al/Ni/Au on AlGaN/GaN substrates.

Ohmic Stack	***Thickness (nm)***	***Lowest contact resistance (Ω·mm)***	***Annealing condition***
Ti/Al/Ni/Au	15/90/45/55	0.75	800°C for 30s in N_2
Si/Ti/Al/Ni/Au	2/17/90/45/55	0.76	825°C for 30s in N_2
Si/Ti/Al/Ni/Au	1/15/90/45/55	0.22	825°C for 30s in N_2
Ti/Si/Al/Ni/Au	15/1/90/45/55	0.72	825°C for 15s in N_2

The stack Si/Ti/Al/Ni/Au (1/15/90/45/55 nm) showed promising results on AlGaN/GaN. However, I was interested in comparing the contact resistance on both AlGaN/GaN and InAlN/GaN substrates. The latter is known to have worse contact resistances as reported in literature due to a more complex heterojunction system and wider bandgap. For AlGaN/GaN system, a later run showed a minimum contact resistance of 0.14 Ω·mm, a specific contact resistivity of $3.7 \cdot 10^{-7}$ Ω·cm^2 and a sheet resistance of 499 Ω/□. For the best InAlN/GaN sample, the minimum contact resistance I measured was 0.17 Ω·mm, a specific contact resistivity of $5.3 \cdot 10^{-7}$ Ω·cm^2 and a sheet resistance of 548 Ω/□. These ultra-low contact resistances are comparable to the costlier GaN-regrowth process highlighted in Section 1.3.2.

2.3. Ohmic Recess

To achieve low-temperature ohmic contact formation, a plasma etch prior to metallization is required. Although $SiCl_4$ plasma seems like a viable approach as reported in literature, the gas chemistry is not widely available on reactive ion etching (RIE) systems. However, since BCl_3 and Cl_2 gases were available on an Oxford PlasmaLab inductively couple plasma-RIE (ICP-RIE), we developed an etching recipe on that system for the removal of the AlGaN barrier layer. The etch had to be very slow to be able to have a highly-controllable etch rate to remove only the AlGaN barrier layer. To characterize the etch rate, I used AlGaN/AlN/GaN (35/1/2000 nm) epi-wafers masked using photo-resist with a trench-style pattern. After etching, the photoresist was thoroughly removed and the trench-depth was measured by atomic force microscopy (AFM). Surface roughness before and after the etching was also measured using AFM.

As a start, I modified the Mesa-device isolation etching recipe to develop the recipe for ohmic recessing along with guidance from what was reported in literature. I first tested the etch rate using course time intervals and once I had a better idea between which time-intervals I was close to the heterojunction, a tested the etch rate using a much finer time-interval. I started with two recipes, R1 and R2, as listed on Table IX. I found that R2 had a slower etch rate so I chose that recipe to further develop. That recipe had a slightly fast etch rate of 8.5 nm/min, so to slow it down further, I decreased the RF power from 10 W to 8 W, listed as R3. The result from this lowered RF power proved to help lower etch rate to 5.8 nm/min. I also tried to decrease the RF power further to 5 W, listed as R4, however, the plasma was highly unstable at such a low power such that there was no controllable etch recorded. The resulting etch depth profile vs. time are shown in Figure 11. Moreover, the surface roughness measured using AFM is shown in Figure 12. Roughness appears to decrease from an average roughness of 1.81 nm before the etch to 1.38

nm after the etching. Recipe 3 developed here is used, thereafter, for low-temperature ohmic contact formation of gold-free contacts and will be further discussed in Section 2.4.

Table IX Etching recipes tested for ohmic recess process using an Oxford ICP-RIE system.

Recipe Label	*Pressure (mTorr)*	*Gases*	*Flow Rate (sccm)*	*ICP Power (W)*	*RF Power (W)*	*Etch Rate (nm/min)*
R1	10	BCl_3/Cl_2	5/5	25	10	12.0
R2			30/5	0	10	8.5
R3				0	8	5.8
R4				0	5	N/A

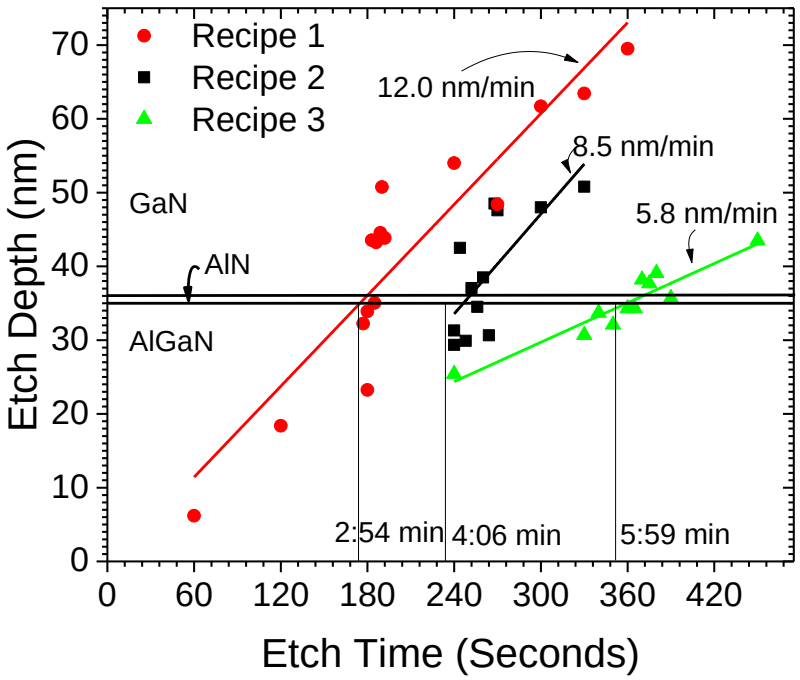


Figure 11 ICP-RIE etch profiles for removal of AlGaN barrier layer in recessed-ohmic technology.

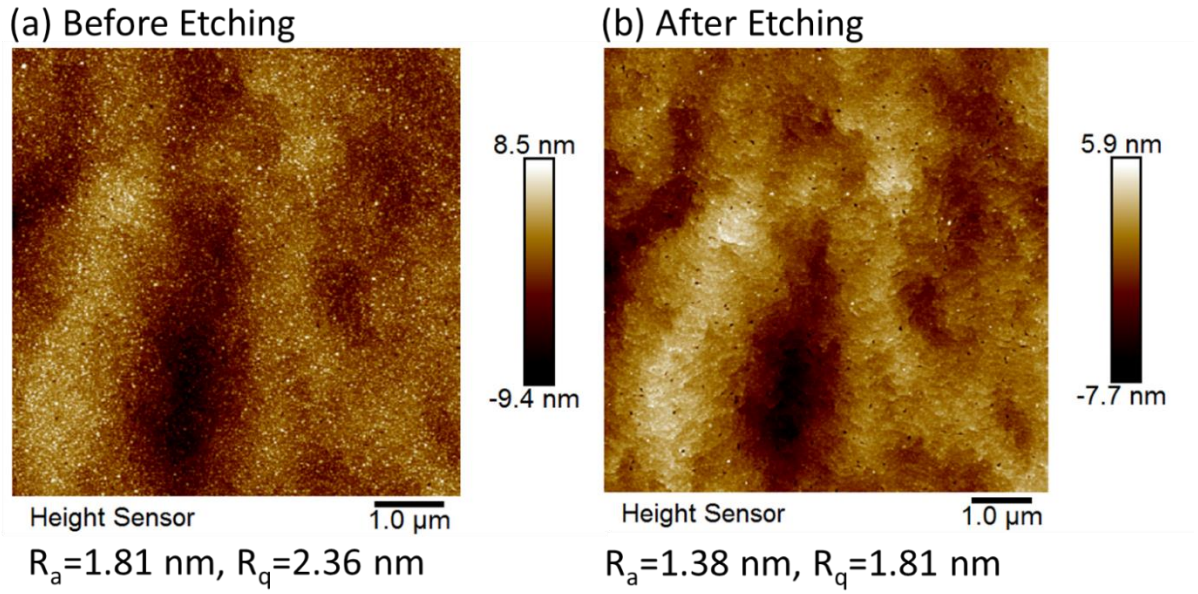


Figure 12 Surface roughness comparison before and after the ohmic-recess etching using Recipe #3.

2.4. Gold-Free Contacts

For gold-free ohmic contacts, the aim was to develop a process with low-temperature metal alloying (< 600° C), while eliminating the use of any gold. To achieve low-temperature annealing conditions, I etched away the barrier layer (AlGaN) using recipe #3 described in the previous section 0 prior to metallization. For the metal stack, I used X/Al (10/280 nm) as the first two layers, where X was either Tantalum, Hafnium, or Titanium, followed by a Tantalum (20 nm) capping layer. The purpose of varying the first layer was to verify which material showed the best results as there are various conflicting reports in literature. After metallization by lift-off, I varied the annealing temperature from 420° C to 600° C while holding time and ambient constant, for 30 s in N_2, respectively. The results are plotted in Figure 13. The Ti/Al/Ta (10/280/20 nm) contacts showed the lowest contact resistances throughout the whole temperature range with a minimum of 2.4 Ω·mm annealed at 450° C. Ta/Al/Ta (10/280/20 nm) showed the next lowest contact resistance of 2.5 Ω·mm annealed at 500° C, however, showed large instabilities if the temperature was increased or decreased by 50° C. The Hf/Al/Ta contacts showed very poor results. The use of refractory metal, Tantalum, may be the cause for large contact resistances since during the deposition, the samples are exposed to extreme high-temperatures.

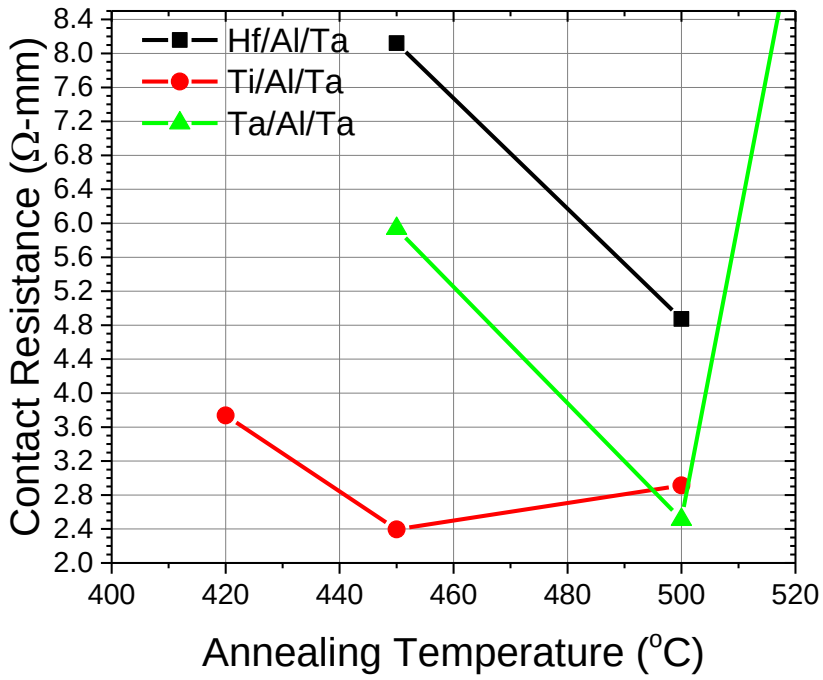


Figure 13 Annealing temperature optimization for gold-free recessed ohmic contacts on AlGaN/GaN substrates.

Previously, I found that an optimum Ti/Al thickness for the standard ohmic stack was 15/90 nm, thus, I decided to investigate using this thickness in the gold-free process. For this study, I used ohmic recessed etching, followed by metallization of Ti/Al/Ta (15/90/20 nm) and compared annealing conditions using different ambient and time. The ambient gases used were: Argon, Nitrogen, annealing in vacuum followed by purging of Nitrogen during cooldown and annealing in vacuum followed by purging of forming gas (H_2/N_2) during cooldown. The results are shown on Table X. Annealing using a vacuum/forming gas ambient showed the lowest contact resistance of 2.89 Ω·mm. Furthermore, I varied the annealing time from 30 s to 5.5 minutes to determine

what was the optimal annealing time. I found an increasing trend in contact resistance with increasing time as depicted in Figure 14. Thus, staying below 30 s is the optimal results. No further studies were performed on annealing temperature for this stack as the Ti/Al/Ta (10/280/20 nm) metals showed better results. It is imperative for me to point out that after annealing of gold-free contacts, I noticed surface color-changes of the metal, which may be due to oxidation of the metal contacts. Thus, while probing the TLM pads, I had to first slightly scratch the surface to remove any native metal-oxides to correctly measure resistances.

Table X Gold-free ohmic recessed contacts with rapid thermal annealing ambient conditions varied. The annealing was performed at 450° C for 30 s.

Annealing Condition	***Extracted Contact Resistance***
Argon	6.61 Ω·mm
Nitrogen	4.76 Ω·mm
Vacuum/Nitrogen	3.63 Ω·mm
Vacuum/Forming Gas	2.89 Ω·mm

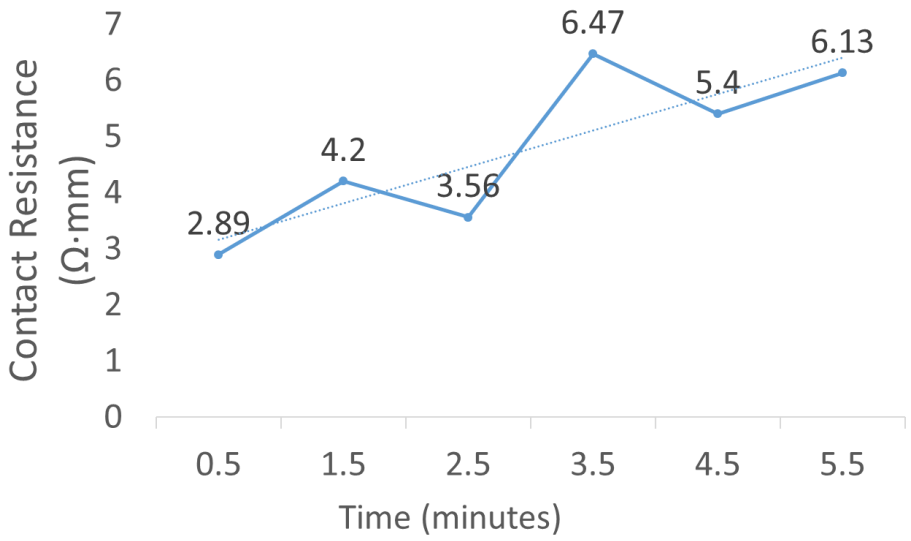


Figure 14 Ti/Al/Ta (15/90/20 nm) gold-free contacts with recessed ohmic annealing time optimization. Annealing temperature was held constant at 450° C using a vacuum/forming gas ambient.

2.5. Conclusions

To summarize, optimization of ohmic contacts was realized through several approaches. Using electron beam evaporation of the standard stack, Ti/Al/Ni/Au, the Ti/Al thicknesses and ratio was optimized followed by annealing conditions. I found a 1:6 Ti:Al ratio gave the best results with thicknesses of 15 and 90 nm, respectively. Using a very thin layer of Silicon (1 nm) prior to the standard stack, further improved the contact resistance with a minimum of 0.14 Ω·mm on AlGaN/GaN. Low-temperature ohmic contacts were also realized through a combination of AlGaN barrier layer etching by ICP-RIE and gold-free metallization (Ti/Al/Ta). However, a large contact resistance was measured. To improve this, I suggest alternate means of depositing high-melting temperature metals either by sputtering or an e-beam evaporation system with better heat dissipation. Table XI summarizes the best contacts realized for each type

Table XI List of optimized ohmic contacts processing on GaN. Metal thicknesses and annealing conditions were optimized for the listed metallization type.

	Standard Stack	***Gold-free***	***Si-incorporated***
Metals	Ti/Al/Ni/Au	Ti/Al/Ta	Si/Ti/Al/Ni/Au
Thickness	15/90/45/55 nm	10/280/20 nm	1/15/90/45/55 nm
Annealing conditions	800°C for 30s in N_2	450°C for 30s in N_2	825°C for 30s in N_2
Ohmic Recess	No	Yes	No
Resistance	0.75 Ω·mm (AlGaN)	2.4 Ω·mm (AlGaN)	0.17Ω·mm (InAlN) 0.14 Ω·mm (AlGaN)
Advantage	Low resistance	Gold free and low temperature	Very low resistance

3. HIGH-κ INSULATING MATERIALS FOR AlGaN/GaN METAL INSULATOR SEMICONDUCTOR HETEROJUNCTION FIELD EFECT TRANSISTORS

One of my earlier studies conducted consisted of HfO_2-based insulators studied through both transistor and capacitor structures. The fabrication process was completed at Cornell University's Nanoscale Science and Technology Facility and the results are published in: [74] Albert Colón, Junxia Shi, High-κ insulating materials for AlGaN/GaN metal insulator semiconductor heterojunction field effect transistors, Solid-State Electronics, Volume 99, September 2014, Pages 25-30, ISSN 0038-1101, http://dx.doi.org/10.1016/j.sse.2014.05.005. (http://www.sciencedirect.com/science/article/pii/S0038110114001208). Permission to reuse this article in my thesis is in Appendix C.1. Additional details have been added to this chapter which are not contained in the original publication.

3.1. Introduction

Aluminum Gallium Nitride/Gallium Nitride (AlGaN/GaN) Heterojunction Field Effect Transistors (HFETs) have gained much interest in the recent years. There exist many advantages of using GaN, which is a wide band gap semiconductor, over Silicon such as less vulnerability from temperature fluctuations during operation and higher power densities that can be handled. Conventional schottky-gate HFETs suffer from problems like high gate leakage and high-frequency drain current collapse [75, 76]. An approach to reduce gate leakage is to insert a dielectric between metal and semiconductor to form a metal-insulator-semiconductor HFET (MISHFET) structure. However, there still exist many challenges that must be resolved with the MISHFET structure. Specifically, optimizing the dielectric material such as to reduce leakage current, eliminate current collapse, reduce capacitance-voltage (C-V) hysteresis and many others,

which are all, in part, a result of large interface trap densities associated with the interface between the dielectric and AlGaN.

There are many novel insulators being used on AlGaN but two of the more popular insulators are HfO_2 [58, 77, 78] and Al_2O_3 [51, 70, 72, 78, 79], or a stack of both [58, 80]. HfO_2 provides high dielectric constant, κ, of ~21 [81] but poor a conduction band offset to GaN of ~1.51eV [82]. On the other hand, Al_2O_3 provides a larger conduction band offset to GaN at ~1.96eV [82] but has a lower dielectric constant around ~9 [83]. A high dielectric constant is preferred to preserve maximum channel control but a large conduction band offset is favorable to reduce gate leakage currents. Furthermore, thermal stability is an important property of a dielectric material since phase change from amorphous to crystalline will give rise to leakage currents through crystal grains [58, 59]. HfO_2 shows a low temperature transition from amorphous to monoclinic phase at 400° C [59] while Al_2O_3 crystallizes near 900° C [61]. It is therefore desirable to create a ternary compound such as $HfAlO_x$ or $HfSiO_x$ to obtain a good trade-off between dielectric constant and conduction band offset such as for $HfAlO_x$ on AlGaN [56, 84-87]. SiO_2 has a very large conduction band offset to GaN at ~2.56 eV [88]. Creating said ternary compounds could result in having higher conduction band offsets of ~1.61 eV [82] and ~1.57 eV [88] for $HfAlO_x$ and $HfSiO_x$, respectively, compared to pure HfO_2 while keeping the dielectric constant relatively high. Thermal stability is also improved with the ternary compounds such that the crystallization temperature increases to 1000° C [59] and 950° C [89] for $HfAlO_x$ and $HfSiO_x$, respectively.

In this experiment, we report using HfO_2, a dual-layer of HfO_2 with Al_2O_3 as a thin interfacial layer directly on top of AlGaN, and ternary compounds of $HfAlO_x$ and $HfSiO_x$ as gate dielectrics. We first discuss electrical characteristics of the MISHFETs in both DC and pulsed

modes of operation. HfO_2 was demonstrated to have the largest transconductance, partially due to the better interfacial quality that is also suggested by the low dispersion in the pulsed I_d-V_d. $HfAlO_x$ and the dual-layer stack shows the lowest gate leakage current but $HfAlO_x$ has the best thermal stability in terms of self-heating effects and crystallization temperature. Next, we present the metal-insulator-semiconductor heterojunction capacitor (MISHCAP) structure and extract material parameters. The ternary dielectrics were shown to have the largest channel current densities. Lastly, we discuss the interfacial quality between the dielectric and the semiconductor, and correlate the interface trap densities (D_{it}) to the electrical characteristics observed. A strong correlation between trap density and pulsed I_d-V_d dispersion was demonstrated among the samples.

3.2. Experiment

Device fabrication started with AlGaN/GaN on sapphire substrate. Ultrasonic cleaning with acetone, methanol, and isopropyl was performed on the samples. Using standard photolithography procedure, mesa isolation etch was performed by inductively coupled plasma reactive ion etching in a mixture of Ar, BCl_3, and Cl_2 gases in a PlasmaTherm 770 system. Ohmic contact stacks, Ti/Al/Mo/Au (15/90/45/55 nm), were deposited by standard lift off after e-beam evaporation of the Ti/Al/Mo metals and thermal evaporation of Au in a CVC SC4500 Evaporation system. After rapid thermal annealing at 800° C for 30 seconds in a AG Associated Model 610 RTA system, transfer length measurements performed on-chip indicated a contact resistance of 0.7 Ω-mm.

Prior to the deposition of the dielectric layer, 200 nm of SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD, Oxford 100) everywhere and then etched away from the active regions of the devices using BOE 10:1 wet etchant. Surface treatment prior to the deposition of gate dielectric is critically important to decrease defects between the dielectric and

AlGaN interface [62, 63]. In this work, we employed a surface pre-treatment similar to [62], which consists of a BOE 10:1 dip for 30 s, followed by DI rinsing. Finally, the plasma deposition of HfO_2, HfO_2/Al_2O_3 stack, $HfAlO_x$ and $HfSiO_x$ was performed using Oxford ALD FlexAL. In-situ thermal anneal of the substrates for 5 minutes on the hot chuck was performed in the ALD system prior to the actual deposition of the films. Ti/Au (28/350 nm) was then deposited as gate electrode. Finally, Ti/Au (28/300 nm) pads for gate, source and drain contacts were deposited. Devices under test (DUT) had gate-source spacing of 2 μm, gate-drain spacing 10 μm, and gate length 2 μm. MISHCAPs were also fabricated on-chip alongside the transistors with gate radius of 100 μm for *C-V* and interface trap density (D_{it}) characterizations. Figure 15 shows the device cross-sectional structure of the MISHFET. Thicknesses of each dielectric layer were 18, 17 (13/4), 21 and 18 nm for HfO_2, HfO_2/Al_2O_3 stack, $HfAlO_x$, and $HfSiO_x$, respectively, measured by ellipsometry using a Woollam spectroscopic ellipsometer.

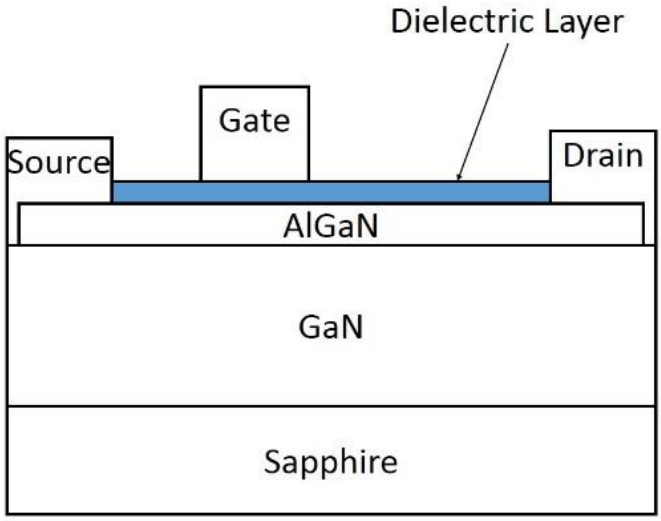


Figure 15 Schematic cross-sectional view of MISFET structure.

3.3. Device Characteristics

3.3.1. MISHFET

Current-voltage (*I-V*) measurements were obtained using a Keithley 4200 Semiconductor Characterization System and a Signatone probe station. Figure 16 shows drain current vs. gate voltage, I_d-V_g, of each of the samples. Drain voltage was held fixed at 5 V while gate voltage was swept. It is seen that both $HfAlO_x$ and $HfSiO_x$ samples have larger threshold voltages.

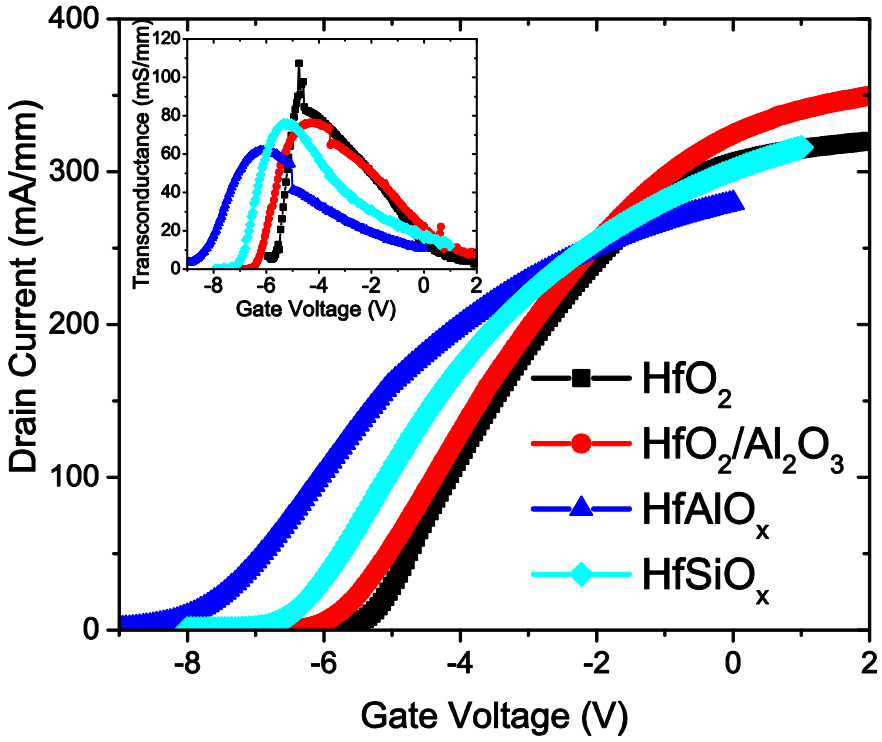


Figure 16 Drain current, I_d, vs. gate voltage, V_g, of each of the samples. The inset shows transconductance. Drain bias was held at 5 V during the measurement while gate voltage was swept.

An observed increase of transconductance, g_m, can be due to smaller gate-to-channel separation and/or an improved interfacial quality between the insulator and AlGaN barrier [76]. The inset of Figure 16 shows g_m of each of the samples. Comparing the two samples with HfO_2/Al_2O_3 and $HfAlO_x$, the lower gate-to-channel separation (17 nm versus 21 nm) is the main reason for the HfO_2/Al_2O_3 sample having larger g_m than that of $HfAlO_x$. However, g_m of the HfO_2 based MISHFET is slightly higher than the rest, hinting at a better interface quality for HfO_2, which will be analyzed in a later section.

Gate leakage currents are plotted in Figure 17. The $HfAlO_x$ and the HfO_2/Al_2O_3 stack devices shows the lowest gate leakage currents on the orders of 10^{-12} A/mm. $HfSiO_x$ shows moderate leakage levels on the orders of 10^{-10} A/mm and HfO_2 sample exhibited the worst with levels on the order of 10^{-8} A/mm for reverse leakage among the tested samples and even higher for forward leakage. One of the major factors associated with HfO_2 having such high leakage currents is the low conduction band offset to AlGaN.

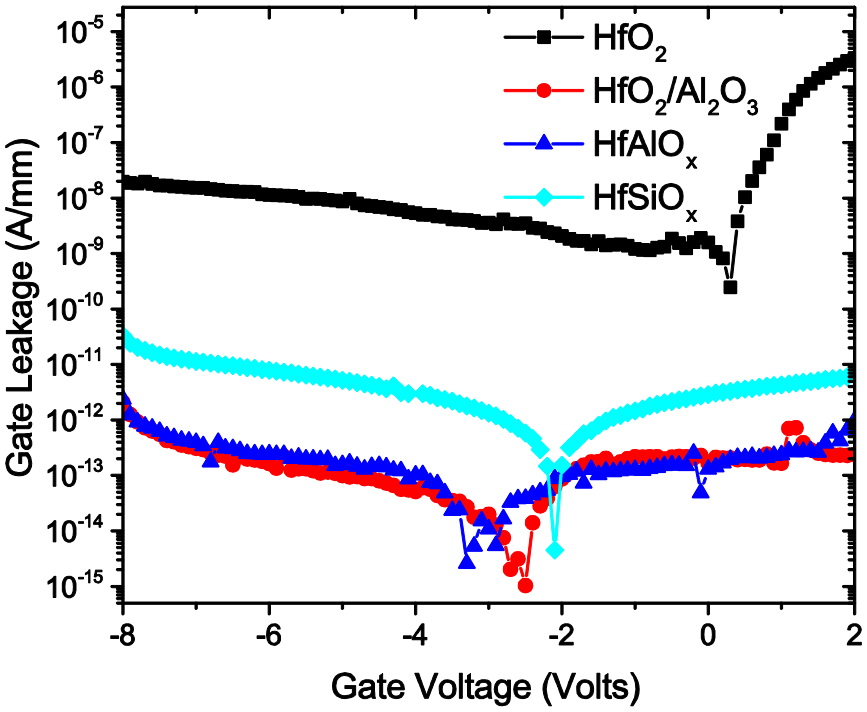


Figure 17 Gate leakage of each of the samples. $HfAlO_x$ and HfO_2/Al_2O_3 show ultra-low leakage levels, followed by the $HfSiO_x$ sample, while HfO_2 showed the worst leakage current.

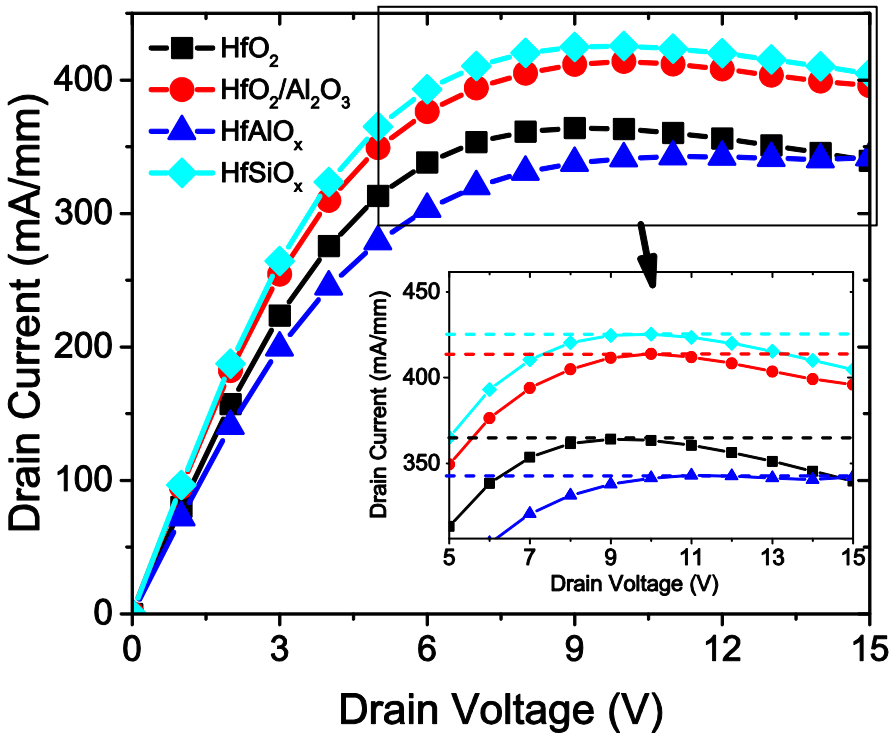
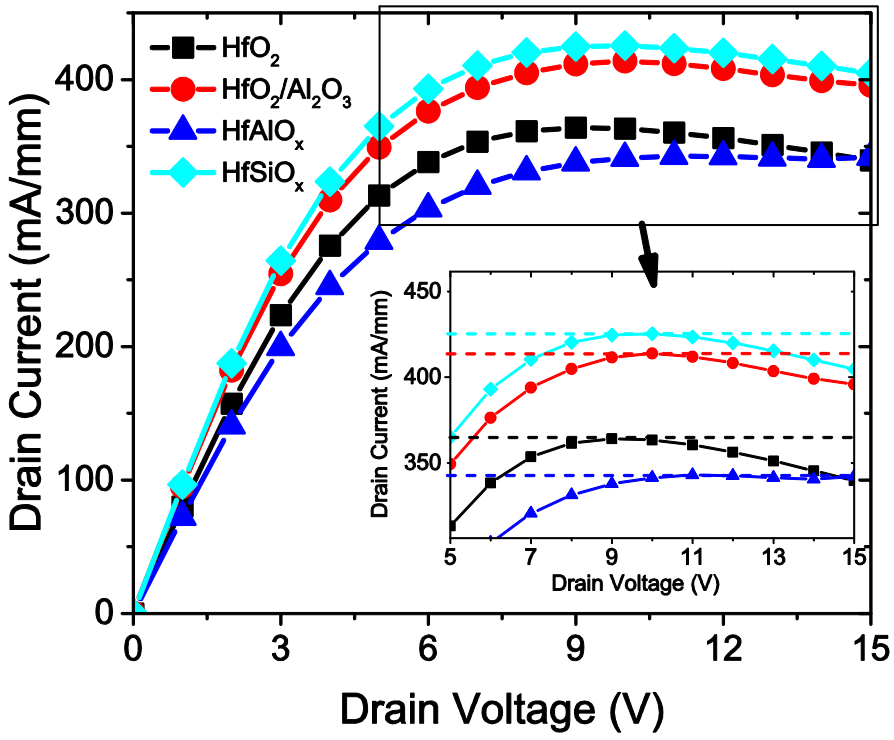


Figure 18 shows the I_d-V_d characteristics of each of the samples at gate voltage of 6 V. Note that all samples are under the same gate bias and have variation in threshold voltage hence the difference in on-resistance. We can see that all transistors show reduction in saturation current at higher drain biases beyond the "knee" voltage due to self-heating of the device deteriorated by

the sapphire substrate [58], however, $HfAlO_x$ notably shows a lower effect from this heating. The



inset of

Figure 18 shows a zoomed in portion which prominently depicts this. The values of Ron, which were extracted from the linear region of the I_d-V_d curves at V_g = 0 V (not shown), are 23.3, 58.7, 24.5, and 15.1 Ω-mm for HfO_2, HfO_2/Al_2O_3, $HfAlO_x$, and $HfSiO_x$, respectively.

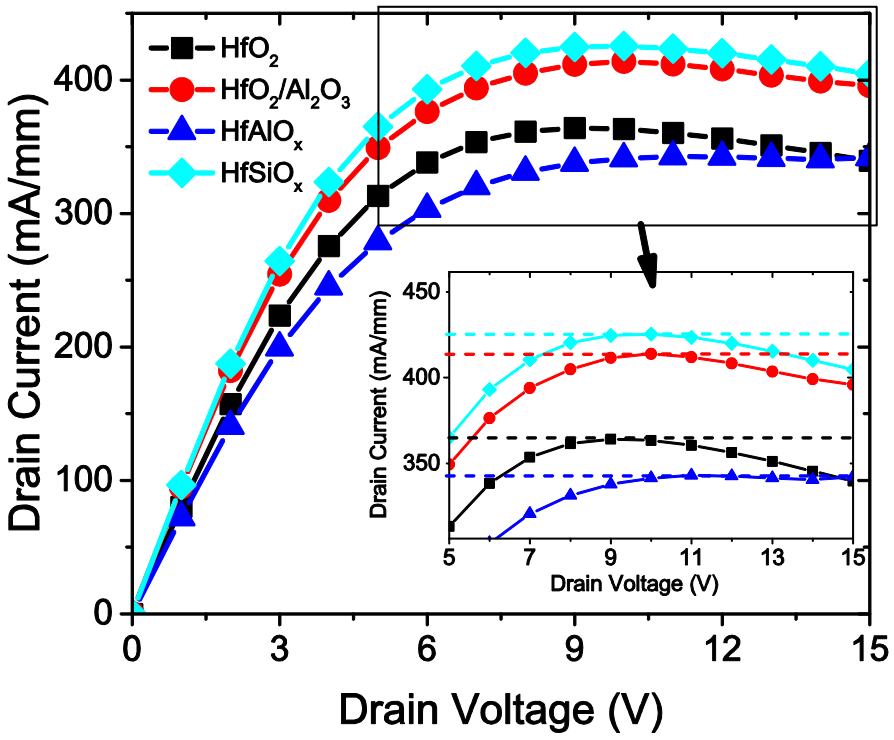


Figure 18 DC drain current vs. drain voltage for HfO_2, HfO_2/Al_2O_3, $HfAlO_x$, and $HfSiO_x$. Only V_g = 6 V is plotted here for clarity. The inset shows a zoomed in portion of the curves beyond V_d = 5 V.

Figure 20 shows the pulsed I_d-V_d measurements of each device. The pulse measurements setups were similar to [90] and is performed as follows. The black solid-figured lines were pulsed from a zero-bias condition (V_d = V_g = 0 V) while the red hollow-figured lines were pulsed from a stressed condition (V_d = 25 V, V_g = -10 V). V_g was stepped through different gate voltages while V_d was swept between 0 to 30 V, however, only V_g = 1 V is plotted in Figure 20 for clarity. The pulse width used was 5 μs and the period was 1 ms. The timing diagram is described in Figure 19. The HfO_2 MISHFET shows little dispersion in drain current followed by HfO_2/Al_2O_3 then $HfAlO_x$

and lastly, $HfSiO_x$ devices. It is believed that a larger dispersion in drain current resulting from the pulse measurements may be due to a larger surface trap density on the surface of AlGaN [91-93]. Therefore, we may conclude that the interface trap density is lower for the HfO_2 sample than for the rest of the samples.

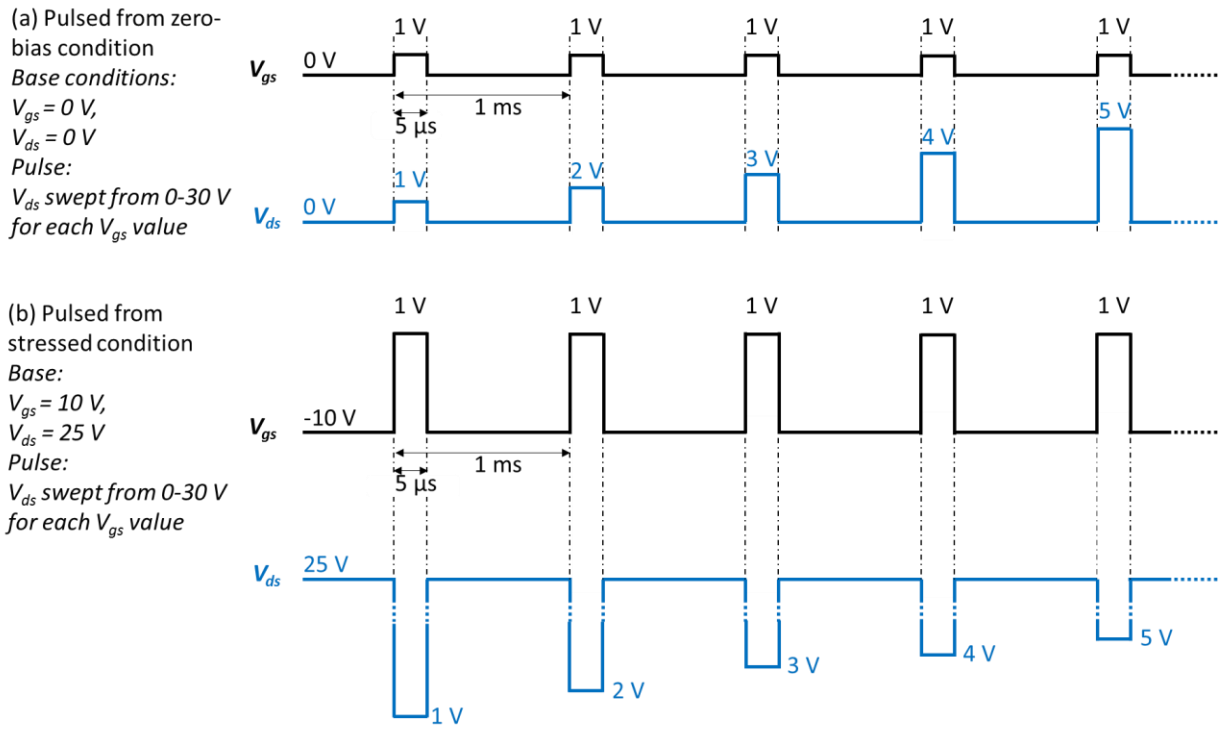


Figure 19 Pulsed I-V timing setup for MISHFETs.

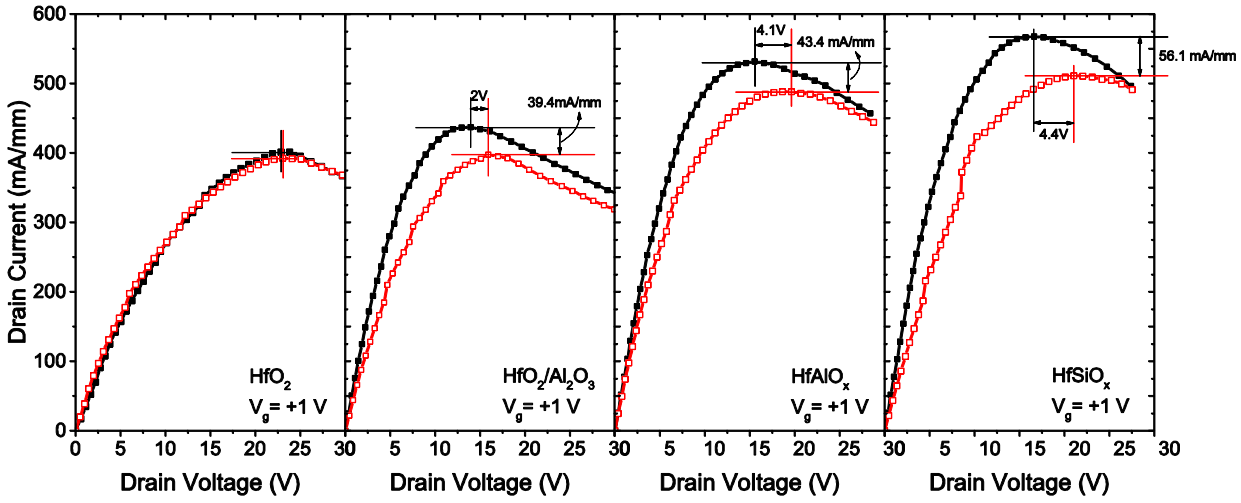


Figure 20 Pulse measurements of drain current vs. drain voltage for HfO_2, HfO_2/Al_2O_3, $HfAlO_x$, and $HfSiO_x$ (left to right). Only V_g = 1 V is plotted here for clarity. Black solid figured curves are pulsed from a zero-bias condition and the red hollow figured curves are pulsed from a stressed condition.

3.3.2. MISHCAP

C-V curves for each of the samples with 200 μm diameter capacitors are plotted in Figure 21. The applied voltage ranged from -10 to 0 V with a 1 MHz signal (dashed line) and a 1 kHz signal (solid line) and was measured in the dark. Assuming a dielectric constant of 21 for HfO_2 [81], capacitance from the AlGaN barrier layer was calculated to be 127.6 pF. Using this value as a reference for all samples, as they are taken from the same wafer, the dielectric constants were found to be 14.0 overall for HfO_2/Al_2O_3 (individually, 21 for HfO_2 and 6.2 for Al_2O_3), 13.2 for $HfAlO_x$ and 15.5 for $HfSiO_x$ using the following:

$$\frac{t_{ox}}{\kappa} = \varepsilon_0 A(C_{MISH}^{-1} - C_{AlGaN}^{-1})$$

where ε_0 is the permittivity of vacuum, A is the area of the MIS gate, C_{AlGaN} is capacitance due to the barrier layer, C_{MISH} is the measured series capacitance due to the oxide and AlGaN layers and t_{ox} is the thickness of insulating layer. The dielectric constants agree well with [58, 89, 94], reporting similar values.

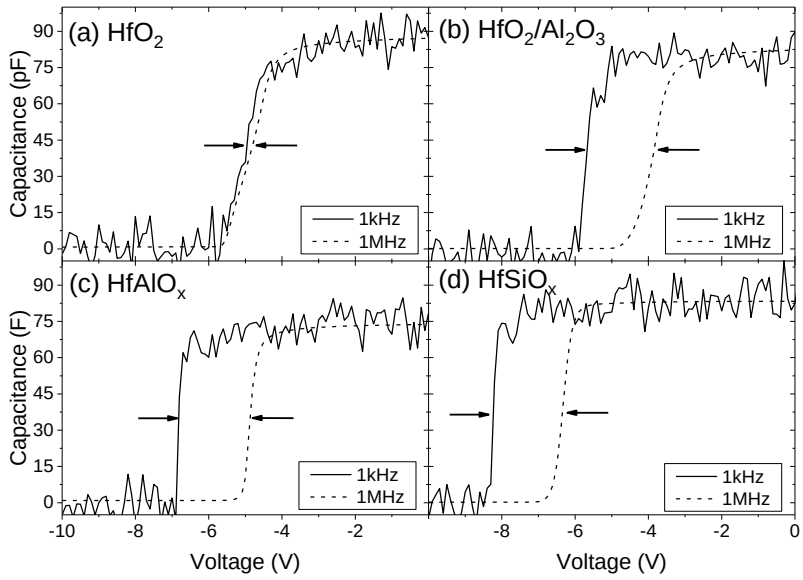


Figure 21 High frequency (1MHz, dashed line) and low frequency (1kHz, solid line) C-V curves of (a) HfO_2, (b) HfO_2/Al_2O_3, (c) $HfAlO_x$ and (d) $HfSiO_x$. Voltage was swept from -10 V to 0 V and was measured in the dark.

Comparing the high frequency and the low frequency *C-V* curves for the MISH capacitor may provide some insight on the D_{it} [95]. The stretch out between these two curves is an indication of the presence of a high D_{it}. As shown in the figures, HfO_2 appears to have the smallest stretch out between all the samples which, once again, hints that the D_{it} is lower for the HfO_2 sample than for the rest of the samples.

Carrier density, $N_{C\text{-}V}$, profiles of each of the samples were extracted from the *C-V* curves by using the following:

$$N_{C-V}(z) = 2 * (q\varepsilon_s\varepsilon_0 A^2 \frac{dC^{-2}}{dV})^{-1}$$

where ε_s is the overall permittivity of the MISH structure. $N_{C\text{-}V}$ as a function of depth is shown in Figure 22. $HfAlO_x$ and $HfSiO_x$ samples show larger carrier densities than HfO_2 or HfO_2/Al_2O_3 samples. This approach to estimate the carrier profile is an accurate estimation used by several groups [51, 83, 96-98]. Although one may argue that due to a high interface trap density the estimation is specious, Mizue et al. [51] noted that their estimation by this method closely matched the density estimated by their Hall Measurements although having the commonly high D_{it} seen among AlGaN/GaN MISH structures.

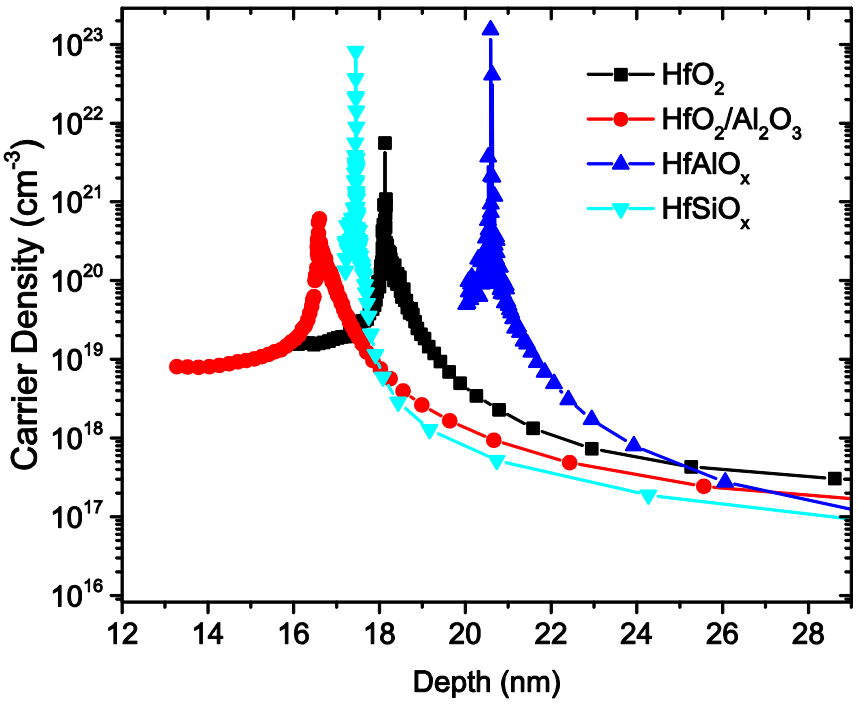


Figure 22 Carrier density, $N_{C\text{-}V}$, as a function of depth. $HfAlO_x$ and $HfSiO_x$ show the largest carrier density between all the samples.

3.3.3. Interface Trap Characterization

A high D_{it} is the leading cause of threshold voltage instability, *C-V* stretch-out, drain current collapse and other degrading phenomena in MISH-type structures [99, 100]. Therefore, it is important to quantitatively characterize the interface trap density to aid in the selection and optimization of gate dielectrics. The conduction method is a widely accepted characterization method for interface trap densities among dielectric/AlGaN/GaN structures [69-71, 101-103] and it is employed in this work. Conductance was measured on a 200 μm diameter capacitor in the

dark. Frequency was varied from 1 kHz to 10 MHz and gate bias was varied between -10 V and 0 V. From the measured conductance and capacitance values, the parallel conductance, G_p, was calculated. Figure 23 (a), (b), (c) and (d) shows the extracted G_P/ω peaks (shapes) within the frequencies used and the fitted curves (lines) for HfO_2, HfO_2/Al_2O_3, $HfAlO_x$ and $HfSiO_x$, respectively.

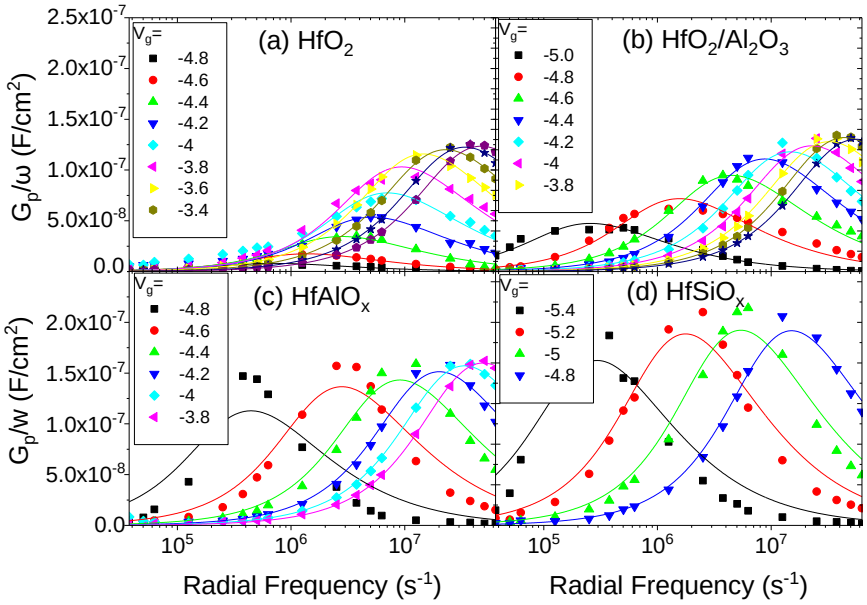


Figure 23 Conductance, G_p/ω, as a function of radial frequency for (a) HfO_2, (b) HfO_2/Al_2O_3, (c) $HfAlO_x$ and (d) $HfSiO_x$ samples. Solid shapes are the measured results and the lines are the fitted curves from which D_{it} and τ are extracted.

It should be noted that only a limited range of gate voltages produced conductance peaks within the frequency range used at room temperature and thus, interface trap densities were measured within a limited energy range. In order to retrieve information on traps closer to the conduction band edge or mid-gap states in AlGaN, measurement temperature must be either lowered or raised, respectively [102]. With our current setup, we were able to retrieve information between 0.17 to 0.32 eV below the conduction band edge which is in agreement to what others reported [69, 70]. Using a process similar to [69, 70] and summarized in Appendix D.2, the peaks were fitted using :

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau}\ln[1 + (\omega\tau)^2]$$

where q is the elemental charge, τ is the trap time constant and D_{it} is the interface trap density. Each G_P/ω peak corresponds to an interface trap density and a trap time constant which responded at the peak's radial frequency. D_{it} and τ were varied to fit the peaks and thus, these values were extracted. Figure 24 shows the trap time constant as a function of gate voltage. The HfO_2 device shows the expected exponential dependence of trap time constant to the applied gate voltage but for the other samples a deviation from this dependence is revealed implying a non-uniformity of oxide charges [70, 101].

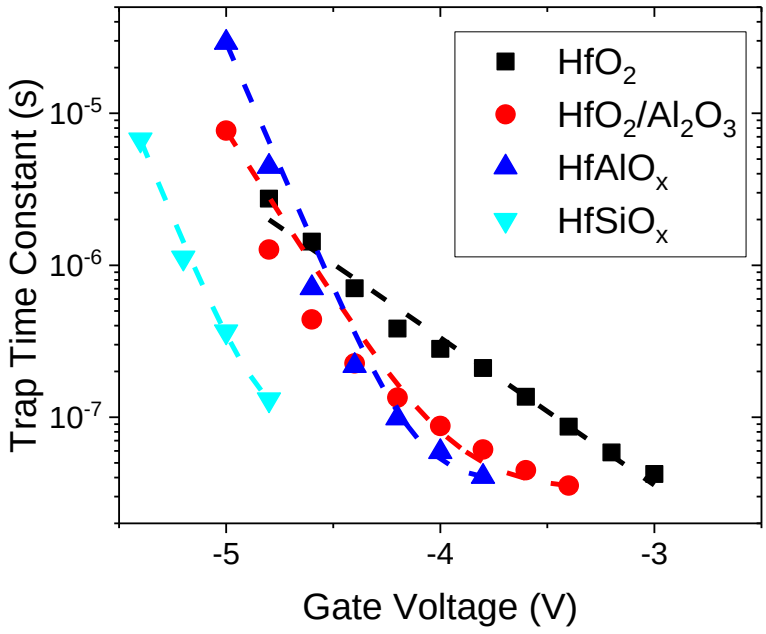


Figure 24 Trap time constants as a function of applied gate voltage. HfO_2 sample shows exponential dependence on gate voltage but the other samples show a deviation from this dependence.

Using the extracted time constant, trap energy, E_T, was calculated using:

$$E_T = kTln(\sigma N_c v_{th} \tau)$$

where σ, trap capture cross section, N_c, density of states in the conduction band, and v_{th}, average thermal velocity of the carriers, were assumed[70] to be $3.4 \cdot 10^{-15}$ cm^{-2}, $2.2 \cdot 10^{18}$ cm^{-3}, and $2.6 \cdot 10^{7}$ cm/s, respectively, k is Boltzmann's constant and T is temperature. The results are shown in Figure 25. The HfO_2 sample shows the lowest trap density of $2.0 \cdot 10^{12}$ $cm^{-2}eV^{-1}$ close to the conduction band edge, and then quickly reduces about an order of magnitude less at 0.28 eV below the conduction band edge. These lower trap densities confirm our previous hint from the

transconductance curves, Figure 16, that the interface quality is better for HfO_2 than for the rest of the samples. The HfO_2/Al_2O_3 sample shows the next lowest trap densities followed by $HfAlO_x$ and then $HfSiO_x$. In fact, these trap densities correlate exactly with the pulse I-V measurements performed in Figure 20 in which the dispersion gets worse in the same order as the trap densities grow larger.

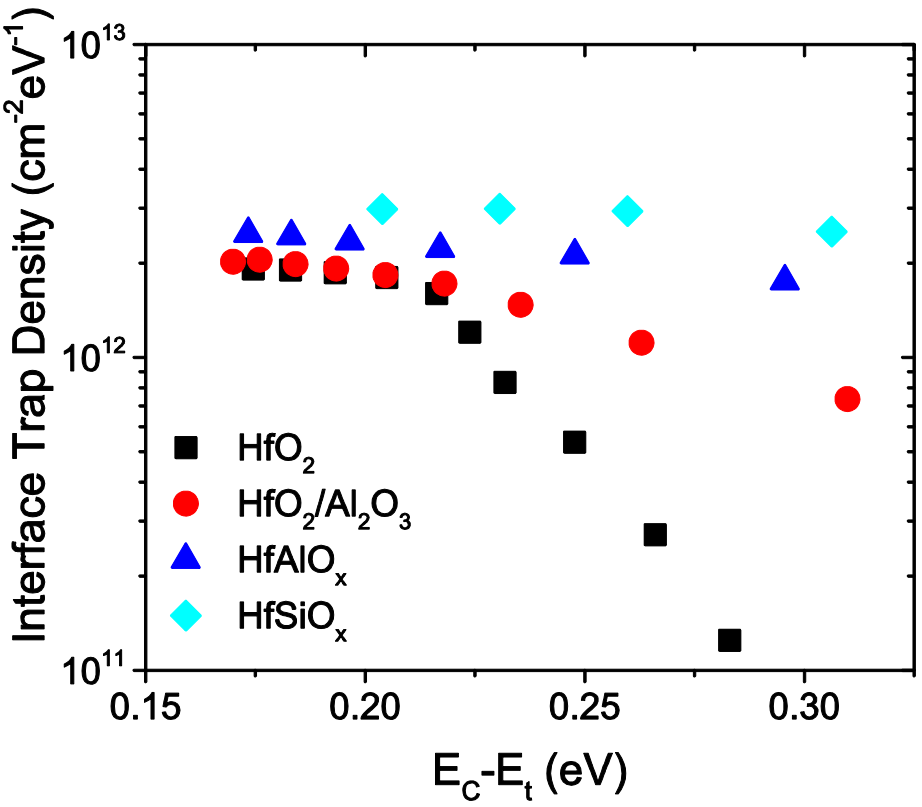


Figure 25 Interface Trap density as a function of activation energy.

3.4. Conclusions

We have presented using HfO_2, HfO_2/Al_2O_3, $HfAlO_x$ and $HfSiO_x$ as gate dielectrics. Although HfO_2 demonstrated low trap densities, gate leakage currents were 4 orders of magnitude greater than $HfAlO_x$ and HfO_2/Al_2O_3 due to a poor conduction band offset which is an unacceptable feature. Both $HfAlO_x$ and $HfSiO_x$ demonstrated larger channel charge densities than HfO_2 or the stack, but $HfAlO_x$ sample showed little degradation in drain saturation current at higher drain voltages. We have also correlated the extracted interface trap densities to the observed transconductance and pulsed I_d-V_d results. Although HfO_2 showed the lowest interface trap density followed by the HfO_2/Al_2O_3 stack, both dielectrics are still vulnerable to the low temperature crystallization of the HfO_2 layer, which will result in increased gate leakage current. Thus, considering the resistance to self-heating effects in the I_d-V_d curves, highest crystallization temperature of 1000° C, lowest gate leakage current, and largest channel carrier density in our set of insulating materials, $HfAlO_x$ appears to be the most promising insulating material in our study.

4. INVESTIGATING COMPOSITIONAL EFFECTS OF ATOMIC LAYER DEPOSITION TERNARY DIELECTRIC Ti-Al-O ON MISH CAPACITOR STRUCTURE FOR GATE INSULATION OF InAlN/GaN and AlGaN/GaN

From my earlier studies of HfO_2-based gate insulators, in Chapter 3, we learned that ternary dielectrics, $HfAlO_x$ and $HfSiO_x$ provided enhanced insulator performance compared to using only HfO_2. In this chapter, we further develop this idea but utilize a very high-κ material, TiO_2, as a basis. Using Aluminum as the 'dopant', I studied Ti-Al-O compounds through GaN capacitor structures. The following results are published in: [104] A. Colon, L. Stan, R. Divan, and J. Shi, "Investigating compositional effects of atomic layer deposition ternary dielectric Ti-Al-O on metal-insulator-semiconductor heterojunction capacitor structure for gate insulation of InAlN/GaN and AlGaN/GaN," Journal of Vacuum Science & Technology B, vol. 34, p. 06K901, Nov-Dec 2016. Permission to reuse this article in my thesis is in Appendix C.2. Liliana Stan assisted me with the deposition of the various dielectrics and Ralu Divan helped me with various aspects of the fabrication process including the electron-beam lithography and reactive ion etching. This work has also been presented at the 60th International Conference on Electron, Ion, and Photon Beam technology and Nanofabrication (EIPBN). Additional details have been added to this chapter which are not contained in the original publication.

4.1. Introduction

GaN-based metal-insulator-semiconductor heterojunction field-effect transistors (MISHFETs) has received much attention in the research community within the last decades. Due to the wide and direct bandgap nature of the material, there are vast applications for GaN-based devices such as high-power [2] (high breakdown voltage capabilities), high-frequency [3] (mm-wave transistors), photonic devices [5] (light emitting diodes) and more [4] (satellites, etc.). The

optimization of several aspects in the MISHFETs structure has been intensely studied within the recent years. A major topic of interest is the insulator quality on nitrides. High dielectric constant (κ) insulators are preferred to maintain high transconductance and minimize threshold voltage shift [57] due to the separation of gate-to-channel distance. However, the bandgaps of insulators typically show inverse relation to dielectric constants, i.e. the larger the κ value, the smaller the bandgap. A larger insulator bandgap is preferred to maintain a large conduction/valence band offset to the semiconductor to properly act as a barrier for electrons/holes [88]. Other important desirable properties for an insulator include thermal stability (crystallization temperature), breakdown strength, interface trap density, leakage current, etc. However, commonly used materials such as HfO_2 [75, 105] or Al_2O_3 [105], involve trade-offs in performance parameters. For example, although TiO_2 may provide a high dielectric constant of 70-90 [106, 107], it suffers from poor conduction band offset to GaN [108] (reported to be ΔE_v = 0.05 eV and ΔE_c = -0.38 eV, measured from Rutile TiO_2 on GaN by XPS), and has a low crystallization temperature of 370° C [60]. On the other hand, Al_2O_3 provides adequate band-offsets to GaN [82] (reported as ΔE_v = 1.24 eV and ΔE_c = 1.96 eV), and high temperature stability up to 900° C [61] but has a low dielectric constant value of ~9 [83]. Creating a ternary compound such as Ti-Al-O and tailoring its composition may result in a reasonably good gate insulating/passivation material in terms of said properties. It has been previously shown in [109, 110] that Ti-Al-O compounds provide superior properties such as lower leakage current and higher breakdown strength over TiO_2. Moreover, it has been demonstrated by Youngseo et. al. [109] that by increasing the Al-content in the Ti-Al-O composite, it may increase the bandgap, thus improving the band-offsets to their respective substrates. However, there is limited knowledge on this ternary compound on AlGaN/GaN and InAlN/GaN substrates. ALD is amongst the more popular insulator deposition method due to its

highly conformal process and its precise deposition control [67]. Moreover, ALD allows relatively easy control and engineering of multicomponent film composition. A nanolaminate or composite film can easily be attained by changing the numbers of alternating cycles of each component. In this study, we investigated the compositional effects of Ti-Al-O films prepared by ALD on the electrical properties of MISH capacitors on AlGaN/GaN and InAlN/GaN.

4.2. Experimental

To characterize insulator quality of Ti-Al-O on GaN, circular MISH capacitors were fabricated. A scanning electron microscope (SEM) image of the completed structure is shown in Figure 26. Device fabrication started with AlGaN/GaN on sapphire and InAlN/GaN on SiC epi-wafers provided by CorEnergy Semiconductor Technology Co. Ltd. and NXP Semiconductors, respectively. An overview of the device fabrication process is described in Figure 27 (a-i). Prior to the device mesa isolation, the substrates were ultrasonic cleaned with acetone, methanol and isopropanol. The lithography was accomplished using Raith 150 electron-beam lithography system and using ma-N 2405 (MicroChem Corp.), a negative-resist exposed using a dosage of 220 $\mu C/cm^2$. The device mesa isolation etch was performed by inductively-coupled-plasma reactive ion etching (ICP-RIE, Oxford PlasmaLab 100) using a $Ar/Cl_2/BCl_3$ plasma. The ohmic contact formation was achieved by patterning, metal stack deposition, lift-off, and thermal annealing. For patterning the contacts, a bi-layer process based on polymethylglutarimide/polymethyl methacrylate (PMGI/PMMA) was used. The Si/Ti/Al/Mo/Au (1/15/90/45/55 nm) metal stack was deposited by e-beam evaporation (Varian Electron Beam Evaporation System), and the lift-off was done by ultrasonication in a 1165 remover bath. After a rapid thermal annealing of the ohmic stack at an optimized annealing condition at 825° C in N_2 for 30 s (Rapid Thermal Processor, Modular

Process Technology Corp.), the transfer length measurements (TLM) performed on-chip indicated an average contact resistance of 0.42 Ω·mm for InAlN and 0.48 Ω·mm for AlGaN.

Following the ohmic contact formation, ternary dielectric deposition was achieved by thermal ALD (Arradiance Gemstar). The ALD films were deposited on InAlN/GaN, AlGaN/GaN, and Si witness samples. Prior to loading into the ALD chamber, the samples were treated with a buffered oxide etch (BOE) 10:1 dip followed by deionized water (DIW) rinse. The Ti-Al-O composite films were achieved by alternating TiO_2 and Al_2O_3 cycles. Each TiO_2 and Al_2O_3 cycles were carried out using tetrakis(dimethylamido)titanium (TDMATi)/H_2O and trimethylaluminum (TMA)/H_2O, respectively. All films were deposited at 200° C at a deposition rate of 0.37 Å/cycle for TiO_2 and 1.12 Å/cycle for Al_2O_3. TiO_2 was deposited as a reference control sample. To vary the composition, 1 cycle of Al_2O_3 was followed by a various number of consecutive TiO_2 cycles, i.e. 1-cycle of Al_2O_3 followed by n-cycle(s) of TiO_2. The TiO_2:Al_2O_3 cycle ratios studied were 10:1, 5:1, and 2:1. To achieve the final target thickness of ~24 nm, the super cycles were repeated. The thicknesses of the films were then measured by X-ray reflectivity (XRR) (Bruker D8 Discover) and the elemental composition was determined by X-ray photoelectron spectroscopy (XPS).

Following the insulator deposition, the gate contacts were patterned by e-beam lithography using the bi-layer resist process, e-beam evaporation of Ti/Au (28/110 nm) and metal lift-off. Lastly, to make electrical contact to the covered ohmic contact regions, the insulator films were etched from these regions using RIE.

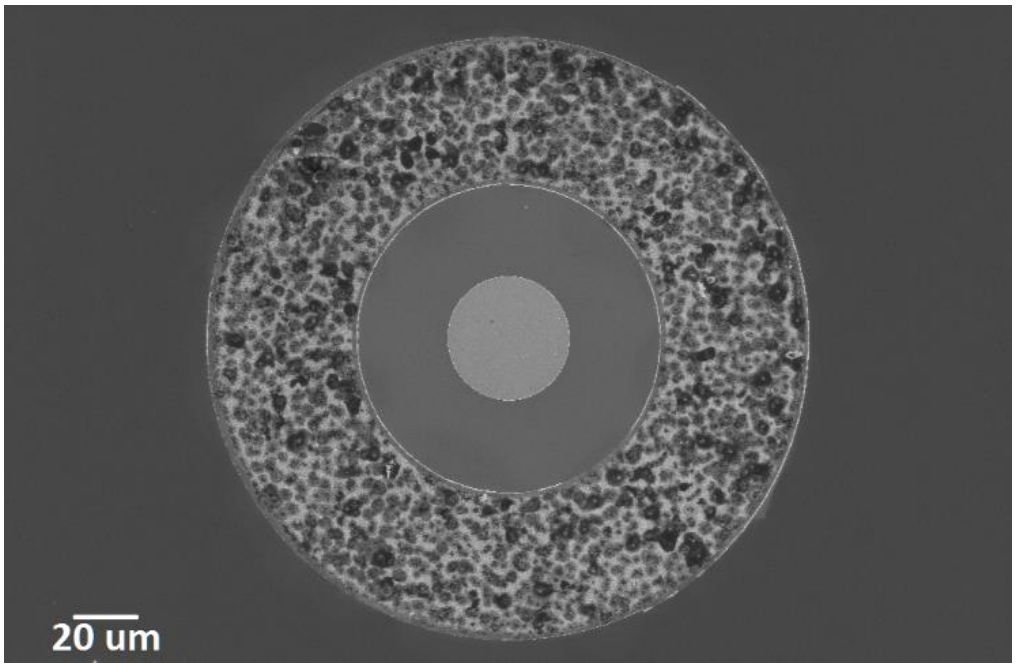


Figure 26 SEM image of the fabricated circular MISH capacitor.

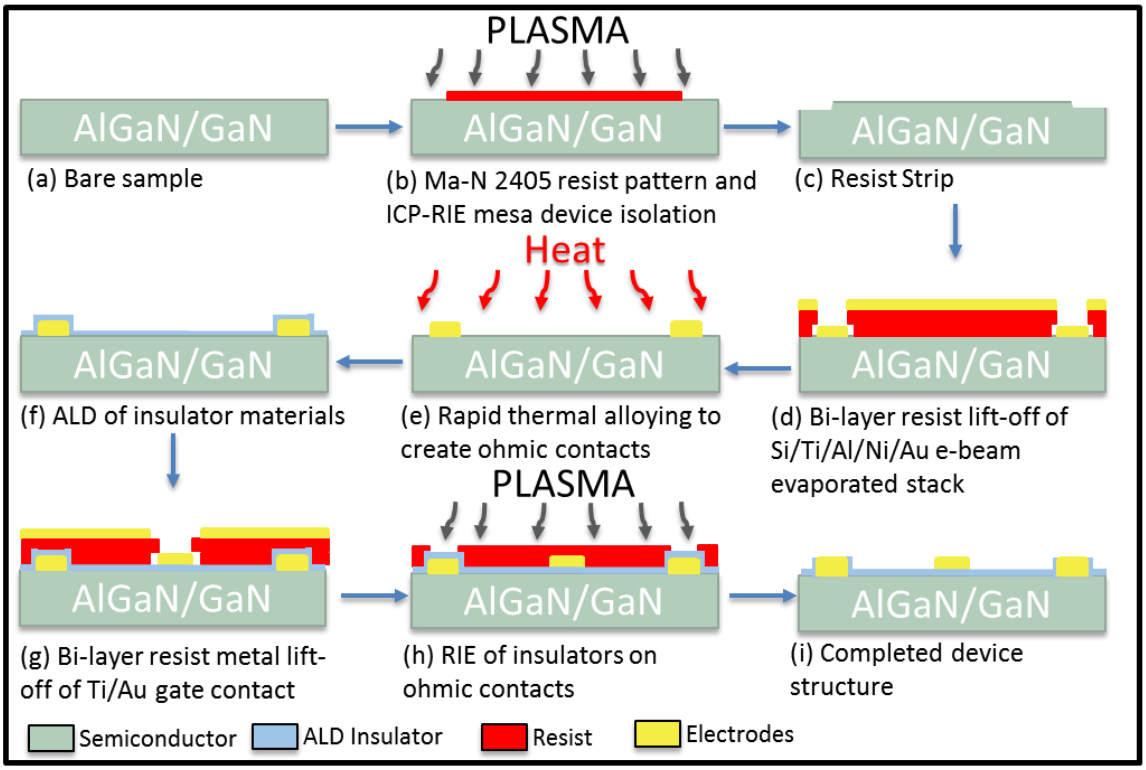


Figure 27 Schematic cross-section of MISH capacitor fabrication steps. (a) AlGaN(InAlN)/GaN starting epi-wafer. (b) Mesa device isolation is achieved by ICP-RIE using a Cl_2-based plasma. (c) Resist is stripped from the surface. (d) Lift-off of ohmic metals deposited by E-Beam evaporation. (e) Rapid thermal annealing at 825° C for 30 s in N_2 ambient to create ohmic contact. (f) ALD of ternary insulator materials. (g) Lift-off of gate electrode. (h) RIE of ALD film over ohmic metals. (i) Completed device.

4.3. Results and Discussion

Ti-Al-O films of compositions in the TiO_2-rich composition range were grown on the InAlN/GaN and AlGaN/GaN substrates. Their elemental composition was evaluated from the XPS spectra and their thickness from the XRR spectra. The results are summarized in Table XII. The X-ray diffraction measurements (not shown) revealed that the amorphous structure of as deposited composite Ti-Al-O films persists in the whole investigated compositional range.

Table XII ALD films processing conditions, thickness and composition. 1:0 ratio is the reference TiO_2 film. TiO_2 and Al_2O_3 ratio was varied to produce different Al-content in the films.

Ratio	TiO_2 cycle(s)	Al_2O_3 cycle	Thickness (nm)	Composition $\frac{Al}{Al+Ti}$ %
1:0	1	0	24.5	0%
10:1	10	1	26.5	36%
5:1	5	1	27.5	45%
2:1	2	1	28	61%

The dielectric properties of the Ti-Al-O films grown on InAlN/GaN and AlGaN/GaN substrates were evaluated through *C-V* measurements. Leakage current density was measured for both AlGaN/GaN and InAlN/GaN MISH capacitors and is plotted at gate voltage of -1 V in Figure 28. The TiO_2 reference sample shows a high leakage current which is commonly reported in literature [109, 111, 112] (first two reported in the 10^1 A/cm^2 range at gate bias of -1 V, and last one reported in the 10^{-3} A/cm^2 range at a gate bias of 1 MV/cm) . However, a decreasing trend in leakage current is observed with increasing Al-content in the film. Compared to the pure TiO_2 sample, leakage current was reduced 2-3 orders of magnitude when a 2:1 TiO_2:Al_2O_3 cycle ratio film was used. The InAlN/GaN-based devices show larger leakage values compared to AlGaN/GaN due to the thinner and wider band-gap properties of the InAlN barrier layer.

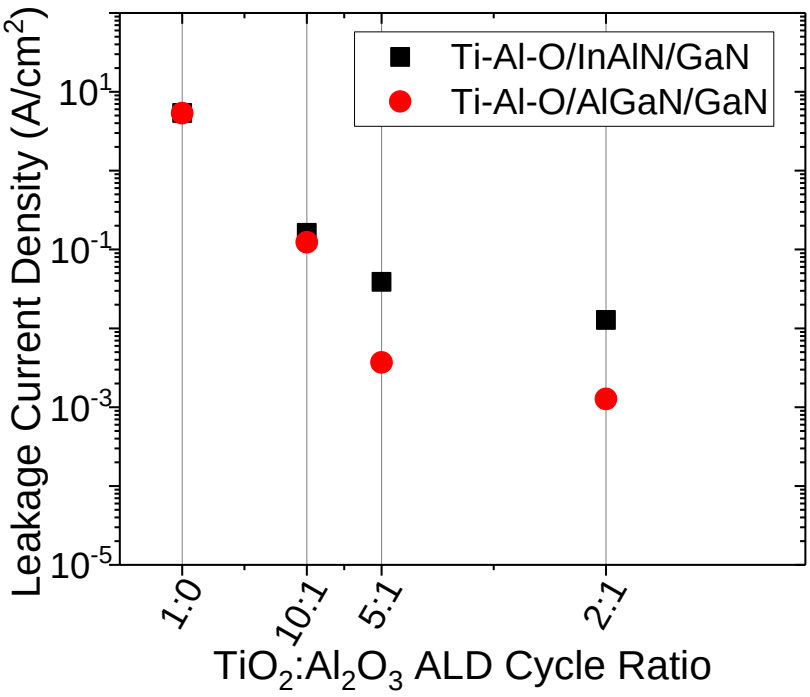


Figure 28 Leakage current density of the ALD grown Ti-Al-O on InAlN/GaN and AlGaN/GaN as a function of TiO2:Al2O3 ALD cycle ratio measured at a gate bias of -1V.

Figure 29 (a) and Figure 29 (b) shows the Capacitance-Voltage (*C*-*V*) characteristics of the Ti-Al-O dielectrics measured on InAlN/GaN and AlGaN/GaN MISH capacitors, respectively. The voltage was swept from +2 (or +1) to -5 V using a 10 kHz AC signal with 10 mV amplitude and .05 V/300 ms step size. A much sharper transition in the depletion region was observed for the 2:1 TiO_2:Al_2O_3 cycle ratio sample compared to the TiO_2 reference sample. This may be associated with a lower trap density at the insulator/semiconductor interface and our further analysis presented in a later section confirms this assumption. The *C*-*V* curve features 2 slopes during the sweep. The 1^{st} slope (at –bias) is associated with the accumulation of electrons at the InAlN(AlGaN)/GaN interface. The 2^{nd} slope (at +bias) shows the spill-over of electrons through the barrier layer onto the insulator/semiconductor interface.

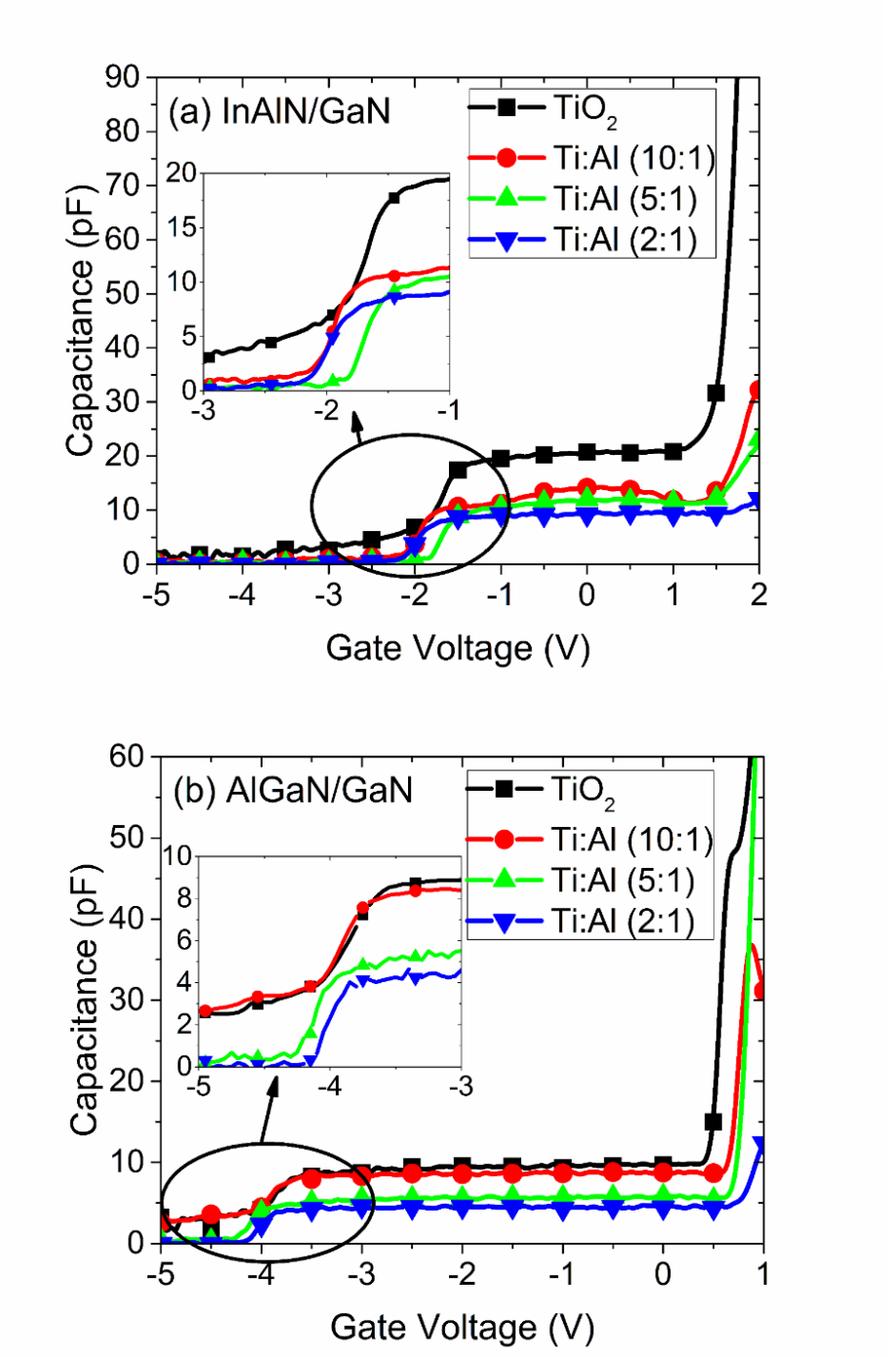


Figure 29 (a) *C-V* sweep from +2 to -5 V for the dielectrics measured on InAlN/GaN. (b) *C-V* sweep from +1 to -5 V for the dielectrics measured on AlGaN/GaN. Both are measured using an AC signal with 10 kHz frequency, 10 mV amplitude and .05 V step size. The insets show a closer view of the depletion region sweeps.

Dielectric constants were measured through the 0 V bias accumulation capacitance values. For the reference TiO_2 sample, a metal-insulator-metal capacitor was fabricated. From the capacitance measured at low voltage 1 MHz signal, the dielectric constant was directly measured to be 79 which matches well to other reported values [107] (reported to be 76). Based on this value, the InAlN barrier layer capacitance was calculated to be ~493 nC/cm^2 from the TiO_2 MISH capacitor. Using this value as a reference for all the samples, the remaining dielectric constant values were calculated using the following equation:

$$\frac{t_{ox}}{\kappa} = \varepsilon_0 A(C_{MISH}^{-1} - C_{Barrier}^{-1})$$

where t_{ox} is the thickness of the insulator, ε_0 is the permittivity of vacuum, A is the area of the MIS gate, C_{MISH} is the measured accumulation capacitance of the MISH capacitor, and $C_{Barrier}$ is the capacitance of the InAlN barrier layer. The results are plotted in Figure 30. Mixing TiO_2 with Al_2O_3 leads to a decrease in the dielectric constant, as expected. The dielectric constant of the sample with 2:1 TiO_2:Al_2O_3 cycle ratio (with Al content of 61 %), is 27 which is relatively high compared to 9, as reported for Al_2O_3 [83]. Moreover, this value is higher than the dielectric constant of HfO_2, which is widely used as gate dielectric. The composition range of our ALD Ti-Al-O films to maintain a relative high dielectric constant is relatively large.

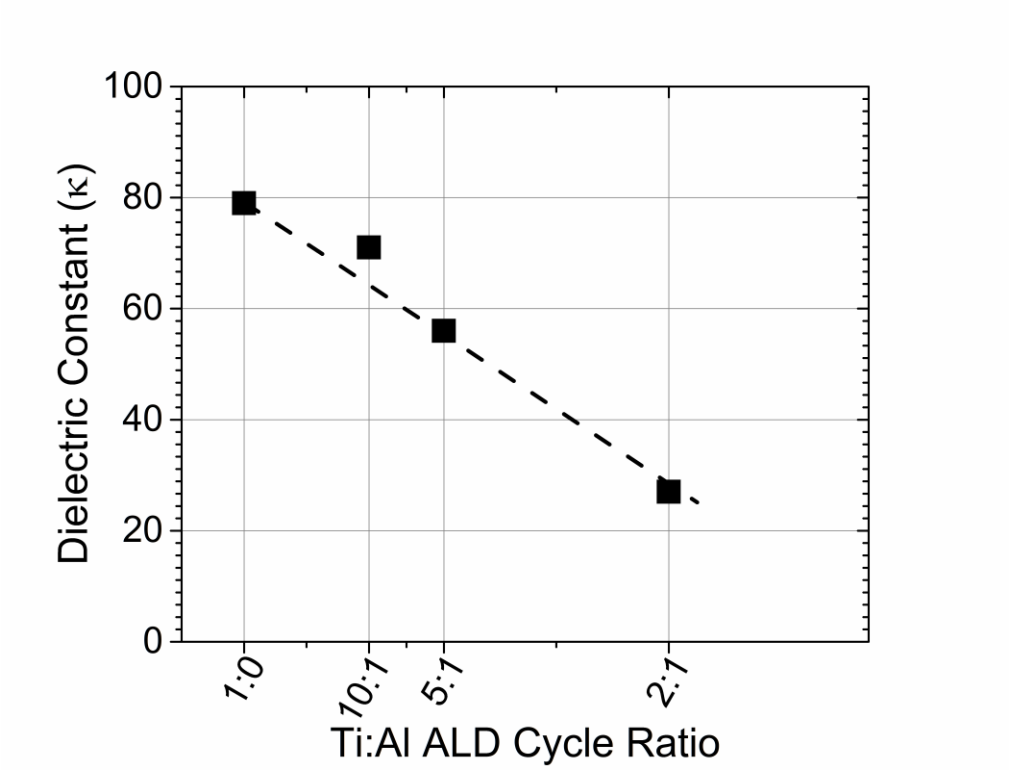


Figure 30 Calculated dielectric constants of the Ti-Al-O films as a function of TiO_2:Al_2O_3 ALD cycle ratio. Dielectric constant of the TiO_2 is 79 while even at a (2:1) ratio, dielectric constant is maintained at a relatively high value of 27.

The interface between the insulator and semiconductor are filled with interface trapped charges caused by structural defects, impurities and dangling bonds [46] described in further detail in Section 1.4. However, unlike the highly compatible Si-SiO_2 interface, which typically contains interface trap densities [113] (D_{it}) on the order of 10^{11} $eV^{-1}cm^{-2}$, high-κ materials on nitrides suffer from much larger values. It is well known that a high interface trap density causes degradation in device performance such as threshold voltage instability and degradation of 2-DEG mobility [45]. Proper selection of insulator materials based on this criterion is also important. D_{it} values were extracted from the *C-V* frequency dispersion in the 2nd slope of the *C-V* sweep using a similar

process as reported in literature [48-50] and described in detail in Section 1.4.1. Based on the onset voltage shift in the 2nd slope (shown in Figure 31), D_{it} values can be calculated for an averaged energy range (E_{avg}) using the following equations:

$$D_{it} = \left(\frac{\varepsilon_0 \kappa}{t_{ox}}\right)\left(\frac{1}{q}\right)\left(\frac{\Delta \mathrm{V}}{\Delta E}\right) = C_{ox}\left(\frac{1}{q}\right)\left(\frac{\Delta \mathrm{V}}{\Delta E}\right)$$

$$\Delta E = kTln(\frac{f_i}{f_{i+1}})$$

where q is the elemental electron charge, $\Delta \mathrm{V}$ is the measured voltage hysteresis between two different frequency sweeps, ΔE is the corresponding trap energy difference based on the measurement frequencies f_i and f_{i+1}, k is Boltzmann's constant, and T is measurement temperature. Next, the average activation energy of the traps can be calculated using:

$$E_{avg} = E_i + \frac{\Delta E}{2}$$

$$E_i = kTln\left(\frac{\sigma_c N_C v}{2\pi f_i}\right)$$

where E_i is the trap activation energy at frequency f_i, σ_c is the interface traps capture cross section, N_C is the effective density of states in the barrier conduction band, and v is the thermal velocity of electrons.

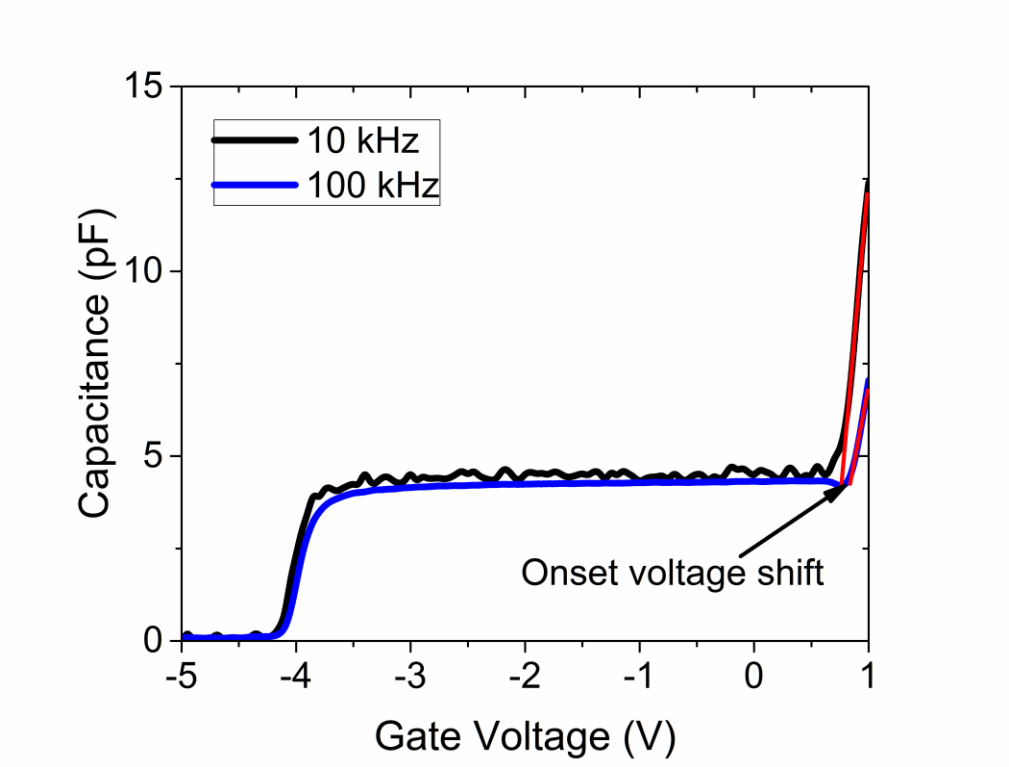


Figure 31 *C-V* sweep of TiO_2:Al_2O_3 (2:1) sample measured from AlGaN/GaN MISH capacitor. Based on the onset voltage shift measured from different frequencies in the 2nd slope, trap density values are extracted. Similar plots are measured for InAlN/GaN capacitors but only this plot is shown for clarity.

For the measured frequency range between 1 kHz to 10 kHz, the trap density is measured at the trap activation energy of 0.44 eV below the conduction band edge. The results are plotted in Figure 32. InAlN/GaN devices show larger trap densities compared to their AlGaN/GaN counterparts. However, the trap density appears to be decreasing with increasing Al-content in the film. From the *C-V* analysis in Figure 29, it appeared that the TiO_2 sample showed larger stretch-out in the depletion region compared to the Ti-Al-O films, suggesting a worse interface quality of the former, and the D_{it} analysis confirmed these results.

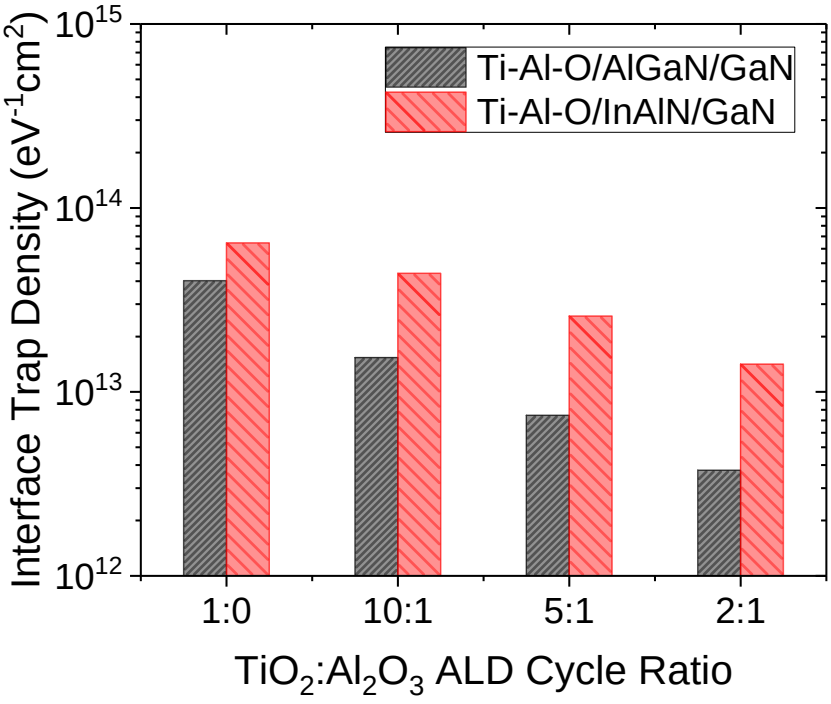


Figure 32 Interface Trap Density measured from the various MISH capacitor structures. The Ti-Al-O dielectric films on InAlN/GaN appear to have larger interface trap density values compared to their AlGaN/GaN counterparts. Trap densities decrease and show improvement with decreasing TiO_2:Al_2O_3 ratio.

4.4. Conclusions

We investigated the electrical properties of AlGaN/GaN and InAlN/GaN MISH capacitors employing ALD grown ternary Ti-Al-O compounds as the insulator. It was revealed that by increasing the Al-content in the Ti-Al-O film, the leakage current was reduced as much as by ≈2-3 orders of magnitude for the Ti-Al-O film with 61 % Al. Regarding the dielectric constant, even for an Al-content of ~61 %, the dielectric constant was maintained at a relatively high value of 27. The correlations between the interface trap-density of the films and the substrate material and

insulator Al-content were also determined through *C-V* frequency dispersion measurements. The insulators deposited on InAlN/GaN showed larger interface trap densities compared to the AlGaN/GaN counterparts. Also, the ternary compounds showed improvement in this aspect with increasing TiO_2:Al_2O_3 ALD cycle ratio. In conclusion, these ternary compounds may be an excellent choice for GaN-based devices.

5. INCORPORATION OF Al OR Hf IN ATOMIC LAYER DEPOSITION TiO_2 FOR TERNARY DIELECTRIC INSULATION OF InAlN/GaN AND AlGaN/GaN MISH STRUCTURE

In Chapter 4, I studied the effects of incorporating Al in TiO_2 to create Ti-Al-O insulating films. For this study, I extend the methodology to include Hf incorporation into TiO_2. Moreover, for a more complete experiment, I compare both Ti-Al-O and Ti-Hf-O. The following results are published in: [114] A. Colon, L. Stan, R. Divan, and J. X. Shi, "Incorporation of Al or Hf in atomic layer deposition TiO2 for ternary dielectric gate insulation of InAlN/GaN and AlGaN/GaN metal-insulator-semiconductor-heterojunction structure," Journal of Vacuum Science & Technology A, vol. 35, p. 01B132, Jan-Feb 2017. Permission to reuse this article in my thesis in in Appendix C.3. Liliana Stan assisted me with the deposition of the various dielectrics and Ralu Divan helped me with various aspects of the fabrication process including the electron-beam lithography and reactive ion etching. This work has also been presented at the 16th International Conference on Atomic Layer Deposition. Additional details have been added to this chapter which are not contained in the original publication.

5.1. Introduction

Gallium Nitride, a wide and direct bandgap semiconductor, has received much attention within the recent decades for transistors applications in high frequency power amplifiers [3], reaching mm-wave performance, and high power switches capable of withstanding breakdown up to 1035 V for a gate-drain spacing of 10 μm [2]. However, the early transistors with Schottky-gates had problems such as current collapse (drops in drain current density at high-frequency operation) and high gate leakage current. To relieve these problems, the Schottky-gate was

replaced with a Metal-Insulator-Semiconductor-Heterojunction (MISH). Thus, there have been intense studies of insulator performance on GaN. A few desired properties of insulators include high dielectric constant [57], large conduction and valence band offsets to the semiconductor [88], high crystallization temperature, low interface trap densities at the insulator/semiconductor interface and others. For further details, you may refer to Chapter 0. A high dielectric constant insulator is desired to maintain maximum channel control, increase AC transconductance [56] and minimize threshold voltage shift [57]. TiO_2 is attractive due to its high reported dielectric constant in the range of 60-120 [106, 107, 115], however it suffers from high leakage current and low crystallization temperature of 370° C [60]. A method to improve these values while maintaining a high dielectric constant is by forming a ternary compound such as Ti-Al-O or Ti-Hf-O [109, 110, 116]. By creating these ternary compounds, adequate trade-offs with these factors can be obtained. For example, as depicted in Figure 33, although Al_2O_3 has a high crystallization temperature of 900° C [61], it has a low dielectric constant value of ~9 [83]. TiO_2, being on the other half of these spectrums, exhibits the opposite behavior. Combining the two materials to create the ternary compound, Ti-Al-O, may allow for an adequate tradeoff in these factors under the 'compromise region' depicted in Figure 33. Another popular insulator, HfO_2, is also a potential material to create a ternary compound Ti-Hf-O. To date, there is limited published work investigating the performance of these ternary compounds on GaN semiconductors. To deposit these compounds, we used Atomic Layer Deposition (ALD), which is amongst the more popular insulator deposition methods due to its highly conformal process and its precise deposition control [67], further details are available in Section 0. Moreover, ALD allows relatively easy control and engineering of multicomponent film composition, thus, a nanolaminate or composite film can easily be attained by changing the numbers of alternating cycles of each component. We investigate the

compositional effects of either Al or Hf inclusion in TiO_2 by fabricating a MISH-capacitor structure using both AlGaN/GaN and InAlN/GaN substrates. By varying the ALD cycle ratio of TiO_2 and either Al_2O_3 or HfO_2, the composition of each film was varied. It was found that there is an overall improvement in insulator performance with increasing Al or Hf content, compared to a reference TiO_2 film. Gate leakage current was reduced by more than 2 orders of magnitude for the Ti-Hf-O compound with 35% Hf. Dielectric constants of the ternary compounds were maintained at a high value with a minimum at 49. Through interface trap density analysis, our studies revealed that the Ti-Hf-O contained less interface traps than the Ti-Al-O compounds at $2.2\times10^{12}\ eV^{-1}cm^{-2}$. Post-deposition annealing of the films revealed that the crystallization temperature of the compounds was increased to up to more than 600° C for the Ti-Al-O film with 45 % Al.

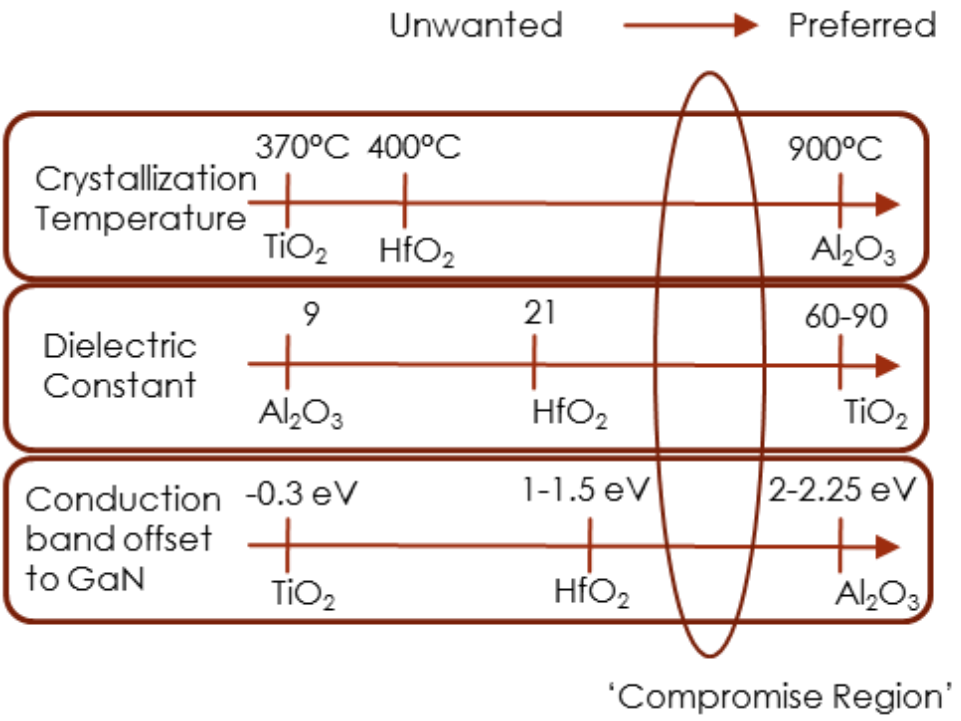


Figure 33 Diagram representing some properties of commonly used dielectrics TiO_2, HfO_2 and Al_2O_3. Desired insulator properties include high crystallization temperature, large dielectric constant, and large conduction band offset to the semiconductor. Mixing TiO_2 with Al_2O_3 or HfO_2 creates ternary compounds Ti-Al-O or Ti-Hf-O, which may provide adequate tradeoffs in these respective properties under the 'Compromise Region'.

5.2. Experimental

To characterize the insulator qualities of Ti-Al-O and Ti-Hf-O on GaN, circular MISH capacitors were fabricated. A schematic cross-sectional image of the completed structure is shown in Figure 34. Device fabrication started with AlGaN/GaN on sapphire (consisting of 1.5 nm GaN cap, 21 nm $Al_{0.25}Ga_{0.75}N$ barrier, 1 nm AlN interbarrier layer, GaN channel layer, Sapphire substrate) and InAlN/GaN on SiC (consisting of 2.0 nm GaN cap, 5.0 nm $In_{0.17}Al_{0.83}N$ barrier, GaN channel layer, AlGaN back barrier, SiC substrate) epi-wafers provided by CorEnergy Semiconductor Technology Co. Ltd. and NXP Semiconductors, respectively, cleaned by ultrasonication in acetone followed by rinsing in methanol and isopropanol. Device isolation was achieved by Inductively-Coupled-Plasma Reactive Ion Etching (ICP RIE) (PlasmaLab 100 Oxford) using an $Ar/Cl_2/BCl_3$ chemistry plasma. Ohmic contacts were formed by lift-off of multi-layered stack of Si/Ti/Al/Ni/Au (1/15/90/45/55 nm) deposited by electron beam evaporation (PVD Varian). Thereafter, ohmic behavior was achieved by rapid thermal annealing at an optimized annealing condition at 825° C in N_2 for 30 s. The transfer length measurements (TLM) performed on-chip indicated an average contact resistance of 0.42 Ω·mm for InAlN and 0.48 Ω·mm for AlGaN.

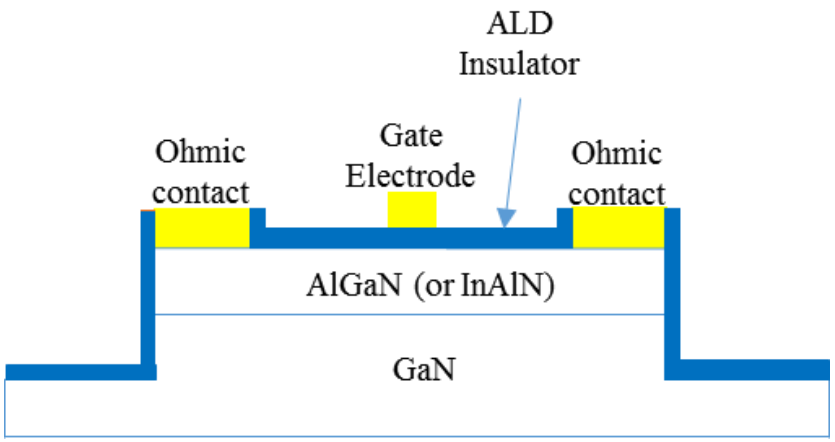


Figure 34 Cross-sectional schematic of AlGaN(InAlN)/GaN MISH-Structure.

Following the ohmic contact formation, ternary dielectric deposition was achieved by thermal ALD (Arradiance Gemstar). The ALD films were deposited on InAlN/GaN, AlGaN/GaN, and Si witness samples. Prior to being loaded in the ALD chamber, the samples underwent a cleaning treatment consisting of buffered oxide etch 10:1 (NH_4F:HF = 90:10 %) dip followed by deionized water rinsing. The Ti-Al-O and Ti-Hf-O composite films were achieved by alternating TiO_2 and either Al_2O_3 or HfO_2 cycles. Each TiO_2, Al_2O_3, and HfO_2 cycles were carried out using tetrakis(dimethylamido)titanium (TDMATi)/H_2O, trimethylaluminum (TMA)/H_2O and tetrakis(dimethylamido)hafnium (TDMAHf)/H_2O, respectively. All films were deposited at 200° C at a deposition rate of 0.37 Å/cycle for TiO_2, 1.12 Å/cycle for Al_2O_3, and 0.85 Å/cycle for HfO_2. TiO_2 was deposited as a reference control sample. To vary the composition, 1 cycle of Al_2O_3 or HfO_2 was followed by a various number of consecutive TiO_2 cycles, i.e. 1-cycle of Al_2O_3 followed by n-cycles of TiO_2. The TiO_2:Al_2O_3 and TiO_2:HfO_2 cycle ratios studied were 10:1 and 5:1. Films of 2:1 cycles ratio was also deposited, however, because of the large Al or Hf concentrations in

the films (>50 %), they are not of great interest for this particular study, in which a high Ti concentration and therefore high k value is desired. To achieve the final target thickness of ~15 nm, the super cycles were repeated. The thicknesses of the films were then measured by X-ray reflectivity (XRR) (Bruker D8 Discover) and the elemental composition was determined by X-ray photoelectron spectroscopy (XPS).

Following the insulator deposition, the gate contacts were patterned by e-beam lithography (Raith 150) using the bi-layer resist process, e-beam evaporation of Ti/Au (28/110 nm) and metal lift-off. Lastly, to make electrical contact to the covered ohmic contact regions, the insulator films were etched from these regions using ICP RIE in an Ar/Cl_2-based plasma.

5.3. Results and Discussion

Ti-Al-O and Ti-Hf-O films of compositions in the TiO_2-rich composition range were grown on the InAlN/GaN and AlGaN/GaN substrates. Their elemental compositions were evaluated from their XPS spectra and their thickness from their XRR spectra. The results are summarized in Table XIII. XPS is a surface sensitive analysis technique but 'surface' in the sense of 8-10 nm deep [117]. During the atomic layer deposition process, we kept the frequency of each deposited material relatively high. For example, at a TiO_2:Al_2O_3 10:1 ratio, we had 10 ALD cycles of TiO_2 which corresponds to ≈ 3.7 Å followed by 1 cycle of Al_2O_3 corresponding to ≈1.12 Å. These super-cycles were repeated several more times to obtain the desired thickness of the composite film. Considering 1 super cycle is a couple-atomic layers thick, we can safely assume XPS can give us an accurate description of film composition. Moreover, we first measured film composition through electron dispersive spectroscopy (EDS) and later precisely confirmed the values using XPS.

Table XIII ALD films processing conditions, thickness and composition. 1:0 ratio (top row) is the reference TiO_2 film. The TiO_2 and Al_2O_3 or HfO_2 ratios were varied to produce different Al or Hf-content in the films.

					Composition	
Ratio	TiO_2 cycle(s)	Al_2O_3/HfO_2 cycle	Ti-Al-O thickness (nm)	Ti-Hf-O thickness (nm)	Al-concentration ($Ti_{1-x}Al_xO$)	Hf-concentration ($Ti_{1-x}Hf_xO$)
1:0	1	0	13.6		0 % (TiO_2)	
10:1	10	1	17.0	13.4	36 % ($Ti_{64}Al_{36}O$)	18 % ($Ti_{82}Hf_{18}O$)
5:1	5	1	18.1	13.7	45 % ($Ti_{55}Al_{45}O$)	31 % ($Ti_{69}Hf_{31}O$)

The X-ray diffraction (XRD) measurements of as-deposited films revealed that the amorphous structure of as-deposited TiO_2, Ti-Al-O and Ti-Hf-O films persists in the whole investigated compositional range. To determine the temperature stability of the films, post-deposition annealing (PDA) was performed at various temperatures in O_2 ambient for 10 minutes and the XRD spectra measured thereafter and shown in

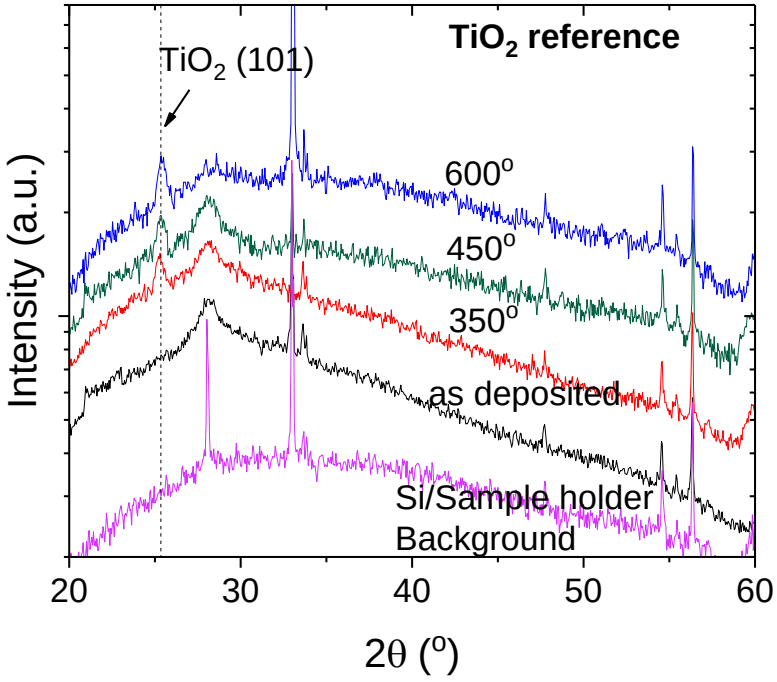


Figure 35 and Figure 36. The presence of the peaks at 25.17° corresponding to the anatase (101) TiO_2 structure in the XRD TiO_2 spectra shown in

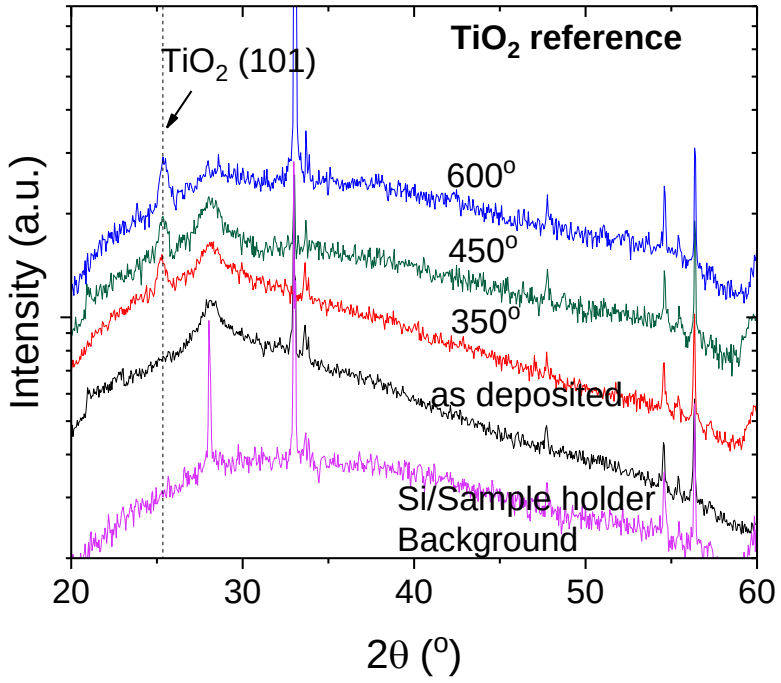


Figure 35, indicates that the films annealed at 350° C and above are crystalline. The other peaks present are the result of the diffraction from the sample holder and the silicon substrate as

they are present during a bare Si/sample holder scan shown in

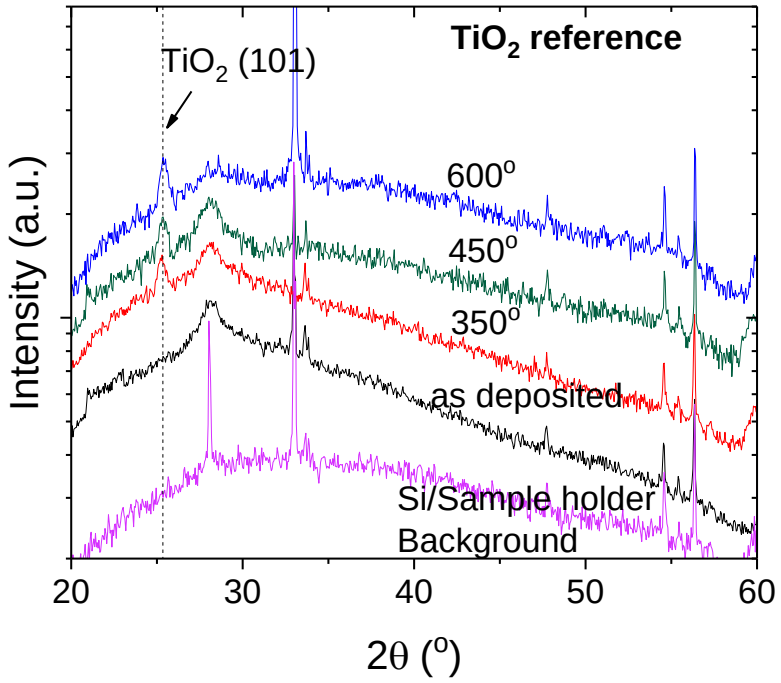


Figure 35. After PDA at 450° C, the TiO_2:HfO_2 (10:1) starts to crystallize while the other composite films remain amorphous (Figure 36a). After PDA at 600° C, all composites except the TiO_2:Al_2O_3 (5:1) become crystalline (Figure 36b). In conclusion, the temperature stability of the composites is increased by adding Al or Hf in the TiO_2 and it is dependent on both the dopant type, whether it is Al or Hf, and the % composition.

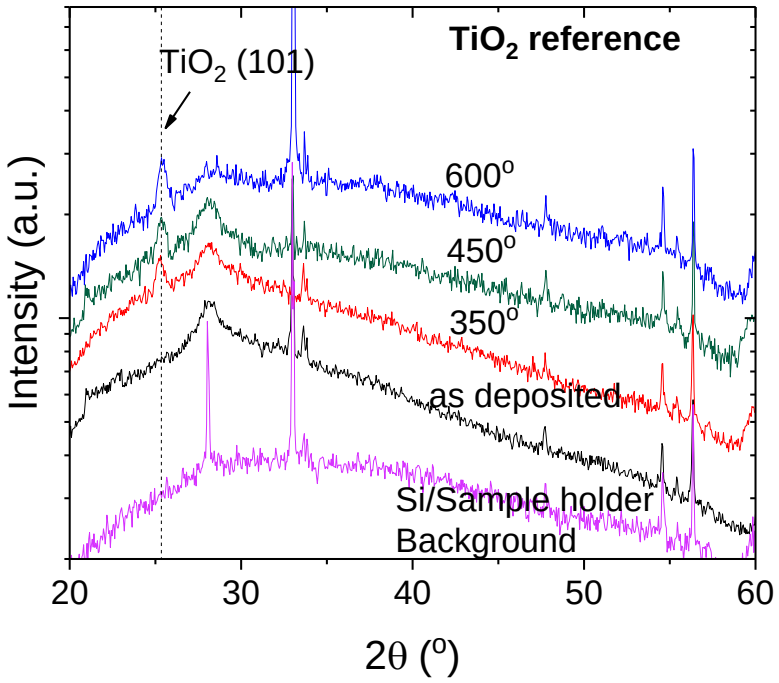


Figure 35 XRD spectra of the TiO_2 reference sample. The bottom spectrum is a background scan from Silicon substrate and sample holder. Thereafter spectra correspond to as-deposited, annealed at 350° C, annealed at 450° C, and annealed at 600° C films.

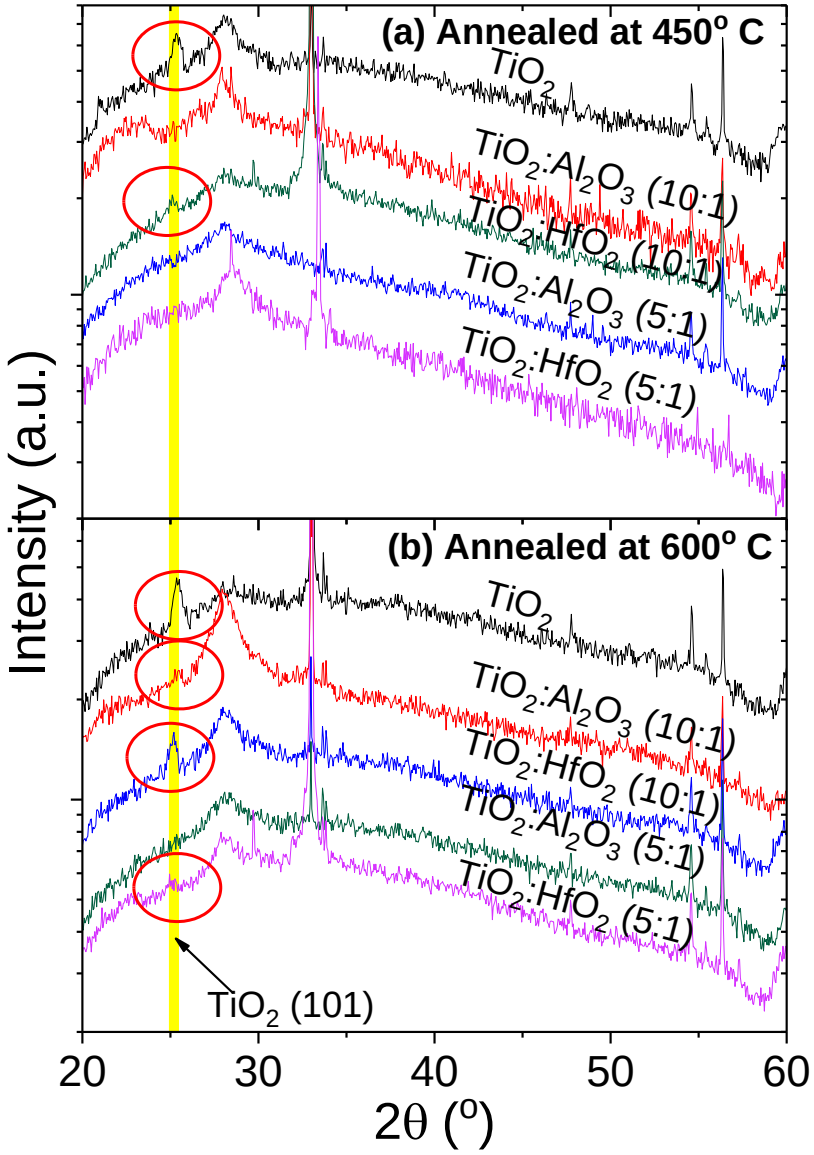


Figure 36 XRD spectra of post-deposition annealed films. (a) After annealing at 450° C. (b) After annealing at 600° C.

The insulating properties of the ternary Ti-Al-O and Ti-Hf-O films grown on InAlN/GaN and AlGaN/GaN substrates were evaluated through current-voltage (*I-V*) measurements. Leakage current density was measured for both AlGaN/GaN and InAlN/GaN MISH capacitors and is plotted with gate voltage swept from -7 V to +1 V with a 0.1 V step size (Figure 37). Although the leaky TiO_2 reference sample shows a high leakage current density, these values are commonly reported in literature [109, 111, 112]. A decreasing overall trend in leakage current is observed with increasing Al or Hf-content in the films. Compared to the pure TiO_2 sample, leakage current was reduced about 2 orders of magnitude using a 5:1 cycles ratio TiO_2:Al_2O_3 composite film. However, the Ti-Hf-O compounds demonstrate lower leakage values than the Ti-Al-O compounds with the lowest being about 3 orders of magnitude lower than TiO_2 measured on InAlN/GaN. The InAlN/GaN-based devices shows larger leakage values compared to AlGaN/GaN due to the thinner barrier layer and wider band-gap properties of the InAlN, which may create a lower conduction band offset to the insulator compared to AlGaN.

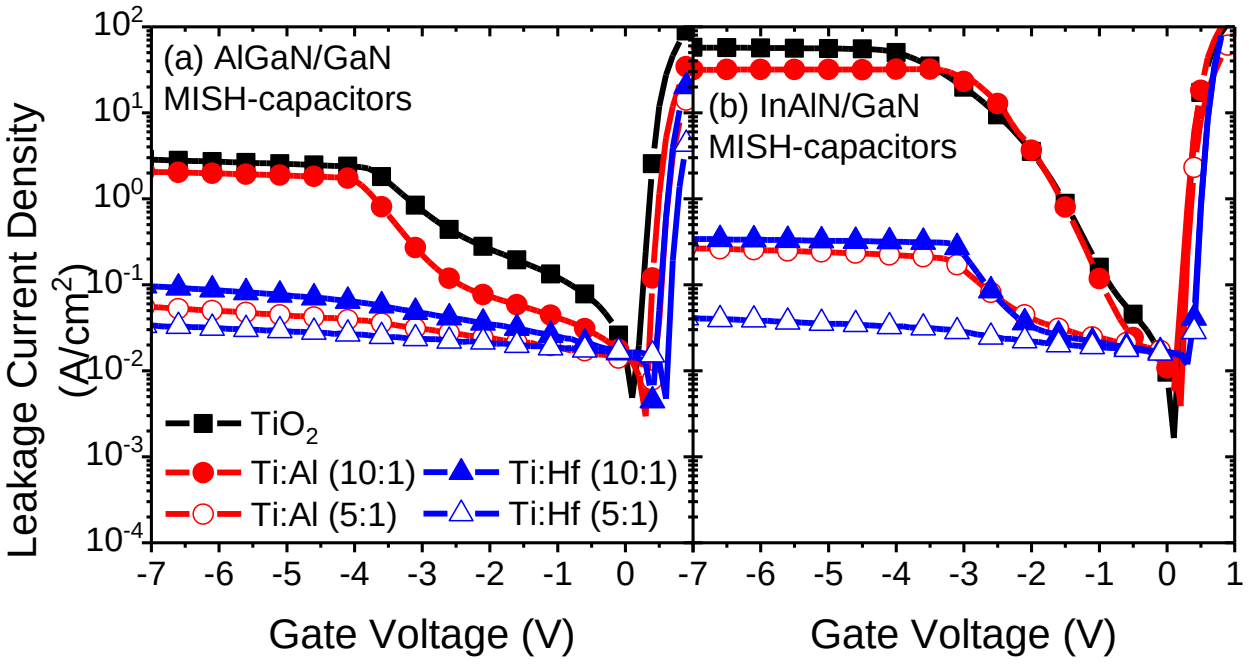


Figure 37 Leakage current density of the ALD grown TiO_2 (black curves), Ti-Al-O (red curves) and Ti-Hf-O (blue curves) on (a) AlGaN/GaN and (b) InAlN/GaN as a function of gate voltage.

Figure 38 (a) and Figure 38 (b) shows the capacitance-voltage (*C-V*) characteristics of the Ti-Al-O and Ti-Hf-O dielectrics measured on AlGaN/GaN (Figure 38a) and InAlN/GaN (Figure 38b) MISH capacitors, respectively. The voltage was swept from 0 V to -5 V using a 1 MHz AC signal with 10 mV amplitude and .05 V / 300 ms step size. A much sharper transition in the depletion region was observed for the 5:1 TiO_2:Al_2O_3 and TiO_2:HfO_2 cycle ratios sample compared to the TiO_2 reference sample on both substrates. A noticeable feature comparing the AlGaN/GaN and InAlN/GaN MISH capacitors is a much sharper *C-V* depletion region sweep for the former set of capacitors.

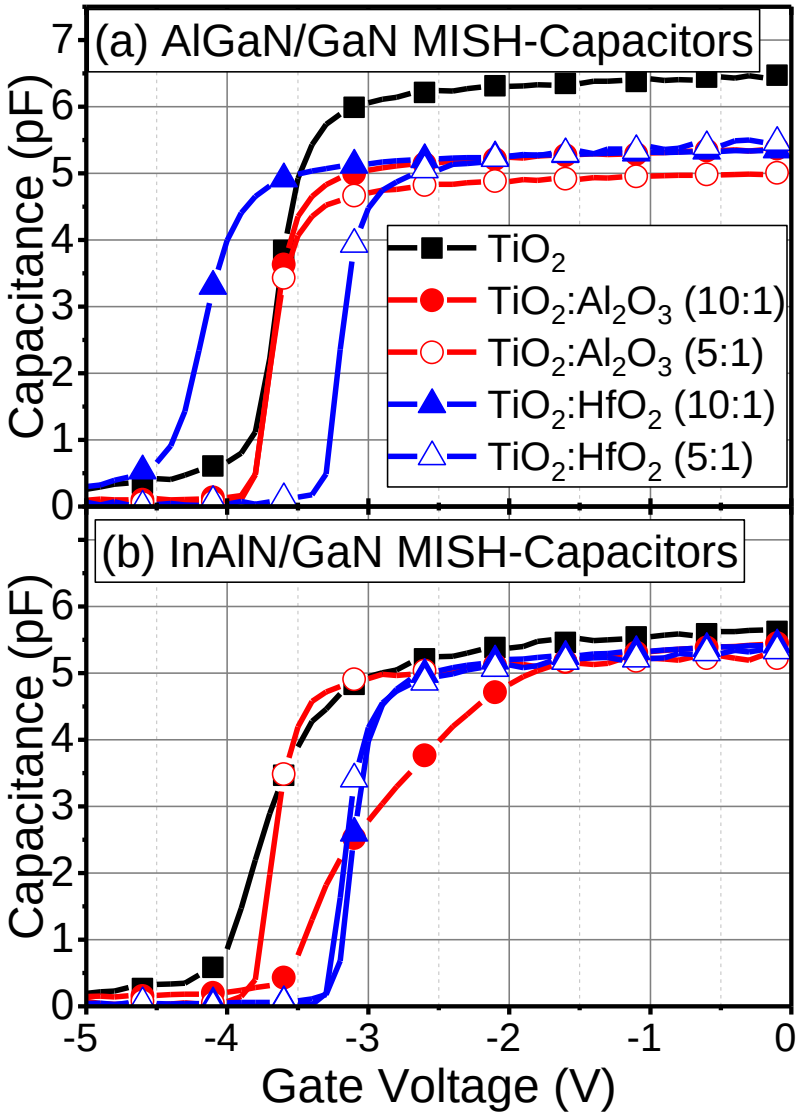


Figure 38 C-V sweeps from 0 V to -5 V for the dielectrics measured on (a) AlGaN/GaN and (b) InAlN/GaN MISH capacitors. Measured using an AC signal with 1 MHz frequency, 10 mV amplitude and .05 V step size.

Dielectric constants were measured through the 0 V bias accumulation capacitance values. For the reference TiO_2 sample, a metal-insulator-metal capacitor was fabricated. From the capacitance measured at low voltage 10 kHz signal, the dielectric constant was directly measured to be 79 which matches well to other reported values [107, 115] (reported to be 76 and 70, respectively). The relatively high dielectric constant of our ALD grown TiO_2 may be, to some degree, attributed to low film density [115]. That also influences the leakage current. Since the insulator forms a parallel plate capacitor in series with the barrier layer capacitance, the InAlN barrier layer capacitance can be calculated using the TiO_2 reference value. Thereafter, the remaining dielectric constant values were calculated from the InAlN MISH capacitors. The results are plotted in Figure 39. Mixing TiO_2 with Al_2O_3 or HfO_2 leads to a decrease in the dielectric constant, as expected. The dielectric constants of the Ti-Al-O and Ti-Hf-O composites studied here remain relatively high (around 50) compared to 9 or 21, as reported for Al_2O_3 [83] and HfO_2 [2], respectively. Counterintuitively, the κ-values of the Al doped films are higher than the Hf doped counterparts. It has been shown that porous films with low density present high dielectric constant (particularly at a low frequency) and high leakage current density [115]. We believe that the Ti-Al-O composite films may be porous. This assumption is sustained by higher thickness of the Ti-Al-O films compared with the expected thickness according to the number of ALD cycles. Also, low-density Ti-Al-O films explain the higher leakage current densities measured on the Ti-Al-O MISH capacitors.

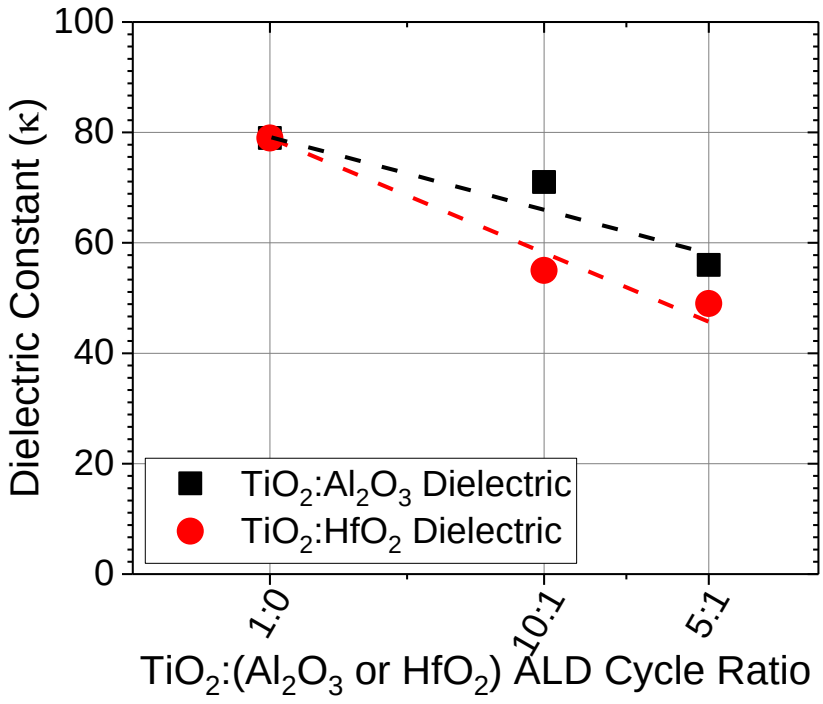


Figure 39 Calculated dielectric constants of the Ti-Al-O and Ti-Hf-O films as a function of TiO_2:Al_2O_3/HfO_2 ALD cycle ratio. The dielectric constants are maintained at a relatively high value of 56 for TiO_2:Al_2O_3 (5:1) and 49 for TiO_2:HfO_2 (5:1).

A quantitative analysis of interface trap density (D_{it}) between the insulator and semiconductor is an important characteristic of the compatibility of an insulator on semiconductors. Interface trapped charges can be caused by several defects such as structural defects, impurities and dangling bonds [46], described in further detail in Section 1.4.1. D_{it} values were extracted from the *C-V* frequency dispersion in the 2nd slope of the *C-V* sweep using a similar process as reported in literature [48-50], and summarized in Section 1.4.1. As shown in Figure 40, a complete *C-V* curve features 2 slopes during a sweep. The 1st slope (at –bias) is associated with the accumulation of electrons at the InAlN(AlGaN)/GaN interface. The 2nd slope (at +bias) occurs

due to the spill-over of electrons through the barrier layer onto the insulator/semiconductor interface. Based on the onset voltage shift in the 2nd slope (shown in Figure 40 inset) with measurement frequency change, D_{it} values may be extracted. By measuring the onset voltage shifts with respect to frequency, an average interface trap density may be extracted using:

$$D_{it} = \left(\frac{C_{ox}}{q}\right) \times \left(\frac{\Delta \mathrm{V}}{\Delta E}\right)$$

where C_{ox} is the insulator capacitance, q is the elemental electron charge, ΔV is the measured voltage hysteresis and ΔE is the corresponding trap energy difference. The corresponding trap energy difference can be calculated by:

$$\Delta E = kTln(\frac{f_i}{f_{i+1}})$$

where k is Boltzmann's constant, T is the measurement temperature and f_i and f_{i+1} are the two different measurement frequencies. The corresponding average trap activation energy is calculated by:

$$E_{avg} = \mathrm{k}Tln\left(\frac{\sigma_c N_C v}{2\pi f_i}\right) + \frac{\Delta E}{2}$$

where σ_c, interface traps capture cross section, N_C, effective density of states in the barrier layer conduction band, and v, thermal velocity of electrons, are assumed [118] to be $3.4 \cdot 10^{-15}$ cm^2, $2.2 \cdot 10^{18}$ cm^{-3} and $2.6 \cdot 10^7$ cm/s.

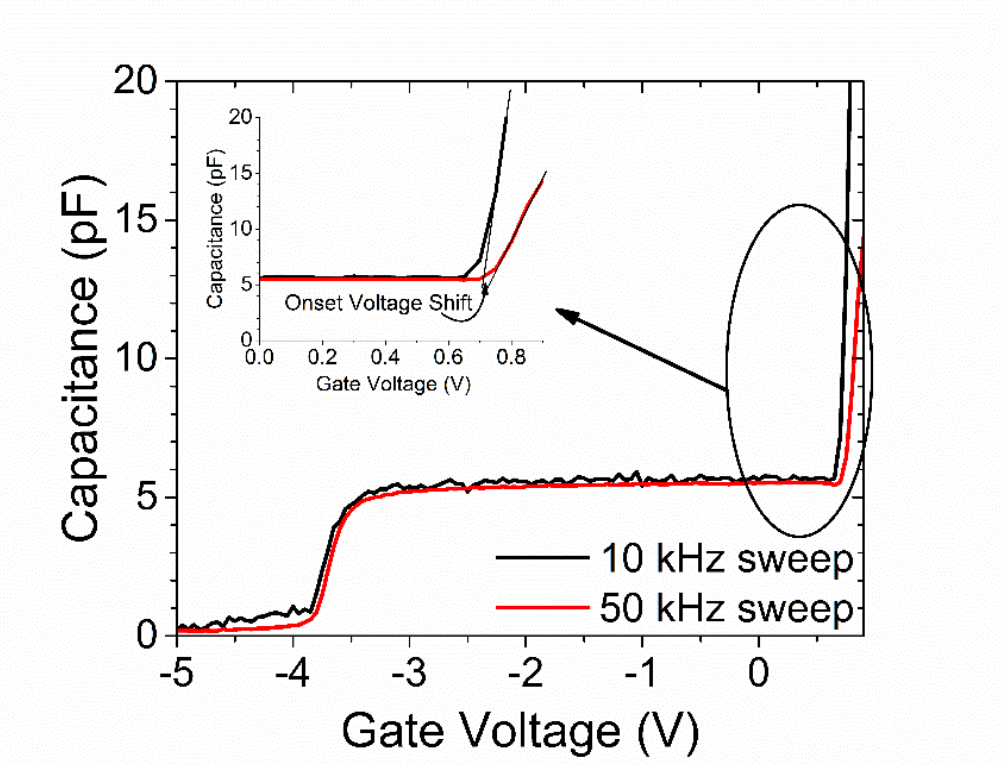


Figure 40 Full C-V sweep of TiO_2:HfO_2 (5:1)/AlGaN/GaN MISH capacitor. The inset shows further detail on the 2nd slope's onset voltage shifts. Similar curves are measured for the rest of the MISH capacitors but are not shown.

The trap activation energy for the measured frequency range of 1 kHz to 10 kHz corresponds to 0.44 eV below the conduction band edge. The extracted D_{it} results are plotted in Figure 41. InAlN/GaN devices show larger trap densities compared to their AlGaN/GaN counterparts. However, the trap density appears to be decreasing with increasing Al or Hf-content in the film with the Ti-Hf-O compound exhibiting better performance than the Ti-Al-O compounds. Compared to values reported in literature for Al_2O_3 and HfO_2 on AlGaN/GaN [105, 119] larger than $4 \cdot 10^{13}$ $eV^{-1}cm^{-2}$, the ternary compounds appear to have lower trap densities. Moreover, there are no reported Ti-Al-O or Ti-Hf-O composites on InAlN/GaN substrate to

compare to. From the *C-V* analysis in Figure 38, it appeared that the TiO_2 sample showed larger stretch-out in the depletion region compared to the compound films, suggesting a worse interface quality of the former, thus, the D_{it} analysis confirmed these results.

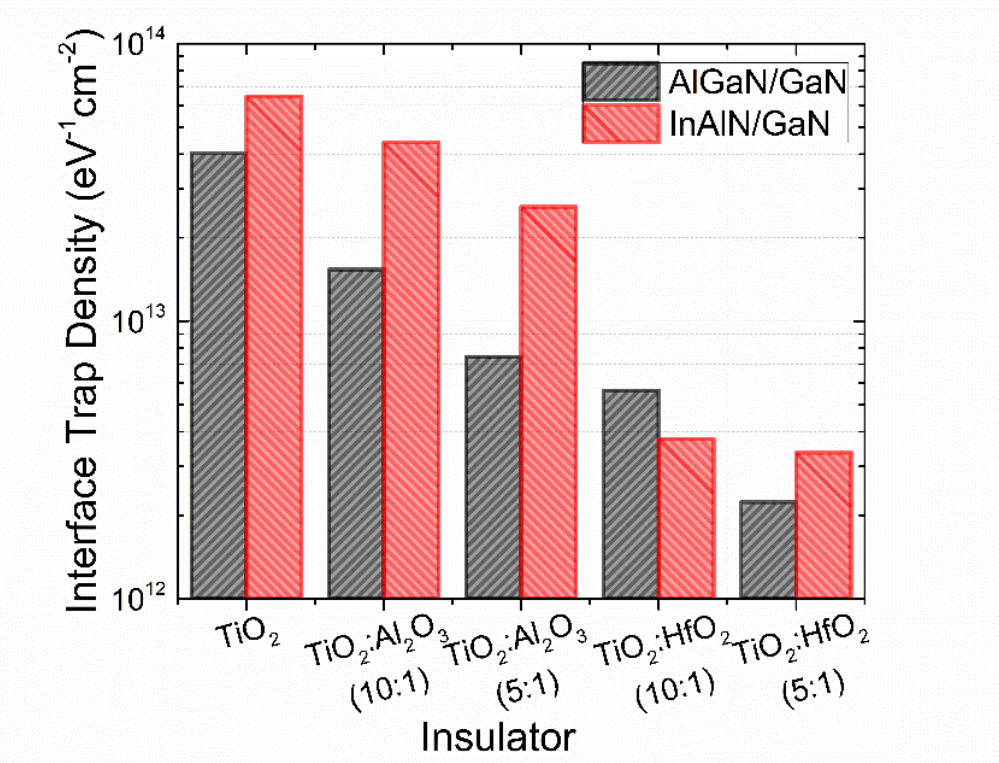


Figure 41 Interface Trap Density measured from the various MISH capacitor structures through frequency-dependent C-V sweeps.

5.4. Conclusions

We investigated the electrical properties of AlGaN/GaN and InAlN/GaN MISH capacitors employing ALD grown ternary Ti-Al-O and Ti-Hf-O compounds of various compositions as an insulator. It was revealed that by increasing the Al or Hf-content in the film, the leakage current was reduced as much as ~2-3 orders of magnitude for the Ti-Al-O, however, the Ti-Hf-O films

showed the lowest leakage overall. Regarding the dielectric constant, the values were held high at 56 and 49 for the $Ti_{55}Al_{45}O$ and $Ti_{69}Hf_{31}O$ composites, respectively. It was shown that the crystallization temperatures of the composite films were increased substantially up to more than 600° C for the TiO_2:Al_2O_3 (5:1) film, compared to a crystallization temperature <350° C found for pure TiO_2. The correlations between the interface trap-density of the films and the substrate material were also determined through *C-V* frequency dispersion measurements. The insulators deposited on InAlN/GaN showed larger interface trap densities compared to the AlGaN/GaN counterparts. While the ternary compounds showed improvement in this aspect with increasing TiO_2:Al_2O_3 or TiO_2:HfO_2 ALD cycle ratio, the Ti-Hf-O composites showed smaller trap densities compared to Ti-Al-O. In conclusion, we have demonstrated the performance of ternary insulator composites of various compositions on both AlGaN/GaN and InAlN/GaN substrates. Through our analysis, we have shown that the composites offer improved properties than TiO_2 while maintaining the attractive high-κ properties of this film. The Ti-Al-O composites offered a larger increase in thermal stability but the Ti-Hf-O films displayed lower leakage current and lower interface trapped charges.

6. InAlN/GaN TRANSISTOR OFF-STATE BREAKDOWN VOLTAGE ENHANCEMENT BY PASSIVATION

This chapter briefly covers a method studied through simulation by my colleague, Chenjie Tang, in [120], on a technique to improve breakdown voltage of an InAlN/GaN transistor. The goal in this study is to experimentally verify these results.

6.1. Introduction

AlGaN/GaN transistors have shown off-state breakdown voltages upwards of 1000 V for a gate-drain spacing of 10 μm in [2]. However, InAlN/GaN transistors of similar dimensions exhibit premature breakdowns much further below both theoretical limits and AlGaN/GaN counterparts of similar dimensions. To date, it is still unclear the exact mechanisms for early breakdown but possible mechanisms may be due to epi-structure design, large peak electric fields in the semiconductor or surface traps inducing electron hopping, among a few to mention. I refer you to [120] to learn more about the subject.

[120] studied the effects of 'capping' an InAlN/GaN power transistor with an insulator, referred to as passivation on breakdown voltage through simulation. This passivation is performed as the last step in fabrication process. Chenjie found that the breakdown voltage of the transistor increases as the product of dielectric constant and thickness ($\kappa \cdot t_{passivation}$) of the passivating layer increases. Thus, to increase breakdown voltage, it is desirable to deposit a very thick (> 5 μm) passivation with low dielectric constant such as SiO_2, or a thinner passivation layer with high dielectric constant.

6.2. Experimental

Device fabrication started with thorough cleaning of InAlN/GaN epi-wafers provided by NXP semiconductors. Metal alignment markers of Ti/Au (10/50 nm) were patterned by co-

polymer lift-off process patterned by electron-beam lithography. Next, device isolation was accomplished by mesa structure through Cl_2-based ICP-RIE dry-etching. Ohmic contact formation was achieved through lift-off of Si/Ti/Al/Ni/Au (1/15/90/45/55 nm) metallization by e-beam evaporation followed by rapid thermal annealing at 825° C for 30 s in N_2 ambient to reveal a minimum contact resistance measured of 0.17 Ω·mm by TLM patterns on chip. Afterwards, SiO_2 was deposited by PECVD as a field-oxide followed by wet etching in BOE from the active regions. Prior to gate metallization of Ti/Au (28/250 nm) by lift-off, 18.1 nm of Al_2O_3 was deposited as gate insulation/passivation by atomic layer deposition. Figure 42 contains an SEM image of the edge of the transistor at this point of the process. Thereafter, Cl_2-based ICP-RIE etching was utilized to remove the Al_2O_3 from the source/drain contacts, masked using resist. Ti/Au metallization was patterned by lift-off for source, drain and gate contact pads. Lastly, to compare the effects of passivating/capping the device, one chip's processing ended here while another underwent passivation of 3 μm of Si_3N_4 by PECVD. Following passivation of the device, the metal contact pads (covered by Si_3N_4) were exposed using CF_4-based RIE with 100 nm of chromium as the etch mask. The device fabrication is summarized in Figure 44. The device's geometry reported here is a 2-finger gated device with width = 100 μm x 2, L_{sg} = 1 μm, L_g = 1 μm and L_{gd} varied. Figure 43 contains the SEM image of a completed transistor with L_{gd} = 10 μm.

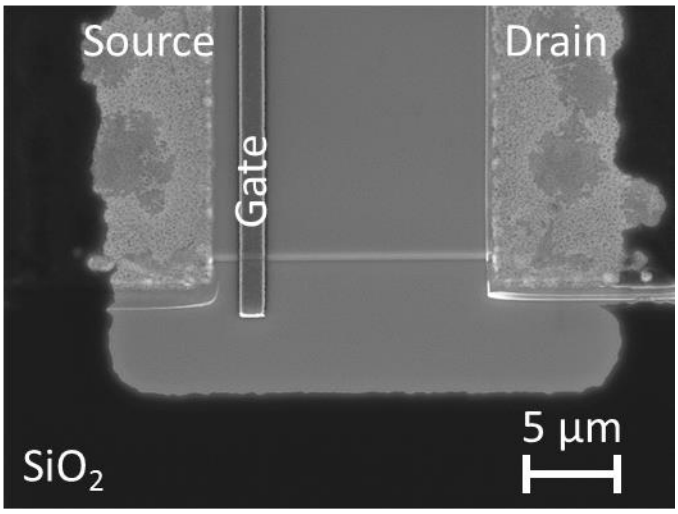


Figure 42 SEM image of InAlN/GaN MISHFET half-way through the fabrication process (i.e. post field oxide etching).

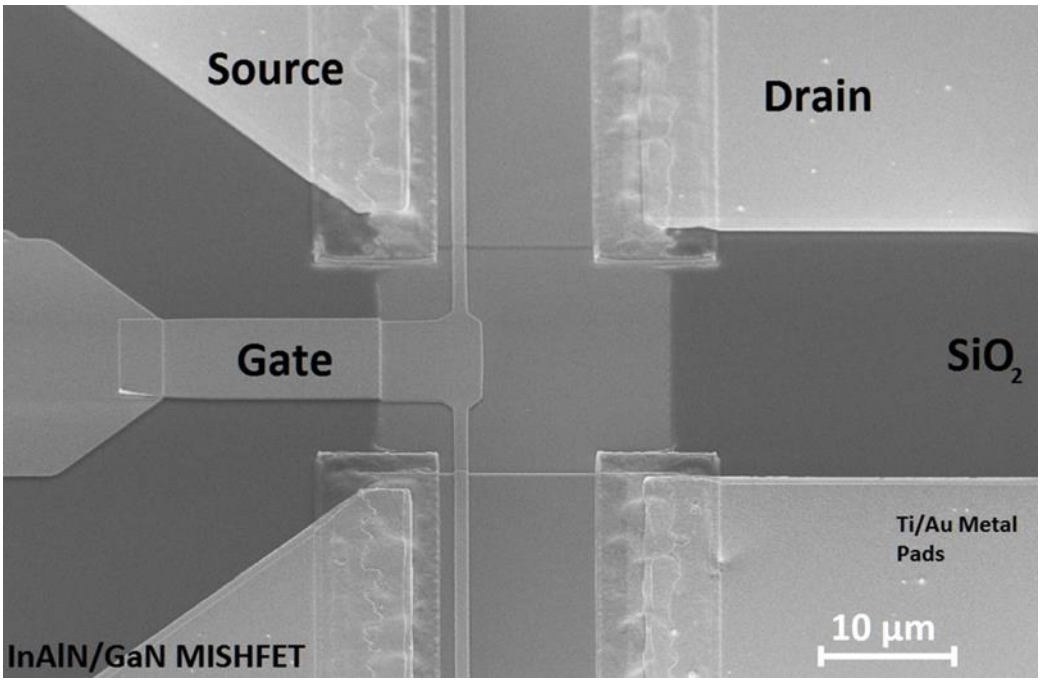


Figure 43 SEM image of completed 2-finger gated InAlN/GaN MISHFET.

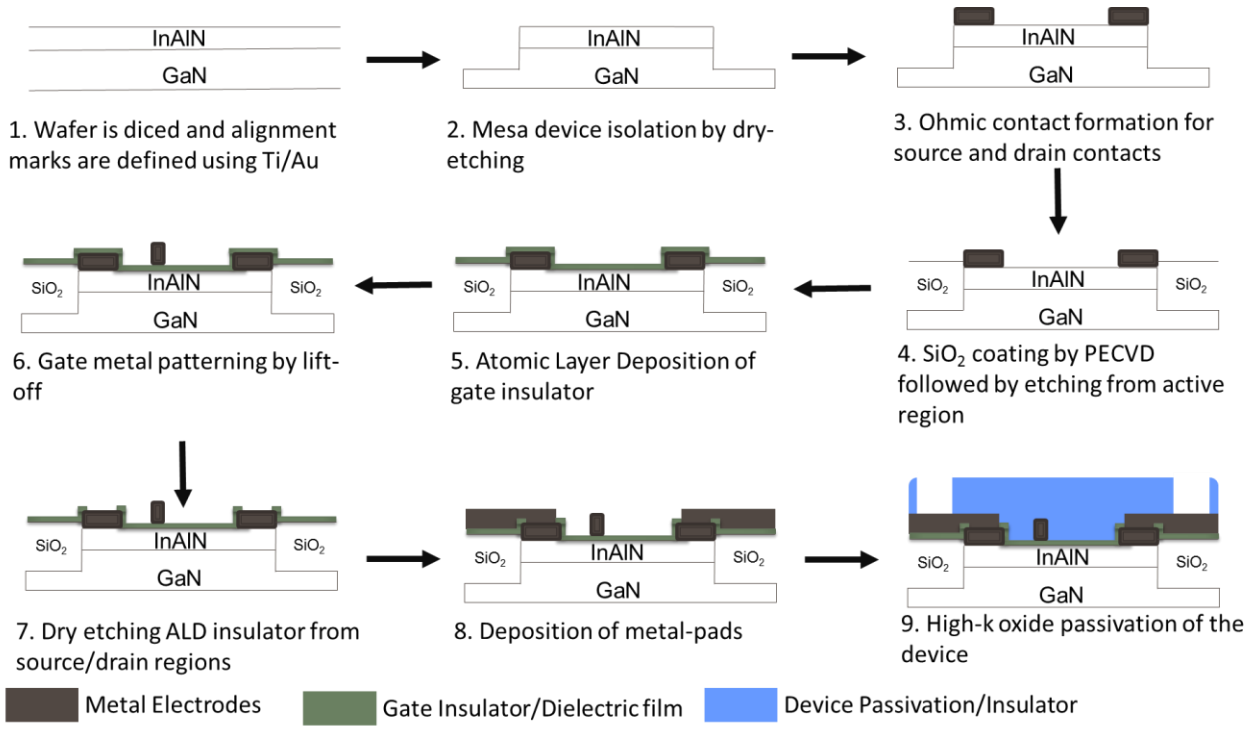


Figure 44 Cross-sectional schematic showing InAlN/GaN transistor device fabrication process.

6.3. Passivation Layer Choice

Since the passivation requires a thick layer, the deposition methods are limited to high-deposition rate methods. Moreover, high-κ materials, are desirable such as TiO_2 (79) or HfO_2 (21). Although TiO_2 is available through atomic layer deposition, it's extremely slow deposition rate makes it an impractical venue. A promising avenue I investigated was at UIC's Laboratory for Oxide Research and Education (LORE), led by Prof. Jeremiah Abiade. Here, they have a pulsed-laser deposition system capable of deposition various ceramic materials at a high rate such as Strontium Titanium Oxide, or STO. STO has been reported to have a dielectric constant > 150 [121], making it an attractive material to use as the passivating layer. However, as I learned in

Chapter 4 and 5, there is an obvious trade off in materials with dielectric constants and bandgap (i.e. leakage current). Thus, it was important to characterize these materials prior to applications for InAlN/GaN power transistors. Chen Chen from LORE agreed to help me do a few deposition test runs of STO. I compared 3 materials: TiO_2 by RF magnetron sputtering, STO by pulsed layer deposition, and Si_3N_4 by plasma enhanced chemical vapor deposition. To characterize the materials, I fabricated metal-insulator-metal capacitors (MIM) and measured leakage current as this was a high priority to maintain low to prevent early breakdown of the transistor. To fabricate MIM capacitors, Si/SiO_2 (bulk/ 2 μm) substrates were coated with 100 nm of Titanium metal. Afterwards, insulator film was deposited: for TiO_2, RF magnetron sputtering of 50 nm of TiO_2 was performed in a CVC system, 4000 pulses (~300 nm) of STO was deposited on a pulsed laser deposition system at LORE by Chen Chen, and ~250 nm of Si_3N_4 was deposited by PECVD. Afterwards, circular gate electrodes were defined by optical lithography followed by lift-off of 50 nm of Titanium. Leakage current of the MIM capacitors was measured by sweeping gate electrode voltage and measuring current. The results are plotted in Figure 45. TiO_2 showed an excessive amount of leakage current followed by STO and Si_3N_4 showed the lowest leakage current from the set. Since the Ti-based insulators showed such large leakage currents, I decided to use Si_3N_4 as passivating material for the transistors. For STO to become a more viable candidate, I would suggest to research methods to improve insulating properties such as by thermal annealing or other methods.

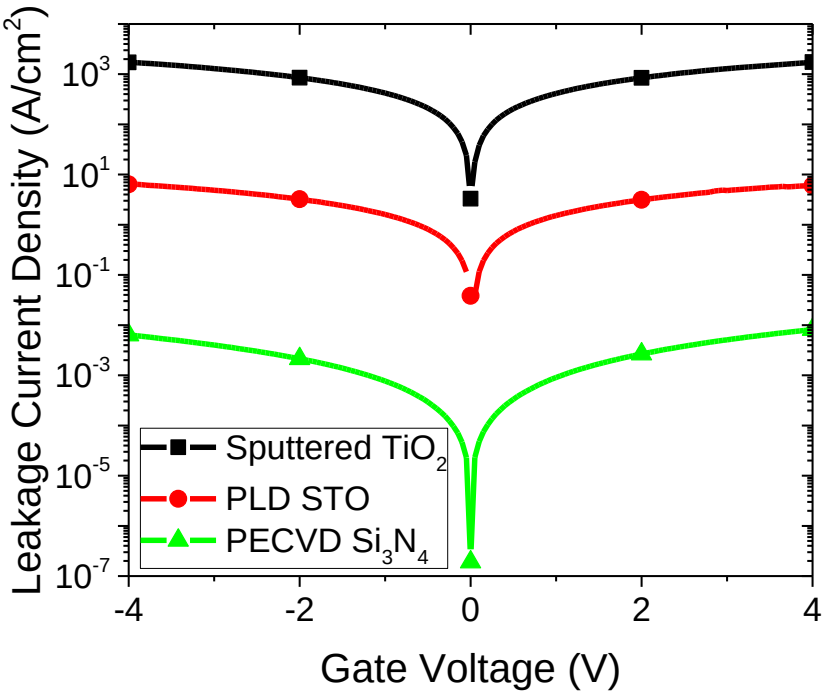


Figure 45 Leakage current density of select dielectric films which are candidates for transistor passivation materials.

6.4. Results and Discussion

6.4.1. Low-Voltage DC Performance

All current-voltage (I-V) measurements were performed in a dark-box using a Keithley 4200-SCS system. Shown in

Figure 46, the transfer curves measured from each respective device indicates a maximum transconductance of ~180 mS/mm with a threshold voltage of -5.45 V for the device without the passivation. However, the device with passivation reported a drop in transconductance by ~25 % along with a positive-shift in threshold voltage to -4.96 V possibly due to the replacement of air's

dielectric constant of 1 with silicon nitride's higher permittivity surrounding the gate. Gate leakage current density is plotted as a function gate voltage in

Figure 47. No degradation is observed in gate leakage after passivating, moreover, very low leakage current densities are measured on the order of 10^{-11} A/mm.

Figure 48 shows the DC I_d-V_d sweeps of the devices with and without the Si_3N_4 passivation. As can be observed, the passivation increases the device's on-resistance along with a drop in maximum drain current density.

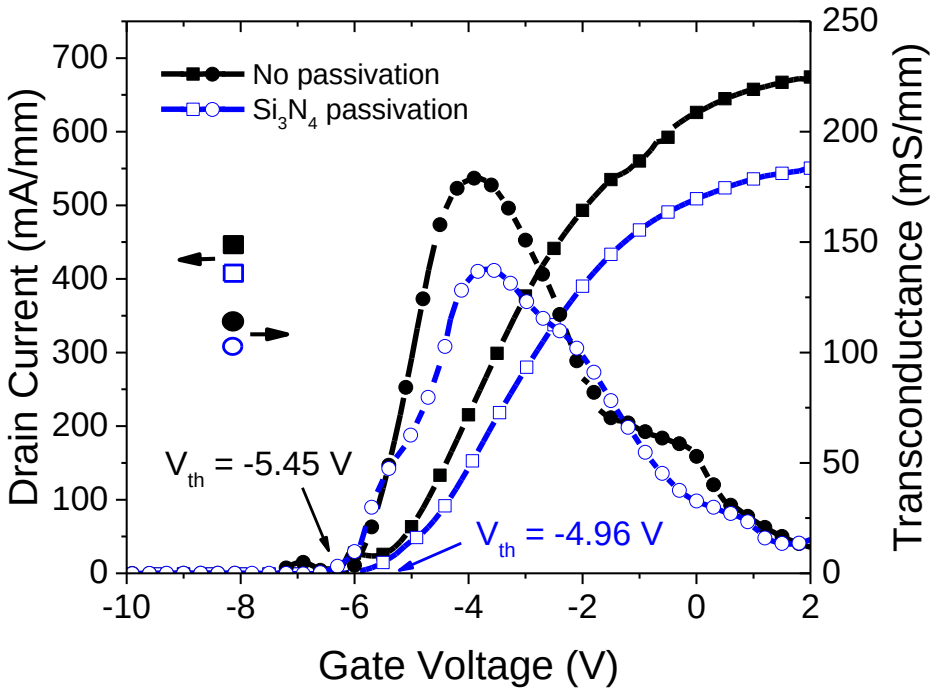


Figure 46 Transfer curves of InAlN/GaN transistors with (hollow-blue symbols) and without (solid-black symbols) the Si_3N_4 passivation.

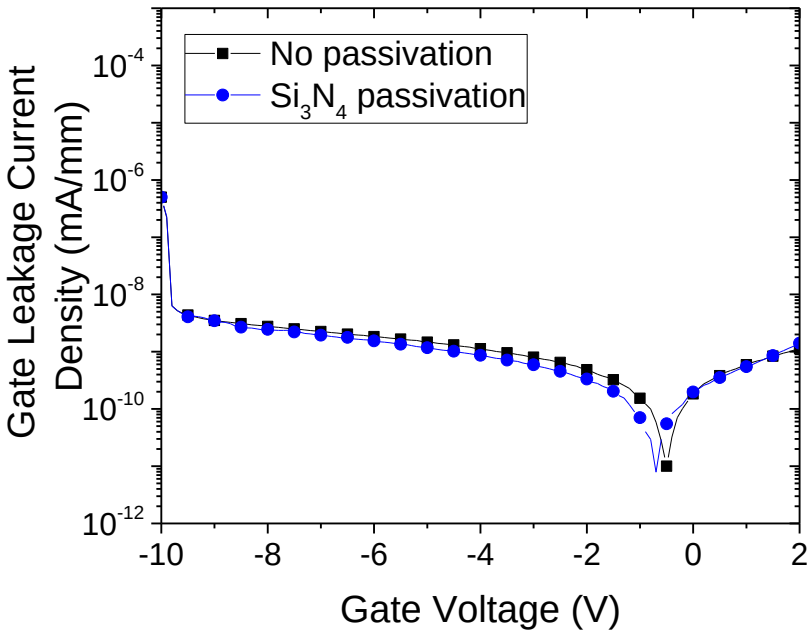


Figure 47 Gate leakage current density for InAlN/GaN transistors with and without Si_3N_4 passivation.

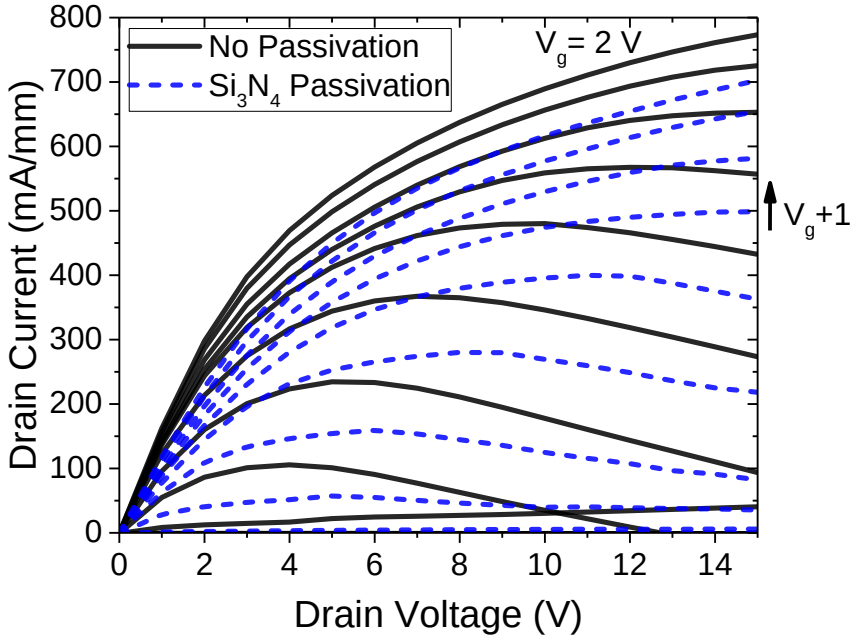


Figure 48 'Family of Curves' (I_d-V_d) measured using gate voltage bias starting from V_g = -6 V incrementing +1 V up to V_g = 2 V. Comparing transistors with (dashed blue line) and without (solid black line) Si_3N_4 passivation.

6.4.2. Off-State Breakdown Voltage

To observe 3-terminal off-state breakdown of the device, during measurement, the sample was immersed with Fluorinert FC-40. Gate voltage was held at 2 V below threshold voltage to fully deplete the 2DEG, source was grounded, while drain voltage was ramped up to device breakdown, i.e. defined when drain or gate leakage current reaches 1 mA/mm. For breakdown measurements > 200 V, the measurement was performed using the Keithley 4200 in conjunction with a Keithley 2290-5, which limits the drain-current reading down to 1 μA resolution. For breakdown measurements < 200 V, the measurement can be run using only the Keithley 4200 which has current resolution down to pA-range. For the un-passivated device, I fabricated several transistors dimensions with different gate-to-drain spacing: 3, 10 and 15 μm, all with the same source-to-gate and gate lengths of 1 μm each. As shown in

Figure 49, breakdown voltage scales as expected with increasing gate-to-drain separation. For L_{gd} = 3 μm, device breakdown occurs at 53 V. Increasing L_{gd} to 10 μm increases the breakdown up to 270 V. At this point, leakage current does not reach 1 mA/mm, however, device destruction occurred. For L_{gd} of 15 μm, device destruction occurs at 614 V. shows a un-passivated transistor after device destruction from the breakdown measurements. The device essential 'blows-up' due to the surge of large currents at the point of breakdown

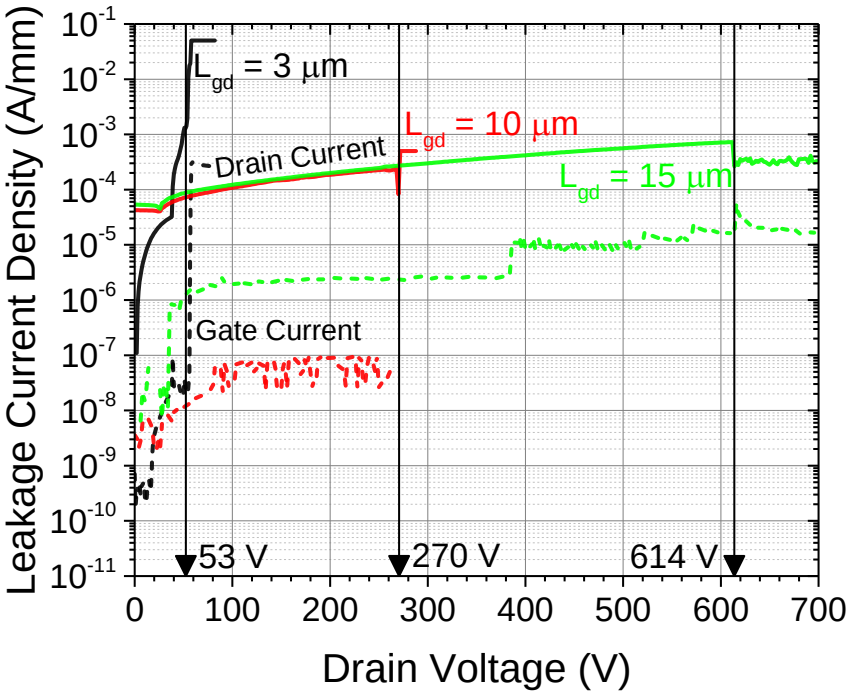


Figure 49 Breakdown voltage scaling with gate-to-drain spacing of InAlN/GaN MISHFETs without a capping/passivating dielectric layer.

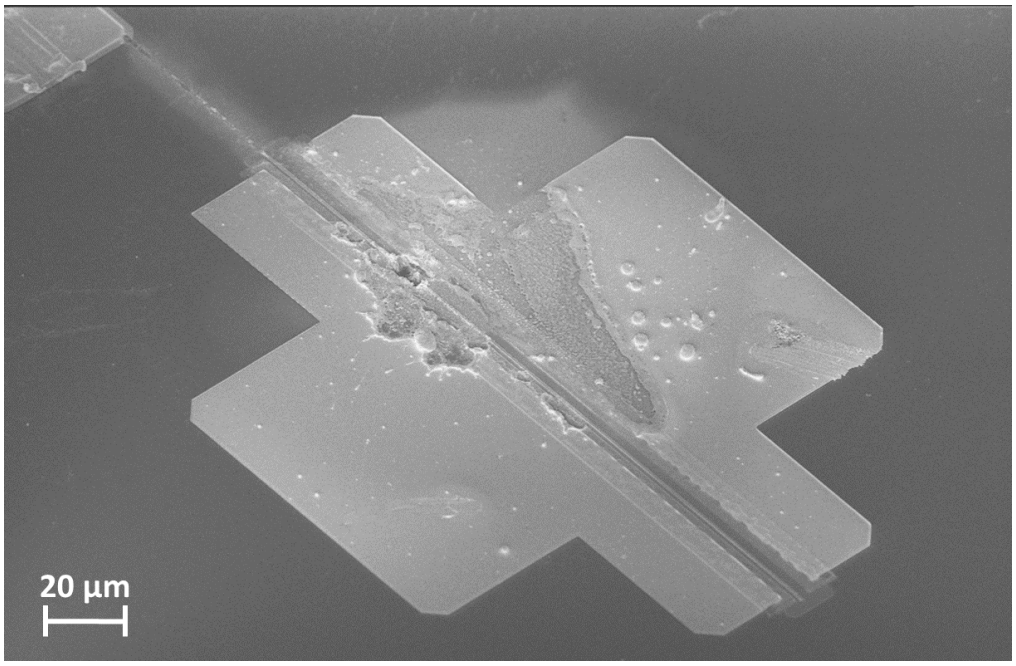


Figure 50 SEM image of InAlN/GaN MISHFET after device destruction during breakdown measurements.

Next, the device passivated with 3 µm of Si_3N_4 was measured and the results are plotted in Figure 51 with the un-passivated device shown as reference. The devices shown here have similar device geometries with L_{sg} = 1 µm, L_g = 1 µm and L_{gd} = 3 µm. As shown, the device without passivation breaks down at 53 V, while the passivated device withstands breakdown up to 200 V, indicating a large improvement upward of 400 % increase in breakdown. I should mention, however, from an array of 3-operational passivated devices, only 1 of them showed breakdown up to 200 V. The other 2 measured devices had breakdown around 60 V. At this point, it is unclear whether the other 2 devices were defective, thus a second process to make more passivated transistors is required to further prove the point.

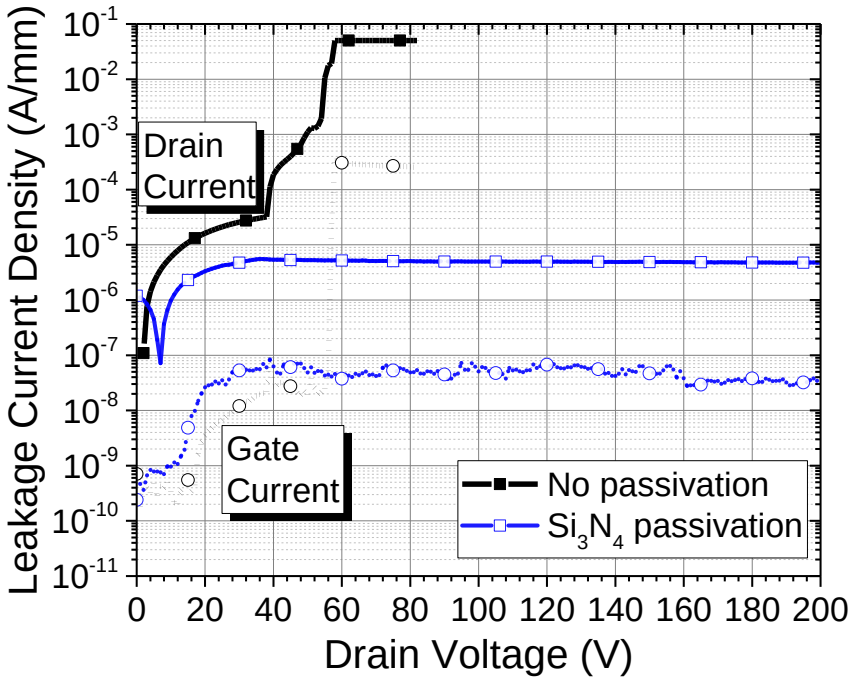


Figure 51 Effects of passivation/capping an InAlN/GaN MISHFET on off-state breakdown voltage.

6.5. Conclusion

To summarize, InAlN/GaN transistors were fabricated to compare the effects of capping the transistor with 3 μm of Si3N4 on the electrical characteristics, more importantly, three-terminal off-state breakdown. Preliminary results show a > 400 % improvement in breakdown voltage after passivation. However, passivation negatively affected on-resistance, decreased the maximum drain current density and slightly degraded transconductance. Future work includes investigating other high-κ materials as the passivating insulator with emphasis on maintaining low leakage films.

7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusion

The preceding chapters have focused on the transistor-level design aspects of a GaN MISHFET organized by fabrication process hierarchy. First, in Chapter 2, I studied techniques towards improving ohmic contact resistance as low as possible; a delicate process dependent on a wide array of parameters such as metal thicknesses, ratios, annealing conditions, pre-treatments, etc. By systematically optimizing each variable, a very low contact resistance of 0.14 Ω·mm on AlGaN/GaN and 0.17 Ω·mm on InAlN/GaN was realized. Moreover, low-annealing temperature (450° C) ohmic contacts were realized using a recessed-ohmic and gold-free process, albeit with much room for improvement.

Chapters 3, 4 and 5 investigated several high-κ insulating materials. Starting with Chapter 3, I investigated the performance of HfO_2, Al_2O_3/HfO_2, $HfAlO_x$, $HfSiO_x$. Here, we learned that leakage current can be suppressed, compared to HfO_2, by either depositing nanolaminate of Al_2O_3 prior to the thicker HfO_2 layer (bilayer stack) or by using ternary compounds $HfAlO_x$ and $HfSiO_x$. More importantly, we studied the insulator/semiconductor insulator traps through the conductance method and correlated the results with electrical phenomena. We found that HfO_2 provides the lowest interface trap densities, within the investigated range.

In Chapter 4, I further expanded on the idea of using ternary dielectric compounds to obtain adequate trade-offs in many important insulator properties. Using TiO_2 as a reference, which provides an excellent high dielectric constant but poor leakage blocking, Aluminum was incorporated in the film using ALD to create Ti-Al-O films. The ternary compounds provided enhanced insulating qualities and lower defect densities all while maintaining the attractive properties of the reference TiO_2 film. Chapter 5 further built upon Chapter 4 by investigating

using either Hf or Al in TiO_2 to improve the TiO_2's insulating capabilities. By increasing the Hf or Al concentration in TiO_2 up to 50%, the dielectric constant was maintained relatively high while decreasing leakage current by more than two orders of magnitude. More importantly, we found that the insulator/semiconductor defects (i.e. interface trap densities), are reduced drastically with Al or Hf inclusion.

From the studies performed in Chapters 3 and 5, I can confirm that HfO_2 provides an excellent compatibility with GaN in terms of insulator/semiconductor defects. If we compare HfO_2 (studied in Chapter 3) and $Ti_{69}Hf_{31}O$ (studied in Chapter 5) interface trap defects at similar activation energy on AlGaN/GaN, the HfO_2/AlGaN structure contains trap defects $\approx 2\times10^{11}$ $cm^{-2}eV^{-1}$ and the $Ti_{69}Hf_{31}O$/AlGaN structure contains trap defects $\approx 2\times10^{12}$ $cm^{-2}eV^{-1}$. These values were less than what was found for the other investigated insulating materials in both chapters.

Lastly, Chapter 6 confirmed the theoretical/simulation results [120] investigated by my colleague, Chenjie Tang, on a technique to increase off-state breakdown of an InAlN/GaN transistor. Using 3 µm-Si_3N_4 capping layer, the last step in the process, the off-state breakdown was increased by more than 400 %, compared to a device without the capping layer.

7.2. Future Work

This thesis has laid the foundation for the culmination of this work: a high-performance RF-power amplifier. However, there is much room for improvement. On the ohmic contact front, the low-temperature gold-free process showed promising results, however, the high contact resistance measured makes it unpractical to use. I believe the main problem with the process is associated with the high-temperature exposure during the e-beam evaporation of the refractory metals (Hf, Ta, etc.). I would suggest an alternate means of deposition such as magnetron

sputtering. However, this process would require patterning by etching instead of the conventional lift-off method. Moreover, instead of BCl_3-based ohmic recess, I would suggest $SiCl_4$-based recessing instead as it has been shown to yield better results in Section 1.3.2.

On the topic of insulators on GaN for gate insulation, we have seen that HfO_2 provides low defect densities. However, the values reported are quite high compared to the SiO_2/Si systems. More work is necessary to investigate techniques towards improving the interface. Either by pre-deposition surface treatment (ozone cleaning, Hydrofluoric acid cleaning) or post-deposition processing (annealing in O_2). This is important to reduce transistor performance degradation, especially in the RF operation regime. Moreover, measurement setup to probe traps with a much wider activation energy range is needed such as by photo-assisted *C-V* or another method. One possible approach to measure photo-assisted C-V is by utilizing LEDs of various wavelengths. I suggest LEDs within the range of 1.5 eV (826 nm, infrared) up to 3.0 eV (400 nm, ultraviolet). Moreover, it would be important to choose LEDs with sufficiently low spectral half width of at minimum 20 nm. This is to obtain a more precise measurement as close as would be obtained using lasers.

Improvement of off-state breakdown voltage by passivation requires more investigation. Although I studied Si_3N_4 as the passivation layer, this material is not considered a 'high-κ insulator'. High-κ materials typically involve a trade-off in insulating properties with dielectric constant. Improving the insulating properties of high-κ materials is necessary to make it practical to use as a passivation layer to improve off-state breakdown. I would suggest investigating using a bi-layer structure (idea similar to the HfO_2/Al_2O_3 structure used in Chapter 3) or a post-deposition treatment (such as annealing) to improve the insulating qualities of the high-κ materials. In the case of a bi-layer structure, at least 50 nm of Al_2O_3 is recommended to minimize leakage current

followed by a much thicker high-κ dielectric such as Strontium Titanium Oxide (STO) to take advantage of its' large permittivity. Insulators such as Strontium Titanium Oxide or Barium Strontium Titanate are extremely attractive due to their large dielectric constant, however, I would advise tackling the issue of leakage prior to applying these for high-voltage transistors.

Lastly, InAlN/GaN transistors are capable of mm-wave performance. Much of the work in this thesis lays the foundation for fabricating such as device. However, to realize a high-performance device requires normally-off operation, low ohmic contact resistance, sub-50 nm gate footprint, high-breakdown strength and mitigation of short-channel effects. In the case of electron-beam lithography, proximity effect correction, or scattering reduction is a major issue concerning the minimum resolution obtainable for fabricating such a transistor. I started investigating this issue and found adequate values for scattering reduction are as follows: Alpha: 13 nm, Beta: 1721 nm, Eta: 0.5. I would suggest using these values as a starting point as they are not fully optimized to the substrates I used, nor the resist (950PMMA-A4/PMGI SF9/InAlN/GaN/SiC). I used these values to obtain a source-drain spacing of 1 μm for patterning the lift-off resist for ohmic metals. T-Gate structure definition still requires investigation. Using a tri-layer resist stack of ZEP502A:Anisole (2:1)/PMGI-SF9/ZEP520A:Anisole (2:1) patterned at 30 kV acceleration voltage using Si substrate, the minimum resolution obtained was 173 nm as depicted in Figure 52. More work is necessary to further reduce the gate footprint and transition to GaN/SiC substrates. To reduce the gate footprint further, I suggest utilizing a high voltage electron beam lithography system (100 kV, JEOL 9300FS) and venturing into cold-development processing.

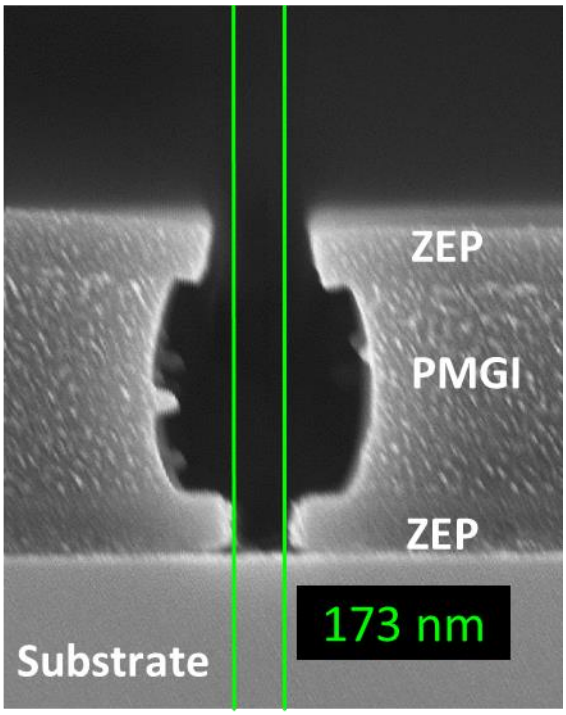


Figure 52 Electron beam lithography tri-layer resist stack after development for T-Gate definition.

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APPENDICES

APPENDIX A

A.1 Introduction

This appendix covers the process flow for various fabrication runs. The listed process flows use a combination of instruments at both Argonne National Laboratories Center for Nanoscale Materials and UIC's Nanotechnology Core Facility.

APPENDIX A (continued)

A.2 Process Flow for Transfer Length Method Pattern (ohmic contacts) Processing

Layer 1- Mesa etch

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake 115° C for 2 minutes
3. Spin Coat S1813 at 4000 RPM for 45 seconds
4. Soft bake at 115° C for 1 minute
5. Exposure: Karl Suss MA6 (at Argonne) 2.6 seconds
6. Develop CD26 for 1 minute followed by DI rinse
7. Etching using Oxford PlasmaLab ICP-RIE
    a. Recipe: “AC GaN Ar/Cl2/BCl3 CH1”
    b. $Ar/Cl_2/BCl_3$ (7/20/9 sccm), RF: 35 W,ICP: 380 W, Pressure: 11 mTorr
    c. Time: 1 minute
    d. Etch rate: ~150 nm/min
8. Resist strip in 1165 Remover for 4 hours
9. Descum in March RIE O_2 plasma
    a. 12 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 40 W

APPENDIX A (continued)

Layer 2- Ohmic metals

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake 180° C for 2 minutes
3. Spin coat LOR 3A at 2000 RPM for 45 seconds
4. Soft-bake at 180° C for 5 minutes
5. Spin coat S1813 at 4000 RPM for 45 seconds
6. Exposure: Karl Suss MA6 (at Argonne) 2.6 seconds
7. Develop CD26 1 minute, DI rinse
8. Bake 125° C for 1 minute
9. Develop CD26 25 seconds
10. Descum in March RIE O_2 plasma
    a. 2 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 20 W
11. Native oxide etch in BOE 20:1 dip for 30 seconds followed by DI rinse
12. Varian E-beam evaporation of Si/Ti/Al/Ni/Au (1/15/90/45/55 nm)
    a. Replace Ti source with Ni after deposition of Ti
13. Lift-off by soaking in 1165 remover overnight
14. Rapid Thermal Annealing at 825° C for 30 seconds in N_2 ambient
    a. Recipe: “AC825C30.RPD”
15. Contact resistance measurement using Probe Station

APPENDIX A (continued)

A.3 Process flow for Power Amplifiers

Layer 1: Alignment Markers

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake at 256° C for 2 minutes
3. Spin coat PMGI SF9 at 2000 RPM for 45 seconds
4. Soft bake at 256° C for 15 minutes
5. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
6. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reduction:
        i. Emitech k675X sputter coat 12 nm
7. Raith Exposure of alignment markers
    a. Properly adjust dosage for smaller features
    b. Write Field: 1000x, 100 μm
    c. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$

    Optional steps:

    7a. Gold coating removal using Au-etchant 15 seconds
8. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
9. Develop MC 101 for 90 seconds followed by DI rinse 20 seconds, N_2 blow dry
10. Descum in March RIE O_2 plasma
    a. 2 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 20 W
11. E-beam evaporation of Ti/Au or Ti/Pt (10/60 nm)
12. Lift-off by soaking in 1165 remover overnight

APPENDIX A (continued)

Layer 2- Mesa etch

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake 90° C for 4 minutes
3. Spin Coat Ma-N 2405 at 3000 RPM for 30 seconds
4. Soft bake at 90° C for 90 seconds
5. Raith Exposure of mesa patterns
    a. Write Field: 500x, 200 μm
    b. EHT: 30 kV, Aperture: 30 μm, Dosage: 220 $\mu C/cm^2$
6. Develop Ma-D 533S:DI (3:1) for 40 seconds followed by DI rinse
7. Hard Bake at 100° C for 10 minutes
8. Etching using Oxford PlasmaLab ICP-RIE
    a. Recipe: “AC GaN Ar/Cl2/BCl3 CH1”
    b. $Ar/Cl_2/BCl_3$ (7/20/9 sccm), RF: 35 W,ICP: 380 W, Pressure: 11 mTorr
    c. Time: 1 minute
    d. Etch rate: ~150 nm/min
9. Resist strip in 1165 Remover for 4 hours
10. Descum in March RIE O_2 plasma
    a. 12 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 40 W

APPENDIX A (continued)

Layer 3- Ohmic metals

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake at 256° C for 2 minutes
3. Spin coat PMGI SF9 at 2000 RPM for 45 seconds
4. Soft bake at 256° C for 15 minutes
5. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
6. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reduction:
        i. Emitech k675X sputter coat 12 nm
7. Raith Exposure of ohmic contacts
    a. Properly adjust dosage for smaller features
    b. Write Field: 1000x, 100 μm
    c. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$

    Optional steps:

    7a. Gold coating removal using Au-etchant 15 seconds

8. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
9. Develop MC 101 for 90 seconds followed by DI rinse 20 seconds, N_2 blow dry
10. Descum in March RIE O_2 plasma
    a. 2 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 20 W
11. Varian E-beam evaporation of Si/Ti/Al/Ni/Au (1/15/90/45/55 nm)
    a. Replace Ti source with Ni after deposition of Ti
12. Lift-off by soaking in 1165 remover overnight
13. Rapid Thermal Annealing at 825° C for 30 seconds in N_2 ambient
    a. Recipe: “AC825C30.RPD”
14. Contact resistance measurement using Probe Station

APPENDIX A (continued)

Layer 4- SiO_2 Field Oxide

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Deposition of SiO_2 by PECVD (STS 310 at UIC)
    a. Recipe name: SiO2-tst
    b. Rate: 77 nm/min
    c. RF: 20 W, Process Pressure: 650 mTorr, Base Pressure: 4 mTorr, SiH_4/N_2O (600/710 sccm), Temperature: 300° C, Time: 3 min:15 s, Thickness: 250 nm
3. Dehydration bake at 180° C for 2 minutes
4. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
5. Soft bake at 180° C for 15 minutes
        a. Optional gold coating for charging reduction:
            i. Emitech k675X sputter coat 12 nm
6. Raith Exposure of wet etching mask
    a. Write Field: 1000x, 100 μm
    b. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$
7. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
8. Wet etching of SiO_2 using BOE 20:1, etch rate: 75 nm/min
9. Resist strip in 1165 Remover for 4 hours
10. Descum in March RIE O_2 plasma
    a. 12 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 40 W

APPENDIX A (continued)

Layer 5- Gate Processing

1. Acetone, Methanol, IPA cleaning
2. Native oxide removal by BOE 10:1 dip for 15 s followed by DI rinse
3. Immediately load into ALD chamber (Gemstar 8)
    a. Recipe name: Al2O3(20 nm) 175C 166cy
    b. *Load Silicon witness samples for ellipsometry measurements*
4. Spin coat PMGI SF9 at 2000 RPM for 45 seconds
5. Soft bake at 256° C for 15 minutes
6. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
7. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reduction:
        i. Emitech k675X sputter coat 12 nm
8. Raith Exposure of ohmic contacts
    a. Properly adjust dosage for smaller features
    b. Write Field: 1000x, 100 μm
    c. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$

    Optional steps:

    7a. Gold coating removal using Au-etchant 15 seconds

9. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
10. Develop MC 101 for 90 seconds followed by DI rinse 20 seconds, N_2 blow dry
11. Descum in March RIE O_2 plasma
    a. 2 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 20 W
12. E-beam evaporation of Ti/Au (28/250 nm)
13. Lift-off by soaking in 1165 remover overnight

APPENDIX A (continued)

Layer 6- Insulator Etch

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake at 180° C for 2 minutes
3. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
4. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reduction:
        i. Emitech k675X sputter coat 12 nm
5. Raith Exposure of dry-etch mask
    a. Write Field: 1000x, 100 μm
    b. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$
        i. Optional: Gold coating removal using Au-etchant for 15 seconds
6. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
7. Dielectric (Insulator) etch on Oxford PlasmaLab ICP-RIE
    a. Recipe: “AC GaN Ar/Cl2/BCl3 CH1”
    b. Ar/BCl_3 (10/20 sccm), RF: 15 W, ICP: 0 W, Pressure: 15 mTorr
    c. Time: 7 minutes
    d. Etch rate: ~4.1 nm/min
8. Resist strip in 1165 Remover overnight
9. Descum in March RIE O_2 plasma
    a. 12 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 40 W

APPENDIX A (continued)

Layer 7- Contact Pads

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Dehydration bake at 256° C for 2 minutes
3. Spin coat PMGI SF9 at 2000 RPM for 45 seconds
4. Soft bake at 256° C for 15 minutes
5. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
6. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reductions:
        i. Emitech k675X sputter coat 12 nm
7. Raith Exposure of contact pads
    a. Properly adjust dosage for smaller features
    b. Write Field: 1000x, 100 μm
    c. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$

    Optional steps:

    7a. Gold coating removal using Au-etchant 15 seconds
8. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
9. Develop MC 101 for 90 seconds followed by DI rinse 20 seconds, N_2 blow dry
10. Descum in March RIE O_2 plasma
    a. 2 minutes, O_2: 22 sccm, Pressure: 160 mTorr, 20 W
11. Varian E-beam evaporation of Ti/Au (28/250 nm)
12. Lift-off by soaking in 1165 remover overnight

APPENDIX A (continued)

Layer 8- Si_3N_4 Passivation

1. Acetone, Methanol, Isopropanol wafer cleaning
2. Deposition of Si_3N_4 by PECVD (STS 310 at UIC)
    a. Recipe name: Si3N4_rc
    b. Rate: 16.6 nm/min
    c. RF: 20 W, Process Pressure: 650 mTorr, Base Pressure: 4 mTorr, SiH_4/NH_3 (500/70 sccm), Temperature: 300° C, Time: 3 hours, Thickness: 3 μm
3. E-beam evaporation of Chromium (as an etch mask) 200 nm
4. Dehydration bake at 180° C for 2 minutes
5. Spin coat 950 PMMA A4 at 3000 RPM for 30 seconds
6. Soft bake at 180° C for 15 minutes
    a. Optional gold coating for charging reduction:
        i. Emitech k675X sputter coat 12 nm
7. Raith Exposure of dry etching mask
    a. Write Field: 1000x, 100 μm
    b. EHT: 30 kV, Aperture: 30 μm, Base Dosage: 250 $\mu C/cm^2$

    Optional steps:

    7a. Gold coating removal using Au-etchant 15 seconds

8. Develop MIBK:IPA (1:3) 45 seconds followed by IPA rinse 15 seconds, N_2 blow dry
9. Chromium wet etching
10. Si_3N_4 dry-etching using STS 340 RIE
    a. RF Power: 20 W, CF_4: 35 sccm, O_2: 5 sccm Pressure: 75 mTorr
    b. Etch Rate: ≈160 nm/min, Etch time: 19 min 38 seconds
11. Chromium complete removal by wet etching
    a. 11 minutes etch time

APPENDIX B

B.1 Introduction

In this appendix, I describe the various setups of the probe station at the laboratory for measuring 3-terminal transistors and 2-terminal resistors and capacitors. The illustrations here make use of a Keithley 4200 SCS system equipped with remote pulse measure (RPM) units. For low-voltage measurements (< 200 V), you may use the SMA connector probe holders. For high-voltage operation, it is required to use High-voltage coax cables attached to the appropriate probe holders. A Keithley 2290-5 power supply is used here to source voltages up to 2000 V.

B.2 Probe station setup for high voltage measurements

This setup requires Keithley 4200 SCS, 2290-5 Power supply, 2290-PM-200 protection module, a triax 'T' splitter, (4) triax black cables, (3) high voltage probes with the high voltage coax cables attached and a high-voltage chuck (namely Signatone's PowerPro package). The 4200 and 2290-5 must be interlocked with the dark box to enable high-voltage operation. Maximum allowed voltage here is 2000 V (rating of the probes and chuck) although the 2290-5 can go up to 5 kV, it is not recommended. Refer to Appendix D.4 for the c-based code to use this system.

APPENDIX B (continued)

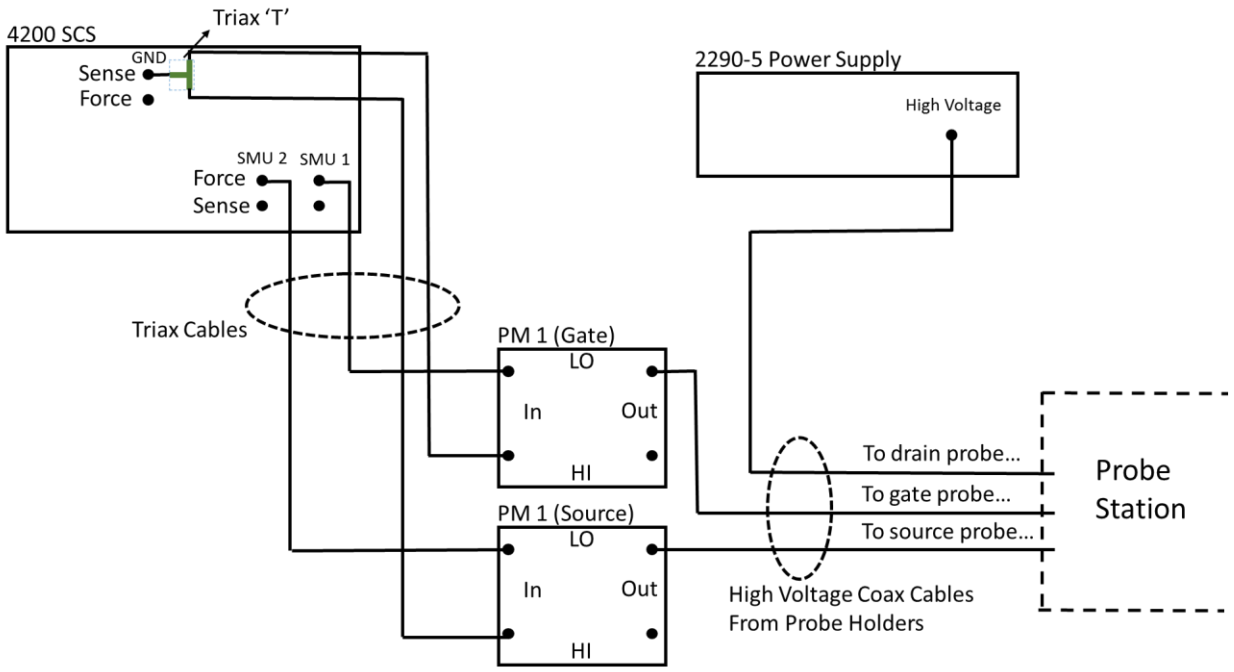

Figure 53 Instrument setup for 3-terminal high-voltage breakdown FET measurements.

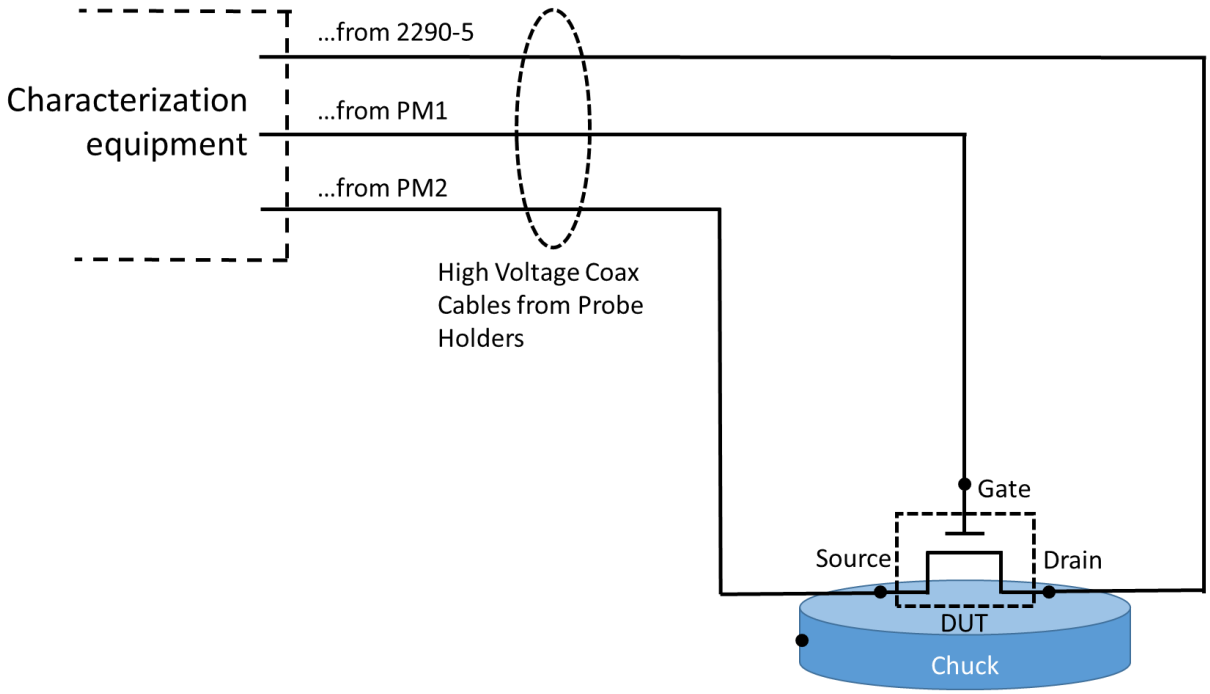

Figure 54 Probe station setup for 3-terminal high-voltage breakdown FET measurements.

APPENDIX B (continued)

B.3 Probe station setup for DC I-V measurements

This setup requires Keithley 4200 SCS, (4) triax black cables running from the 4200 to RPMs, (2) triax black cables running from the 4200 GND to the source, (4) blue 50 Ω triax cables running from the RPMs to the probe holders, (3) triax ‘T’s, (3) triax-coax-SMA converters and (3) low-voltage SMA probe holders.

APPENDIX B (continued)

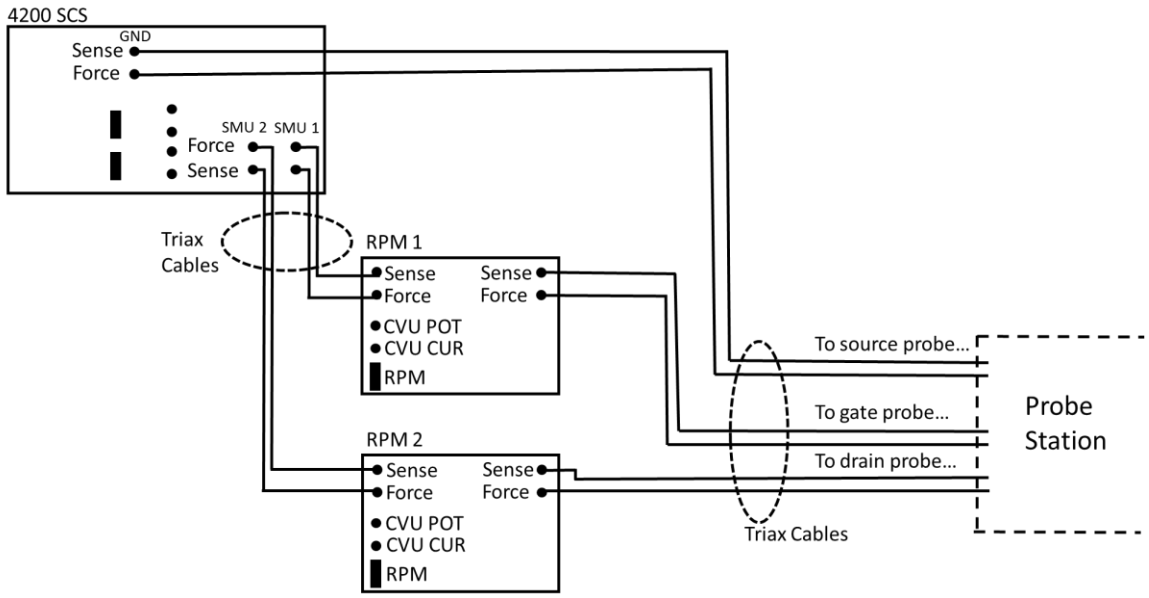

Figure 55 Instrument setup for 3-terminal FET measurements.

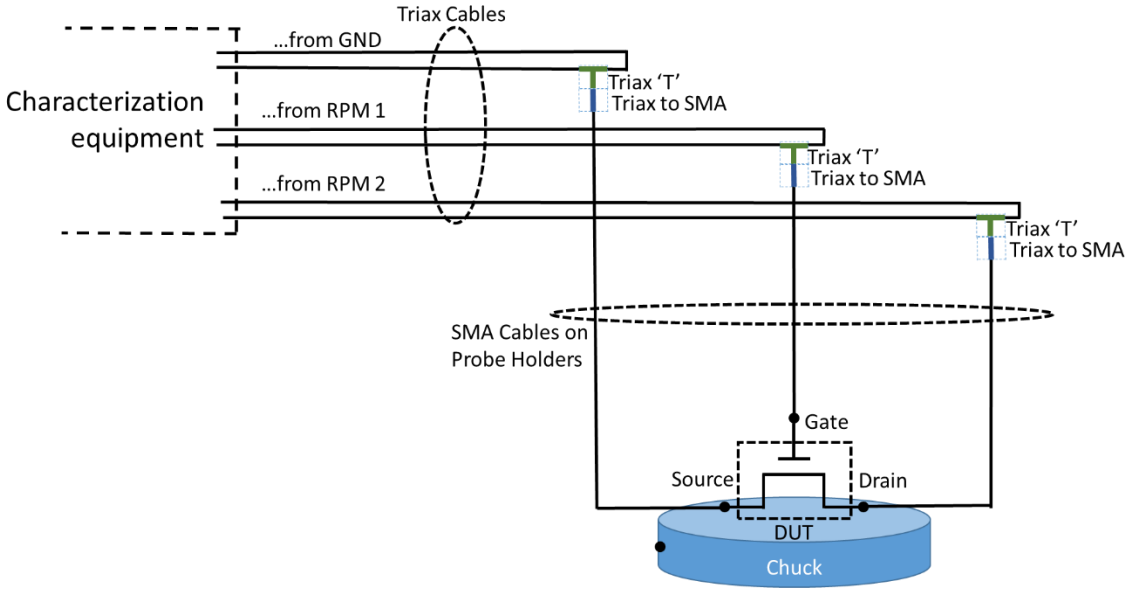

Figure 56 Probe station setup for 3-terminal FET measurements.

APPENDIX B (continued)

B.4 Probe Station Setup for C-V measurements

This setup requires Keithley 4200 SCS, (4) triax black cables running from the 4200 to RPMs, (4) blue 50 Ω triax cables running from the RPMs to the probe holders, (2) triax 'T's, (2) triax-coax-SMA converters and (3) low-voltage SMA probe holders. You may use this configuration for both lateral and vertical devices. In the case of vertical device, where you use the chuck as a contact to the semiconductor, you must drive the chuck with the signal. In other words, the chuck would be your 'gate' electrode and the electrode patterned on your sample is grounded.

APPENDIX B (continued)

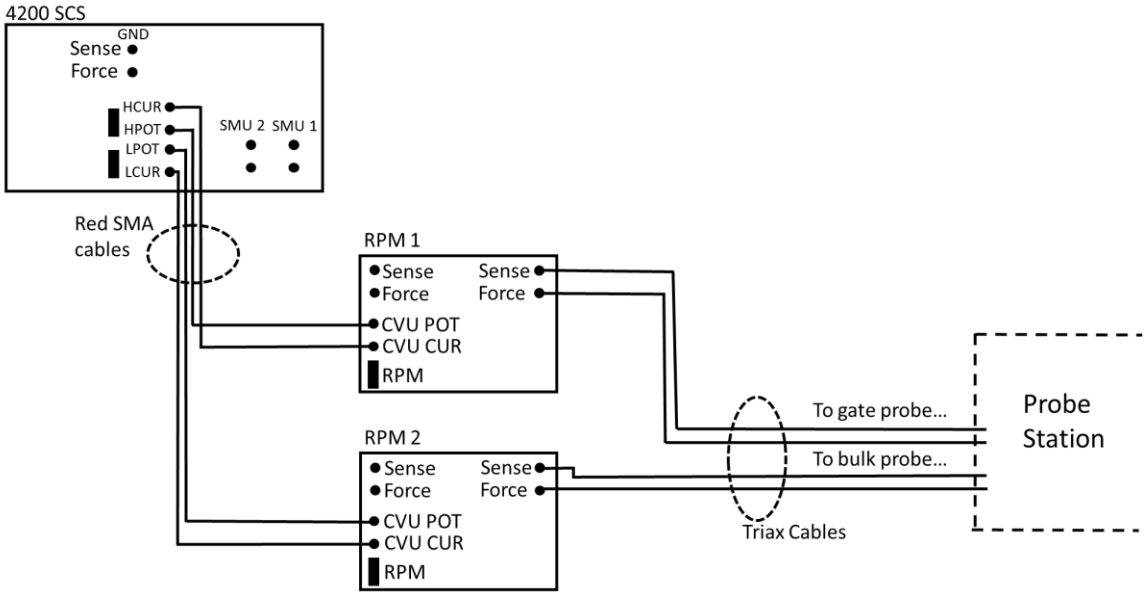

Figure 57 Instrument setup for capacitance-voltage measurements.

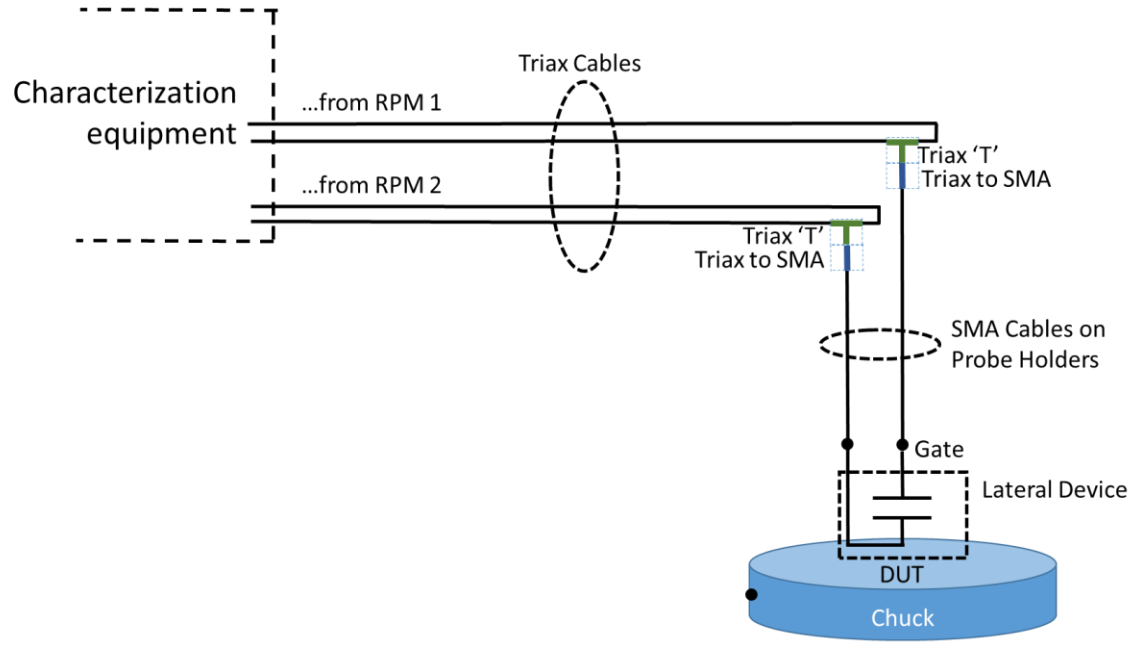

Figure 58 Probe station setup for lateral capacitors measurement.

APPENDIX B (continued)

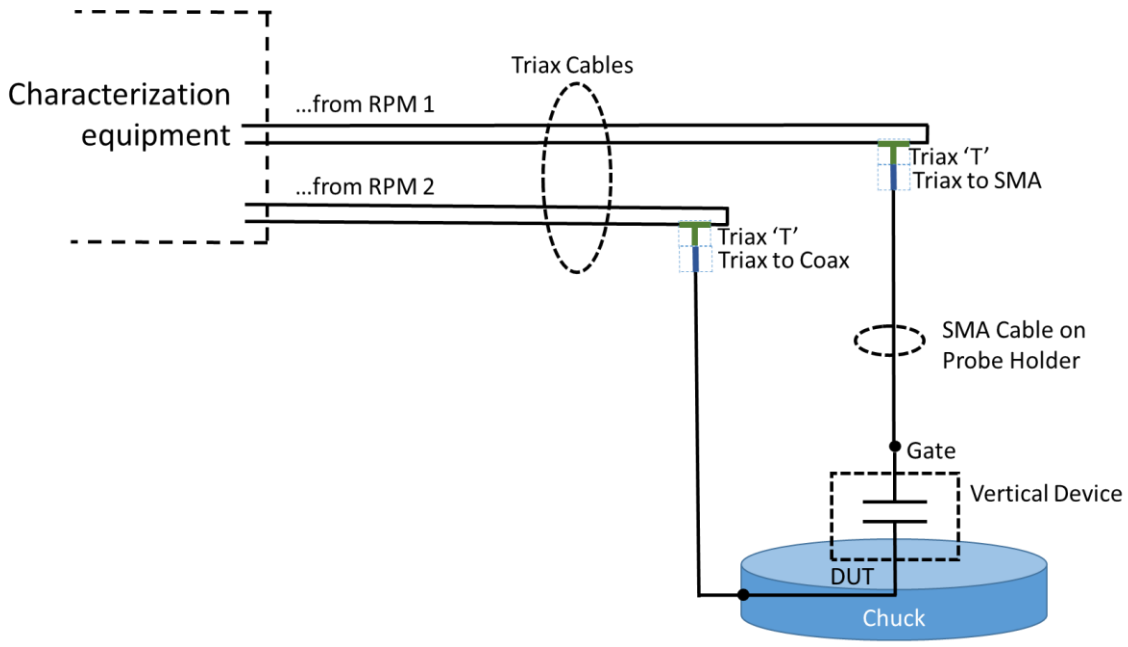

Figure 59 Probe station setup for vertical capacitors measurement.

APPENDIX B (continued)

B.5 Probe station setup for pulsed I-V measurements

This setup requires Keithley 4200 SCS, (2) high-quality HDMI cables running from the 4200 to RPMs, (4) blue 50 Ω triax cables running from the RPMs to the gate and drain probe holders, (2) triax ‘T’s, (2) triax-coax-SMA converters, (3) low-voltage SMA probe holders and (1) CAP-29 BNC Shorting plug which shorts the signal and shield lines on the source connector. It is important to connect the shields of the cables together as close as possible to the DUT.

APPENDIX B (continued)

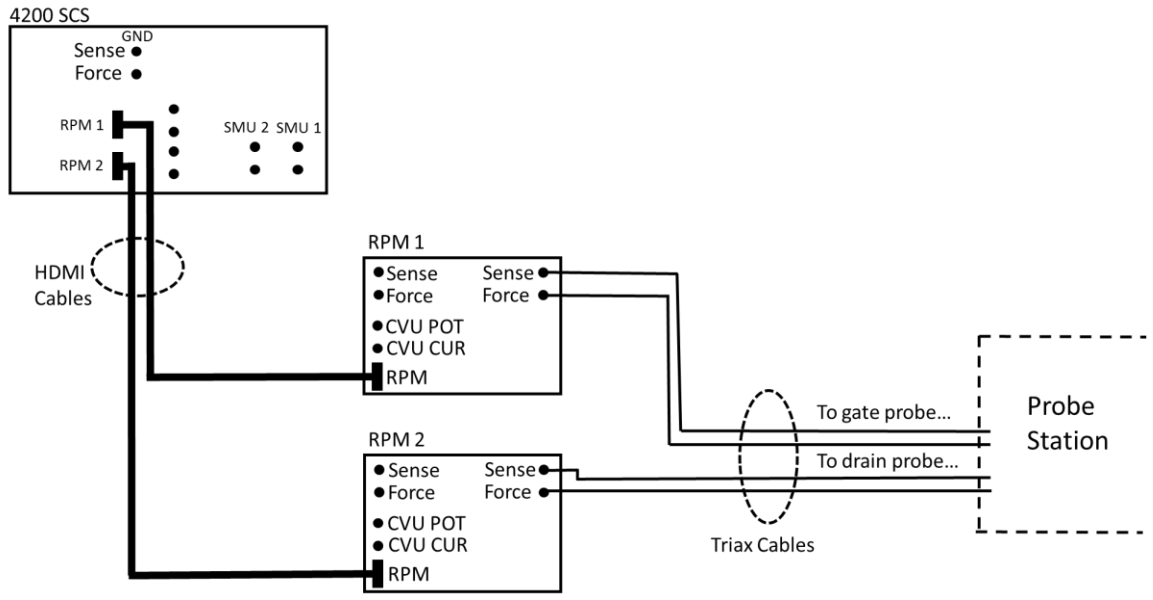

Figure 60 Instrument setup for pulsed I-V measurements.

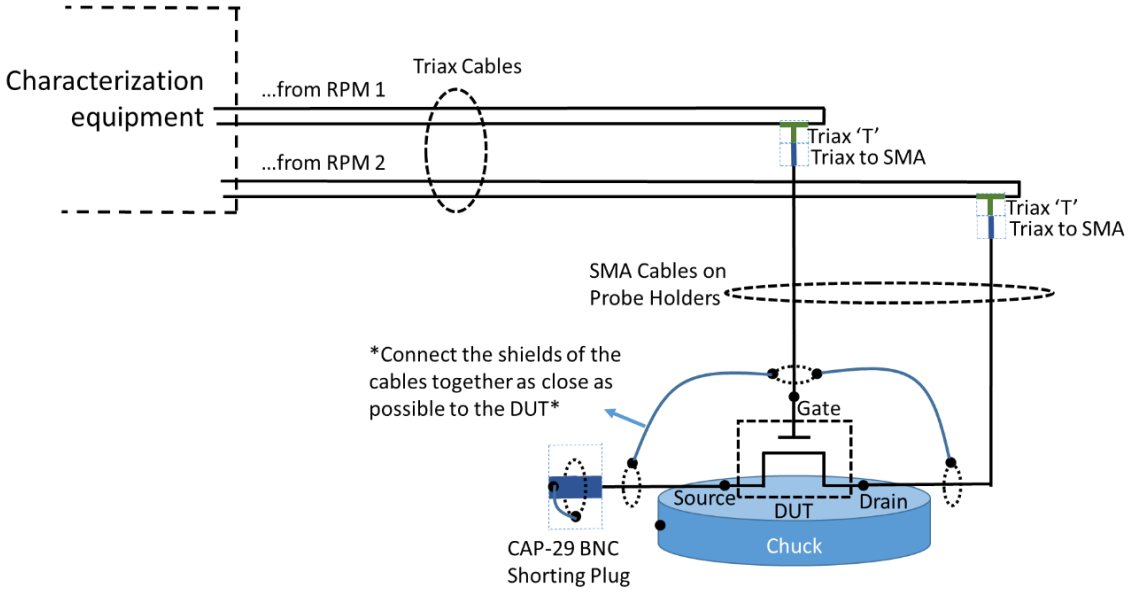

Figure 61 Probe station setup for pulsed I-V measurements.

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Type of Use	Thesis/Dissertation
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Format	Print and electronic
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Will you be translating?	No
Title of your thesis / dissertation	Design and Optimization of GaN-based Power Semiconductor Transistors
Expected completion date	Mar 2017
Estimated size (number of pages)	200
Requestor Location	Albert Colon 1105 N Kostner Ave Unit 1 CHICAGO, IL 60651 United States Attn: Albert Colon
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Will you be translating?	No
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APPENDIX D

D.1 Introduction

This appendix contains some extraneous information. I first describe the procedure to measure interface trap densities in an GaN MISH structure in Appendix D.2. Appendix D.3 contains the MATLAB code used to calculate what is needed in Appendix D.2. Appendix D.4 contains the C-based code used to measure 3-terminal off-state breakdown voltage of a transistor, written with the help of Nathaniel Nicandro.

D.2 Conductance Method Procedure to Extract Interface Trap Density

1. Measure conductance (G) of the MOS capacitor in the dark.
2. Sweep the voltage from about -2V beyond pinch off voltage to about 0V with small intervals such as 0.2V
3. Vary the frequency from 1kHz to 10MHz with many data points in between (1, 2, 4, 6, 8 kHz; 10, 20, 40, 60, 80 kHz; 100, 200, 400, 600, 800 kHz; 1, 2, 4, 6, 8, 10 MHz)
    a. Measure in the following temperatures: 25°, 100°, 200°, and 300° C
4. Calculate G_p from the measured conductance/capacitance using the model shown in Figure 62.

APPENDIX D (continued)

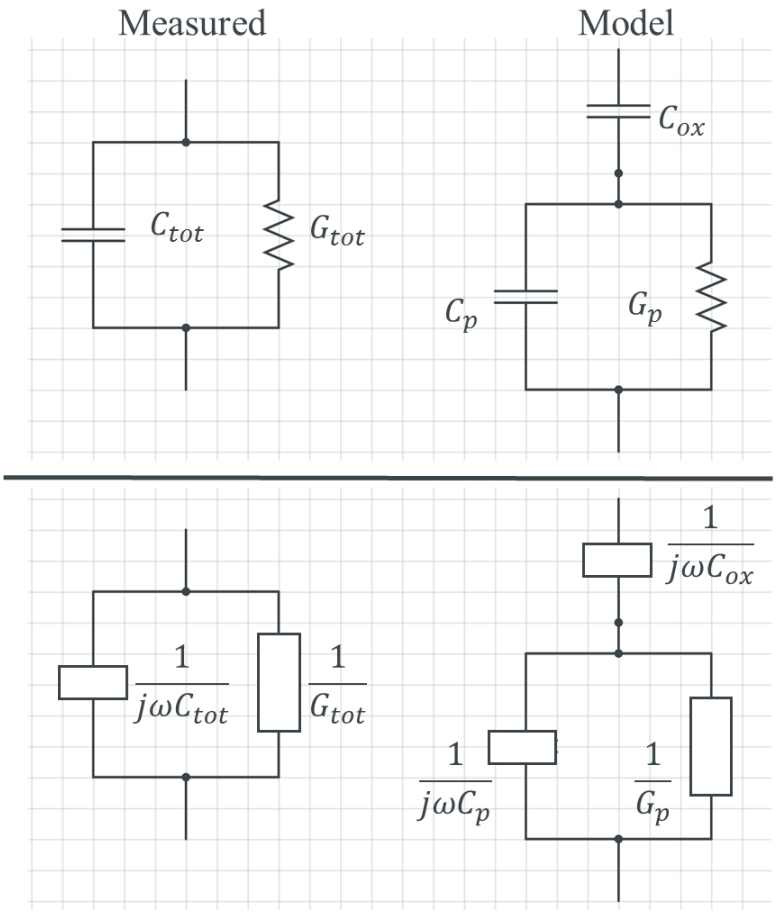

Figure 62 Conductance method model for trap density extraction.

$$Z_{measured} = \frac{1}{\frac{1}{j\omega C_{tot}}^{-1} + \frac{1}{G_{tot}}^{-1}} = \frac{1}{j\omega C_{tot} + G_{tot}}$$

$$\frac{1}{j\omega C_{tot} + G_{tot}} = Z_{measured} = Z_{model} = \frac{1}{j\omega C_{ox}} + \frac{1}{j\omega C_p + G_p}$$

$$\frac{1}{j\omega C_{tot} + G_{tot}} - \frac{1}{j\omega C_{ox}} = \frac{1}{j\omega C_p + G_p}$$

$$(G_p + j\omega C_p)^{-1} = (G_{tot} + j\omega C_{tot})^{-1} - j\omega C_{ox}{}^{-1}$$

APPENDIX D (continued)

5. Once this data is collected, divide the conductance by the area of the capacitor and the radial frequency, ω, to obtain $\frac{G_p}{\omega}$ [F/cm^2].
6. Plot $\frac{G_p}{\omega}$ as a function of ω.
7. Compare the several plots at different gate voltages and choose the plots containing a peak for the fitting.
8. Fit the above functions to the following equation to extract D_t and τ: $\frac{G_p}{\omega} = \frac{qD_t}{2\omega\tau}\ln[1 + (\omega\tau)^2]$ [69, 70]

   where: q is the elementary charge, 1.6*10^{-19} [C], D_t is the trap density [cm^{-2}eV^{-1}], and τ is the trap time constant [s]
9. Once D_t and τ are extracted for each selected gate voltage (step 4, 5), use the trap time constant to calculate the energy for the corresponding trap density using the following equation:

   $E_T = kTln(\sigma N_C v_t \tau)$ [70]

   where: k is Boltzmann's constant, 8.62*10^{-5}[eV/K], T is the temperature measurements were performed [300K], σ is the trap cross section assumed as 3.4*10^{-15}[cm^2] [70], N_c is the density of states in the conduction band assumed to be 2.2*10^{18}[cm^{-3}] [70], V_{th} is the average thermal velocity of the carriers, 2.6*10^7[cm/s] [70]
10. Plot D_t as a function of τ.

APPENDIX D (continued)

D.3 MATLAB code for extracting conductance from MISH capacitor

```
% Albert Colon
% Updated July 2016
% This program calculates Gp/w curves from measured overall (or total) capacitance in
% parallel with conductance of a MOS capacitor.  Important parameters that must
% be entered is insulator thickness, dielectric constant of the insulator,
%
% Conduction method calculations
% All calculations are for radius-sized capacitor
% units: cm, F, eV, K, Hz, 1/s, C

clc; clear;
format longEng
radius= 0.0050;       % radius of capacitor in (50um medium sized) [cm]
a=pi*radius^2;       % area of 'radius'-sized capacitor [cm^2]
t_Device1= 0;    % Device1 thickness [cm]
k_Device1= 0;          % dielectric constants of each material

e0=8.854E-14;        % permittivity of vacuum [F/cm]
kB=8.617E-5;         % boltzmann's constant[eV/K]
f=1E3.*[10 20 40 60 80 100 200 400 600 800 1000 2000 4000 6000 8000 10000]; % [Hz]
w=2*pi*f;   % [rad/s]
q=1.602E-19;        % charge of an electron
cox_Device1=k_Device1*e0*a/t_Device1;        % calculation of oxide capacitace =
epsilon*k*Area/thickness

%%%%%%%%%% MEASURED DATA INITIALIZATION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%             Columns are sorted by frequency.. 10k, 20k, 40k, etc...
%%%             Whereas rows are sorted by gate voltage
%%%             *****Device1*********  Vg goes from -8 to 0 V in + 0.2V increments..
%%%             Temperature
%%%             ranges are: 25, 100, 200, and 300 degrees Celsius
firstgtot_Device1_25=[];
firstctot_Device1_25=[];

%
%%
%%%%
%%%%%%%%
%%%%%%%%%%%%%%%%
%%%%%%%%%%%%% 100 degrees Celsius measurements
%%%%%%%%%%%%%%%%%%%%
```

APPENDIX D (continued)

```
firstgtot_Device1_100= [];
firstctot_Device1_100= [];

%
%%
%%%%
%%%%%%%%
%%%%%%%%%%%%%%%%
%%%%%%%%%%%%% 200 degrees Celsius measurements
%%%%%%%%%%%%%%%%%%%%
firstgtot_Device1_200= [];
firstctot_Device1_200= [];

%
%%
%%%%
%%%%%%%%
%%%%%%%%%%%%%%%%  Device1_300
%%%%%%%%%%%%% 300 degrees Celsius measurements
%%%%%%%%%%%%%%%%%%%%
firstgtot_Device1_300= [];
firstctot_Device1_300= [];

% begin calculations for each insulator
% trying to get Gp+i*w*Cp=[ (Gtot + i*w*Ctot)^-1 - (i*w*Cox)^-1 ]^-1
% row,column, where row is # of points measured...
% and column is # of frequency sweeps performed
firstgp_Device1_25=zeros(size(firstgtot_Device1_25,1),size(firstgtot_Device1_25,2));      %
initialize the Gp+i*w*Cp=yp(admittance)
firstgp_Device1_100=firstgp_Device1_25;
firstgp_Device1_200=firstgp_Device1_25;
firstgp_Device1_300=firstgp_Device1_25;



row=1;
column=1;
% trying to get Gp+i*w*Cp=[ (Gtot + i*w*Ctot)^-1 - (i*w*Cox)^-1 ]^-1
while (column<=length(w))
   row=1;
   while (row<=41)
      % Device1  "_Device1_"

firstgp_Device1_25(row,column)=(w(column)*firstgtot_Device1_25(row,column)*cox_Device1
```

APPENDIX D (continued)

```
^2)/(firstgtot_Device1_25(row,column)^2+w(column)^2*(cox_Device1-
firstctot_Device1_25(row,column))^2);

firstgp_Device1_100(row,column)=(w(column)*firstgtot_Device1_100(row,column)*cox_Devic
e1^2)/(firstgtot_Device1_100(row,column)^2+w(column)^2*(cox_Device1-
firstctot_Device1_100(row,column))^2);

firstgp_Device1_200(row,column)=(w(column)*firstgtot_Device1_200(row,column)*cox_Devic
e1^2)/(firstgtot_Device1_200(row,column)^2+w(column)^2*(cox_Device1-
firstctot_Device1_200(row,column))^2);

firstgp_Device1_300(row,column)=(w(column)*firstgtot_Device1_300(row,column)*cox_Devic
e1^2)/(firstgtot_Device1_300(row,column)^2+w(column)^2*(cox_Device1-
firstctot_Device1_300(row,column))^2);


      row=row+1;
   end
   column=column+1;
end

%%%%% Divide by the area to get mS/cm^2 units

%% Device1
firstgp_Device1_25=firstgp_Device1_25./a;
firstgp_Device1_100=firstgp_Device1_100./a;
firstgp_Device1_200=firstgp_Device1_200./a;
firstgp_Device1_300=firstgp_Device1_300./a;

%%%% Taking the transpose
%%% First set of devices
firstgp_Device1_25=transpose(firstgp_Device1_25);        % lets take the transpose to sort
columns by gate voltage instead of frequency
firstgp_Device1_100=transpose(firstgp_Device1_100);
firstgp_Device1_200=transpose(firstgp_Device1_200);
firstgp_Device1_300=transpose(firstgp_Device1_300);

%% Plot to figure out which parts matter in the conductance figures
% you must manually verify which peaks appear within the range of the measurement
frequencies
figure(1)
semilogx(w(1:16), firstgp_Device1_25(1:16,8:13))
%%% Write Data in excel file
```

APPENDIX D (continued)

```
xlswrite('Device1_Gp',firstgp_Device1_25(1:length(f), 1:length(w)),'1_Device1_25')  %%
DONE!!
xlswrite('Device1_Gp',firstgp_Device1_100(1:length(f), 1:length(w)),'1_Device1_100')
xlswrite('Device1_Gp',firstgp_Device1_200(1:length(f), 1:length(w)),'1_Device1_200')
xlswrite('Device1_Gp',firstgp_Device1_300(1:length(f), 1:length(w)),'1_Device1_300')


%%% Write Data in excel file
xlswrite('Device1_Gp',firstgp_Device1_25(1:length(f), 1:length(w)),'1_Device1_25')  %%
DONE!!
xlswrite('Device1_Gp',firstgp_Device1_100(1:length(f), 1:length(w)),'1_Device1_100')
xlswrite('Device1_Gp',firstgp_Device1_200(1:length(f), 1:length(w)),'1_Device1_200')
xlswrite('Device1_Gp',firstgp_Device1_300(1:length(f), 1:length(w)),'1_Device1_300')

%csvwrite('radial_frequency.csv', transpose(w))
```

APPENDIX D (continued)

D.4 C-based Code to Measure 3-Terminal Off-State Breakdown Voltage

```
/* USRLIB MODULE INFORMATION

        MODULE NAME: HV_Sweep_ver01_05
        MODULE RETURN TYPE: double
        NUMBER OF PARMS: 19
        ARGUMENTS:
                InstIdStr,      char *, Input,  "GPI1",         ,
                VdMin,          double,Input,   0,      ,
                VdMax,          double,Input,   100,    0,      2000
                VdStepSize,     double,Input,   10,     ,
                IdMeas,         D_ARRAY_T,      Output,         ,       ,
                IdMeasSize,     int,    Input,  1000,   ,
                GateSMU,        char *, Input,  "SMU1",         ,
                SourceSMU,      char *, Input,  "SMU2",         ,
                VgApply,        double,Input,   -8,     ,
                IgMeas,         D_ARRAY_T,      Output,         ,       ,
                IgMeasSize,     int,    Input,  1000,   ,
                VsApply,        double,Input,   0,      ,
                IsMeas,         D_ARRAY_T,      Output,         ,       ,
                IsMeasSize,     int,    Input,  1000,   ,
                VdForce,        D_ARRAY_T,      Output,         ,       ,
                VdForceSize,    int,    Input,  1000,   ,
                DelayTime,      int,    Input,  100,    1,      10000
                VdMeas,         D_ARRAY_T,      Output,         ,       ,
                VdMeasSize,     int,    Input,  1000,   ,
        INCLUDES:
#include "keithley.h"
#include "ulib_internal.h"
#include "math.h"
#pragma warning( disable: 4996 )
        END USRLIB MODULE INFORMATION
*/
/* USRLIB MODULE HELP DESCRIPTION
MODULE: HV_Sweep
================

DESCRIPTION:
============
The HV Breakdown testing uses a Keithley 2290-5 (5kV supply) to sweep drain voltage while biasing
gate and measuring both source and gate currents.
```

APPENDIX D (continued)

```
INPUTS:
=======
InstIdStr       (char *) The CMTR instrument ID. This can be
                CMTR1 through CMTR4, depending on your
                system's configuration.

IntegrationTime  (int)  The integration time to use. Valid values
                are: 0 (SHORT), 1 (MEDIUM), and 2 (LONG).

nPLC            (double) number of Power Line Cycles for integration
                        time.Valid input 0.01 to 10.0

RETURN VALUES:
==============
0          OK.

-10000     (INVAL_INST_ID) The specified instrument does
           not exist.

-10030     (HP4284_NOT_IN_KCON) No HP4284 LCR is defined in your
           system's configuration.

-10031     (HP4284_MEAS_ERROR) A measurement error occurred.

-10090     (GPIB_ERROR_OCCURRED) A GPIB communications error occurred.

-10091     (GPIB_TIMEOUT) A timeout occurred during communications.

-10102     (ERROR_PARSING) There was an error parsing the
           4284's response.
           END USRLIB MODULE HELP DESCRIPTION */
/* USRLIB MODULE PARAMETER LIST */
#include "keithley.h"
#include "ulib_internal.h"
#include "math.h"
#pragma warning( disable: 4996 )

double HV_Sweep_ver01_05( char *InstIdStr, double VdMin, double VdMax, double
VdStepSize, double *IdMeas, int IdMeasSize, char *GateSMU, char *SourceSMU, double
VgApply, double *IgMeas, int IgMeasSize, double VsApply, double *IsMeas, int IsMeasSize,
double *VdForce, int VdForceSize, int DelayTime, double *VdMeas, int VdMeasSize )
{
/* USRLIB MODULE CODE */
```

APPENDIX D (continued)

```
char   GPIBAddressStr[8];                    // Instrument Address
int    GPIBAddress=-1;                      // Instrument Address
int    InstrumentIDHi=1;                    // KI Instrument Hi term
int    InstrumentIDLo=2;                    // KI Instrument Lo term
int    fcnstat = 0;                        // Function Return Status
int    rcv_size;                           // Actual # chars read from inst.
int    max_size=99;                         // Max # of characters to read
int    x;
int    gSMU;                               // Gate SMU
int    sSMU;                               // Source SMU
char   tempstr[6];
char   RawReading[99];
char   RawReading_two[99];
char   CommandString[80];                   // Command to the instrument
char   InstrumentType[80]="KI2290";
double  temp1 = 0.0;
double  temp2 = 0.0;


// Get the 2290 ID from KCON
getinstid(InstIdStr, &InstrumentIDHi);          // First the hi term...
strncpy(tempstr, InstIdStr, 5);                 // ...then the lo.
strcat(tempstr, "L");
getinstid(tempstr, &InstrumentIDLo);

if ((InstrumentIDLo < 0) || (InstrumentIDHi < 0))
       return( INVAL_INST_ID );                 // No such Instrument

// Get the GPIB Address from KCON
getinstattr(InstrumentIDHi, "GPIBADDR", GPIBAddressStr);
GPIBAddress = atoi( GPIBAddressStr );

// Now that we have the GPIB address, let's setup the instrument
// Reset the meter to clear any errors
sprintf(CommandString, "*RST\n");
fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
if (fcnstat > 0) return(-1);
devint();    // device initialize

// Get instrument IDs from SMUs
getinstid(GateSMU, &gSMU);
getinstid(SourceSMU, &sSMU);

sprintf(CommandString, "TCLR\n"); // Clearns any voltage or current trips
```

APPENDIX D (continued)

```
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   if (fcnstat > 0) return(-2);

   sprintf(CommandString, "*CLS\n");
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   if (fcnstat > 0) return(-2);

   sprintf(CommandString, "*RCL 0\n");
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   if (fcnstat > 0) return(-3);

         // Set filter for High current (5.25mA) and low voltage (3kV) to minimize
         // output ripple
   sprintf(CommandString, "FILT 1\n");
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   if (fcnstat > 0) return(-3);

   delay(500);

   limiti(gSMU, 1E-4);  // Set current limit of gate SMU to 100uA
   limiti(sSMU, 1E-2);  // Set current limit of source SMU to 10mA which is much higher than the
2290 can go
   // Bias the gate and source
   forcev(gSMU, VgApply);  // apply gate and source voltage through settings in KITE
   forcev(sSMU, VsApply);

   setmode(gSMU, KI_INTGPLC, 2);  // Set integration mode for SMU1 for higher time...trying
to avoid E+22 spikes
   setmode(sSMU, KI_INTGPLC, 2);

   // initialize the output arrays
   for (x = 0; x < 1000; x++){
      IgMeas[x] = DBL_NAN;   // stands for 'DouBLe Not A Number'
      IsMeas[x] = DBL_NAN;
      IdMeas[x] = DBL_NAN;
      VdForce[x] = DBL_NAN;
   }

   sprintf(CommandString, "HVON\n");  // Initialize High Voltage switch on 2290-5
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   if (fcnstat > 0) return(-4);
   delay(2000);
```

APPENDIX D (continued)

```
   sprintf(CommandString, "VLIM %d\n", 2000);        // Set Drain Voltage Limit, IMPORTANT:
POWER PRO PACKAGE RATED AT 2000V MAX!
   fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
   delay(2000);


   for (x=0; x<(VdMax-VdMin)/VdStepSize; x++)  // x increments from Vdmin to Vdmax to set
voltage on drain
   {
      int Vd = (int)(x*VdStepSize + VdMin);  // calcluate drain voltage bias

      sprintf(CommandString, "VSET %d\n", Vd);  // Send voltage set command to 2290-5
      fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
      delay(DelayTime);  // delay to stabilize output

      // Read current through 2290-5
      sprintf(CommandString, "IOUT?\n", x);  // Read current on drain side through the 2290-5
      fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
      delay(1);
      kibrcv(GPIBAddress, -1, 0x0A, GPIBTIMO, max_size, &rcv_size, RawReading);  // Receive
raw reading value
      RawReading[rcv_size] = 0;
      if (sscanf(RawReading, "%lf", &temp1) != 1)
      {
        // Error parsing the reading
        return(ERROR_PARSING);
      }
      delay(DelayTime);    // some delay time to stabilize the outputs(set through KITE)
      IdMeas[x] = temp1;    // save drain current value from 2290-5

      //Read voltage through 2290-5
      sprintf(CommandString, "VOUT?\n", x);  // Read voltage on drain side through the 2290-5
      fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);
      delay(1);
      kibrcv(GPIBAddress, -1, 0x0A, GPIBTIMO, max_size, &rcv_size, RawReading_two);   //
Receive raw reading value
      RawReading_two[rcv_size] = 0;
      if (sscanf(RawReading_two, "%lf", &temp2) != 1)
      {
        // Error parsing the reading
        return(ERROR_PARSING);
      }
      delay(DelayTime);
      VdMeas[x] = temp2;  // save drain voltage value
```

APPENDIX D (continued)

```
        delay(DelayTime);
        intgi(gSMU, &IgMeas[x]);    // measure gate current through 4200 SMU
        delay(DelayTime);
        intgi(sSMU, &IsMeas[x]);    // measure drain current through 4200 SMU

        VdForce[x] = Vd;        // Save the drain voltage

        PostDataDouble("IgMeas", IgMeas[x]);   // save the measured gate current in the array
        PostDataDouble("IsMeas", IsMeas[x]);   // save the measured source current in the array
        PostDataDouble("IdMeas", IdMeas[x]);    // PostDataDouble is to update the graph with values
        PostDataDouble("VdForce", VdForce[x]);
        PostDataDouble("VdMeas", VdMeas[x]);
        }


    sprintf(CommandString, "HVOF\n");  // turn off high voltage
    fcnstat = kibsnd(GPIBAddress, -1, GPIBTIMO, strlen(CommandString), CommandString);  // send the command to 2290
    if (fcnstat > 0) return(GPIB_ERROR_OCCURED);  // report error if command was not sent

    return(OK);  // return ok if code acted properly
    execut();  // Clear all instruments and reset to default states
/* USRLIB MODULE END  */
}                   /* End HV_Sweep_ver01_05.c */
```

VITA

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EDUCATION

Ph.D. Electrical and Computer Engineering, University of Illinois at Chicago, 2017.

B.S. Electrical and Computer Engineering, University of Illinois at Chicago, 2012.

WORK EXPERIENCE

Graduate Research Assistant, Nanotechnology Core Facility, Jan 2014-May 2017

Teaching Assistant, University of Illinois at Chicago, Jan 2013-May 2015

Internship, Alcatel-Lucent, Jun 2012-Aug 2012

Tutor, UIC College of Engineering, Jan 2010-Jun 2011

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PUBLICATIONS

Colon, A., Stan, L., Divan, R. and Shi, J., Incorporation of Al or Hf in atomic layer deposition TiO2 for ternary dielectric gate insulation of InAlN/GaN and AlGaN/GaN metal-insulator-semiconductor-heterojunction structure, J. Vac. Sci. Technol. A, 35: 01B132, 2017.

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