Universal High-Frequency-Link Inverter for Renewable/Alternative Energy

BY

SIAMAK MEHRNAMI
B.S., University of Tabriz, 2006
M.S., University of Tehran, 2009

THESIS

Submitted as partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Chicago, 2015

Chicago, Illinois

Defense Committee:

Sudip K. Mazumder, Chair and Advisor
Derong liu
Sabri Cetinkunt, Mechanical & Industrial Engineering
Tomy Sebastian, Halla Mechatronics
Byeong Mun Song, Argonne National Laboratory

This Dissertation is dedicated to my mother (Negar) who has always bestowed me with love, support and passion to work hard, and my father (Samad) who showed me the way in life, and my grandmother (Aziz) who raised me and my uncle (Iraj), who help me to make right decisions during my academic life. I would also like to appreciate my M.Sc. advisor (Dr. S. Farhangi) whose impact on my life has been invaluable and my memories of him will be everlasting.

ACKNOWLEDGMENTS

First and foremost, my special thanks go to my PhD advisor Prof. Sudip K. Mazumder. I also acknowledge the support and assistance of my Committee Members. Professor Mazumder has been helping me and supporting my Dissertation work since 2011. Without his guidance, this Dissertation work would not be accomplished. I would also like to thank my lab mates specially Hossein Riaz Montazer, Alireza Tajfar and Alireza Mojab for their help and guidance during the course of my Dissertation work.

SM

TABLE OF CONTENTS

LIST OF FIGURES

FIGURE PAGE

LIST OF FIGURES (continued)

FIGURE PAGE

LIST OF FIGURES (continued)

FIGURE PAGE

LIST OF FIGURES (continued)

FIGURE PAGE

LIST OF ABBREVIATIONS

CMS	Continuous Modulation Scheme
DMCI	Differential-Mode Ćuk Inverter
DMS	Discontinuous Modulation Scheme
DTCI	Differential-mode Three-phase Ćuk Inverter
HC	Harmonic Compensator
HFL	High-Frequency Link
PEI	Power Electronic Interface
PR	Proportional Resonant
SLB	Static Linearization Block
THD	Total Harmonic Distortion

SUMMARY

This Dissertation introduces new modulation schemes for single-phase differential-mode Ćuk inverter (DMCI) and differential-mode three-phase Ćuk inverter (DTCI) to improve inverter efficiency by reducing its circulating power.

The DMCI is a single-stage inverter with low device count. It offers advantages over other topologies because of compactness, higher power density, and reduced cost. It is a promising topology configuration for renewable-/alternative-energy applications encompassing both isolated and non-isolated configurations. The continuous modulation scheme (CMS), which was introduced originally for DMCI, activates all of the modules of the DMCI. The new discontinuous modulation scheme (DMS) deactivates one module in each half line-cycle leading to discontinuous operation of the inverter modules. Chapter 2 outlines the DMS and a mechanism to realize it. The experimental open-loop and closed-loop results of the DMCI using CMS and DMS are provided along with comparisons of their performances. It is shown that, the DMS reduces the circulating power and mitigates the losses of the DMCI, the voltage ratings of the devices of the DMCI are also reduced with the DMS. In contrast, the CMS-based DMCI exhibits wider linearity in its normalized dc-voltage gain and yields reduced harmonic distortion of the output voltage. For DMS, to achieve comparable linearity in normalized dc-voltage gain and distortion, harmonic compensation under closed-loop control is a pathway that has been demonstrated.

The DTCI is introduced in Chapter 3. The DTCI has some advantage over other differential-mode and three-phase topologies, including fewer switches, bidirectional power flow capability, and galvanic isolation. It is a promising configuration for renewable-/alternative-energy applications with isolated as well as non-isolated structures.

The CMS, which was introduced originally for DTCI, activates all of the three modules of the DTCI. This modulation scheme increases the circulating power in modules and hence increases the inverter power loss. Chapter 3 introduces DMS for DTCI. DMS deactivates one module at a time resulting in a discontinuous operation of DTCI modules. It also outlines DMS and its implementation with a proper control mechanism. The proposed implementation of the DMS is straight forward. The experimental open-loop and closed-loop results of the DTCI using CMS and DMS are provided along with comparisons of their performances. It is shown that, the DMS reduces the circulating power and hence mitigates the losses.

The voltage ratings of the DTCI devices also are reduced with the DMS for the same reason. DTCI exhibits a nonlinear voltage-gain with both CMS- and DMS-based modulations. It has been demonstrated that by feed-forwarding the input voltage and incorporating a static linearization method, the harmonic distortion of the DTCI output is considerably reduced.

Chapter 1

INTRODUCTION

A. Background

Increasing cost of the energy and the environmental impact of the fossil fuels encourage the use of renewable energy [1]. The global consumption of electrical energy is increasing steadily in an ever-growing economy due to industrialization leading to a pressing need for an increase in the power generation capacity. Renewable energy sources offer the promise of clean, abundant energy gathered from resources such as sun, wind, earth, hydro power, geothermal, bio-fuels [2], [3]. Renewable energy technologies show promising benefits compared to those of the conventional energy sources [4]. Most of these systems are modular and have the flexibility for growth in energy consumption [2]. They are usually located close to consumer and they don't need long distance transmission line. The interface between a renewable energy source and consumer which is utility grid or a stand-alone load are power electronic interface (PEIs) such as dc/ac converters (or inverters) [5]. The major obstacles for expansion of renewable energies are their commercial cost and reliability. The PEI is an inseparable part of renewable energy industry and has a significant role in both cost and reliability of the whole system. Such interfaces control power to the load as well as optimize source (e.g. photovoltaic source) energy utilization. Also, considering the efficiency of the inverter as a critical parameter, the inverters show a key role in amount of the harvested and delivered power from the renewable energy sources to the application loads or the power grid. The inverter is also a considerable part of overall system cost [6]–[8]. All the above factors affect the overall cost energy generation from renewable energy sources. The inverter has a major effect on the reliability of the system as well. Experience with existing renewable energy sources indicate that inverters are often responsible for bottleneck system failures [9]. Along with advances in renewable/alternative energy sources, research in power electronics to achieve cheaper, efficient and reliable PEI is essential for development and expansion of cleaner energy sources in USA and globally.

B. Power electronics interface (PEI)

The reliability, power density, cost, and efficiency are important for PEI designer and manufacturers for the renewable/alternative energy industry. Reliability can be enhanced by increasing the modularity of the PEI, reducing

the stresses in the components, reduced system complexity and by increasing the efficiency. Power density can be increased by decreasing the size of inductors, capacitors, and transformers by increasing the system frequency. It can be further increased by integrating the magnetics. Efficiency of the system is enhanced by reducing the conduction and switching losses of the system while the cost of the system is reduced by using fewer and cheaper components and by implementing modularity. So topology and operating frequency are the important factors, which essentially affect all of the above-mentioned parameters. This increases the scope of the PEI to be modified to suit the application. Few advantages of modularity are as follows: a) ease of system configuration and flexibility; (e.g. if the application requirements are three-phase, additional modules can be incorporated in the system to cater the needs of the consumer); and b) reduction in engineering and manufacturing cost and time. The frequency of the PEI also plays a major role to attain higher power density. Typically, the higher the switching frequency of a PEI, the smaller and lighter the magnetics and the capacitors embedded in the PEI. Further, the dynamic characteristics of the PEI improve with increasing switching frequency and so does the control-loop response and disturbance rejection capability.

C. Configurations of PEI

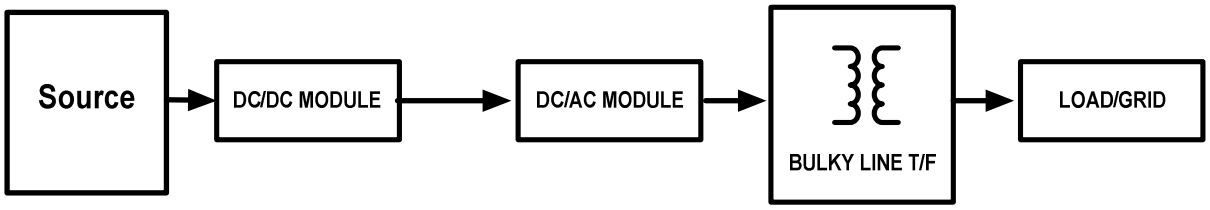
Depending on the application need, PEI can be isolated or non-isolated. Isolation may be required due to safety or technical needs. For instance in a PV application, a non-isolated PEI causes leakage currents due to the presence of parasitic capacitances in distributed PV modules. With regard to interconnection, this is an important issue since it leads to safety, reliability, protective coordination, electromagnetic compatibility, and PV module lifetime issues [10]. Transformer-less (i.e., non-isolated) inverters show some advantages such as high efficiency and simple schematic [11], [12]. However, majority of these topologies are not able to provide isolation for PEI. Besides, ground current and noise issues make these topologies less attractive for distributed generation (DG). Finally, transformer-less inverter cannot adapt the voltage level of the energy source and the load. Therefore, they may not be suitable for energy sources with low output voltage such as photovoltaic and full-cell sources.

Galvanic isolation is normally implemented by a transformer. Line-frequency (LF) transformers are conventionally employed to provide galvanic isolation and voltage scalabilities for PEIs [13]–[15]. But, such low-frequency transformers are bulky and heavy. This also leads to an increase in the cost of manufacturing and maintenance of the LF transformers. Therefore, the LF transformers are the main obstacle to towards realizing PEIs and/or PEI-based systems with high power densities.

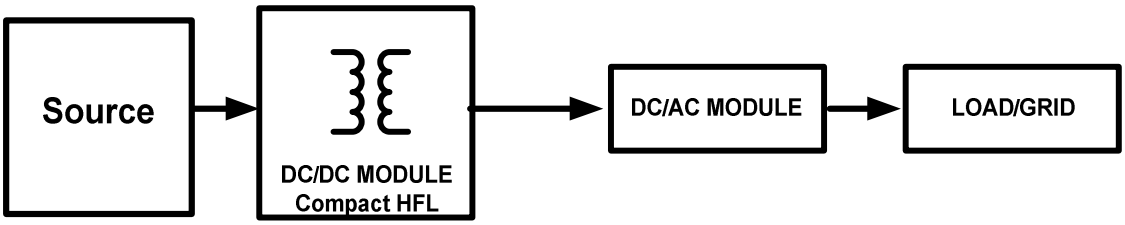
Advancements in power semiconductors devices and high-frequency magnetic cores [16], has enabled the usage of high-frequency (HF) transformers instead of the traditional LF transformers. Consequently, the power densities of the high-frequency-link (HFL) inverters [17] have increased multifold. Thus, HFL inverters provide the required galvanic isolation and voltage scalability while yielding reduced footprint. However, HFL inverters usually require more conversion stage (and hence more switches) than the conventional inverters, which results in higher switching losses. As such, the losses of the HFL inverters need to be decreased to increase the overall efficiency of the PEIs.

The isolated PEIs are implemented in multiple different ways as illustrated in Fig. 1. The architecture in Fig. 1(a) represents a conventional approach that requires bulky, expensive, and high-footprint LF transformer. The architectures shown in Fig. 1(b) and Fig. 1(c) incorporate the galvanic isolation using a HF transformer in the dc/dc or dc/ac stage. This yields high power density but increase the number of power stages. As such, for low power applications the single-stage architecture shown in Fig. 1(d) is a viable candidate. The direct power conversion (DPC) in this architecture also precludes the need for an intermediate dc-link capacitor.

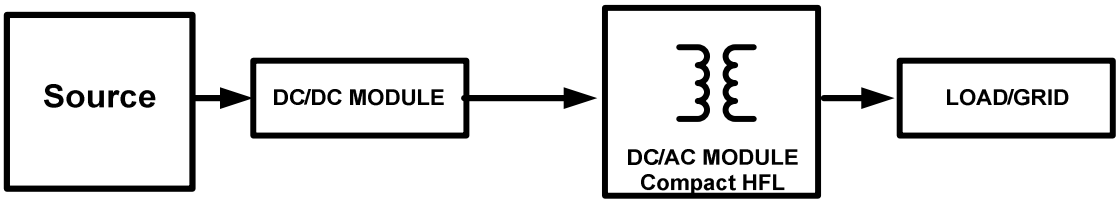
Most configurations have a dc/dc power-conversion stage followed by a dc/ac power-conversion stage. The basic functions of the dc/dc converter are boosting and regulating the low output from the renewable energy source. Some basic criteria for choosing a dc/dc converter for a renewable energy source input are as follows: a) large step-up ratio, b) low input current ripple, and c) galvanic isolation between the source and the load. The dc/dc converters are either voltage-fed or current fed and can be either a half-bridge or a full-bridge topology. Half-bridge topologies are used for low- and medium-power applications while full-bridge topologies are typically used for higher-power applications. The voltage-fed converters require a high winding ratio between primary and secondary sides of the HF transformer since boosting action in voltage-fed converters is only performed by the transformer.



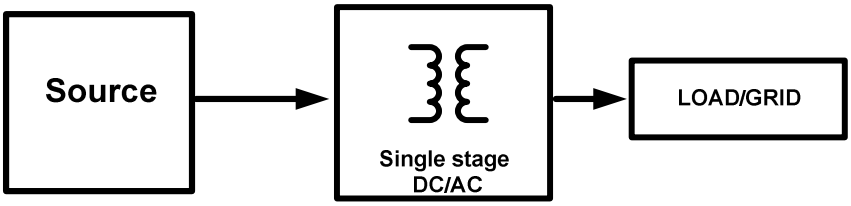
(a)



(b)



(c)



(d)

Fig. 1. Possible configurations for PEI topologies.

1. Single-stage single-phase topologies

A single-stage inverter is an inverter that performs the power conversion from dc to ac- both stepping up the low dc voltage and modulating the sinusoidal load current and voltage, in a single stage. Many single-stage inverters, both isolated and non-isolated inverters have been proposed in the literature.

One of the single-stage topologies proposed earlier was the differential-boost topology [18]. This topology achieves dc-ac conversion by connecting the inputs of two identical dc-dc boost converters in parallel with a dc source and the load is connected across the outputs of the two dc-dc converters. As opposed to the conventional buck voltage-source inverters (VSIs), this topology can generate an output voltage higher than the input voltage. Fig. 2 shows the single-stage differential boost topology. The major advantages of this topology are the reduced number of switches and a simple topology. The disadvantages of the differential boost topology are : a) the topology is non-

isolated; b) the switches are operated at a low switching frequency; c) the size of the magnetics are large leading to a larger footprint for a non-isolated topology; d) there is amount of circulating power in circuit.

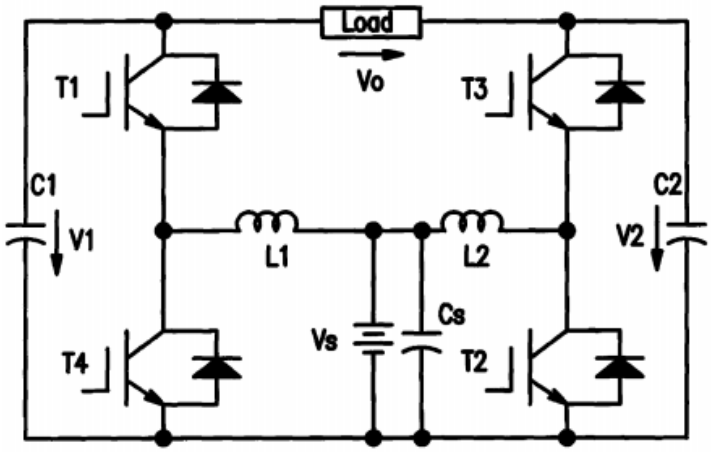


Fig. 2. Topology of a differential-mode boost inverter [18].

A differential buck-boost inverter, proposed in [19] is shown in Fig. 4. This operates similar to the differential boost inverter shown in Fig. 3. This inverter can produce an output voltage either higher or lower than the input dc voltage.

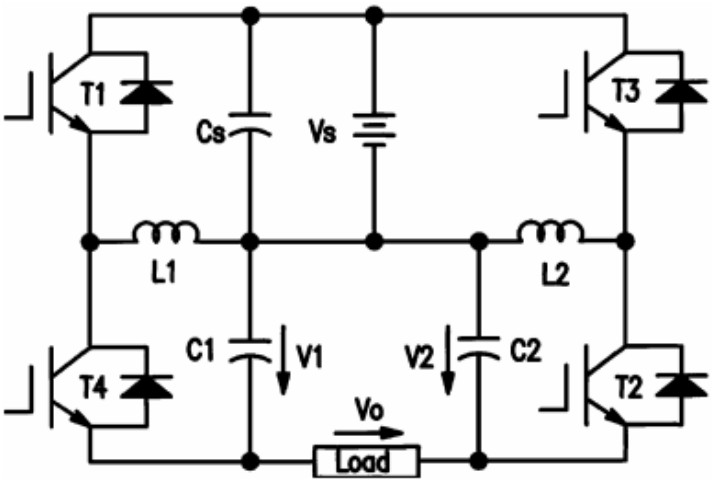


Fig. 3. Topology of a differential-mode buck-boost inverter [19].

Another single-stage buck–boost inverter topology, described in [20], is shown in Fig. 4. This topology overcomes the disadvantage of low input voltage range of the buck-boost topology proposed in [19]. But, this inverter requires a split input dc voltage source. Two sets of input voltage sources and buck-boost chopper type

circuits are connected in anti-parallel to the output capacitor, which generates the output topology. Both the chopper circuits are operated at fixed-frequency in discontinuous-conduction mode (DCM). Both the buck-boost topologies do not provide a HF galvanic isolation though they have lower component count. They also operate at a lower switching frequency and incur switching losses.

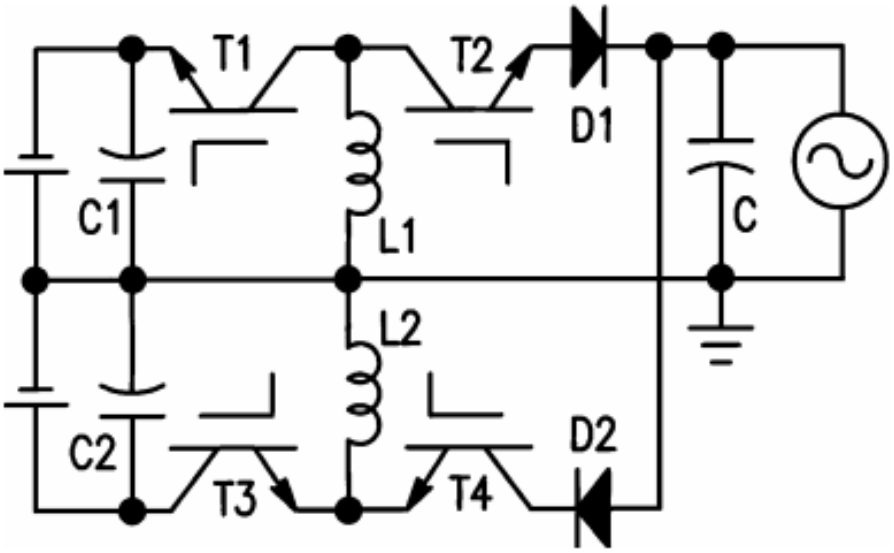


Fig. 4. Topology of a differential buck-boost inverter[20].

Fig. 5 shows the topology of a single-stage flyback inverter. In [21], two bidirectional flyback converters are connected in parallel to the input voltage source and the load is connected across the two converters. The main advantage of this topology over the above-mentioned topologies is the galvanic isolation provided by the HF transformers in both the flyback converters. But the galvanic isolation in this topology has increased foot print. The switches also incur switching losses and hence are limited to low-switching-frequency operation.

Reference [22] introduces a single-stage and single-phase inverter with three controlled devices (with two of them being high-side devices) and three diodes based on a modified flyback topology. It is shown in Fig. 6. This inverter can achieve ripple mitigation. However, the inverter does not have bi-directional power-flow capability.

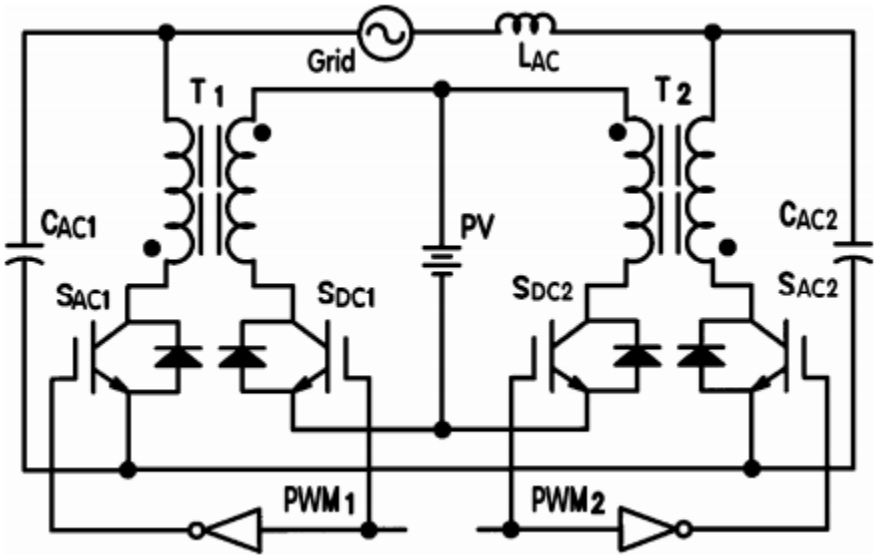


Fig. 5. Topology of a single-stage flyback inverter [21].

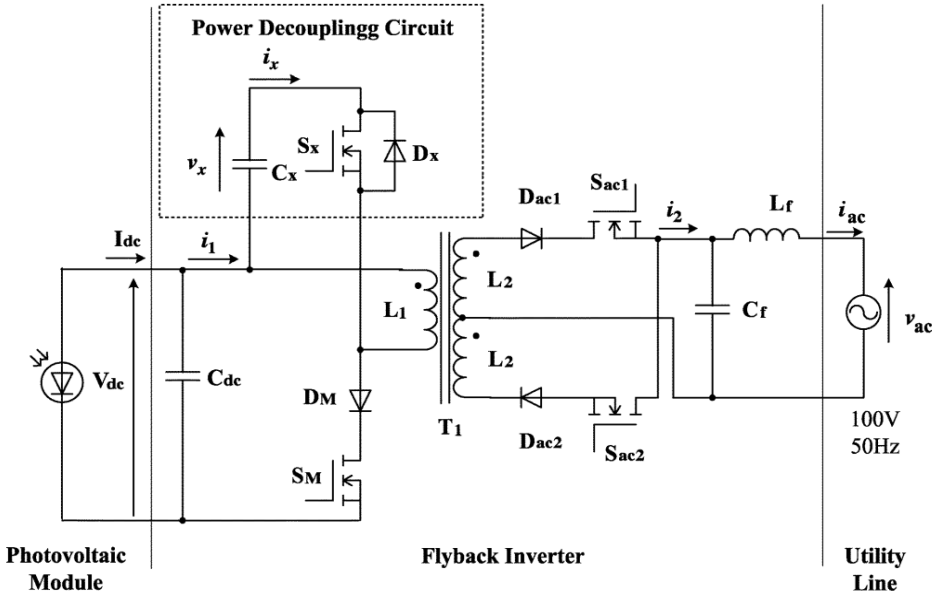


Fig. 6. Topology of modified single-stage flyback inverter [22].

Fig. 7 represents a single-stage full-bridge buck-boost inverter outlined in [23]. This inverter has a full-bridge inverter with a LC resonant tank. The inverter has four main switches (S_1, S_2, S_3 and S_4), two diodes (D_1 and D_2), two resonant inductors (L_1 and L_2), one resonant capacitor (C), one filter inductor (L) and capacitor. The positive half-cycle at the output is generated with the switches S_1, S_3 and diode D_2 and the negative half-cycle is generated

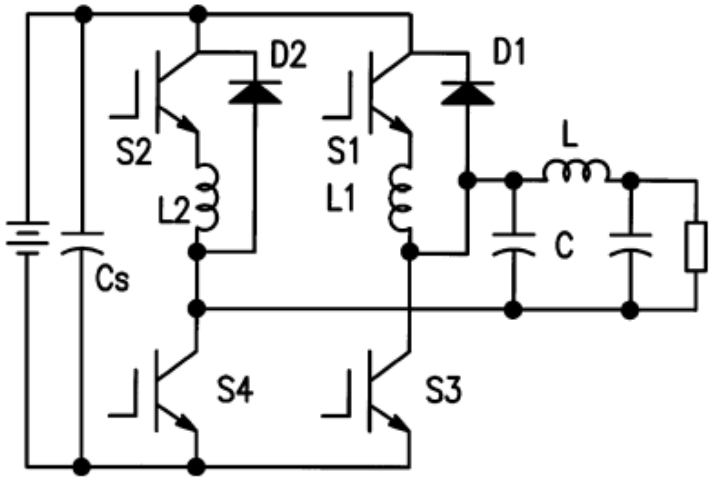


Fig. 7. Topology of a single-stage full-bridge buck-boost inverter [23].

with the remaining three devices. Though the inverter topology has only four power switches and two diodes, only two switches are soft switched. Also, the generated sinusoidal waveform consists of quasi sinusoidal pulse robes. This topology also does not isolate the source and the load or grid.

A single-stage buck-boost PWM power inverter proposed in [24] is given in Fig. 8. This inverter topology has two buck-boost choppers forming a four switch bridge and an additional two more power switches for synchronous commutation in each half cycle of the output. The major advantage of this topology is the galvanic isolation provided by the HF transformer. But, this topology is only suitable for low-power applications with a reported maximum power of 140 W.

Fig. 9 shows the topology of a transformer-less voltage boosting inverter proposed in [25]. This topology is a buck-boost derived topology and has six power switches and an energy storage inductor, *L*. This topology was proposed for low power applications. The ac output is synthesized by charging the inductor, L from different directions in each half cycle. This topology is highly compact without any huge magnetics but is only suitable for very low power applications (50 W). The absence of a galvanic isolation and the higher device for count for even low power applications are the major disadvantages of the topology.

The buck-boost derived topologies prevent direct connection between the source and the load, which is a key advantage. However, the main issue with the buck-boost derived topologies is the high peak inductor current stress due to the sudden transfer of energy through the inductors from source to load during each switching cycle. The buck-boost topologies also have lower boost capability when compared to the boost-derived topologies. The

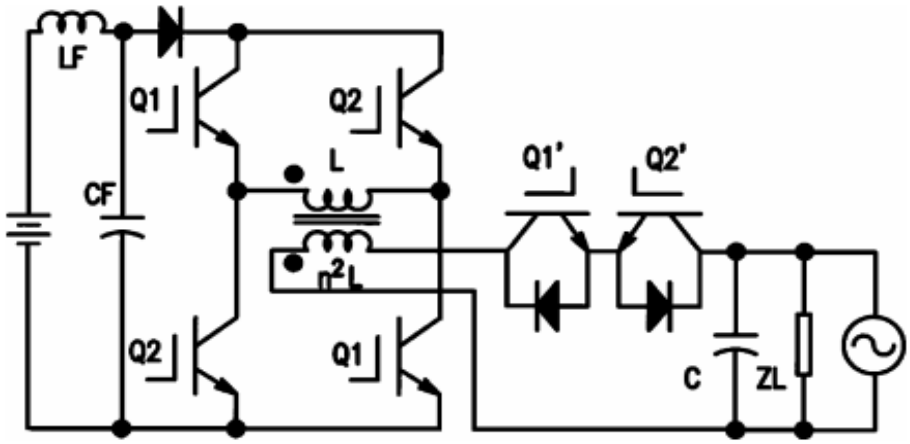


Fig. 8. Topology of single-stage buck-boost PWM power inverter [24].

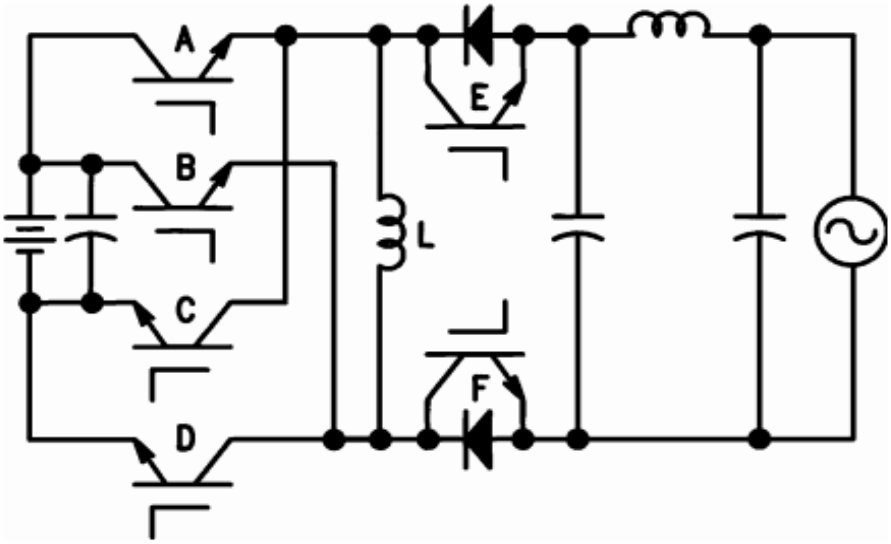


Fig. 9. Topology of a transformerless voltage boosting inverter [25].

differential-mode boost inverter demonstrated in [18] and the inverter proposed in [26] are free from the high inductor current stress but are non-isolated topologies.

Another single-stage converter based on a differential-mode Ćuk topology, is outlined in [27] and illustrated in Fig. 10. This topology achieves direct dc/ac conversion by connecting the load differentially across two bidirectional dc/dc Ćuk converters and modulating them sinusoidally with 180^{o} phase difference. This topology utilizes only four main switches, making the inverter topology simple and yield reduced the cost. The differential-mode Ćuk inverter also has room for magnetics integration, thereby reducing the foot print of the inverter.

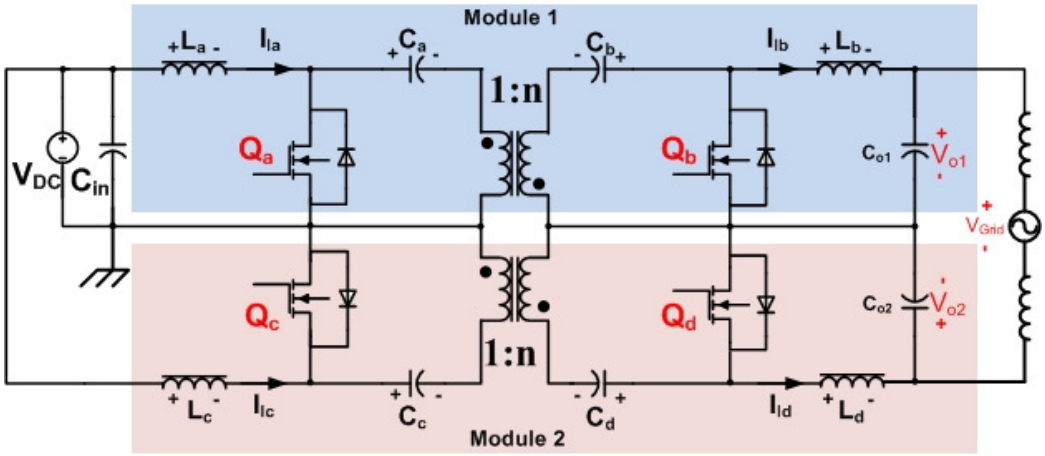


Fig. 10. Topology of a single-stage differential-mode Ćuk inverter [27], [28].

2. Three-phase PEI configurations

Many topologies have been introduced for three-phase inverters in literatures [29], [30]. A typical transformer-less topology has a bridge architecture [31], [32]. This topology can be cascaded with boost converter on the dc side to achieve a peak gain higher than unity [33]. This topology may yield common-mode leakage current for some application [34]. For some other applications, higher peak voltage gains requirement may give rise to the need for a transformer. Given the need for low-cost inverter with galvanic isolation, HFL inverters have emerged as a potential front runner [35]–[40]. The simplest HFL topology often has a multi-stage topological architecture to accommodate the high-frequency transformer. The stages of multi-stage topology may be decoupled by a dc-link capacitor or dc-link inductor [41]. That may add to system cost, reliability, loss, and power density. Slightly modified topologies have been presented [10], [12]. They remove the dc link capacitor/inductor by using special modulation techniques [14]–[16] while they may achieve reduction in switching loss. Overall, for low-power applications the cost-benefit tradeoff of a multi-stage HFL inverter topology requires careful attention. As such, for low-power three-phase HFL inverter applications, there is an enhanced thrust to seek single-stage topological solutions [42]–[45].

Single-stage topologies are categorized, reviewed and compared in [29]. References [46], [47] introduce input-series-output-parallel topologies. Differential-modes single-phase Ćuk inverter is introduced in [48], and its design and modulation are presented by [28], [49]. Reference [46], [50] shows that topological embodiment of the differential inverter with Ćuk converter has some advantages. Reference [51] discusses the general concept of poly-phase differential inverters and introduces the differential-mode three-phase Ćuk inverter (DTCI) topology

originally. The isolated DTCI as shown in Fig. 11. Reference [52] presents the DTCI control and design with continuous modulation scheme (CMS).

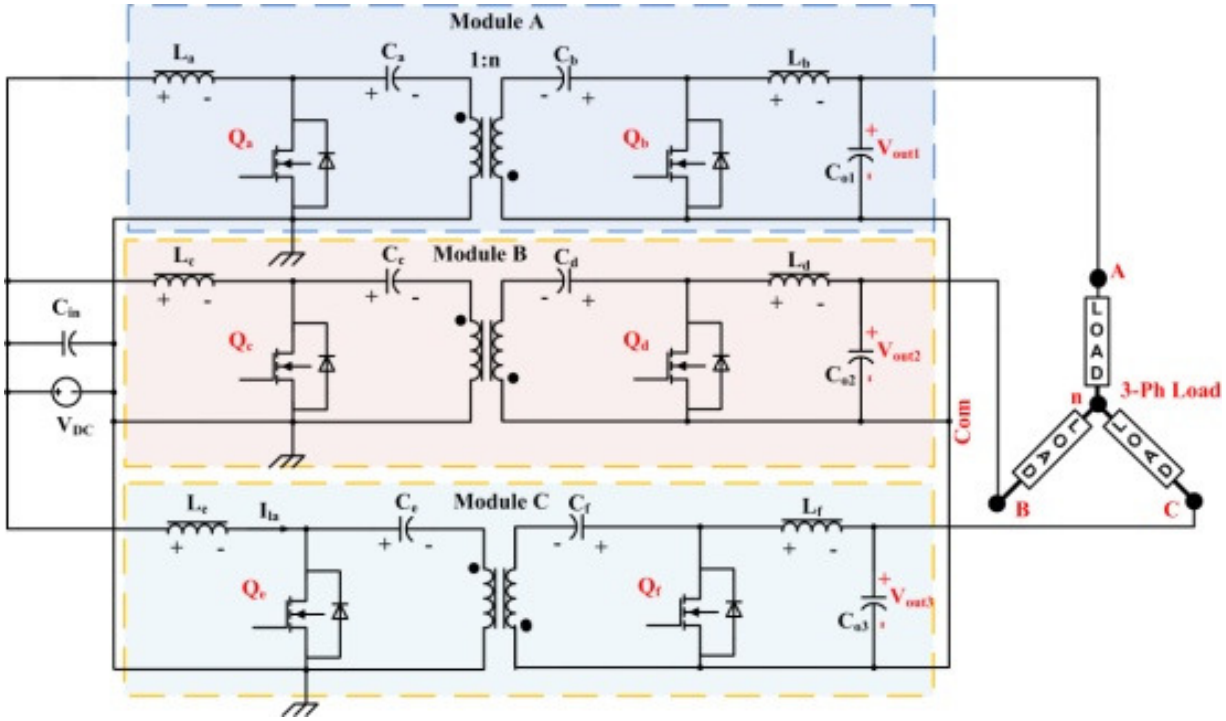


Fig. 11. Illustration of the DTCI topology, which comprises three modules (Module A, Module B and Module C).

D. Motivation and objectives of this doctoral Dissertation

One topological embodiment for the single-stage HFL inverter is the differential-mode Ćuk inverter (DMCI) topology, shown in Fig. 10. The DMCI topology [27], [28] comprises two modules, which are connected in parallel at the dc side and connected in series at the ac side. The DMCI topology is promising one among the different topologies introduced in the Section 1. The DMCI yields several useful features [46] that directly impact the cost, reliability, and power density too. To begin, with the DMCI comprises limited number of switches all of which are low-side driven. Further, the DMCI has the ability to support bi-directional power flow using the same set of switches and a seamless control. Yet another feature of the DMCI is its ability to support voltage step-up and step-down functionalities that also enables the utility of the basic differential-mode topology for even non-isolated applications. An added capability of the DMCI is its ability to support LF ripple current without a large isolation transformer. Due to the presence of the two blocking capacitors on the primary and secondary sides of the transformer, the magnetizing current of the transformer is essentially devoid of any line-frequency current

component. Finally, the possibility of coupled inductors and transformer has been introduced in [48], which enhances the compactness of the inverter and leads to reduced input and output ripples. The modular structure of the each Ćuk converter can be used to extend the application to three-phase or even poly-phase systems, or multilevel inverters. The motivation of this research is to study and explore the possible modulation and controller schemes for single-phase and multi-phase structures of this converter, aiming to reduce the cost, losses and size.

This doctoral dissertation outlines a discontinuous modulation scheme (DMS) for a single-phase DMCI in Chapter 2 and presents an experimental realization of it for a single-phase DMCI. The experimental open-loop and closed-loop results of the DMCI using DMS are compared to those obtained using a conventional modulation scheme referred to as the CMS for various inverter performance and design parameters. It is shown that DMS reduces the circulating power and hence mitigates the inverter losses. The voltage ratings of the DMCI devices also reduce with this scheme. However, the CMS yields more linear behavior and causes reduced distortion. It is demonstrated in Chapter 2 that DMS results in a practically viable inverter; however, proper controller design and nonlinear and harmonic compensation are essential to avoid harmonic distortion of the output waveforms [49] and address nonlinearity in behavioral response [53].

Chapter 3 presents the isolated DTCI as shown in Fig. 11. The isolated DTCI topology comprises three modules, which are connected in parallel at the dc side and connected to common ground at the ac side. Three phase load is connected differentially to the positive terminal of each module. The DTCI yields several useful features [52] that directly impact the cost, reliability, and power density. The DTCI comprises limited number of switches all of which are low-side driven. Further, the inverter has the ability to support bi-directional power flow using the same set of switches and a seamless control. Yet another feature of the inverter is its ability to support voltage step-up and step-down functionalities that also enables the utility of the basic differential-mode topology for even non-isolated applications. An added capability of the HFL Ćuk inverter is its ability to support line-frequency ripple current without a large isolation transformer. Due to the presence of the two blocking capacitors on the primary and secondary sides of the transformer, the magnetizing current of the transformer is essentially devoid of any line-frequency current component. Finally, the possibility of coupled inductors and transformer has been introduced by [54], which enhances the compactness of the inverter and leads to reduced input and output ripples. The DTCI topology originally outlined with a continuous modulation scheme (CMS) [24] in which primary devices have three-phase sinusoidal modulating signals with a dc offset. The secondary side devices are complementary with respective

primary side switch and considering a proper dead time. The dc offset of the output terminal voltages cancel each other because the load is connected differentially across the output-voltage terminals. However, this modulation scheme leads to circulation of power or reactive power flow through modules even with resistive load. This yields higher switching and conduction losses. Further, the dc offset voltage on output terminals of modules increases the peak voltages on the devices [55].

There is hardly any discussion on the need for proper modulation scheme for DTCI in literatures [24], [25]. As such this Doctorate Dissertation outlines a DMS for the DTCI along with a description of the CMS in Chapter 3. Further, the chapter provides analytical insight into the performance comparison of DMS-based and CMS-based DTCI. The nonlinear behavior of DTCI leads to distortion of DTCI output operating with either CMS or DMS. A static linearization method with input voltage feed-forward is proposed to address the problem. It has been shown that by using this method, the total harmonic distortion (THD) is reduced significantly below the acceptable level. Closed loop control system is designed based on proportional resonant (PR) controller [56] and experimentally implemented. Chapter 3 also presents the experimentally obtained results of efficiency, device peak voltages, closed loop transient and THD. The experiments are carried out with proposed structures in the Dissertation for both CMS and DMS. These results verify the analytical/simulation results and show the significant superiority of DMS over CMS. Appendix outlines the design aspects of the experimental DTCI prototype.

Chapter 2

NEW MODULATION SCHEME FOR SINGLE-PHASE DIFFERENTIAL MODE ĆUK INVERTER AND RESULTS

A. DMCI

Common single-phase inverters have two stages: 1) The dc-dc stage, 2) The dc-ac stage. The dc-dc converter usually boosts the input voltage. The second stage is usually an H-bridge inverter [57]. The two stages are connected through a decoupling dc-link. The galvanic isolation can be realized in two ways. One possible architecture is a bulky line-frequency transformer at the ac side and the other approach is the use of dc-dc converter with high-frequency transformer isolation.

The alternative topologies has been proposed [18]- [27], which can do the voltage step up and inversion within one stage. The details of these alternative topologies have been shown in previous chapter. A class of single-stage topologies developed by parallel-series connection of two dc-dc converters [46], which also known as differential inverters. The differential-mode inverters are modular and can be extended for three phase inverters as well [58]. The boosting function can be realized either by step-up transformer [59] or boosting capability of the converter. Among various dc-converters for differential mode configuration, the Ĉuk converter is advantageous [47] because it fulfills the following conditions:

1) Low number of switches, which leads to smaller size and robustness [60].

2) All switches are low side driven and it makes the design and the fabrication simpler and reduces the cost.

3) Bi-directional power flow capability simply achieved by using switch at both sides of the converter.

4) Buck-boost ability of the converter, so it can be used in transformer-less configuration.

5) The converter can be easily extended to have high frequency transformer with interstice rejection of line frequency components of the magnetizing current.

6) The possibility of coupled inductors and transformer which has been introduced in [48], [54], reduces the size further and gives less ripple on input and output, which means less EMI.

The differential-mode Ĉuk topology [48], [54] is single-stage inverter and composed of two modules. Each module is a single Ĉuk converter, which can be configured in both isolated and non-isolated structures. The two

modules are connected in parallel at the dc side and they are in series at the ac side as shown in with grid connection.

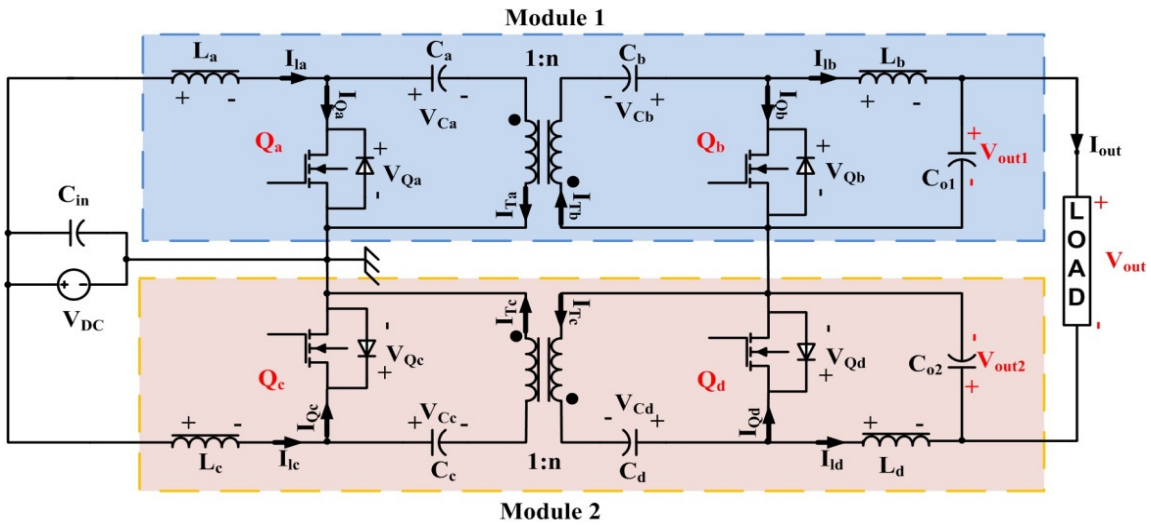


Fig. 12 DMCI connected to the grid.

The original DMCI topology [54] outlined switching of the inverter using a continuous modulation scheme (CMS), in which diagonal devices switch simultaneously and continuously. Reference [54] has mentioned that the structure could be used as switched mode power supply (SMPS), but it did not discuss anything about its modulation and control. The linearity between duty cycle and output voltage is essential for the power amplifiers, which are used in analog circuit design. The power loss is more important for SMPS rather than class B signal amplifier. This Scheme is proposed for a C-class switching power amplifier. In CMS, one module pulls the power while the other one pushes it. This leads to enhanced circulation of power yielding higher switching and conduction losses. Thus, it does not suit the SMPS application. Further, the continuous modulation of all of the switches implies that a control system for this inverter sees an eight-order dynamics under all operating conditions which has adverse implications of control complexity and bandwidth. References [46], [47] mention the discontinuous operation of the modules depending on voltage polarity, but they do not present anything about control or modulation scheme and its realization. Reference [60] introduces similar topology, which includes two additional switches. It demonstrates the standalone operation with one module at a time modulation and sliding mode control. Further, either of these two papers does not provide any insight into the performance comparison between DMS and CMS operation of the DMCI.

This chapter of dissertation outlines a discontinuous modulation scheme (DMS) for the DMCI along with a description of the CMS. It builds on the abridged work outlined in [49], [53] by the author. A detailed analysis on the performance of the DMCI operating with DMS as well as CMS is provided in the Section C based on theoretical and experimental results. The results indicate the positive impact of DMS on the DMCI with regard to efficiency and reduction in device breakdown voltage rating and the need for nonlinear closed-loop compensation in DMS to achieve satisfactory harmonic distortion and linearity in voltage gain.

B. Modulation of the DMCI

1. Continuous modulation scheme (CMS)

The output voltage (V_{out}) of the inverter is the differential of the output voltages (V_{out1} and V_{out2}) of the two dc-dc converter modules. This results in the following normalized dc-voltage gain relationship:

$$\frac{V_{out}}{n\times V_{DC}} = \frac{V_{out1}}{n\times V_{DC}} - \frac{V_{out2}}{n\times V_{DC}} = \left(\frac{D_1}{1-D_1} - \frac{D_2}{1-D_2}\right). \quad (1)$$

In (1), V_{DC} is the dc input voltage and n is turns ratio of the transformers. The duty ratios (D_1 and D_2) of Modules 1 and 2 (operating using CMS) are related by $D_1 = 1 - D_2$, so the normalized dc-voltage gain (g) in terms of D_1 is described by the following:

$$g = \frac{V_{out}}{n\times V_{DC}} = \left(\frac{2D_1-1}{D_1(1-D_1)}\right). \quad (2)$$

As will be demonstrated later, depending on n, CMS-based DMCI exhibits relatively linear normalized dc-voltage gain over a finite range of duty cycle.

For CMS, the diagonal switches (i.e., $Q_a(Q_b)$ and $Q_d(Q_c)$) of the two modules are fed with the same gating signals while the two switches ($Q_a(Q_b)$ and $Q_c(Q_d)$) in each of the modules are fed with complementary gating signals. Because the inverter operates in a differential mode, the inductor currents flow from one Ćuk module to the

other. There are 4 modes in all. Modes 1 and 2 are for the positive half of the line cycle while Modes 3 and 4 are for the negative half of the line cycle. Fig. 13 illustrates the four modes of the inverter using CMS.

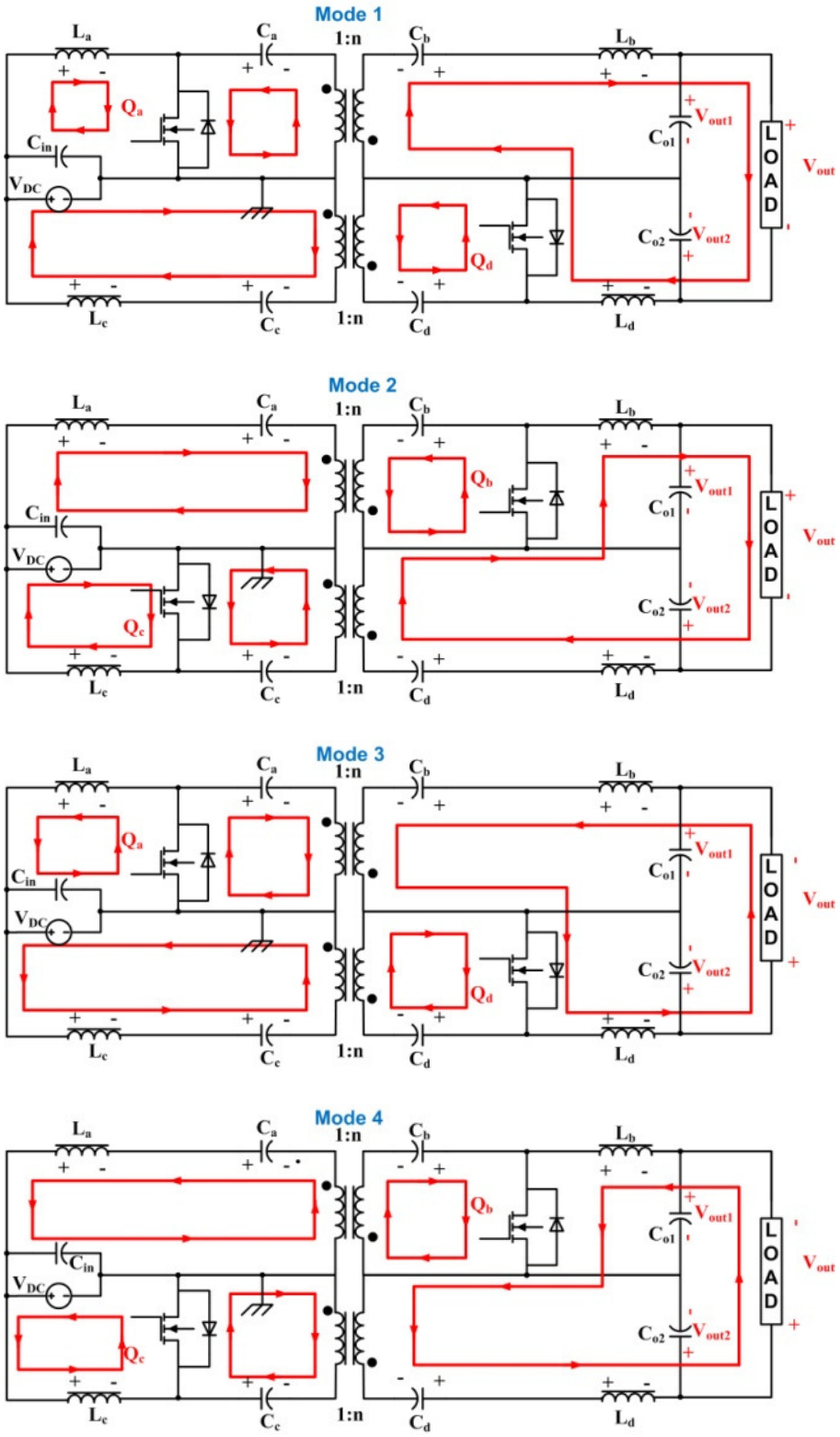
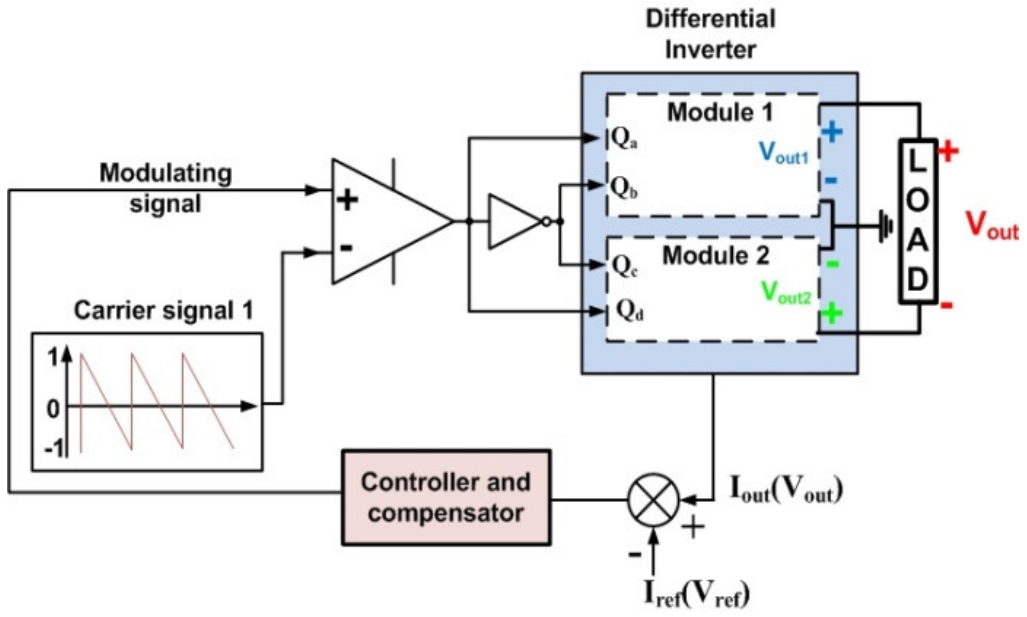


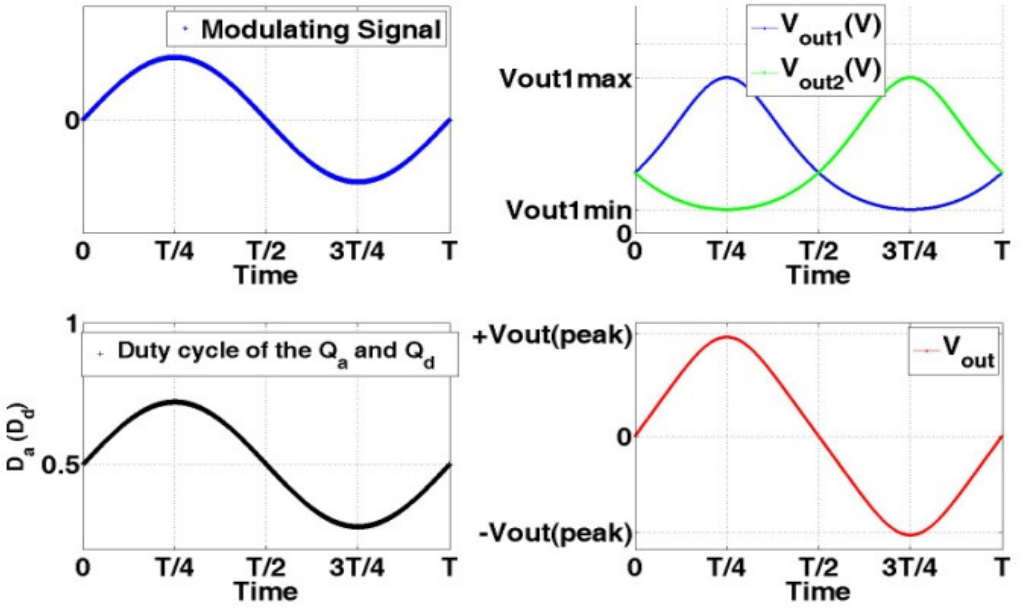
Fig. 13.Modes of operation of the DMCI with CMS.

In Mode 1, switches Q_a and Q_d are turned on while switches Q_b and Q_c are turned off. The current flowing through the input inductor L_a increases and the inductor stores energy. The capacitor C_a discharges through switch Q_a resulting in a transfer of energy from the primary to the secondary side of the top transformer. The energy stored in the capacitor C_b is discharged to the circuit formed by L_b, C_2, and the load R. During this time interval, the inductor L_d stores energy leading to an increase in its current. The capacitor C_d discharges through switch Q_d. For Module 2, power flows from the secondary to the primary side. The capacitor C_c is discharged to provide the power. In Mode 2, switches Q_a and Q_d are turned off while switches Q_b and Q_c are turned on. Capacitors C_a and C_d and C_b and Cc are charged using the energy which was stored in the inductors L_a and L_d while switches Q_a and Q_d were on. During this time interval, inductors L_b and L_c release their stored energy. Finally, Modes 3 and 4 are similar to Modes 1 and 2 with the exception that the load current is negative.

Fig. 14 (a) illustrates the realization of the CMS with control loop. The output voltage of the inverter (V_{out}), the output voltage of each module (V_{out1} and V_{out2}), the modulating signal and the duty cycle of Q_a are shown in Fig. 14(b). The output voltages of both modules are always positive and the minimum voltage depends on amplitude of the modulating signal, with the CMS. The instantaneous power ($p_{out}(t)$) delivered to the load and the instantaneous powers ($p_{out1}(t)$ and $p_{out2}(t)$) flowing through the two modules are shown in Fig. 15(a), assuming a unity power-factor load. Module 1 delivers positive power from the source to the load in the positive half line-cycle, while Module 2 returns part of it from the load to the source. A part of the delivered power returns to the source through Module 1 in the negative half of the line cycle. The power flow diagrams in the positive and negative halves of the line cycles are illustrated in Fig. 15(b) and Fig. 15(c), respectively.

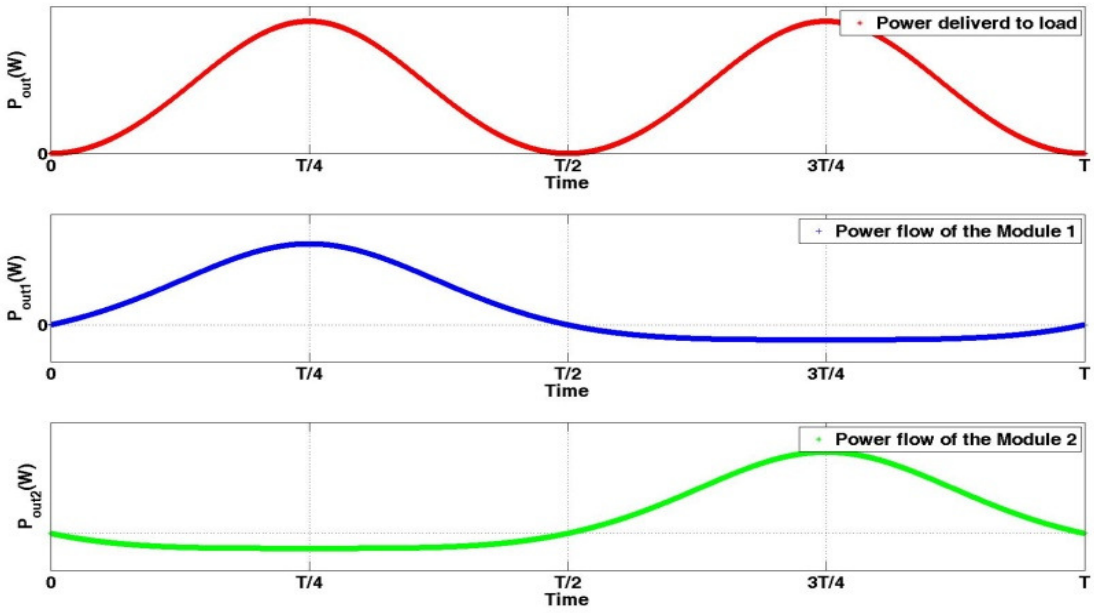


(a)

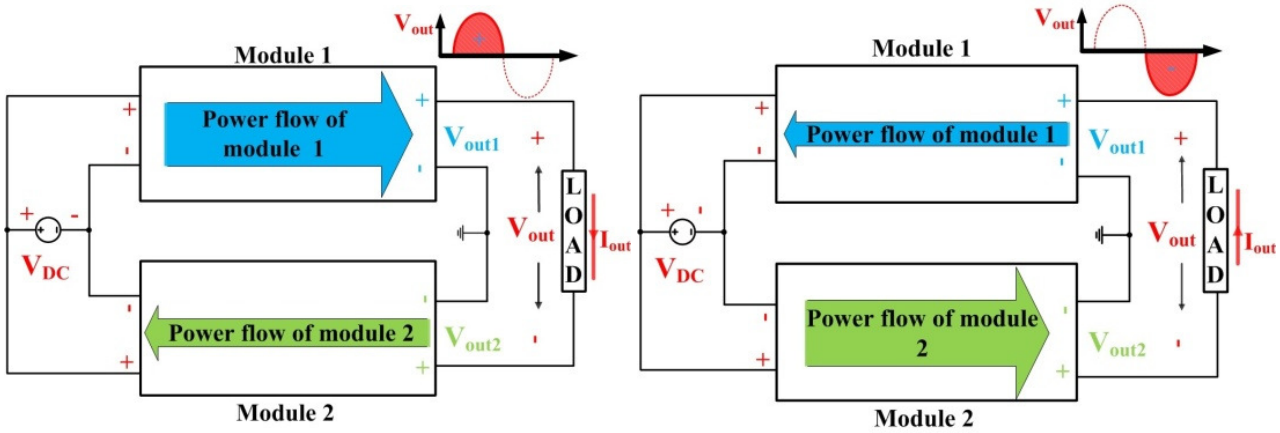


(b)

Fig. 14. (a) Illustration of realization of the CMS for the DMCI. (b) Illustration of the modulating signal, duty cycles of the switches Qa (Qd), output voltages (Vout1 and Vout2) of Modules 1 and 2, and output voltage (Vout) of the DMCI using the CMS.



(a)



(b) (c)

Fig. 15. (a) Instantaneous output powers of the DMCI and its two modules when the DMCI is operated using CMS. (b) and (c) Illustrations of power-flow mechanisms of Modules 1 and 2 during the positive and negative halves of a line cycle.

2. Discontinuous modulation scheme (DMS)

The CMS was originally introduced for the low-power amplifiers of analog circuits [54] with reduced focus on power loss. For DMCI, and as evident from the illustration in Fig. 15, one of the main drawbacks of the CMS is that it leads to circulating power in the converter yielding enhanced loss. Moreover, this circulating power also enhances the peak current and peak voltage of the switching devices. Therefore, the main motivation for developing the DMS

is to mitigate the circulating power by activating only one of the two modules of the DMCI along with the ac-side switch of the inactive module in negative or positive halves of a line cycle. As such, and as evident in (3), the dc voltage-gain relation of the inverter is dependent in a piecewise manner on D_1 and D_2.

$$\frac{V_{out}}{n\times V_{DC}} = \left(\frac{D_1}{1-D_1}\right) \quad (\text{for } V_{out} > 0) \quad \text{or} \quad \frac{V_{out}}{n\times V_{DC}} = \left(\frac{D_2}{1-D_2}\right) \quad (\text{for } V_{out} < 0) \tag{3}$$

Fig. 16 shows the modes of operation with DMS. Modes 1 and 2 are for positive half of the line cycle while Modes 3 and 4 are for the negative half of the line cycle. For each of the modes, a section of the inverter which is inactive is not shown. The capacitor voltage and inductor current in the inactive part of the inverter is zero.

Fig. 17 illustrates the closed-loop realization of the DMS based DMCI. The output voltage (or current) error signal is fed back to the controller, which in turn generates the reference signal for modulation. The modulating signal is bipolar because the output voltage (or current) is bipolar. This signal is fed to the two modules alternately depending on the polarity of the output voltage. Consequently, the resultant modulating reference signals for each module is discontinuous in nature, as illustrated in Fig. 17. As evident in Fig. 17, even though the resultant output voltages (V_{out1} and V_{out2}) of the modules are discontinuous in nature, the differential output voltage (V_{out}) of the DMCI is continuous in form. Assuming a unity-power-factor load (for illustration only), the instantaneous power delivered to the load (P_{out}) and the instantaneous power flowing through each of the two modules (P_{out1} and P_{out2}) is shown in Fig. 18a. The flow of power flow in the DMCI in the positive and negative halves of the line cycle are illustrated, respectively, in Fig. 18b and Fig. 18c.

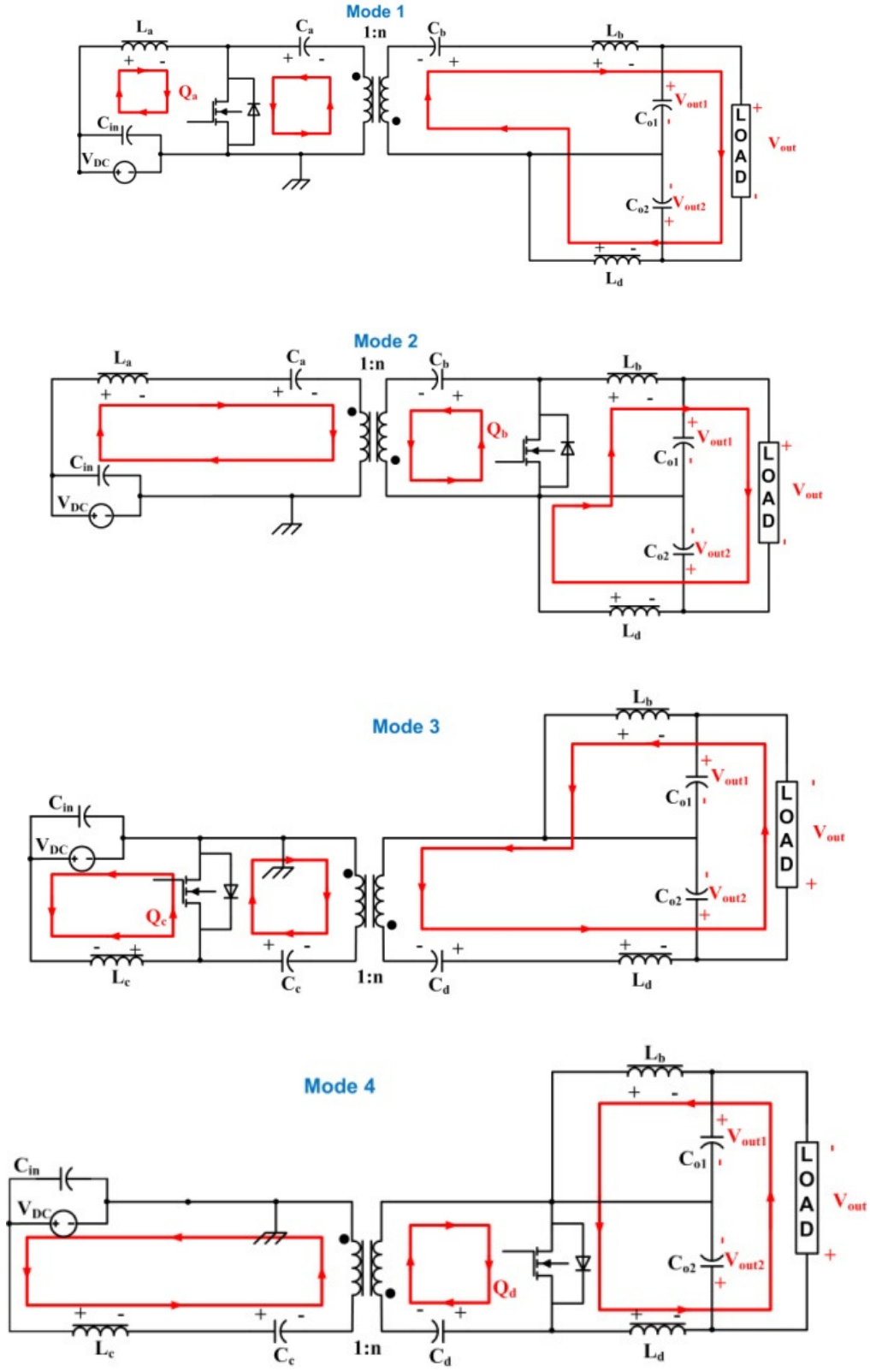


Fig. 16. Modes of operation of the DMCI using DMS.

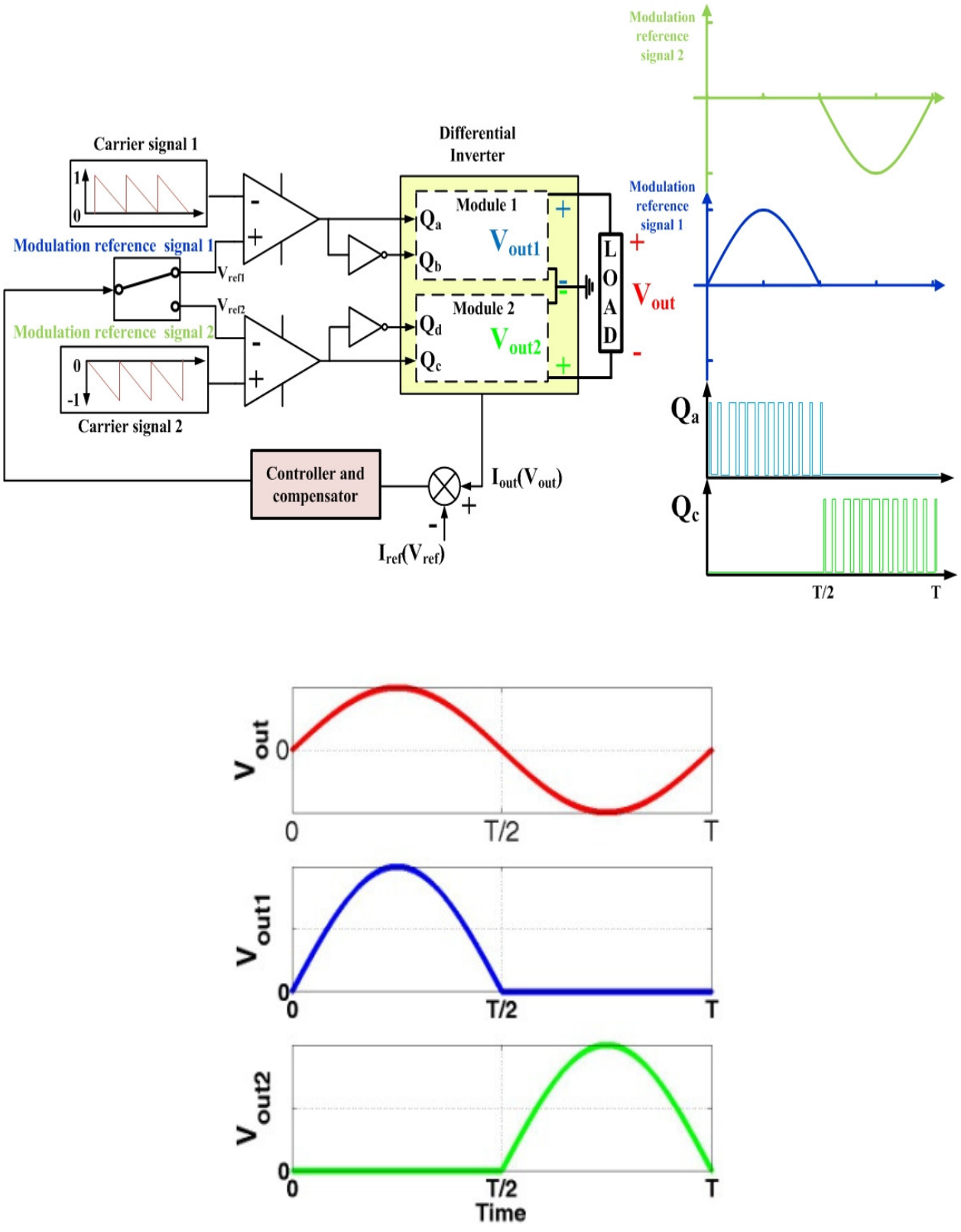
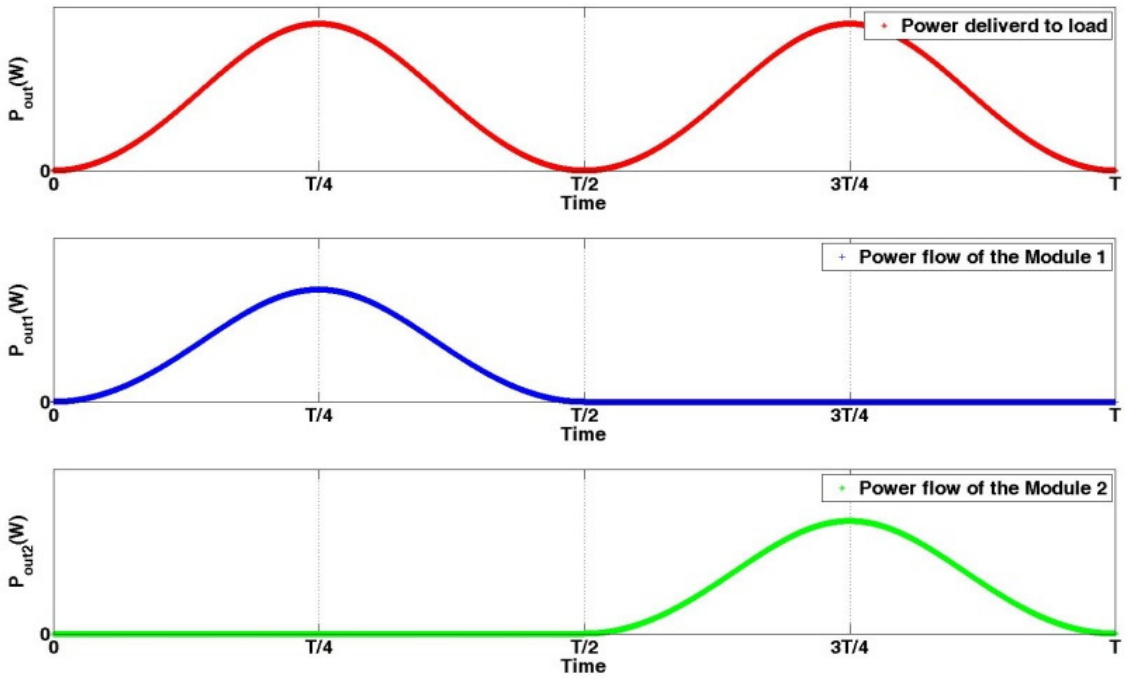
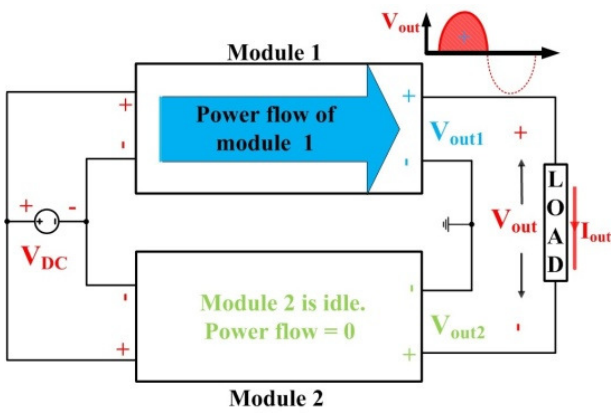


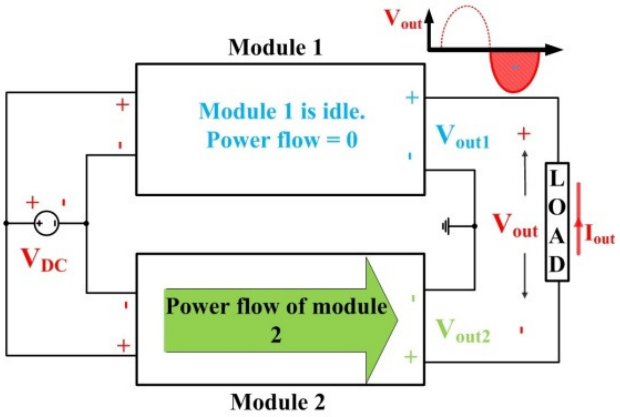
Fig. 17. Illustration of realization of the DMS for the DMCI and the corresponding signals for modulation, switching, and output voltage.



(a)



(b)



(c)

Fig. 18. (a) Instantaneous output power of the DMCI and its individual modules using DMS. (b) and (c) Mechanisms of power flow for the modules of the DMCI during the positive and negative halves of the line cycle.

C. Analysis of DMS and CMS

This section provides the theoretical evaluation and comparison of the CMS and the DMS assuming ideal switching condition. In Section D, validating experimental results are provided.

1. Circulating power

As explained in Section 1, there is no circulating power with the DMS operated DMCI. In contrast, the CMS-based DMCI incorporates active as well as circulating reactive power, as illustrated in Fig. 15(a). Using the Fryze's definition [61], one can calculate the reactive power of each module of the DMCI. Because both modules have the same power ratings, only one module (i.e., Module 1) is selected here for the calculation of the active and the reactive powers as outlined below:

$$P_{out1} = < p_{out1}(t) >_{avg} = \frac{1}{T}\int_0^T V_{out1}(t) \times I_{out}(t)dt \tag{4}$$

$$S_{out1}^2 = P_{out1}^2 + Q_{out1}^2 = V_{out1}^2(rms) \times I_{out1}^2(rms) = \frac{1}{T}\int_0^T V_{out1}^2(t)dt \times \frac{1}{T}\int_0^T I_{out1}^2(t)dt. \tag{5}$$

In (4) and (5), $p_{out1}(t)$ is the instantaneous power, $P_{out1}$is the active power, Q_{out1} is the circulating reactive power, S_{out1} is the apparent power, and V_{out1} and I_{out} are output voltage and output current of Module 1. Using (4) and (5), the ratio of the reactive to the active power can be derived to be the following:

$$\frac{Q_{out1}}{P_{out1}} = \sqrt{\frac{\frac{1}{T}\int_0^T V_{out1}^2(t)dt \times \frac{1}{T}\int_0^T I_{out}^2(t)dt}{[\frac{1}{T}\int_0^T V_{out1}(t) \times I_{out}(t)dt]^2} - 1}\,. \tag{6}$$

Assuming a unity-power-factor load and negligible total harmonic distortion (THD) for the load voltage and the load current, we obtain

$$\begin{cases} I_{out} = I_{out}^* \sin(\omega t) \\ V_{out} = V_{out}^* \sin(\omega t) = nV_{DC} \times g^* \sin(\omega t) \end{cases} \tag{7}$$

where $g*$ represents the peak normalized dc-voltage gain and is defined to be equal to $\frac{V_{out}^*}{n\times V_{DC}}$. The dc-voltage gains of the DMCI is defined by (2) while the dc-voltage gain of Module 1 (i.e., g_1) is defined by (8) for operation of the DMCI using the CMS:

$$g_1 = \frac{V_{out1}}{n\times V_{DC}} = \left(\frac{D_1}{1-D_1}\right) \tag{8}$$

Using (2) and (8), the relation between g and $g_1$is found to be the following:

$$g_1 = \frac{g}{2} + \sqrt{\left(\frac{g}{2}\right)^2 + 1}. \tag{9}$$

Using (8) and (9), $V_{out1}$is found to be the following:

$$V_{out1} = nV_{DC}\left(\frac{g^*\sin(\omega t)}{2} + \sqrt{\left(\frac{g^*\sin(\omega t)}{2}\right)^2 + 1}\right). \tag{10}$$

Substituting $V_{out1}$from (10) and I_{out} from (7) into (6) and simplifying the resultant expression yields:

$$\frac{Q_{out1}}{P_{out1}} = \sqrt{\frac{\int_0^T\left(\frac{g^*\sin(\omega t)}{2}+\sqrt{\left(\frac{g^*\sin(\omega t)}{2}\right)^2+1}\right)^2 dt\times\int_0^T\sin^2(\omega t)dt}{[\int_0^T\left(\frac{g^*\sin(\omega t)}{2}+\sqrt{\left(\frac{g^*\sin(\omega t)}{2}\right)^2+1}\right)\times\sin(\omega t)dt]^2} - 1} = \sqrt{\frac{\int_0^T(\frac{g^{*2}\sin^2(\omega t)}{2}+1)dt\times\int_0^T\sin^2(\omega t)dt}{[\int_0^T\frac{g^*}{2}\sin^2(\omega t)dt]^2} - 1} \tag{11}$$

$$\frac{Q_{out1}}{P_{out1}} = \sqrt{\frac{g^{*2}+8}{g^{*2}}}. \tag{12}$$

Note that, V_{out} using CMS is a sinusoidal waveform while V_{out1} is a non-sinusoidal waveform. Fig. 19 plots the ratio of Q_{out1} and P_{out1} as a function of the normalized peak dc-voltage gain as captured in (12). The circulating power is significant for lower peak dc-voltage gains leading to additional power loss.

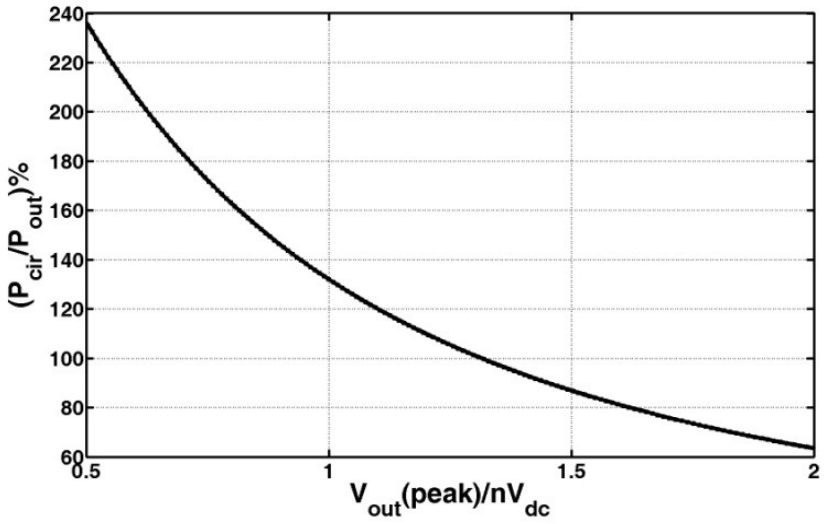


Fig. 19. For Module 1, the ratio of the reactive (circulating) power to the active power for varying peak normalized dc-voltage gain for the DMCI when the inverter is operated using CMS. The DMCI has no circulating-power when it is operated using DMS.

2. Device rating

Following Fig. 12, the off-state voltage of each device in the DMCI (V_{Qa}, V_{Qb}) is given by the following set of expressions:

$$\begin{cases} V_{Qa} = V_{ca} + \frac{V_{cb}}{n} \\ V_{Qb} = nV_{ca} + V_{cb} \end{cases}. \tag{13}$$

In the steady state, using $V_{ca} = V_{DC}$ and $V_{cb} = V_{out1}$, (13) translates to the following expression:

$$\begin{cases} V_{Qa} = V_{DC} + \frac{V_{out1}}{n} \\ V_{Qb} = nV_{DC} + V_{out1} \end{cases}. \tag{14}$$

The voltage ratings of the devices should be designed for the worst case, which happens at the peak output voltage.

For the DMS-based DMCI, the peak output voltages of Modules 1 and 2 (V_{out1}^{*} and V_{out2}^{*}) equal V_{out}^{*}. However, when DMCI is operated using CMS, the peak output voltage of each module is higher than the V_{out}^{*}. These can be expressed as follows:

$$\begin{cases} V_{out1}^* = V_{out2}^* = V_{out}^* & for\ DMS \\ V_{out1}^* = V_{out}^* + V_{out2}(min) & for\ CMS \end{cases} \quad (15)$$

where $V_{out2}(min)$ is always positive. Equations (15) and (16) show that the voltage ratings of the devices of the DMCI when operated using CMS are higher than those obtained using DMS. The ratio of the peak voltage of the device using CMS to the peak voltage of the device with DMS can be obtained by substituting (15) into (14). This ratio is rewritten as a function of peak dc-voltage gain using (2) and (3):

$$\frac{V_{Qa}^*(CMS)}{V_{Qa}^*(DMS)} = \frac{V_{Qb}^*(CMS)}{V_{Qb}^*(DMS)} = \frac{V_{DC} + \frac{V_{out1}^*}{n}}{V_{DC} + \frac{V_{out}^*}{n}} \quad (16)$$

where V_{Qa}^* and V_{Qb}^* are peak voltages of the primary side and the secondary side devices, respectively. It is noted that, (16) does not include any device voltage spike, which is dependent on the load, leakage inductance of the transformer, the off-state voltage of the device, and printed-circuit-board (PCB) layout. As such, the actual peak voltages are slightly higher and (16) indicates an approximate value. Using (2), (8) and (9) and (16), the device voltage ratio can be written as a function of g^*as follows:

$$\frac{V_{Qa}^*(CMS)}{V_{Qa}^*(DMS)} = \frac{V_{Qb}^*(CMS)}{V_{Qb}^*(DMS)} \approx \frac{1 + \frac{g^*}{2} + \sqrt{(\frac{g^*}{2})^2 + 1}}{1 + g^*} \quad (17)$$

The ratio $V_{Qa}^*(CMS)/V_{Qa}^*(DMS)$ as described by (17) is plotted in Fig. 20. It is always greater than one and the ratio decreases with increasing normalized dc-voltage gain. The purpose of calculations and plot is to demonstrate the effect of modulation on reduction of device voltage rating, which has modeled well by (17) as shown by simulation and experimental results as follows. However actual peak voltages of devices also depend on spikes of the switches. The spike on Q_a is due to discharge of the energy stored in the leakage inductance of the transformer and parasitic inductances during the turn off of Q_a. It mostly depends on the switch turn-off time, snubber circuit, energy stored in leakage inductance of the transformer. The spike on Q_b is due to the reverse recovery of the diode during the diode turn-off.

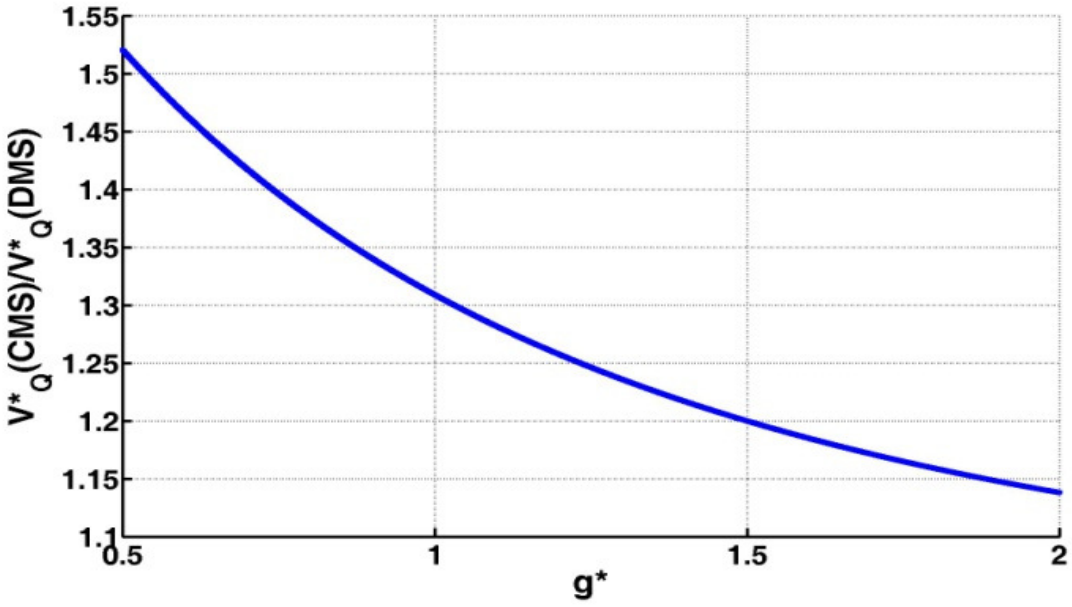


Fig. 20. $V^*_{Qa}(CMS)/V^*_{Qa}(DMS)$ **as a function of** g^***.**

Fig. 21 shows the (Saber-based) simulation results for the peak drain-to-source voltages of Q_a and Q_b operating with DMS and CMS. These simulations are carried out using circuit parameters that match those of the experimental prototype described in Section D. Using these parameters, the ratios of $V_{Qa}(CMS)/V_{Qa}(DMS)$ and $V_{Qb}(CMS)/V_{Qb}(DMS)$ are found to be 1.34 and 1.22, respectively, for $g^* = 1$, $V_{DC} = 60$ V, $V^*_{out} = 120$ V, and an output power (P_{out}) of 500 W. This is found to be close to the theoretically-predicted value as shown in Fig. 20 for $g^* = 1$. DMS also reduces the current rating of the devices. This is evident from the simulation results in Fig. 22, which demonstrates the peak-current waveforms for Q_a and Q_b.

In addition, Fig. 23 shows that, using DMS, a reduction in the voltage of output capacitor and blocking capacitor or current ratings of input filter inductor and transformer of the DMCI is also achieved. These simulations are carried out using circuit parameters that match those of the experimental prototype described in next section including $g^* = 1$, $V_{DC} = 60\,V$, $V^*_{out} = 120\,V$, and $P_{out} = 500\,W$. Further, all of these results are captured during the positive peak of the output voltage.

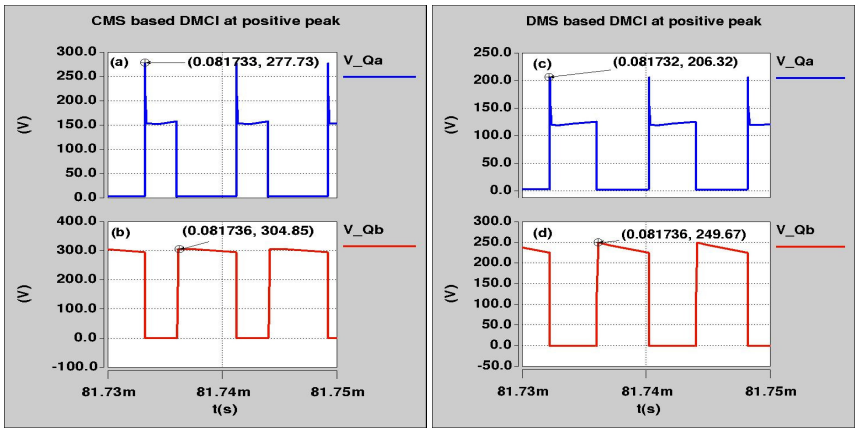


Fig. 21. Simulation results for V_{Qa} and V_{Qb} obtained using CMS and DMS when the output voltage attains maximum positive value.

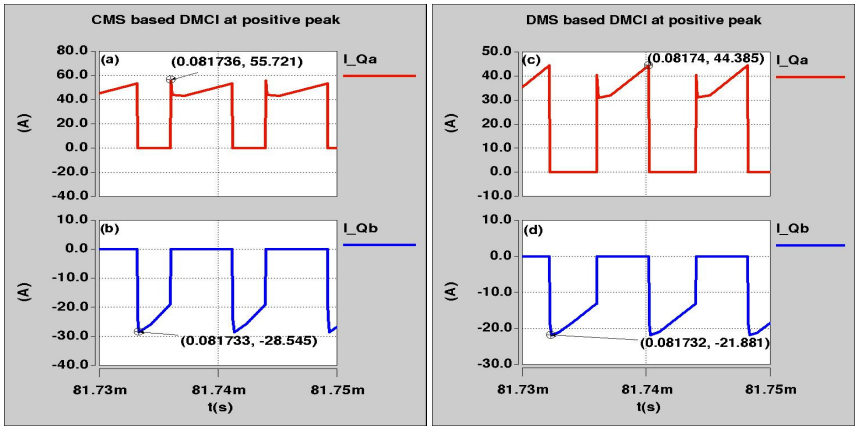
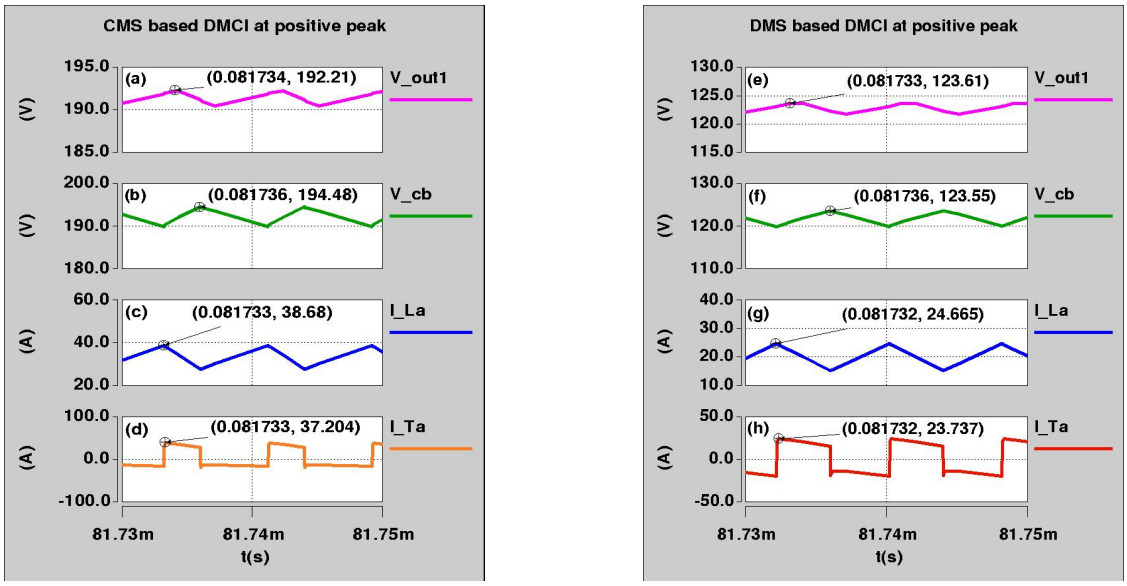


Fig. 22. Simulation results for I_{Qa} and I_{Qb} obtained using CMS and DMS when the output current attains maximum positive value.



(a) **(b)**

Fig. 23. Simulation results showing V_{out1}, V_{cb}, I_{La}, and I_{Ta} for the DMCI shown in Fig. 10 when the inverter is operated using CMS and DMS and when the output voltage attains maximum positive value.

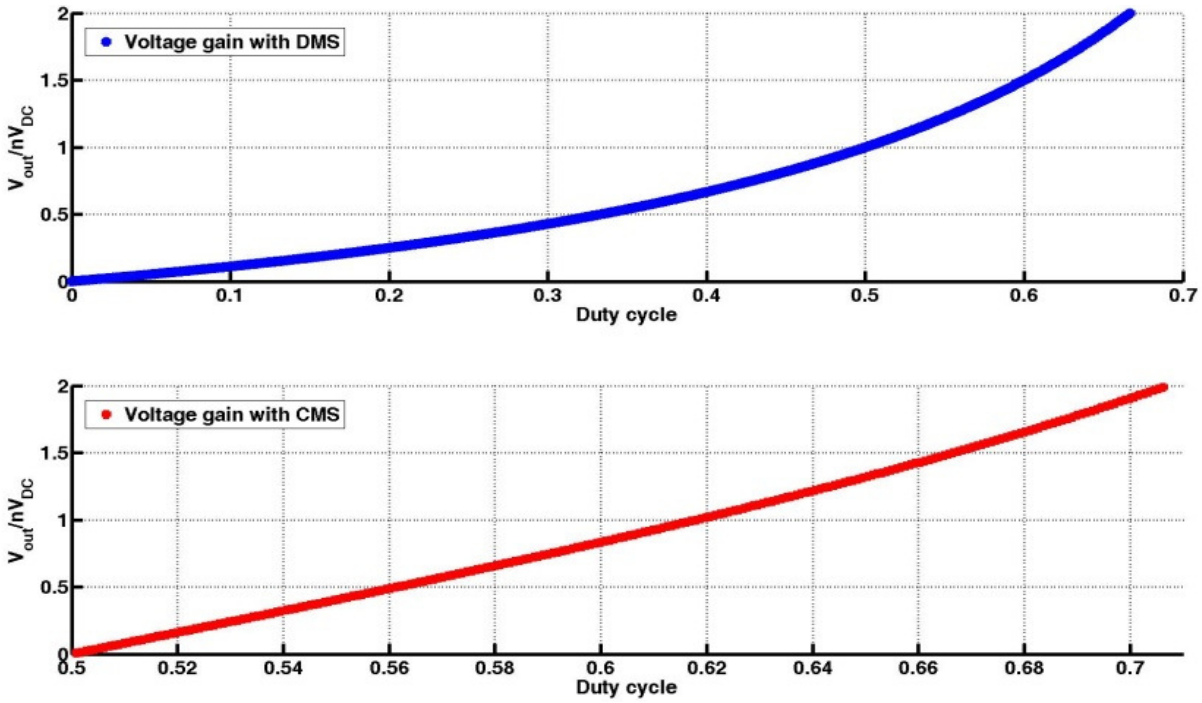


Fig. 24. The normalized dc voltage-gain of the DMCI as a function of the duty cycle when the inverter is operated using DMS and CMS.

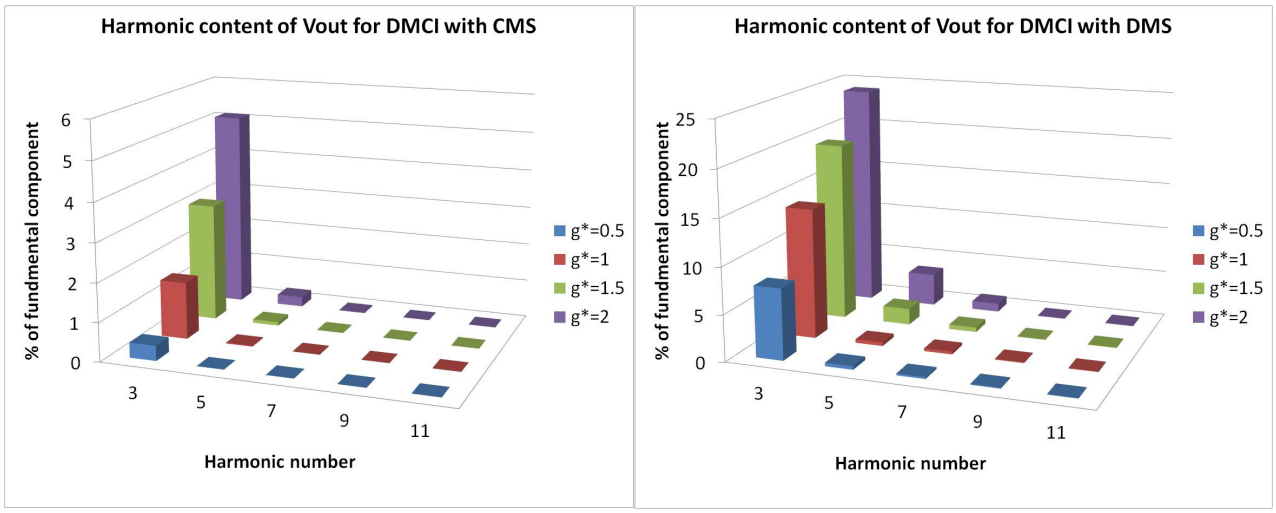


Fig. 25. Harmonic analysis of the output-voltage distortion caused by the nonlinearity in the dc voltage gain of the DMCI operated with (a) CMS and (b) DMS. Magnitudes of the 3rd, 5th, 7th, 9th and 11th harmonics are shown as a percentage of the magnitude of the fundamental-frequency component of the DMCI output voltage for different peak-voltage gains.

3. Distortion

The normalized dc-voltage gain of the DMCI is a nonlinear function of the duty cycle for both CMS and DMS as evident in (2) and (3), respectively. In order to compare the nonlinearity of the two modulation schemes, normalized dc-voltage gains of the DMCI are plotted as a function of the duty cycle in Fig. 24. It shows that the nonlinearity of the normalized dc-voltage gain of the inverter using DMS is more than that obtained using CMS in the given range. The voltage-gain nonlinearity leads to distortion at the output voltage, but it only causes limited number of harmonics at the output voltage. In order to study and compare the nonlinearity effect, the FFT analysis is done for the ideal open loop output voltage of DMCI operating with CMS and DMS. The results are shown in Fig. 25(a) and Fig. 25(b) at different peak voltage gains for CMS and DMS based DMCI, respectively. Comparing the results for CMS and DMS shows that amplitudes of harmonic components of the output voltage of CMS based DMCI are about 5% at the worst condition, while DMS based DMCI shows higher harmonic magnitudes. As second conclusion, the magnitude of 11th and higher order harmonics are negligible (less than 0.1%) in practice. Thus, 3rd, 5th, 7th and 9th harmonics compensators are considered for output voltage distortion problem. It will be demonstrated in next section that the nonlinearity effect can be overcome by using a harmonic-compensation of first few harmonics.

D. Experimental results

This section provides the experimental results of the DMCI obtained using DMS and CMS. A 500-W experimental prototype of the DMCI, as shown in Fig. 26 is implemented and tested using both modulation schemes. A TMS320F28335 DSP based digital controller is used for implementing DMS and CMS with closed-loop control, which has 150-MHz clock. Execution time of implemented control loop for CMS based DMCI takes 1.9 µs, while this duration for DMS based controller is about 2.6 µs. This means roughly 35% more execution time of DMS based control for the digital device. Specifications of the DMCI prototype are provided in Table .

Fig. 27 shows the efficiency of the DMCI for an output voltage of 120 V (RMS) and an output power of 500 W with normalized dc-voltage gain varying between 0.5 and 2 (corresponding to an input-voltage (V_{DC}) variation between 30 V and 120 V). The difference in the efficiencies of the DMCI using DMS and CMS is found to be significant. The improvement is considerably more at lower normalized dc-voltage gain and is consistent with the prediction of Fig. 19.

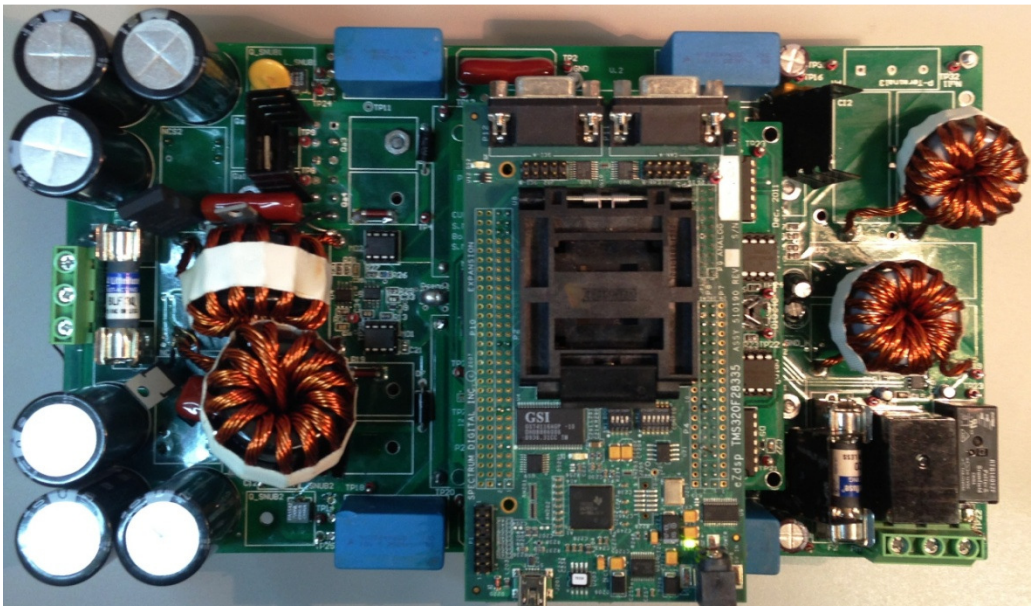


Fig. 26. Experimental prototype of the DMCI. It shows the TMS320F28335 DSP based digital controller on the top feeding the DMCI power stage at the bottom.

Table I. Specifications of the DMCI experimental prototype.

Input voltage	Peak output voltage (V_{out}^{*})	Output power	Output frequency	Transformer turns ratio (n)	Switching frequency	Primary-side filter inductance	Secondary-side filter inductance
20-120 V	170 V	500 W	60 Hz	2	125 kHz	50 µH	100 µH

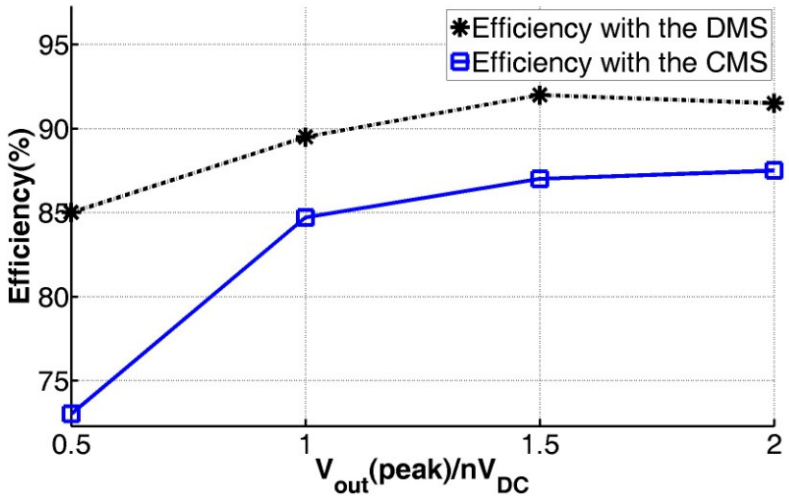
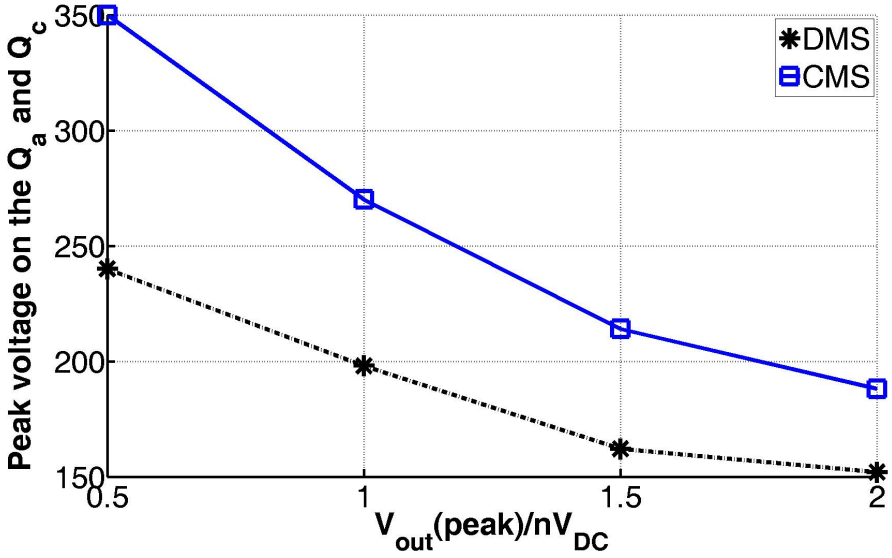
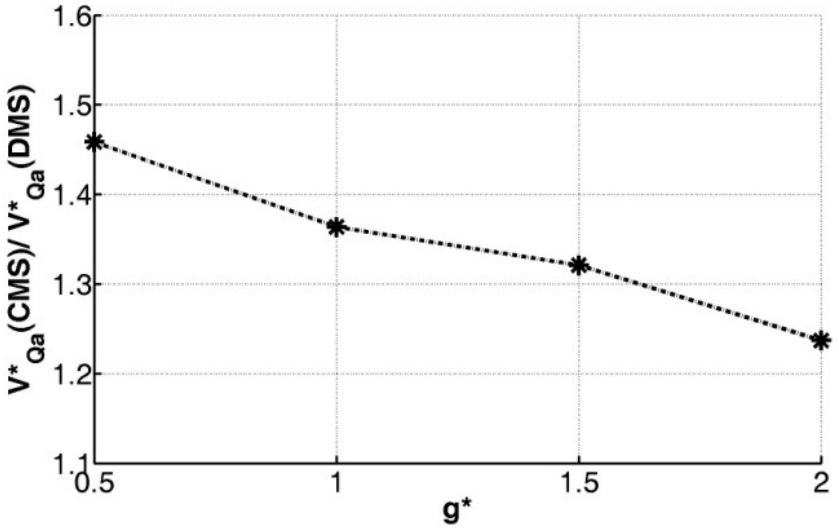


Fig. 27. Experimental efficiency of the DMCI for varying normalized dc peak voltage gain obtained using DMS and CMS.

Next, the peak voltages of the switches (Q_a and Q_c) on the primary side of DMCI obtained using DMS and CMS are measured and plotted in Fig. 28 (a). It is noted that, the voltage ratings of the switches on the ac side are proportional to the switches on the dc side with the proportionality constant being the transformer turns ratio. To obtain the plot in Fig. 28, the input voltage is varied between 30 V and 120 V for a constant output power of 500 W while keeping the output peak voltage set at 120 V. The results show that the gap between the peak voltage of the switches using DMS and CMS increases (decreases) with decreasing (increasing) normalized dc-voltage gain. The ratios of the measured peak voltages of the primary-side switches of the DMCI are shown in Fig. 28(b) and they are consistent with the predictions in Fig. 20 and the simulation results in Fig. 21.



(a)

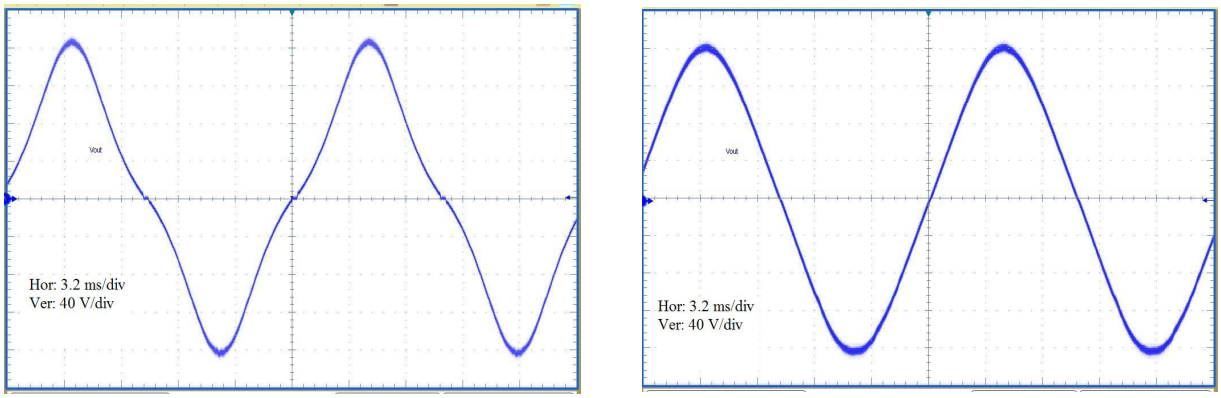


(b)

Fig. 28. (a) Experimentally-determined peak voltage of the primary-side switches of the DMCI with CMS (solid line) and DMS (dotted line). (b) Ratios of the two traces in (a).

Next, distortion caused by nonlinearity of the open-loop inverter operating with DMS and CMS is considered. The output voltages of the DMCI operating using DMS and the CMS are shown in Fig. 29(a) and Fig. 29 (b), respectively. The peak instantaneous output voltages for both results are set at 170 V (corresponding to 120-V RMS) while the input voltage and output power are set, respectively, at 40 V and 500 W. The DMS yields a total harmonic

distortion (THD) of 22% for the open-loop DMCI as against a THD of 4% obtained by operating the DMCI using CMS. Further illustration of the problem is provided in Fig. 30 which shows that for the open-loop DMCI, DMS has a progressively adverse effect of the THD of the output voltage with increasing normalized dc voltage gain. As such, a closed-loop control mechanism to compensate for the harmonic is pursued next.



(a) (b)

Fig. 29. Experimentally obtained output voltage of the open-loop DMCI operated using (a) DMS (yielding a THD of 22%) and (b) CMS (yielding a THD of 4%). Horizontal scales for both the results are set 3.2 ms/div while corresponding vertical scales are set at 40 V/div.

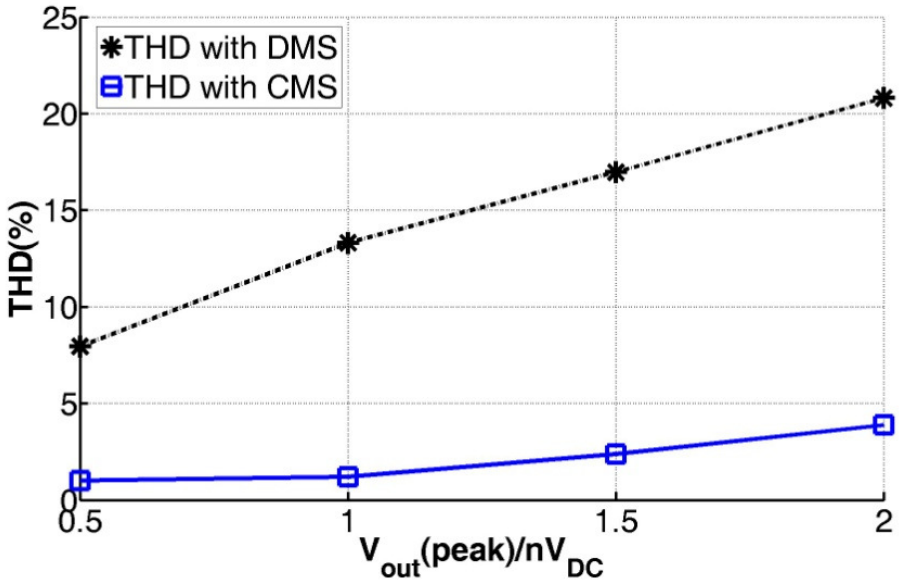


Fig. 30. Experimentally obtained THD of the output voltage of the open-loop DMCI obtained using DMS and CMS as a function of the normalized dc voltage gain.

The architecture of the closed-loop controller for the DMCI is shown in Fig. 31. It comprises mechanisms for harmonic compensation. The choice of 3rd, 5th, 7th, and 9th harmonic compensation in Fig. 31 is guided by the determination that when the open-loop DMCI is operated using DMS based on a sinusoidal modulation signal, the resultant output voltage of the inverter is found to have appreciable components of 3rd, 5th, 7th, and 9th harmonics apart from the dominant fundamental 60-Hz ($= \frac{\omega_o}{2\pi}$) component with a desired amplitude of V_{amp} and an initial phase of θ. The choice of the fundamental and harmonic compensation is based on proportional-resonant (PR) compensating scheme [56] that is tuned to keep a balance between good steady-state performance and acceptable transient response. The output of the compensation (i.e. comprising fundamental and harmonic compensation) block feeds the control command to the modulator that implements CMS or DMS. The output switching signals of the modulation block are fed to the DMCI. It is noted that, when the DMCI is operated using CMS, the harmonic compensator is not needed; instead, only a PR based fundamental-frequency controller is used to close the loop. This is because, and as illustrated in Fig. 24 and Fig. 29(b), the DMCI exhibits almost linear characteristics when it is operated using CMS.

The closed loop output voltages of the DMCI operating using DMS and the CMS are shown in Fig. 32(a) and Fig. 32(b), respectively. The peak instantaneous output voltages for both results are set at 170 V (corresponding to 120-V RMS) while the input voltage and output power are set, respectively, at 40 V and 500 W. The DMS yields a THD of 5.5%, while THD of 5% obtained by operating the DMCI using CMS. Fig. 33 shows the THD of the output voltage of the closed-loop DMCI operated using DMS and CMS. By comparing the open- and closed-loop results of DMCI shown, respectively, in Fig. 30 and Fig. 34, one can observe that the (PR-based) harmonic compensators reduce the THD of the DMS-based closed-loop DMCI. In addition to achieving an acceptable THD, a further goal is to achieve an acceptable transient performance for the DMCI. Consequently, for the DMS-based DMCI, the gains of the fundamental and harmonic compensators have to be so chosen such that an optimal tradeoff between a lower harmonic distortion and a satisfactory transient response is achieved. In our present design, the tuning of the compensator gains are skewed more towards achieving a reduced THD (as evident in Fig. 34) because the open-loop dc-voltage-gain response of the DMS-based DMCI is highly nonlinear, which yields higher distortion. This is further evident in Fig. 34. It shows that even though the topological control of the DMS-based DMCI has to address a reduced-order system (as evident in Fig. 16) as compared to the CMS-based DMCI (as evident in Fig. 13), the transient response of the inverter is slightly slower due to choices of the gains of the PR compensators. Essentially,

if the proportional gains of the PR compensators are increased then, while it increases the control bandwidth, it increases distortion because of the spread in the control spectrum around the fundamental and harmonic frequencies. This sets an upper limit on the proportional gains.

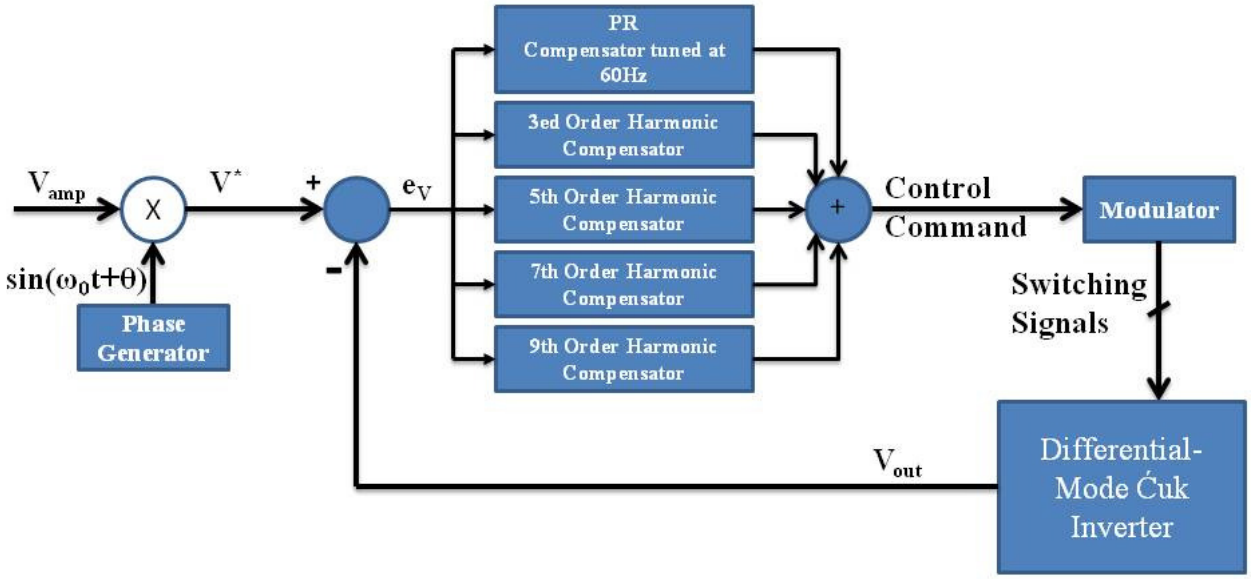
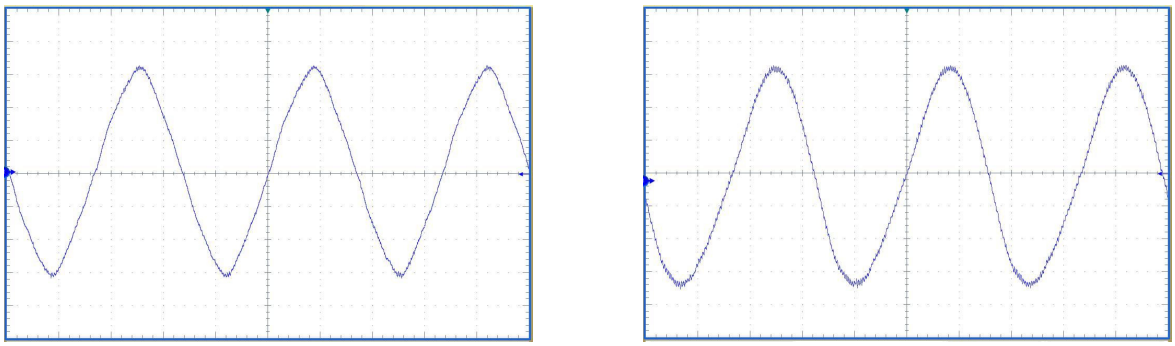


Fig. 31. Architecture of the closed-loop controller for the DMCI.



(a) **(b)**

Fig. 32. Experimentally obtained output voltage of the closed-loop DMCI operated using (a) DMS (yielding a THD of 5.5 %) and (b) CMS (yielding a THD of 5%). Horizontal scales for both results are set 5 ms/div while corresponding vertical scales are set at 50 V/div.

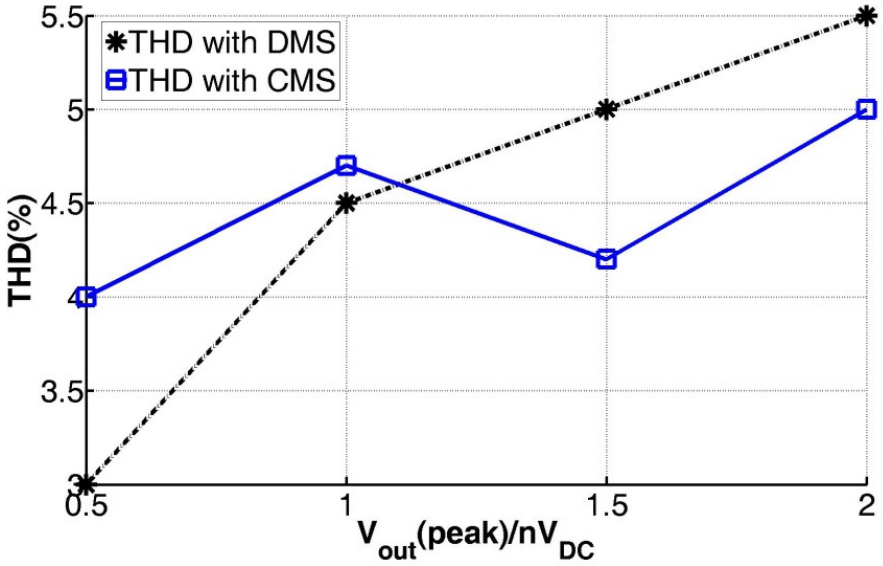
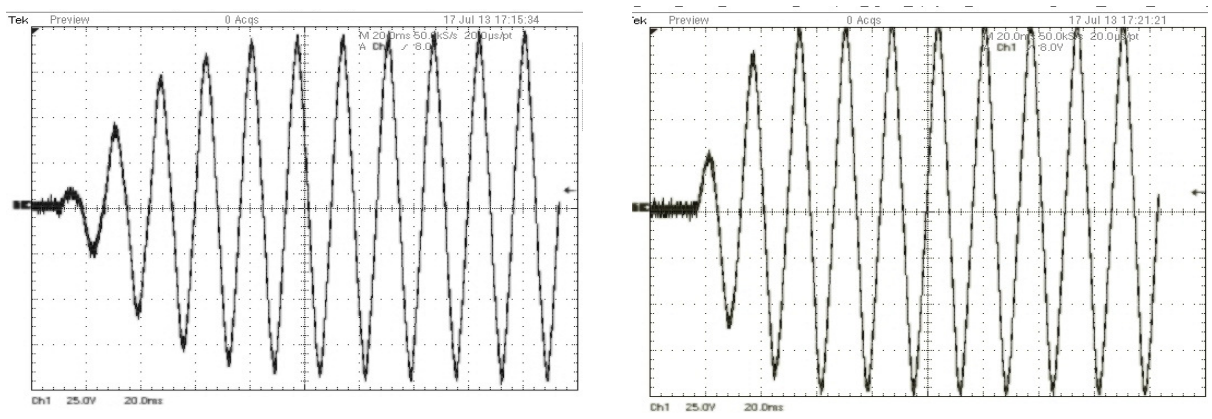


Fig. 33. Experimentally obtained THD of the output voltage of the closed-loop DMCI operated using DMS and CMS as a function of the normalized peak dc voltage gain of the inverter. It shows a marked improvement in the THD of the closed-loop DMCI using DMS.



(a) **(b)**

Fig. 34. Transient start-up response of the closed-loop DMCI when it is operated using (a) DMS and (b) CMS. Horizontal and vertical scales for (a) and (b) are set at 20 ms/div and 25 V/div, respectively.

In contrast, for the CMS-based closed-loop DMCI, the choice of the PR compensator gain is skewed towards achieving a satisfactory dynamic response. This is because the topological control of the CMS-based DMCI has to address a higher-order system as compared to the DMS-based DMCI; and additionally, the open-loop dc-voltage gain of the inverter, as a function of the duty ratio, has a wide range of linearity, which yields reduced THD compared to the DMS-based DMCI. As evident in Fig. 34(b), the transient response of the CMS-based DMCI is better that obtained using the DMS-based DMCI. However, this improvement in transient response comes at the

price of a slight increase in the THD, as evident in Fig. 33. Essentially, while an increase in the proportional gain of the PR compensator increases the control bandwidth, it also spreads the control spectrum around the fundamental harmonic. Even though for the CMS-based open-loop DMCI, the magnitude of the lower-order harmonics around the fundamental harmonic is small, the spread in the control spectrum amplifies the response of these lower-order harmonics thereby slightly increasing the THD for the closed-loop DMCI.

E. Nonlinearity Compensation of DMS based DMCI with Grid Connection

Two modulation schemes have been introduced for the inverter in Section B. As evident from the results in Section C, DMS suits the switched mode power supply applications because of better efficiency and lower device ratings. But, the DMS shows nonlinear control-to-output relation. The effect of nonlinearity on the THD is more adverse in grid-connected mode. This section introduces a static-linearized DMS (SLDMS) scheme. It mitigates the control-to-output nonlinearity of the DMCI statically. It uses the input and output voltages as feed forward to generate the needed modulating signal. The results demonstrated in the following section provide the validity to the new mechanism.

1. SLDMS Scheme

For grid-connected application V_{out} can be replaced with V_{Grid} as demonstrated in Fig. 35. SLDMS is implemented by incorporating an additional control block (Fig. 35), which is fed with additional feed-forward variable from the DMCI. The overall forward (open loop) system is defined to include the feed-forward block followed by modulator and power-module. The feed-forward block is designed so that a linear control-to-output characteristic is obtained for this open loop system. If V_c represents the control input to the system and symbol α represents a static control-to-output gain constant, then $V_{grid} = \alpha Vc$ is yield. In order to obtain this linear relation, it is substituted into (3) and then rearranged it to obtain the duty cycle as obtained in (18). Equation (18) is used to implement feed-forward block, because it gives the needed duty cycle versus input voltage (V_{DC}) and input control voltage (V_c), so that the linear input-output characteristic ($V_{grid} = \alpha V_c$) holds for DMCI. If carrier signal of PWM is between 0 and 1 (as illustrated in Fig. 5) then D_1 and D_2 can be applied directly to V_{ref1} and V_{ref2} respectively; otherwise a proper scale coefficient is needed. α is also chosen so that the control signal levels are at acceptable rang for implementation.

$$\begin{cases} D_1 = \frac{1}{1+\frac{n\times V_{DC}}{\alpha V_c}} & \text{and } D_2 = 0 \quad (V_{out} > 0), \\ D_2 = \frac{1}{1+\frac{n\times V_{DC}}{\alpha V_c}} & \text{and } D_1 = 0 \quad (V_{out} < 0) \end{cases} \tag{18}$$

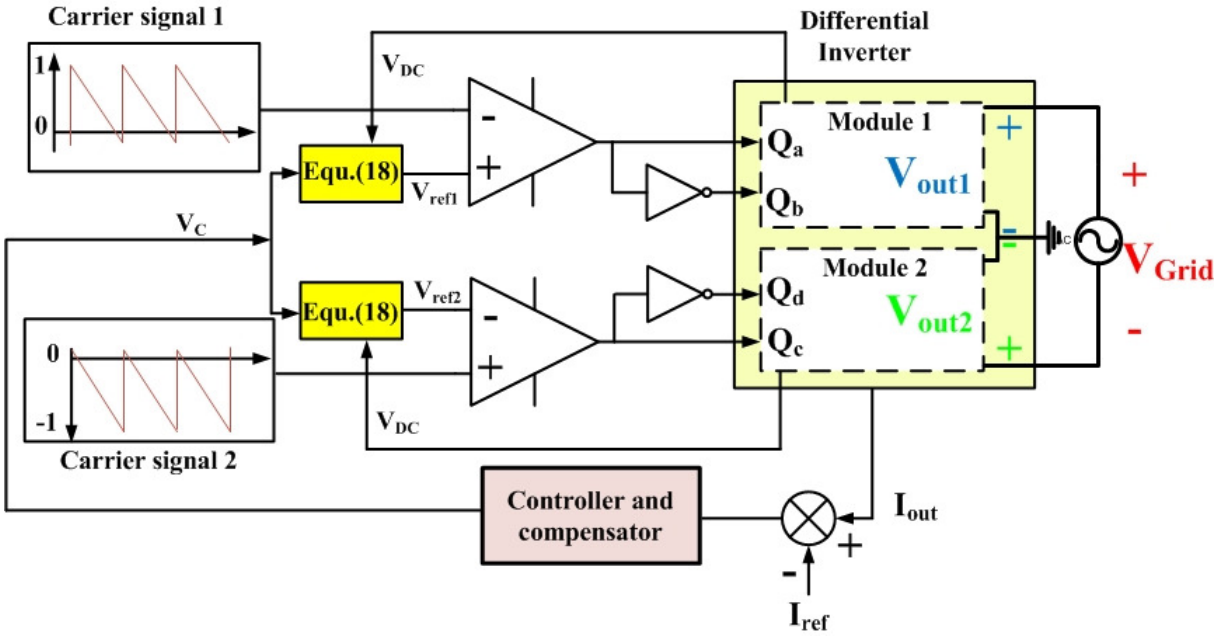


Fig. 35. Realization method of the SLDMS.

2. SLDMS Results

This section presents the comparison between the SLDMS and DMS. Fig. 36 shows an open loop simulation results with sinusoidal input signal applied in Saber. From the results it is apparent that, the SLDMS-based DMCI yields a much lower harmonic distortion in open loop. On a similar note, in the grid-connected model, the transient response of the start-up currents of the DMCI using SLDMS, as demonstrated in Fig. 37 is significantly better compared to the performance obtained using DMS. Fig. 38 also demonstrates the steady state current injection results with both DMS and SLDMS. The dotted lines are ideal sinusoidal waveform for comparison purposes.

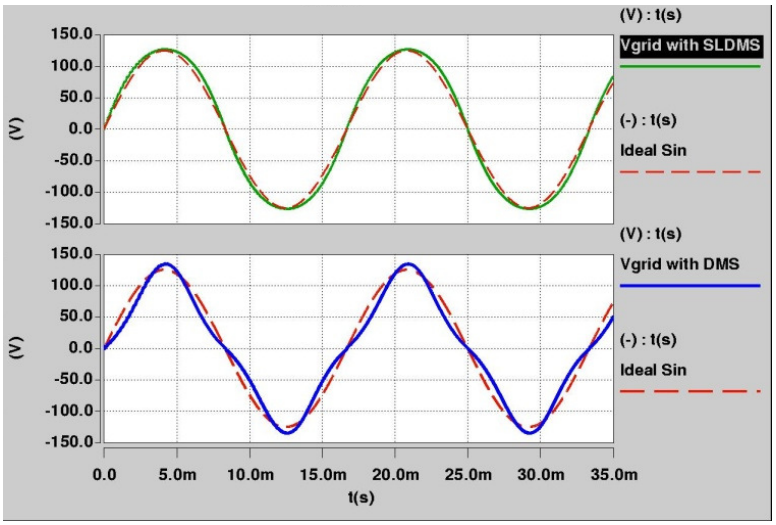


Fig. 36. Comparison of the SLDMS and DMS with open loop SPWM.

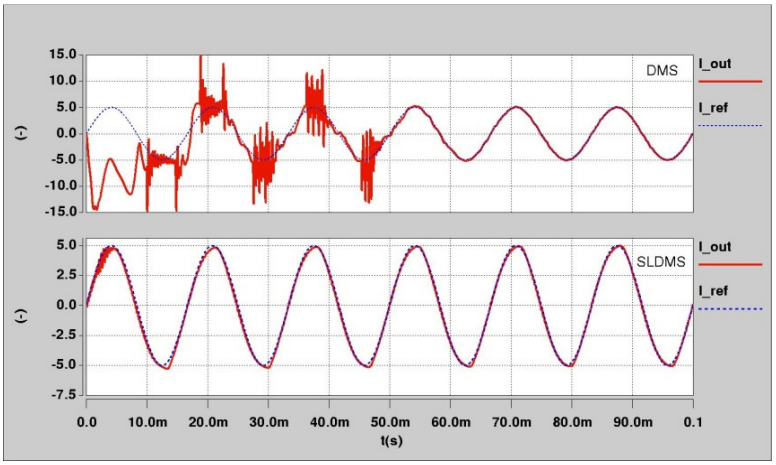


Fig. 37. Startup current in grid connection mode with DMS and SLDMS.

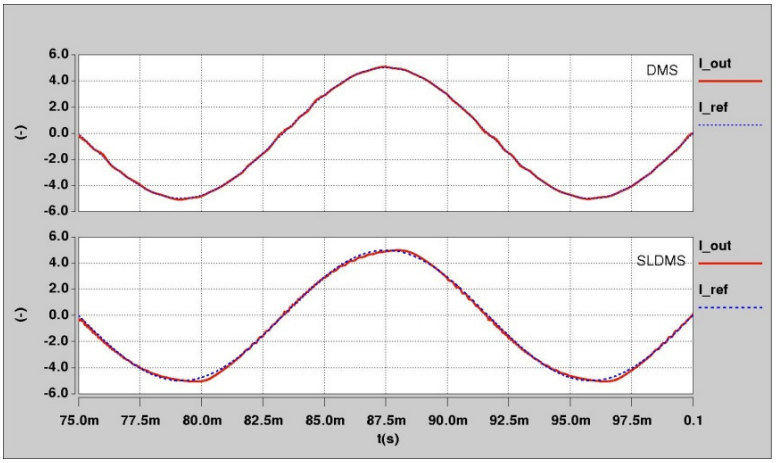
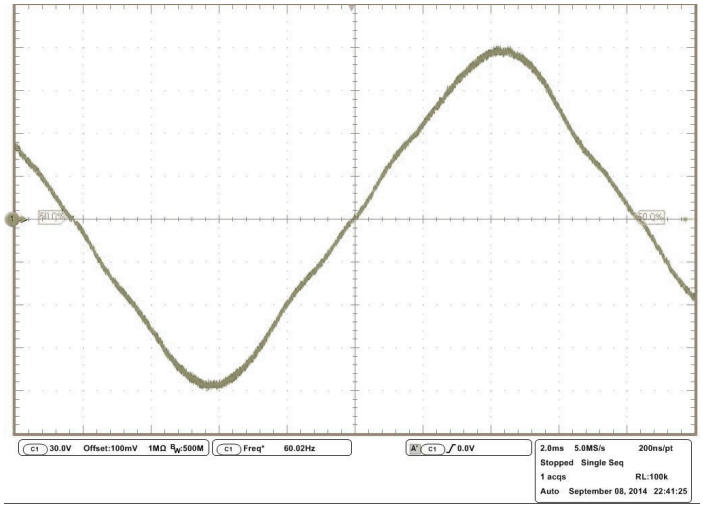
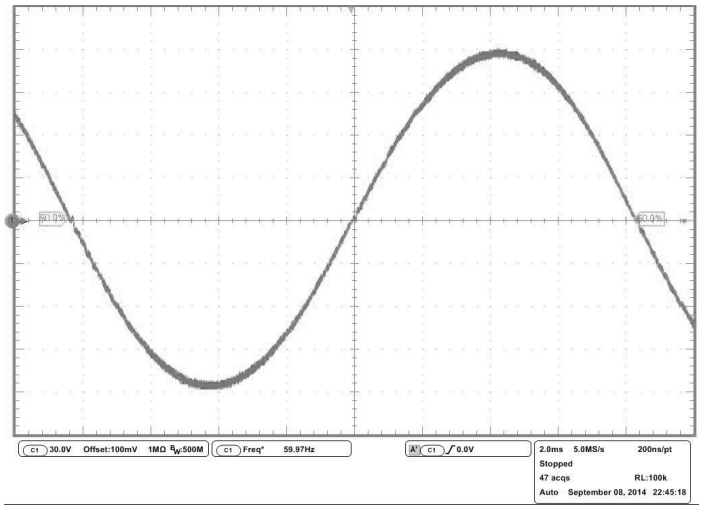


Fig. 38. Injected current in grid connection mode at steady-state with DMS and SLDMS.

The introduced SLDMS is implemented on experimental prototype too. Both SLDMS and DMS are tested under similar conditions and the controller coefficients are tuned to obtain a stable start-up and steady state results for both. The experimental steady state waveforms are shown in Fig. 39(a) for DMS and in Fig. 39(b) for SLDMS. As evident from these results SLDMS has less distortion in comparison to DMS. The experiments are for 30V input voltage and 120V peak output voltage, and while THD of 5% is obtained with DMS, the THD of 1.6 is obtained for SLDMS.



(a)



(b)

Fig. 39. Experimental output waveforms of DMCI with (a) DMS and (b) SLDMS. Horizontal axes are 2.0ms/div and Vertical axes are 30V/div.

F. Conclusions

This chapter describes DMS for DMCI and compares the mechanism and performance of the DMS-based DMCI to that of a prior-art CMS-based DMCI. An experimental hardware prototype was developed for the DMCI to validate and compare the results obtained using the two modulation schemes focusing on energy-conversion efficiency, device rating, output-voltage distortion, and transient response of the inverter. It has been found that DMS, which leads to topological switching of the DMCI, yields significant improvement in efficiency of the inverter compared to that obtained using CMS. This is because DMS eliminates the pathway for circulating reactive power in the DMCI. For the same reason, the reduction in the voltage rating of the DMCI switches is also found to be significant using DMS.

With regard to the THD of the output voltage of the DMCI, CMS demonstrated better results compared to DMS for the inverter when the inverter was operated under open-loop control. The DMS-based DMCI has a better dynamic response because of the reduced order of the topological control system; however, the DMS-based DMCI has wide range of nonlinearity in its dc-voltage gain, which yields higher THD. Consequently, a closed-loop control for the DMCI-based on harmonic compensation was designed and the experimental results obtained using DMS demonstrated a marked improvement in the THD of the inverter output voltage. The slightly slower response of the DMS-based DMCI is due to the fact that a higher-order PR based harmonic compensation for the closed-loop controller is needed that reduces the control bandwidth. To address this issue, work is currently underway on an optimal controller that promises to address this tradeoff between steady-state and transient performances more effectively.

A overall qualitative comparison between the DMS- and CMS-based operations of the DMCI, as implemented currently, indicates that the DMS based operation of the DMCI has the potential to yield relatively higher saving in the power stage due to the reduced requirements of the device breakdown-voltage, heat-sinking, and power-handling. However, the DMS-based control scheme, in contrast to the CMS-based control scheme, yields a relatively higher complexity for control implementation.

Chapter 3

MODULATION SCHEME FOR DIFFERENTIAL-MODE THREE PHASE ĆUK INVERTER

A. Differential-Mode Three-Phase Ćuk Inverter (DTCI)

As photovoltaic, batteries, and other renewable/ alternative power sources continue their rapid growth, inverters are getting increasingly important both economically and environmentally. Three-phase differential-mode inverters are single-stage inverters, which have potential to reduce the number of devices and cost with higher power density. Among such inverter topologies, the differential-mode three-phase Ćuk inverter (DTCI) has some advantage over other topologies, such as fewer switches, bidirectional power flow capability, and galvanic isolation. It is a promising configuration for renewable-/alternative-energy applications with isolated and non-isolated topological realizations. This chapter describes the isolated DTCI as re-illustrated in Fig. 11.

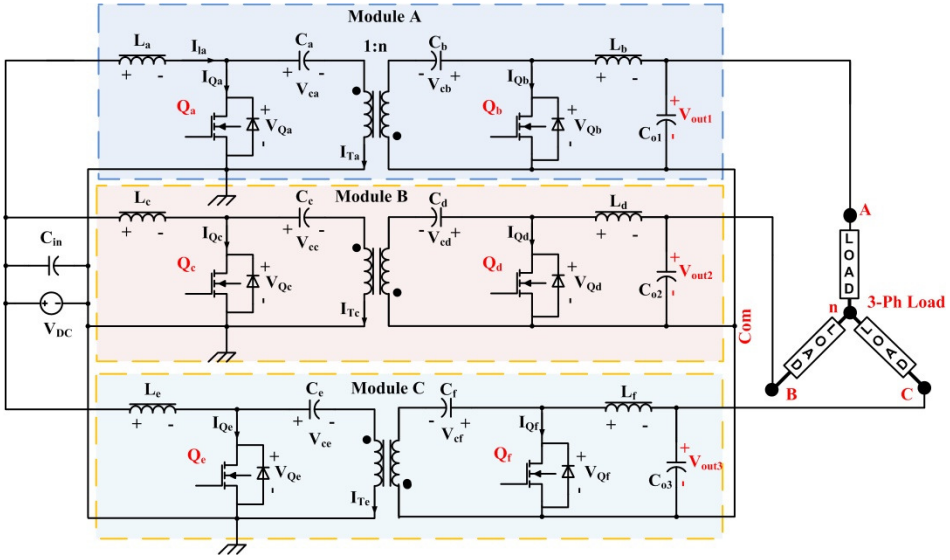


Fig. 11. Illustration of the DTCI topology, which comprises three modules (Module A, Module B and Module C).

The CMS, which was introduced originally for the DTCI, activates all of the three modules of the DTCI. This modulation increases the circulating power in modules and hence increases power loss. This Dissertation introduces a discontinuous modulation scheme (DMS) for the DTCI. DMS deactivates one module at a time leading to

discontinuous operation of modules. This chapter outlines DMS and its implementation with a proper control scheme. The implementation of DMS is straight forward and precludes the need for complex modulation schemes. The experimental open-loop and closed-loop results of the DTCI using CMS and DMS are provided along with a comparison of their respective performances. It is shown that, the DMS reduces the circulating power in DTCI and hence mitigates the inverter losses aside from reducing the voltage ratings of the devices also are reduced with the DMS for the same reason. DTCI has nonlinear voltage-gain with both types of modulations. It has been demonstrated that, feed-forwarding the input voltage along with static-linearization method is a pathway for getting lower distortion.

B. Modulation Schemes for the Differential-Mode Three-Phase Ćuk Inverter (DTCI)

In this section we first present the CMS for completeness of the discussion. The power flow mechanism will be presented to point to the motivation for searching another modulation technique. Then, the DMS will be proposed as a way to reduce the circulation power. It helps to mitigate part of losses and to reduce the ratings of the active devices. Its implementation on a digital control processor is also easy as it does not involve complex control algorithms.

1. Continuous Modulation Scheme (CMS)

The line voltages of the inverter (V_{AB}, V_{BC}, and V_{CA}) are calculated by subtraction of output terminal voltages (V_{out1}, V_{out2} and V_{out3}). Based on that, the normalized static line-voltage gain relations can be defined as follows:

$$\begin{cases} g_{AB} = \frac{V_{AB}}{n\times V_{DC}} = g_A - g_B = \frac{V_{out1}}{n\times V_{DC}} - \frac{V_{out2}}{n\times V_{DC}} = \left(\frac{D_a}{1-D_a} - \frac{D_c}{1-D_c}\right) \\ g_{BC} = \frac{V_{BC}}{n\times V_{DC}} = g_B - g_C = \frac{V_{out2}}{n\times V_{DC}} - \frac{V_{out3}}{n\times V_{DC}} = \left(\frac{D_c}{1-D_c} - \frac{D_e}{1-D_e}\right) \\ g_{CA} = \frac{V_{CA}}{n\times V_{DC}} = g_C - g_A = \frac{V_{out3}}{n\times V_{DC}} - \frac{V_{out1}}{n\times V_{DC}} = \left(\frac{D_e}{1-D_e} - \frac{D_a}{1-D_a}\right) \end{cases} \quad (19)$$

where D_a through D_e are duty cycles of switches Q_a through Q_e , respectively, V_{DC} is the dc input voltage and n is turns ratio of the transformers. The method of modulation that suggested by [51] is to generate three sinusoidal waveforms with 120 degree phase-shift at the output terminals of the DTCI modules. The output voltages of the modules are unipolar, thus dc offset is added to the sinusoidal waveforms. The dc offset voltages, assuming they are

equal for all phases, cancel out when line voltages are considered. So, the normalized phase-voltage gains (g_A, g_B and g_C) are defined by (20) in CMS-based DTCI. Line voltages are obtained by (21), in which g^* is normalized peak phase-voltage gain, ω is angular line frequency and γ is represents an arbitrary initial phase.

$$\begin{cases} g_A = g^*(1+\sin(\omega t+\gamma)) \\ g_B = g^*(1+sin(\omega t-\frac{2\pi}{3}+\gamma)) \\ g_C = g^*(1+sin(\omega t-\frac{4\pi}{3}+\gamma)) \end{cases} \tag{20}$$

$$\begin{cases} V_{AB} = \sqrt{3}n \times V_{DC} \times g^* \sin(\omega t+\frac{\pi}{6}+\gamma) \\ V_{BC} = \sqrt{3}n \times V_{DC} \times g^* \sin\left(\omega-\frac{\pi}{2}+\gamma\right) \\ V_{CA} = \sqrt{3}n \times V_{DC} \times g^* \sin(\omega t-\frac{7\pi}{6}+\gamma) \end{cases} \tag{21}$$

This modulation is called CMS because the power flows continuously in all modules. In order to understand the effect of modulation on the power loss, the flow of power in the modules is investigated next. It is shown that, using CMS, reactive power flows in modules even in the case of pure resistive load.

Assuming that the three-phase load is resistive, the output currents of the modules are in synchronism with their respective phase voltage as captured by (22):

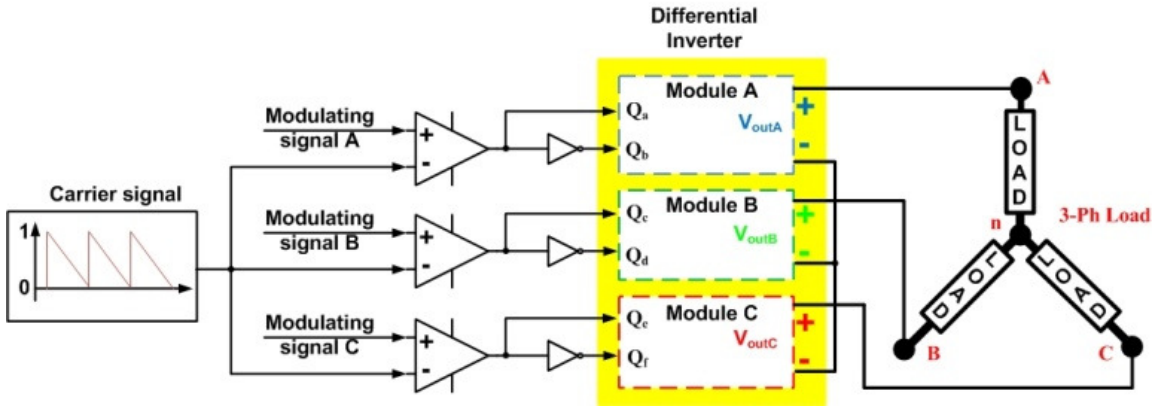
$$\begin{cases} I_A = \frac{n\times V_{DC}\times g^*}{R}\sin(\omega t+\gamma) \\ I_B = \frac{n\times V_{DC}\times g^*}{R}\sin(\omega t-2\pi/3+\gamma) \\ I_C = \frac{n\times V_{DC}\times g^*}{R}\sin(\omega t-4\pi/3+\gamma) \end{cases} \tag{22}$$

where R is the load resistance. The instantaneous power of module (p_A, p_B or p_C) is the multiplication of the respective phase voltage and the phase current as shown in (23):

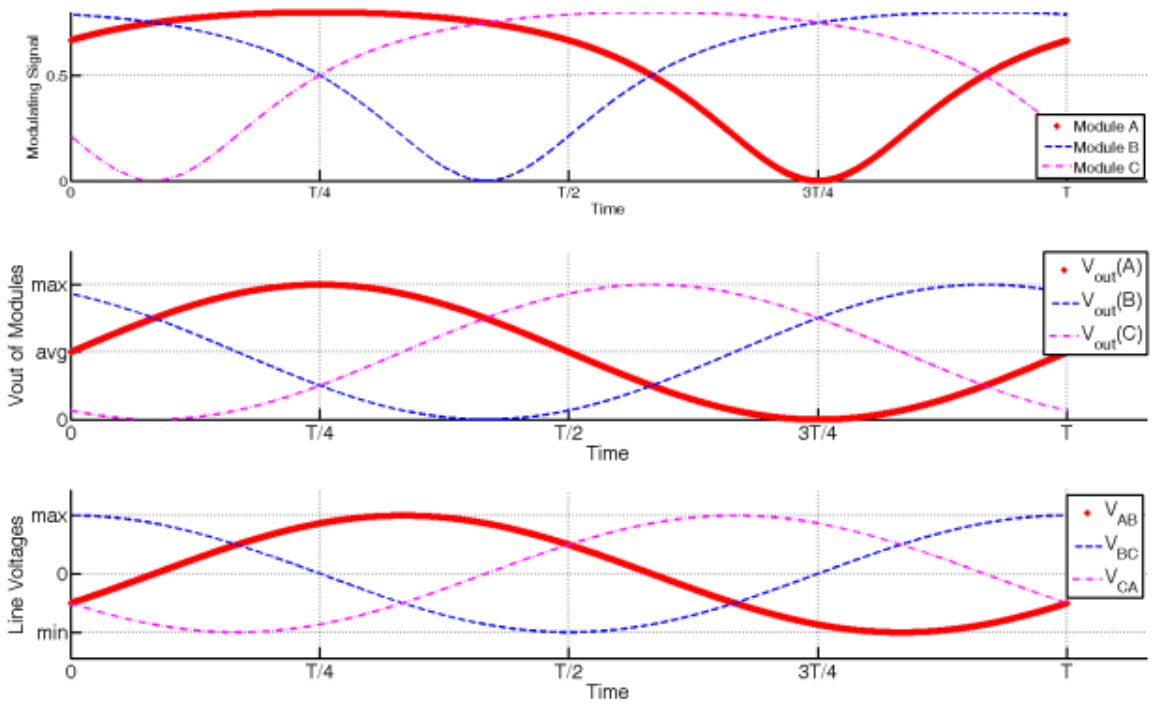
$$\begin{cases} p_A = \frac{(n\times V_{DC}\times g^*)^2}{R}[\sin^2(\omega t+\gamma)+\sin(\omega t+\gamma)] \\ p_B = \frac{(n\times V_{DC}\times g^*)^2}{R}[\sin^2\left(\omega t-\frac{2\pi}{3}+\gamma\right)+\sin\left(\omega t-\frac{2\pi}{3}+\gamma\right)] \\ p_C = \frac{(n\times V_{DC}\times g^*)^2}{R}[\sin^2\left(\omega t-\frac{2\pi}{3}+\gamma\right)+\sin\left(\omega t-\frac{2\pi}{3}+\gamma\right)] \end{cases} \tag{23}$$

Fig. 40 illustrates the simple implementation of CMS-based on DTCI and it also shows the waveforms of the modulating signals, output terminal voltages and line voltages. Fig. 41 shows the power waveforms of the three

modules of the DTCI operating with CMS during a complete line cycle; they are derived using (23). The piecewise power flow direction diagrams are also illustrated. It can be seen that the power flow is positive during half a cycle for modules, which implies that, power is transmitted from source to load with a peak of $2 \times \frac{(n \times V_{DC} \times g^*)^2}{R}$. During the other half of the same line cycle, a small amount of negative power flows, which reaches the peak of $-\frac{1}{4} \times \frac{(n \times V_{DC} \times g^*)^2}{R}$ at two points. This implies that during this time, a part of power which has been transmitted to the load side by other module(s) returns to the source. So it is evident that, instantaneous power changes direction, which indicades the presence of circulating (or reactive) power. The reactive power is not desirable because it increases the peak power which leads to higher peak voltage or higher current stress on the components; further, the conduction and switching loses increase as well. The reactive power of the CMS-based DTCI will be mathematically calculated and it will be compared with the corresponding results obtained using DMS; this will be illustrated in Chapter C.



(a)



(b)

Fig. 40. (a) Illustration of realization of the CMS for the DTCI. (b) Illustration of the modulating signal of the primary side switches (duty cycle), terminal voltages (V_{out1}, V_{out2} *and* V_{out3}) of Modules A, B and C, and line voltages (V_{AB}, V_{BC} and V_{CA}) of the DTCI using the CMS.

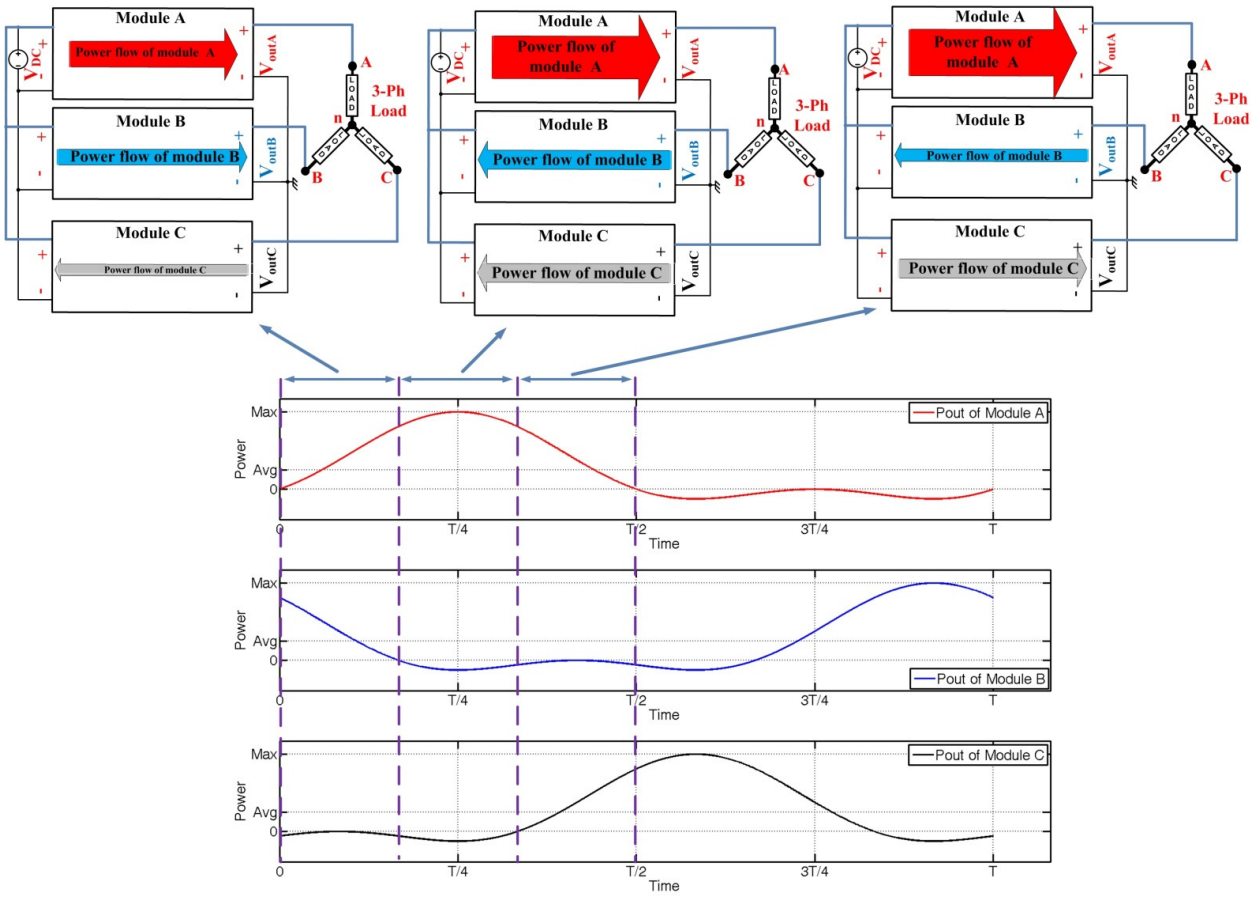


Fig. 41. Instantaneous output powers waveforms of the DTCI when the DTCI is operating with CMS, and the piecewise power flow illustration of modules in half a line cycle.

2. Discontinuous Modulation Scheme (DMS)

The CMS was originally introduced for the low-power amplifiers of analog circuits [51] with limited focus on power loss. For the DTCI, and as evident from the illustration in Fig. 41, the modulation scheme needs to be revised with enhanced emphasis on reducing circulating power and associated power loss. Therefore, the major motivation for development of a new scheme is to mitigate the circulating power. A closer scrutiny of (23) reveals that, because the first term is squared and is always positive, the negative portion of the power is caused by the second expression inside the bracket. This expression is originated from the dc offset voltage at the output terminal voltages. Thus any reduction in the dc-offset voltage reduces the circulating power the device voltage-stress.

The reason for adding such a dc-offset voltage to the phase voltages is to meet the voltage polarity restriction of DTCI modules. Fig. 42 shows the output terminal voltages of any ideal differential-mode inverter modules, which are assumed to be bipolar; and no offset voltage is added to any module of this inverter consequently. V_{min} is the

smallest voltage between three terminal voltages (V_{out1}, V_{out2}, and V_{out3}) of the above mentioned ideal inverter, as highlighted in Fig. 42.

In the case of DTCI an offset voltage is needed to be added to the terminal voltages to keep them positive. But the point is that, the offset voltage does not need to be a dc value and it can vary with time. The idea is to add a variable-offset voltage, which is equal to absolute value of the voltage V_{min} at each instant of the line cycle. It is noted that if the unique offset voltage is added to the all three terminal voltages at a time, it will be canceled out at the line voltages of DTCI. The advantage of using this minimized variable-offset voltage is the reduction of reactive power of DTCI as can be inferred by (23). The V_{min} is identical to either of the phases at each 120 degrees; as a result, one terminal voltage equals to zero during a 120 degrees interval. The positive terminal voltages are always guaranteed with offset voltage minimized at each instant of the time, by using the described offset-voltage.

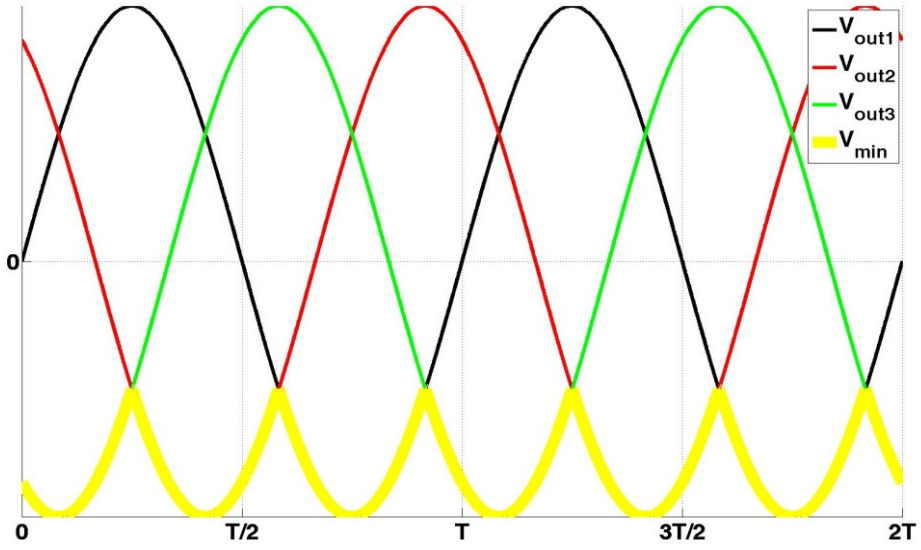


Fig. 42. The three phases of the output terminal voltages of ideal DTCI assuming no offset. The yellow curve shows the minimum of the three phase voltages.

The output terminal voltage will be zero during the 1/3rd of a line cycle with the proposed method. As such, this modulation scheme is referred to as discontinuous modulation scheme (DMS). Equation (24) shows the mathematical presentation of output terminal voltages of DMS-based DTCI

$$\begin{cases} V_{out1} = n \times V_{DC} \times g^{*}[\sin(\omega t + \gamma) + |V_{min}|] \\ V_{out2} = n \times V_{DC} \times g^{*}\left[\sin\left(\omega - \frac{2\pi}{3} + \gamma\right) + |V_{min}|\right] \\ V_{out3} = n \times V_{DC} \times g^{*}\left[\sin\left(\omega t - \frac{4\pi}{3} + \gamma\right) + |V_{min}|\right] \end{cases} \quad (24)$$

in which V_{min} is defined by (25):

$$V_{min} = \begin{cases} \sin(\omega t - \frac{4\pi}{3} + \gamma) & if \ -\frac{\pi}{6} + 2\pi m < \omega t + \gamma < \frac{\pi}{2} + 2\pi m \\ \sin\left(\omega t - \frac{2\pi}{3} + \gamma\right) & if \ \frac{\pi}{2} + 2\pi m < \omega t + \gamma < \frac{7\pi}{6} + 2\pi m \\ \sin(\omega t + \gamma) & if \ \frac{7\pi}{6} + 2\pi m < \omega t + \gamma < \frac{11\pi}{6} + 2\pi m \end{cases} \quad (25)$$

where m is an integer.

Fig. 43 shows the ideal waveforms of the modulating signals, output terminal voltages and line voltages of the DMS-based DTCI. Even though the output terminal voltages do not look like sinusoidal waveforms and have discontinuity, the line (i.e., phase to phase) voltages are clean sinusoidal waveforms. Fig. 44 illustrates the power flow direction along with power waveforms. The power varies between the positive peaks of $1.616 \times \frac{(n \times V_{DC} \times g^{*})^2}{R}$ and negative peaks of $-0.116 \times \frac{(n \times V_{DC} \times g^{*})^2}{R}$. Comparing the results for DMS with the same results for CMS shows DMS has smaller positive and negative peaks at the first place.

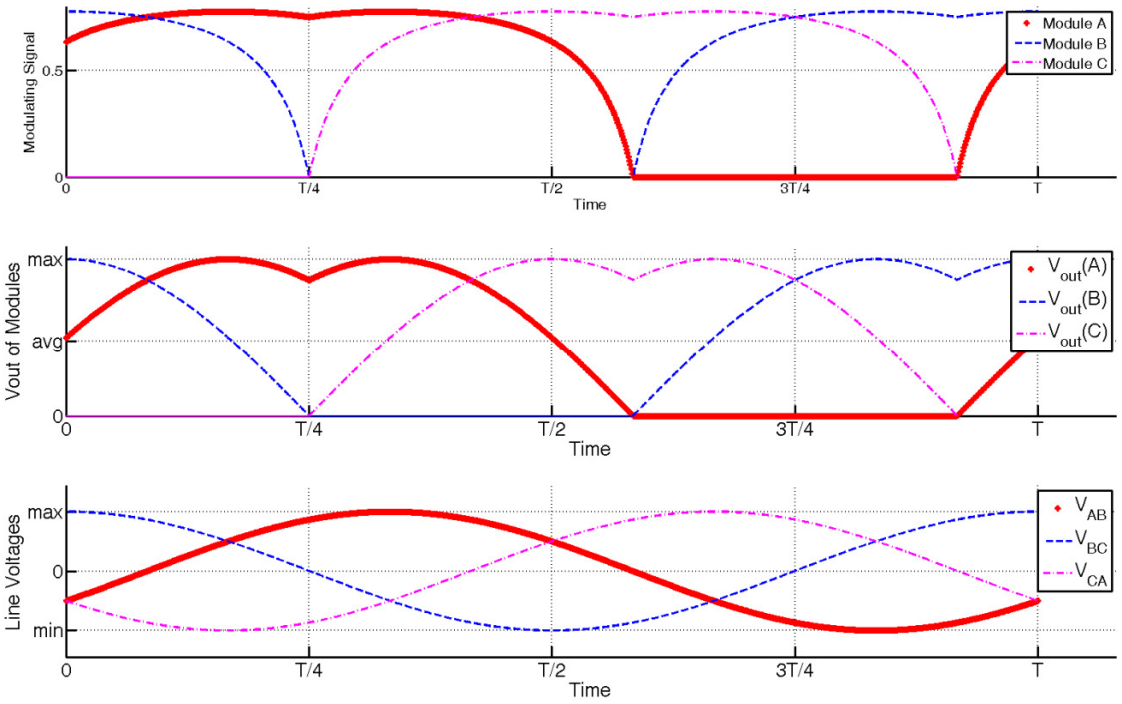


Fig. 43. Illustration of the modulating signal (representing the duty cycle) of the primary side switches, terminal voltages (V_{out1}, V_{out2} *and* V_{out3}) of Modules A, B and C, and line voltages (V_{AB}, V_{BC} and V_{CA}) of the DMS-based DTCI.

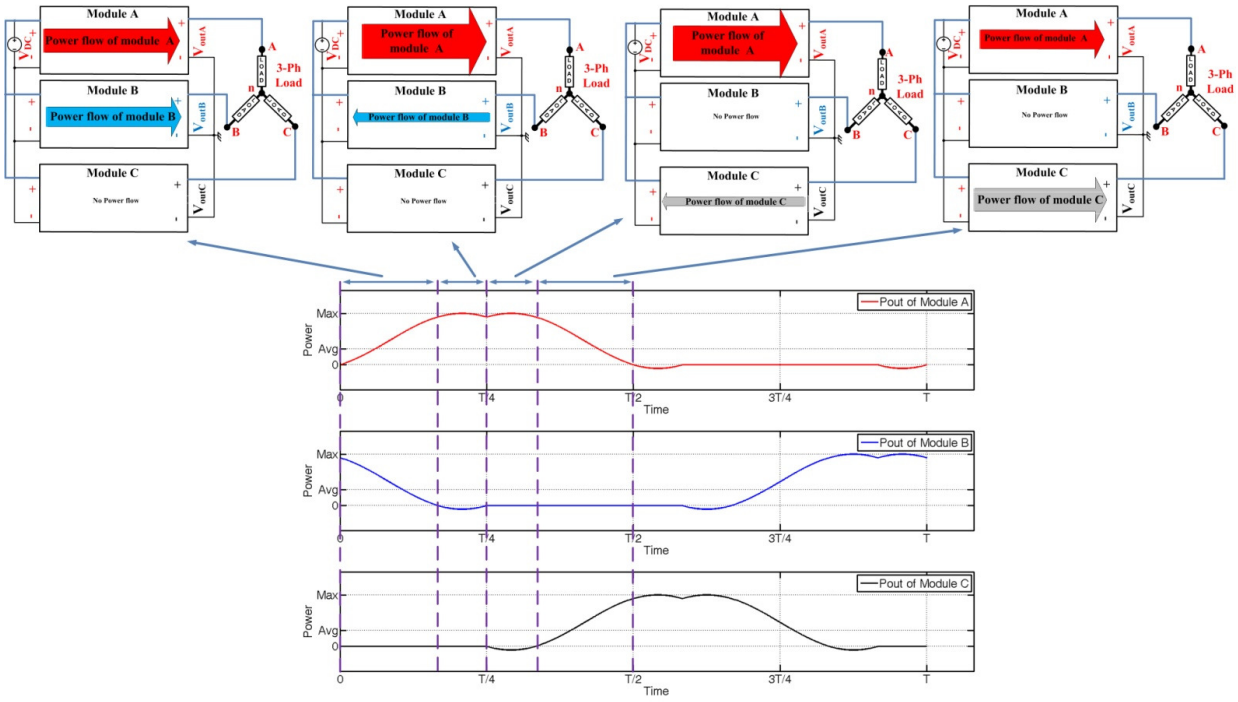


Fig. 44. Instantaneous output powers waveforms of the DMS-based DTCI, and the piecewise power-flow illustration of the three modules during the first half of a line cycle.

C. Analysis

This section provides the theoretical evaluation and analysis of the CMS and the DMS assuming ideal switches. Section E provides validating experimental results.

1. Circulating Power

As explained in Section B, both modulations yields circulating power but, the magnitudes of the circulating power are different. In order to have a base for measurement and comparison of the circulating power in CMS- and DMS-based DTCI, the reactive power concept, referred to as Fryze's definition and defined in [61] will be used. Because each of the nominal modules of the DTCI has identical topology, only one module (i.e., Module A) is selected here for the calculation of the active and reactive power of the DTCI. Fryze's definition of reactive power is a comprehensive definition, which also encompasses nonlinear circuits the following equations can be used to capture the reactive power of Module A:

$$P_A = < p_A(t) >_{avg} = \frac{1}{T}\int_0^T V_{out1}(t) \times I_A(t)dt \tag{26}$$

$$S_A^2 = P_A^2 + Q_A^2 = V_{out1}^2(rms) \times I_A^2(rms) = \frac{1}{T}\int_0^T V_{out1}^2(t)dt \times \frac{1}{T}\int_0^T I_A^2(t)dt. \tag{27}$$

where $p_A(t)$ is the instantaneous power, P_A is the active power, Q_A is the reactive power, S_A is the apparent power, and V_{out1} and I_A are output terminal voltage and phase current of Module A. Using (26) and (27), the ratio of the reactive to the active power can be derived as follows:

$$\frac{Q_A}{P_A} = \sqrt{\frac{\frac{1}{T}\int_0^T V_{out1}^2(t)dt \times \frac{1}{T}\int_0^T I_A^2(t)dt}{[\frac{1}{T}\int_0^T V_{out1}(t) \times I_A(t)dt]^2} - 1}\,. \tag{28}$$

Now assuming a load with unity-power-factor and a negligible total harmonic distortion (THD) of the load voltage and the load current, we obtain the following relations for the CMS-based DTCI:

$$\begin{cases} I_A = \frac{n \times V_{DC} \times g^*}{R}\sin(\omega t + \gamma) \\ V_{out1} = g_A \times n \times V_{DC} = n \times V_{DC} \times g^*(1 + \sin(\omega t + \gamma)) \end{cases} \tag{29}$$

Substituting V_{out1} and I_A from (29) into (28) and simplifying the resultant expression one obtains:

$$\frac{Q_A}{P_A}(\text{CMS}) = \sqrt{\frac{(n\times V_{DC}\times g^*)^2 \int_0^T (1+\sin(\omega t+\gamma))^2 dt \times (\frac{n\times V_{DC}\times g^*}{R})^2 \int_0^T \sin^2(\omega t+\gamma) dt}{\frac{(n\times V_{DC}\times g^*)^4}{R^2}[\int_0^T (1+\sin(\omega t+\gamma))\times \sin(\omega t+\gamma) dt]^2} - 1} = \sqrt{\frac{\frac{3}{2}\times\frac{1}{2}}{[\frac{1}{2}]^2} - 1} = \sqrt{2} = 1.414 \qquad (30)$$

It is noted that (30) is valid only for a unity-power-factor load and for a lossless CMS-based DTCI. It shows that, the ratio of the reactive power to the active power is constant and do not vary with peak voltage gain of inverter. Also note that, the reactive power of DTCI is due to the nonlinear nature of inverter and it is not caused by any passive components of the topology.

Similar calculation is carried out for DMS-based DTCI to compare the results with those obtained using CMS-based DTCI. Current IA is obtained in (22) and Vout1 for DMS-based DTCI is described by (24) and (25). If these values are substituted into (28), one obtains the ratio of the reactive power to the active power as follows:

$$\frac{Q_A}{P_A}(\text{DMS}) = \sqrt{\frac{(1+\frac{3\sqrt{3}}{8\pi})\times\frac{1}{2}}{[\frac{1}{2}]^2} - 1} = \sqrt{1.413} = 1.188 \qquad (31)$$

This ratio is smaller than that obtained for the CMS-based DTCI. By dividing these ratios we will have the circulating power ratio of CMS to DMS, which is $\frac{Q_{CMS}}{Q_{DMS}} = 1.19$. It means that CMS has 19% more circulating power than DMS. The significant effect of this reduction on inverter efficiency will be shown by experimental results in Section E.

2. Device Rating

The other advantage of using DMS over CMS is to reduce the stress on some of the components. The mathematical comparison of the peak voltage of the active components is provided below. The simulation results are also provided to compare the voltage and current peaks on other components.

Fig. 45 compares the output terminal voltage of phase A (V_{out1}) of DTCI operating with CMS and DMS under the equal line voltage levels. The peak voltage of V_{out1}, (i.e., by V_{out1}^*), is higher for DTCI operating with CMS ($V_{out1}^*(CMS)$). Using (29) $V_{out1}^*(CMS)$ is found to be $2nV_{DC}g^*$, while the peak line-voltage is $\sqrt{3}nV_{DC}g^*$. In order to

obtain V_{out1}^{*} for DMS, one of the phase voltages should be calculated by substituting (25) into (24) as demonstrated in (32) for phase A:

$$V_{out1} = \begin{cases} \sqrt{3}nV_{DC}g^{*}\sin(\omega t - \frac{\pi}{6} + \gamma) & if\ -\frac{\pi}{6} + 2\pi m < \omega t + \gamma < \frac{\pi}{2} + 2\pi m \\ \sqrt{3}nV_{DC}g^{*}\sin\left(\omega t + \frac{\pi}{6} + \gamma\right) & if\ \frac{\pi}{2} + 2\pi m < \omega t + \gamma < \frac{7\pi}{6} + 2\pi m \\ 0 & if\ \frac{7\pi}{6} + 2\pi m < \omega t + \gamma < \frac{11\pi}{6} + 2\pi m \end{cases} \quad (32)$$

As evident from (32), the peak output terminal voltage of DTCI operating with DMS ($V_{out1}^{*}(DMS)$) equals $\sqrt{3}nV_{DC}g^{*}$ and the line voltage matches that obtained using the DCMS-based DTCI. Equation (33) summarizes these results:

$$\begin{cases} V_{out1}^{*}(\text{CMS}) = 2nV_{DC}g^{*}, \\ V_{out1}^{*}(\text{DMS}) = \sqrt{3}nV_{DC}g^{*} \end{cases} \quad (33)$$

Following Fig. 11, the off-state voltage of each device in the module (V_{Qa}, V_{Qb}) is given by the following set of expressions:

$$\begin{cases} V_{Qa} = V_{ca} + \frac{V_{cb}}{n} \\ V_{Qb} = nV_{ca} + V_{cb} \end{cases}. \quad (34)$$

where V_{ca} and V_{cb} are the voltages across the blocking capacitors C_a and C_b, respectively. In the steady state, using $V_{ca} = V_{DC}$ and $V_{cb} = V_{out1}$, (34) yields:

$$\begin{cases} V_{Qa} = V_{DC} + \frac{V_{out1}}{n} \\ V_{Qb} = nV_{DC} + V_{out1} \end{cases}. \quad (35)$$

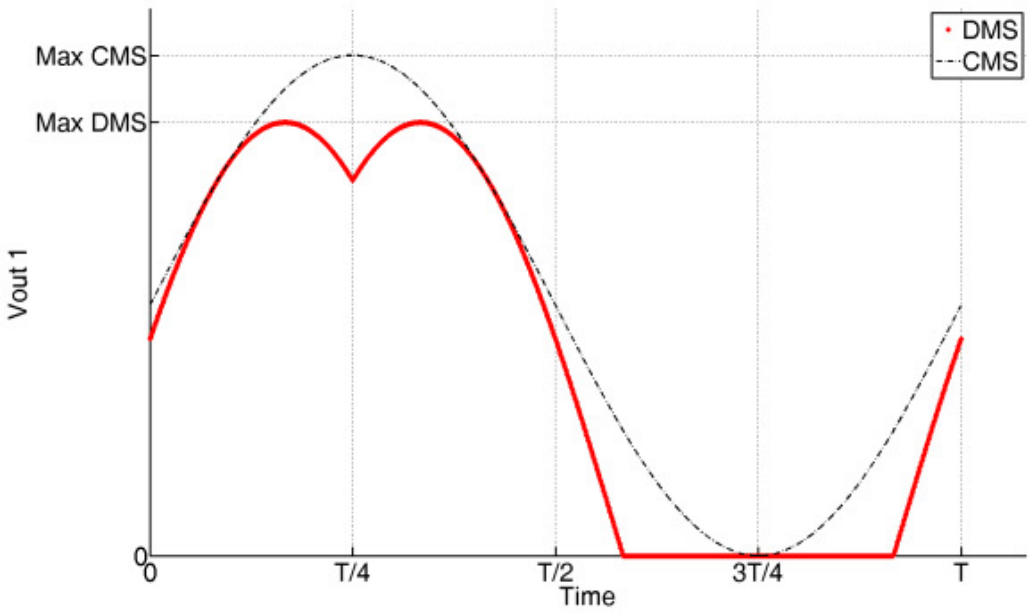


Fig. 45. Comparison of the output terminal voltages of DTCI operating with CMS and DMS. The CMS-based DTCI results in higher peak for the output terminal voltage; even though the line voltage of the DTCI remains the same for both cases.

The voltage ratings of the devices should be designed for the worst-case condition, which happens at the peak output voltage. The ratio of the peak voltage of either of devices using CMS-based DTCI to the peak voltage of the device with DMS-based DTCI can be obtained by using (33) and (35). This ratio is simplified as a function of peak phase-voltage gain in (36), where V_{Qa}^{*} and V_{Qb}^{*} are peak voltages on primary and secondary switches respectively.

$$\frac{V_{Qa}^{*}(CMS)}{V_{Qa}^{*}(DMS)} = \frac{V_{Qb}^{*}(CMS)}{V_{Qb}^{*}(DMS)} = \frac{V_{DC}+\frac{V_{out1}^{*}(\mathrm{CMS})}{n}}{V_{DC}+\frac{V_{out}^{*}(\mathrm{DMS})}{n}} = \frac{1+2g^{*}}{1+\sqrt{3}g^{*}} \tag{36}$$

It is noted that, (36) does not include any device voltage spike, which is dependent on the load, leakage inductance of the transformer, the off-state voltage of the device, and printed-circuit-board (PCB) layout. As such, the actual peak voltages are slightly higher than (35). Nevertheless, (36) still provides a good approximation for comparison purposes as proved by experimental results in Section E.

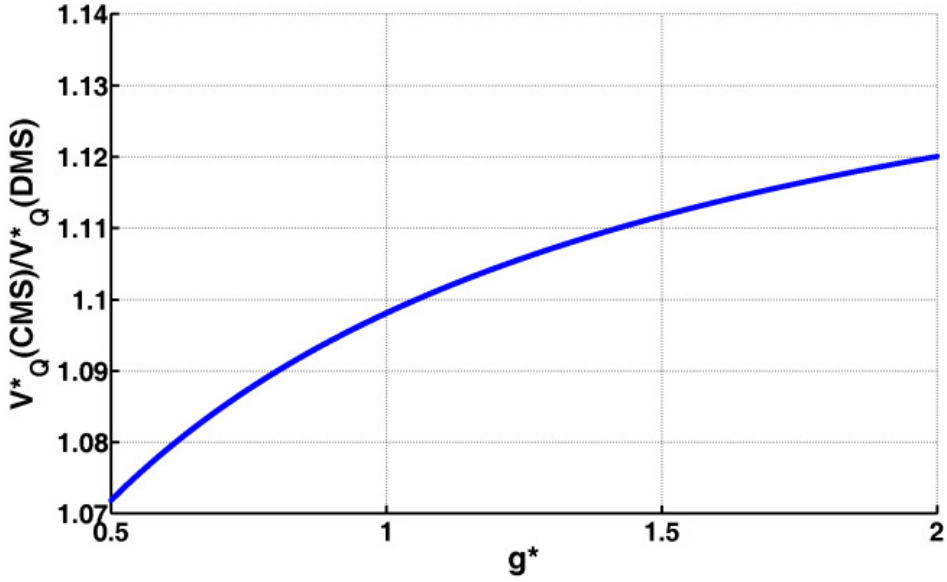


Fig. 46. $V^*_{Qa}(CMS)/V^*_{Qa}(DMS)$ as a function of g^*.

The ratio $V^*_{Qa}(CMS)/V^*_{Qa}(DMS)$ as described by (36) is plotted in Fig. 46. The ratio is always greater than one and the ratio increases with increasing normalized phase-voltage gain. The purpose of the plot is to demonstrate the effect of modulation on reduction of device voltage rating following (36) and is validated using simulation and experimental results later in this chapter.

Fig. 47 shows the (Saber-based) simulation results for the peak drain-to-source voltages of Q_a and Q_b operating with DMS and CMS. These simulations are carried out using circuit parameters that match those of the experimental prototype described in Section E. Using these parameters, the ratios of $V_{Qa}(CMS)/V_{Qa}(DMS)$ and $V_{Qb}(CMS)/V_{Qb}(DMS)$ are found to be 1.11 and 1.06, respectively, for $g^* = 1$, $V_{DC} = 50$ V, $V_{AB} = 120$ V RMS, and an output power (P_{out}) of 500 W. This is found to be close to the theoretically-predicted value as shown in Fig. 46 for $g^* = 1$. DMS also reduces the current rating of the devices. This is evident from the simulation results in Fig. 48, which demonstrates the peak-current waveforms for Q_a and Q_b.

In addition, Fig. 49 shows that, using DMS, a reduction in the voltage of output capacitor (V_{out1}) and blocking capacitor (V_{cb}) or current ratings of input filter inductor (I_{La}) and transformer current (I_{Ta}) of the DTCI is also achieved. Further, all of these results are captured during the positive peak of the output voltage with transformer turns ratio of 2 (i.e., n=2).

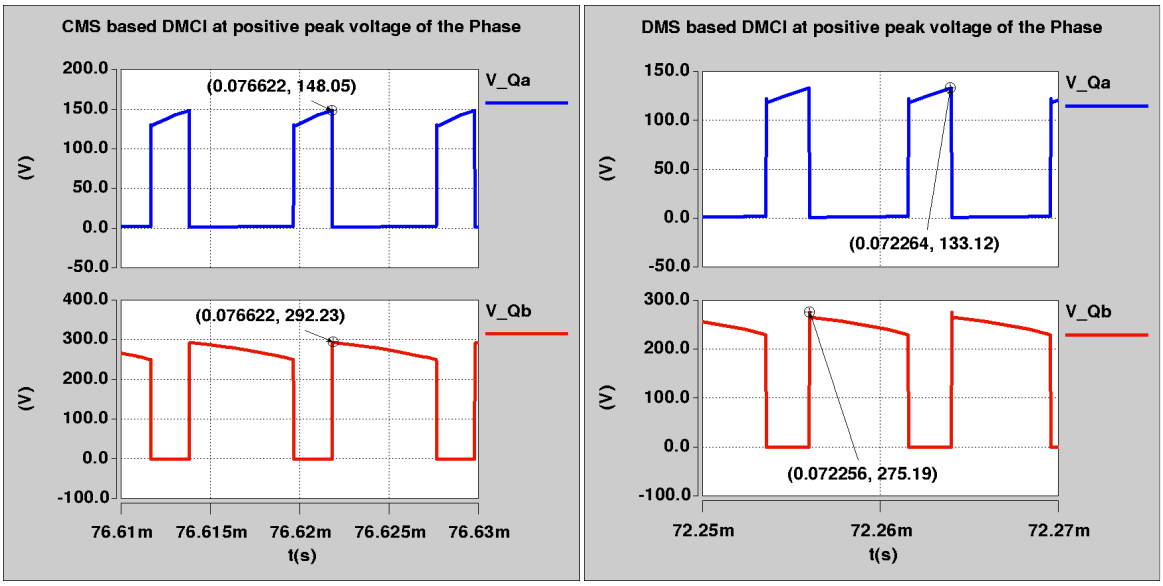


Fig. 47. Simulation results for V_{Qa} and V_{Qb} obtained using CMS (left) and DMS (right) when the output voltage attains the maximum positive value.

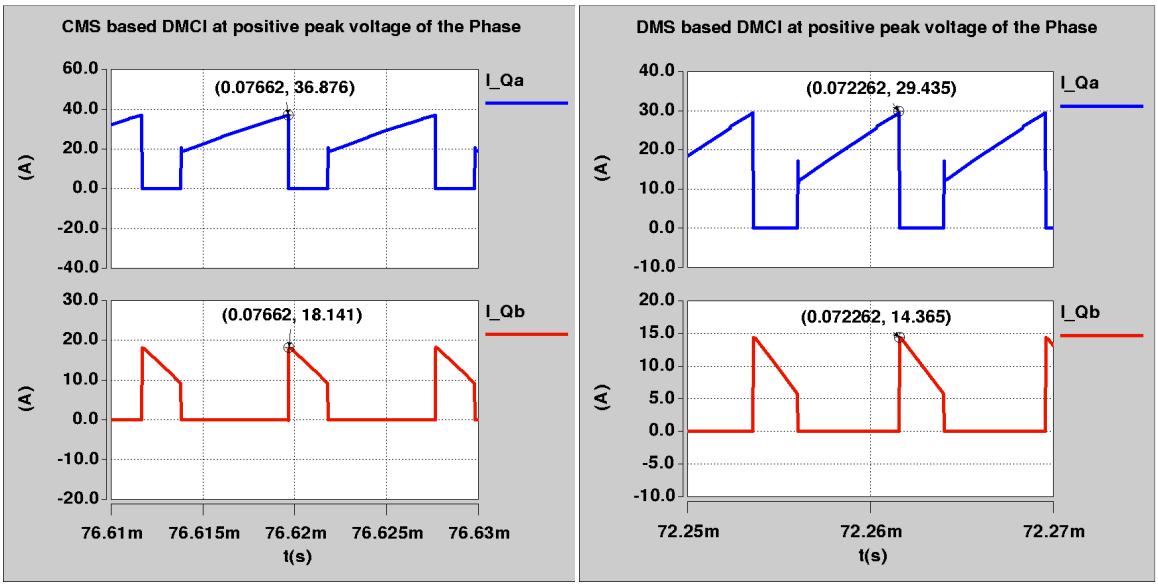
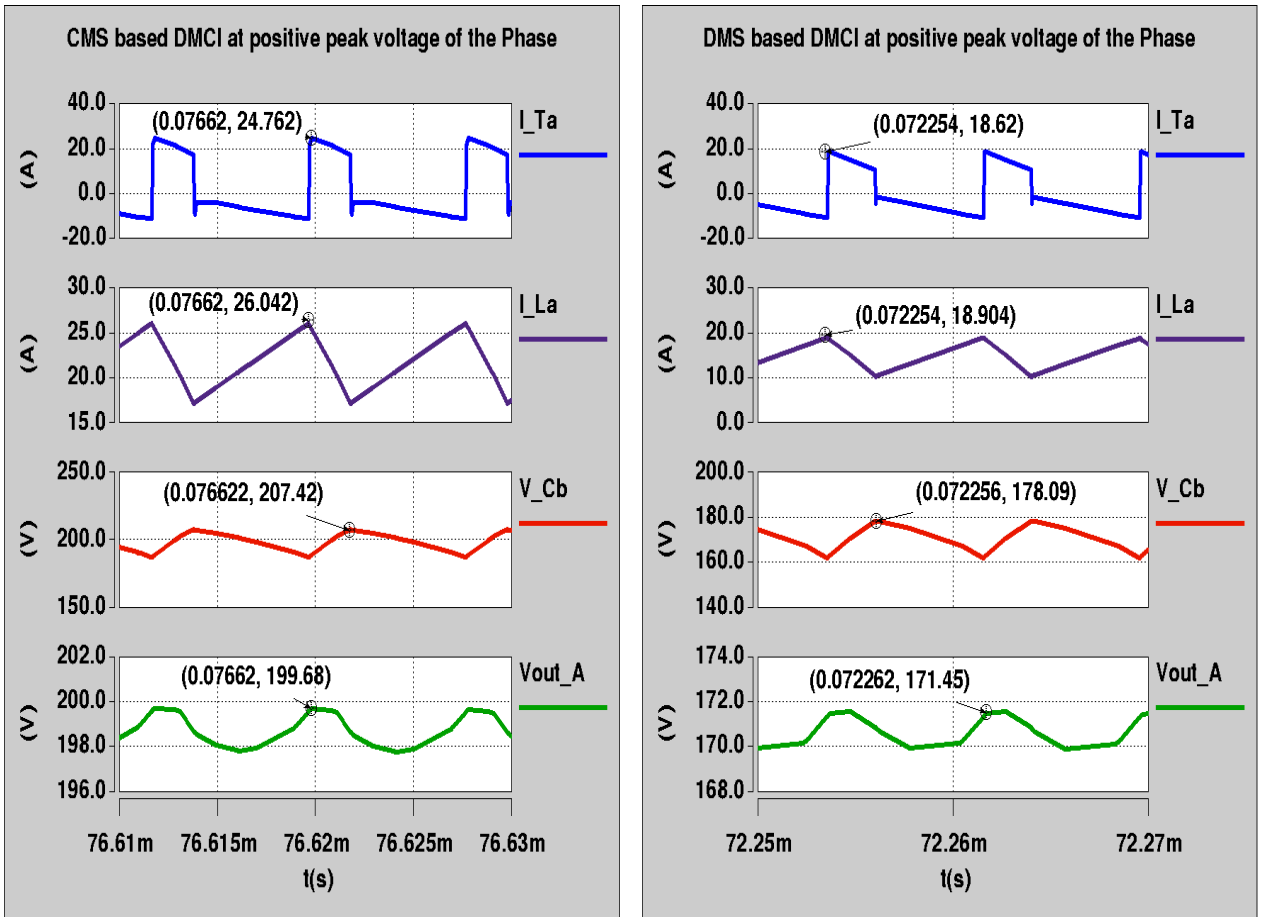


Fig. 48. Simulation results for I_{Qa} and I_{Qb} obtained using CMS (left) and DMS (right) when the output current attains the maximum positive value.



(a) **(b)**

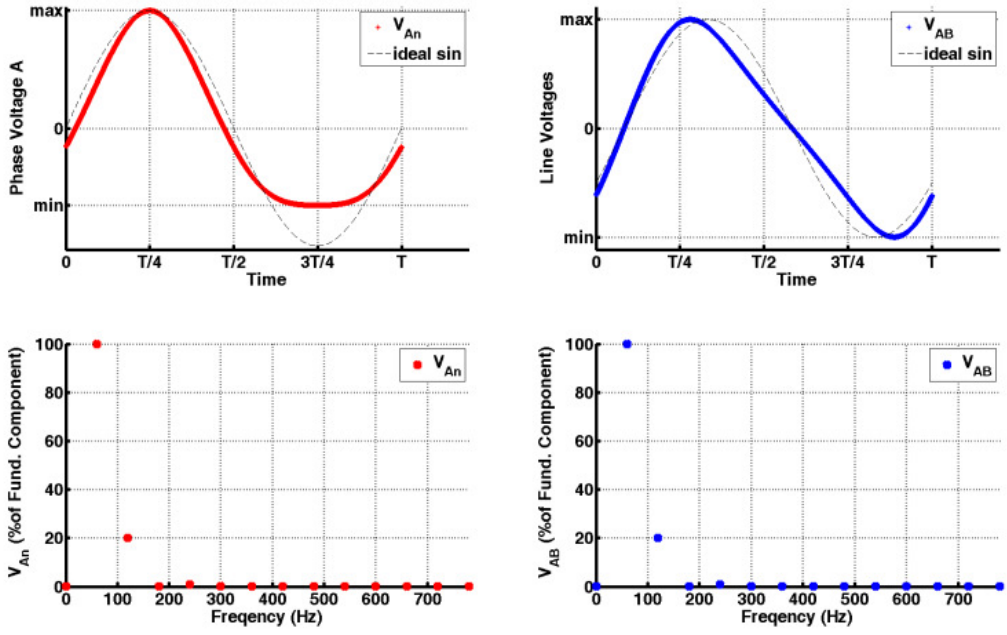
Fig. 49. Simulation results showing V_{outA}, V_{cb}, I_{La}, and I_{Ta} for the DTCI shown in Fig. 11 when the inverter is operated using (a) CMS and (b) DMS and when the output voltage attains the maximum positive value

3. Distortion

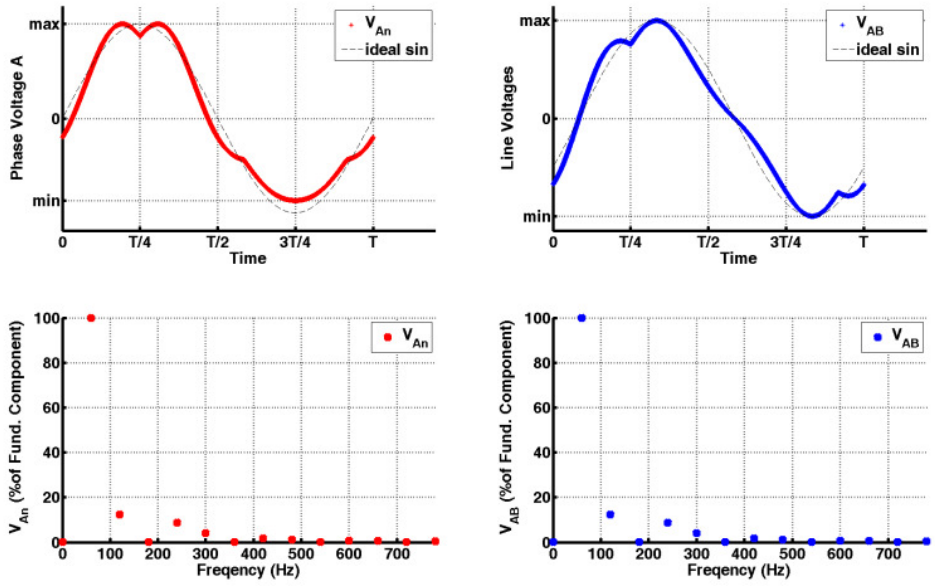
The line-voltage of the DTCI is a nonlinear function of the duty cycle for both CMS and DMS as evident in (19). In order to compare the nonlinearity of the CMS and DMS, open loop sinusoidal modulating signal is applied to DTCI operating with CMS and DMS. The simulation results are provided along with harmonic analysis. Fig. 50 (a) shows phase voltage (V_{An}) and line voltage (V_{AB}) of DTCI operating with CMS while open loop sinusoidal modulating signals are applied. Fig. 50 (b) shows the similar waveforms for DTCI operating with DMS. Both simulations are carried out for line frequency of 60Hz and g*=0.6. Fourier analysis of each waveform are also shown right below each waveform in Fig. 50. These plots show the magnitude of Fourier series coefficients, which are normalized to the magnitude of fundamental-frequency component. As is evident from these results, nonlinear

voltage gain of DTCI causes distorted output but the distortion is different for CMS and DMS. The distortion magnitude also depends on the variation of the duty cycle range, which duty cycle swings during a line cycle. The rang of duty cycle swing is proportional to normalized peak phase-voltage gain (g*).

Fig. 51 shows a similar Fourier series analysis for line voltages versus g*. As expected, magnitudes of the harmonics increase at higher gains, because duty cycle swings over a wider range for CMS- and DMS-based DTCI. Also comparison of CMS and DMS results reveals that DTCI exhibits considerable distortion while operating with CMS and DMS. The distortion of the DTCI operating with CMS appears mostly as second harmonic; however, the harmonic distortion of the DTCI operating with DMS is spread over a wider range of harmonics. Therefore, no matter what type of modulation is used, there should be a mechanism to compensate or overcome the non-linear voltage gain effect. Section D is devoted to discuss this issue and closed loop implementation of the DMS-based DTCI.

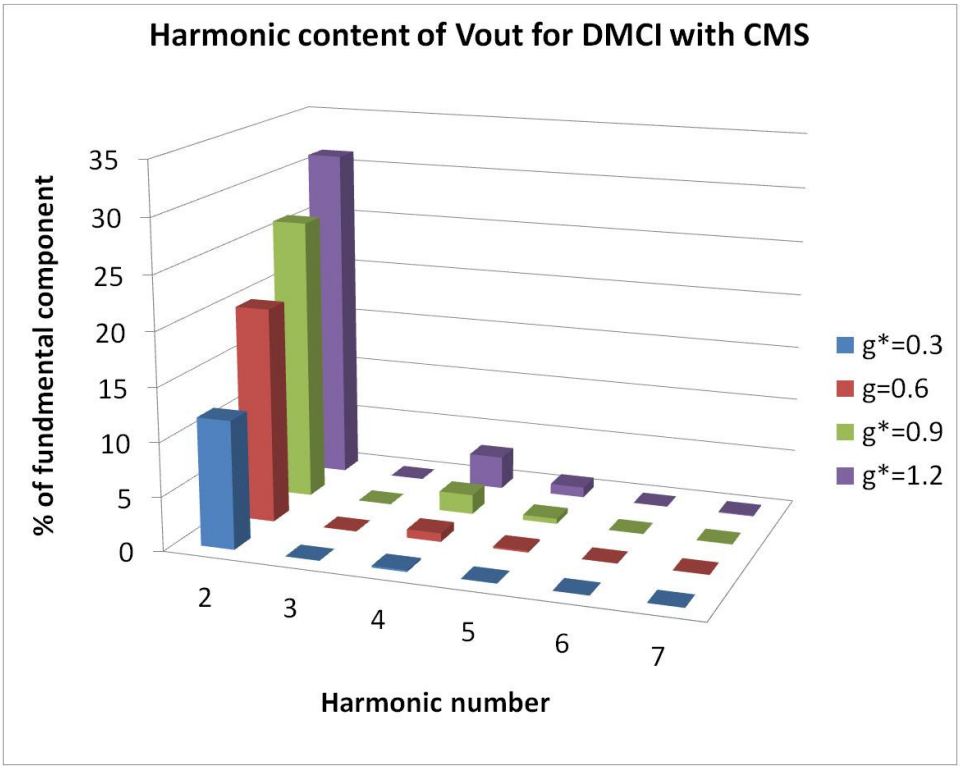


(a)



(b)

Fig. 50. The phase voltage and line voltage of DTCI operating with (a) CMS and (b) DMS, and their normalized magnitude harmonics as a percentage of the magnitude of fundamental-frequency (60Hz) component.



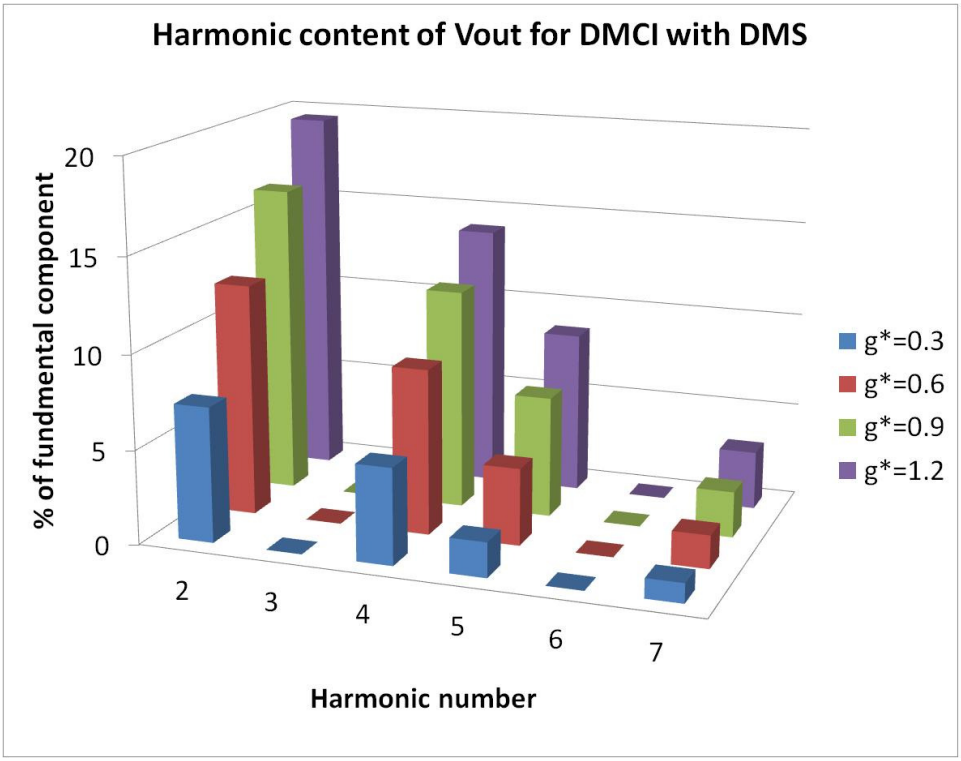


Fig. 51. Harmonic analysis of the line-voltage distortion caused by the nonlinearity in the static voltage-gain of the DTCI operated with CMS (top) and DMS (bottom). Magnitudes of the 2^{ed}, 3rd, 4th, 5th, 6th and 7th harmonics are shown as a percentage of the fundamental-frequency (60-Hz) component magnitude versus peak phase-voltage gain.

D. Non-linearity and closed loop

In Section 3, it is shown that the non-linearity in the voltage gain of the DTCI causes considerable amount of voltage distortion, which needs to be dealt with. Reference [52] uses Harmonic Compensation (HC) method to reduce the THD by eliminating some specific harmonics. The same method has also been adopted generally for single-phase inverters to reduce the THD [55]. However; harmonic compensator reduces the loop gain - band-width. Non-linear compensation method may leads to enhanced transient responses while yielding lower THD [62]. Furthermore, as is evident from Fig. 51, at least 4 harmonics with considerably large magnitudes need to be mitigated using 4 HCs. This implies additional computational overhead for the DSP-based controller and further impact on the transient response/ stability of the system.

The dynamic behavior of DTCI is nonlinear like most of the converters and a proper component selection and control design should be carried out for a practical system. The dynamic model and closed loop controller design

consideration of Ćuk-topology based inverters have been studied extensively in literatures [51], [52], [63]. But a major part of the output voltage distortion is due to non-linear static relation of the DTCI as shown in Fig. 51. It is noted that he distortion results of Fig. 51 are simulated for a simple DTCI without considering dynamics of the system. This Dissertation proposes the proportional resonant (PR) compensator for the DTCI in conjunction with a static nonlinearity compensator along with feed-forward input voltage. The compensator architecture is as shown in Fig. 52.

The reference voltages ($Vref_A$, $Vref_B$ and $Vref_C$) in Fig. 52 represent the voltage reference signals for the three phases. The measured phase-voltages are fed back to close the control loops. Phase voltage (V_{An}, V_{Bn}, or V_{Cn}) is the difference of output terminal voltage of each DTCI module and the mid-point (null point) voltage (V_{null}). Voltage V_{null} can be measured directly by a sensor or can be calculated based on output terminal voltages as obtained in (37) assuming that the three-phase load is symmetrical.

$$V_{null} = \frac{V_{out1}+V_{out2}+V_{out3}}{3} \tag{37}$$

Error signal is fed to the PR compensator and the outputs of the compensators (C_A, C_B, and C_C) are fed to the modulator.

The dc-offset voltage is added to control signal for the implementation of CMS as shown in Fig. 52 (a). Then the resultant signal (i.e., $Gain_A$, $Gain_B$, and $Gain_C$) is applied to linearization block, which is followed by PWM generating block for implementing CMS.

A minimum signal generator block calculates the minimum of three-phase control signals (C_A, C_B or C_C) for implementation of DMS, as is marked with "min" in Fig. 52 (b). This obtained minimum signal (i.e. C_{min}) is subtracted from each of three-phase control signals (C_A, C_B or C_C); the resulting signal (i.e., $Gain_A$, $Gain_B$, and $Gain_C$) is applied to linearization block, which is followed by PWM generating block for implementing DMS. It is noted that the PWM generator block generates pulses with constant frequency and variable duty cycle; and linearization block is explained next.

If gain signals (i.e., $Gain_A$, $Gain_B$, and $Gain_C$) are directly connected to the PWM generator blocks without any intermediate block (i.e., linearization block), the output of inverter would be distorted as described in Section 3. This is because the gain signals, which in this case would be identical to the duty cycle signal, would be essentially a

single frequency signal; and it is shown that the response of the inverter to single frequency duty cycle is highly distorted. Since the relationship between the phase voltage-gain and duty cycle in (19) is static, this nonlinearity can be mitigated effectively by calculating the inversion of relationship in (19). The phase voltage-gain of phase A (G_a) and normalized phase voltage-gain (g_A) are described by

$$\begin{cases} \mathrm{G_A} = \frac{\mathrm{V_{out1}}}{\mathrm{V_{DC}}} = \mathrm{n}\frac{\mathrm{D_a}}{1-\mathrm{D_a}} \\ \mathrm{g_A} = \frac{\mathrm{G_A}}{\mathrm{n}} = \frac{\mathrm{V_{out1}}}{\mathrm{nV_{DC}}} = \frac{\mathrm{D_a}}{1-\mathrm{D_a}} \end{cases} \tag{38}$$

With rearrangement of D_a in terms of g_A in (38), one can obtain:

$$D_a = \frac{g_A}{1+g_A} = \frac{\mathrm{V_{out1}}}{\mathrm{nV_{DC}}+\mathrm{V_{out1}}} \tag{39}$$

The output signal of the first stage of modulator (e.i., $Gain_A$) can be assumed to be proportional to the output terminal voltage. This assumption is useful because both $Gain_A$ signal and V_{out1} are supposed to have a single frequency and added offset. Note that the added offset value to $Gain_A$ (and consequently to V_{out1}) is not important, because this value is added equally to all phases and will be canceled out on line and phase voltages. Thus; the following assumption is purposefully made for phase A, and identical assumptions can be made for other phases as well:

$$Gain_A = k_s \times Vout_1 \tag{40}$$

where k_s is the scaling factor that can be obtained by using loop gains after controller design. By substituting (40) into (39) one obtains:

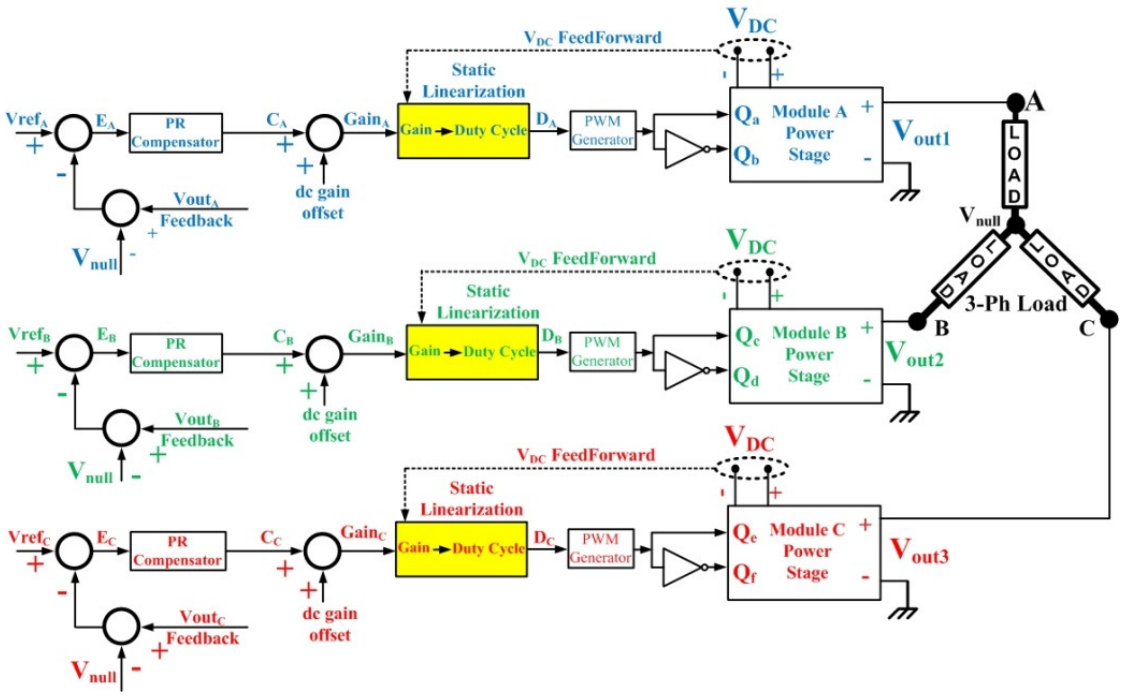
$$D_a = \frac{g_A}{1+g_A} = \frac{Gain_A}{k_s\mathrm{nV_{DC}}+Gain_A} \tag{41}$$

Equation (41) is important because, it captures the relationship between the duty cycle and $Gain_A$. The other parameters are either constant (n and k_s) or can be measured (V_{DC}). Thus, if (41) is implemented between the gain

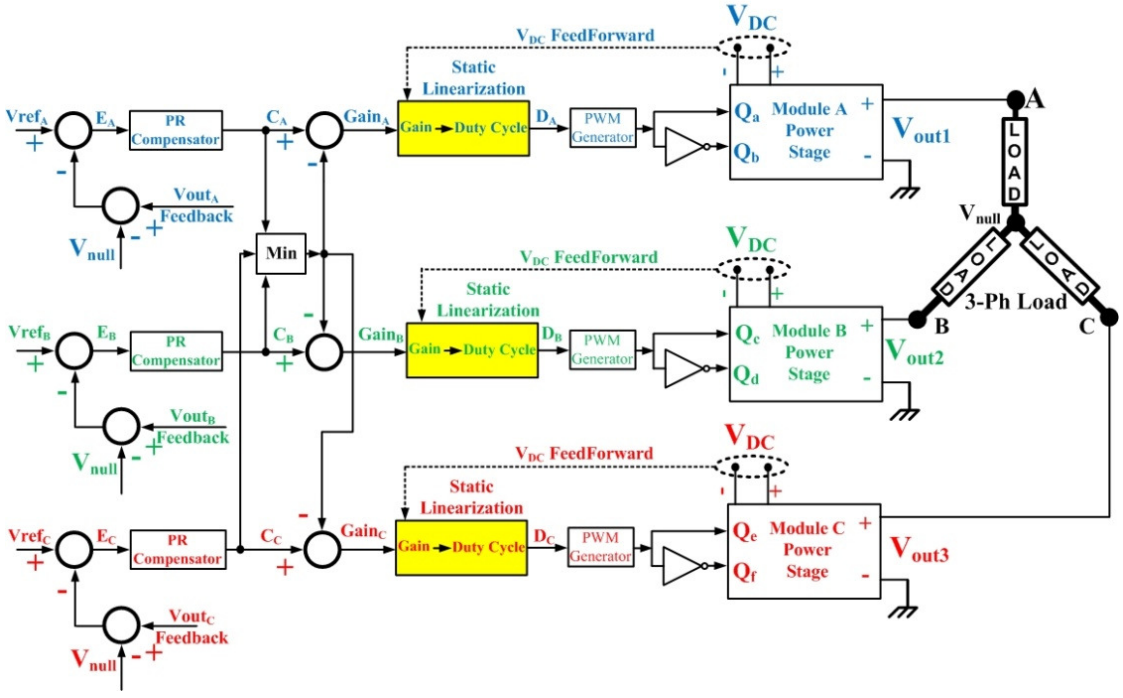
signals and duty cycle signals for CMS and DMS, it will remove the static nonlinearity of the open loop gain of DTCI. We represent this block as "static linearization block" or SLB as illustrated in Fig. 52. The new open loop module consists of series connection of SLB, PWM generator and power module. The static voltage gain relation of this new open loop system is linear as defined by (40).

E. Experimental Results

This section provides the experimental results of the DTCI operating using DMS and CMS. A 500-W experimental prototype of the DTCI, as shown in Fig. 53 is implemented and tested with CMS and DMS. A TMS320F28335 DSP based digital controller, with a 150-MHz clock, is used for implementing DMS and CMS. Real-time execution time for closed-loop control is close to 5 μs for DTCI with CMS or DMS. Specifications of the DTCI prototype are provided in Table . This section continues with experimentally obtained efficiency results first, which demonstrates a significant improvement in performance of the DMS-based DTCI compared to that obtained using the CMS-based DTCI. Subsequently, the measured peak device voltages are provided using CMS and DMS. These results are consistent with analytical and simulation results in Section C. The open loop oscilloscope results will be presented as well with and without SLB. The results prove the effectiveness of SLB to reduce distortion. Then experimental transient and steady state results for the proposed closed loop schemes (Fig. 52) are provided, which prove the effectiveness of control structure.



(a)



(b)

Fig. 52. Proposed architecture of the closed-loop controller for DTCI operating with (a) CMS and (b) DMS.

Fig. 54 shows the efficiency of the DTCI for a line voltage fixed at 120 V (RMS) and an output power of 500 W with normalized dc-voltage gain varying between 0.5 and 2 (corresponding to an input-voltage (V_{DC}) variation between 25 V and 100 V). The difference between the efficiencies of the DTCI operating with DMS and CMS is found to be significant. The improvement is almost flat at different peak gains and is consistent with the prediction from section 1, because the reactive power ratio of DTCI operating with CMS to that of operating with DMS is constant and it is not dependent on peak voltage gain.

Next, the peak voltages of the switches (Q_a, Q_c or Q_e) on the primary side of DTCI obtained using DMS and CMS are measured and plotted in Fig. 55(a). It is noted that, the voltage ratings of the switches on the ac side are proportional to the switches on the dc side with the proportionality constant being the transformer turns ratio. To obtain the plot in Fig. 55, the input voltage is varied between 25 V and 100 V for a constant output power of 500 W, while keeping the line-voltage set at 120 V (RMS). The results show that the gap between the peak voltage of the switches using DMS and CMS increases a little with increasing normalized phase-voltage gain. The ratios of the measured peak voltages of the primary-side switches of the DTCI are shown in Fig. 55(b) and they are consistent with the predictions in Fig. 46 and the simulation results of Fig. 47.

Next, distortion caused by nonlinearity of the open-loop inverter operating with DMS and CMS is presented with experimental results. First, the open loop DTCI without SLB is excited with sinusoidal signals for both modulation schemes. The experimental line-voltages and phase-voltages of the DTCI operating using CMS are shown in Fig. 57(a) and Fig. 57(b), respectively. Fig. 57 (a) and Fig. 57 (b) show the line-voltages and phase-voltages of DTCI operating using DMS, respectively. For these experiments the peak instantaneous line-voltages for both results are set at 170 V (corresponding to 120-V ACRMS) while the input voltage and output power are set, respectively, at 33 V and 500 W. The 30% THD is measured for this experiment with DMS, while CMS yields THD of 24% under the similar conditions. Further illustration of the problem is provided in Fig. 58, which compares the measured THD results for the open-loop DTCI operating with CMS (solid line) and DMS (dotted line) versus peak line-voltage gains. The progressively adverse effect of the line voltage THD with increasing peak line-voltage gain is predictable with increasing range of duty cycle swing. Higher THD results for DMS-based DTCI compared to CMS-based DTCI are consistent with Section 3 results. The effect of SLB on open loop responses is pursued next.

Table II. Specifications of the DTCI experimental prototype.

Input voltage	Peak output voltage (V_{out}^{*})	Output power	Output frequency	Transformer turns ratio (n)	Switching frequency	Primary-side filter inductance	Secondary-side filter inductance
20-120 V	170 V	500 W	60 Hz	2	125 kHz	50 µH	100 µH

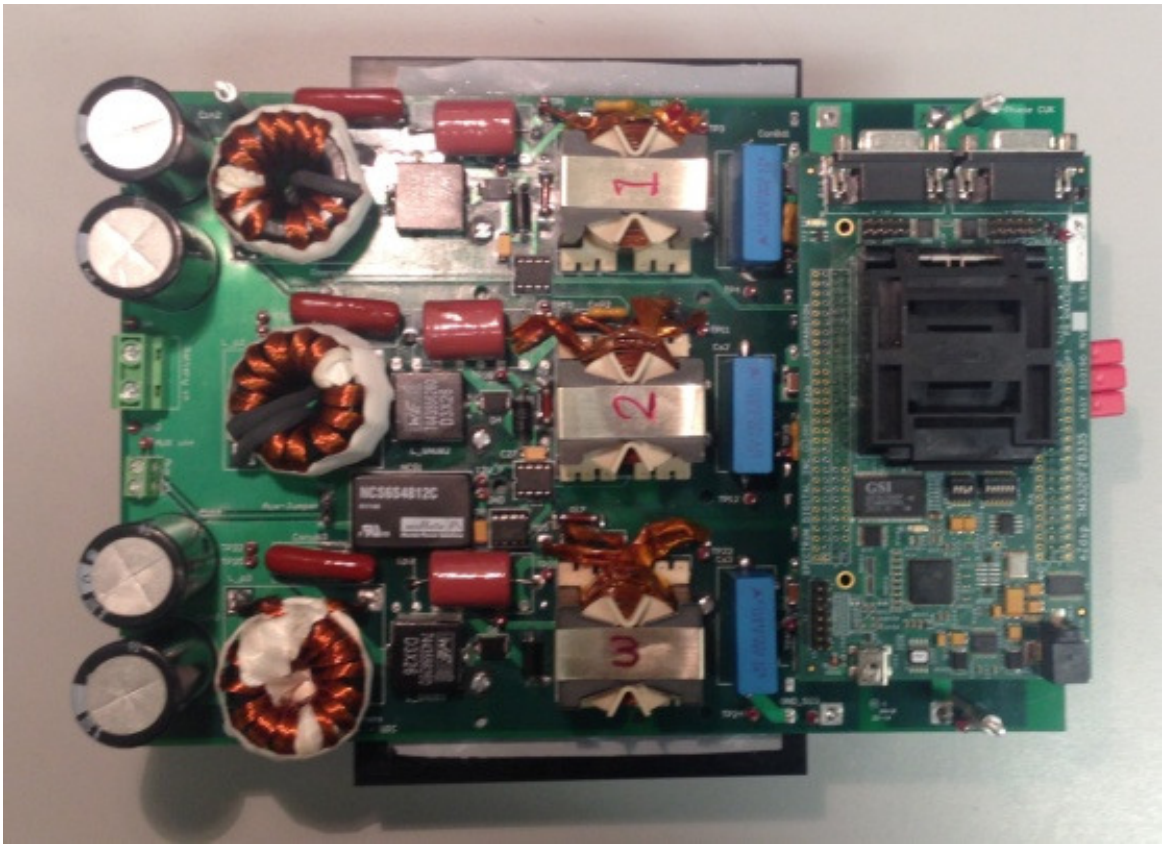


Fig. 53. Experimental prototype of the DTCI. It shows the TMS320F28335 DSP based digital controller on the top right, three transformers in the middle, and primary side filter inductors and capacitors to the left.

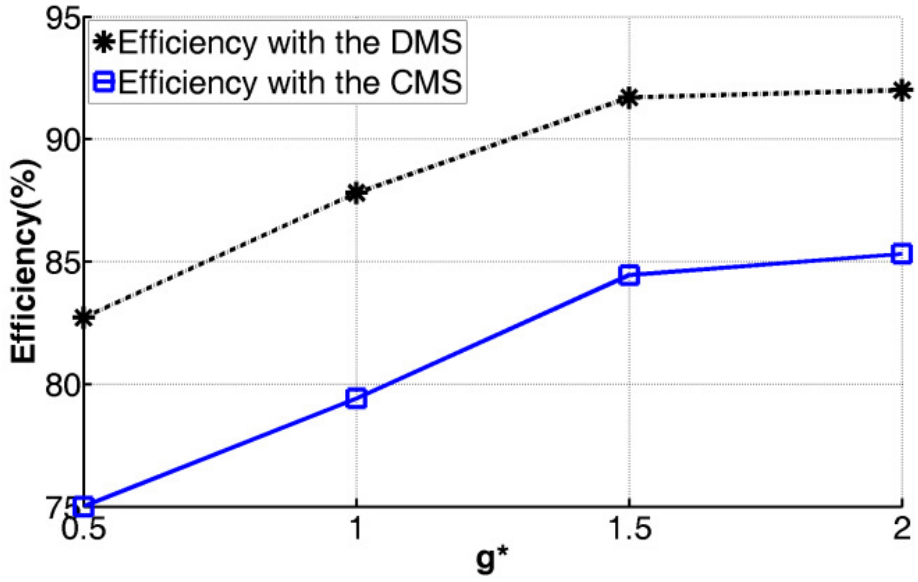
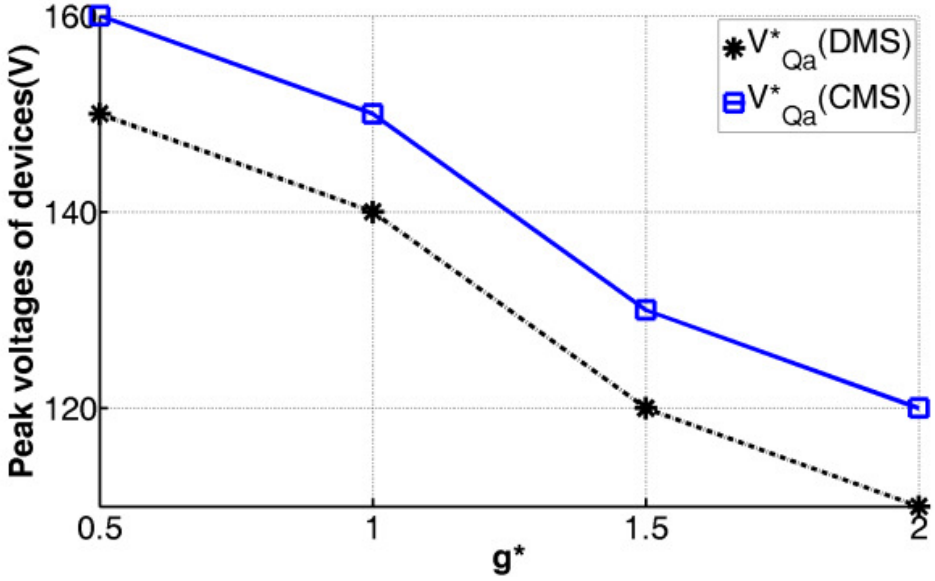
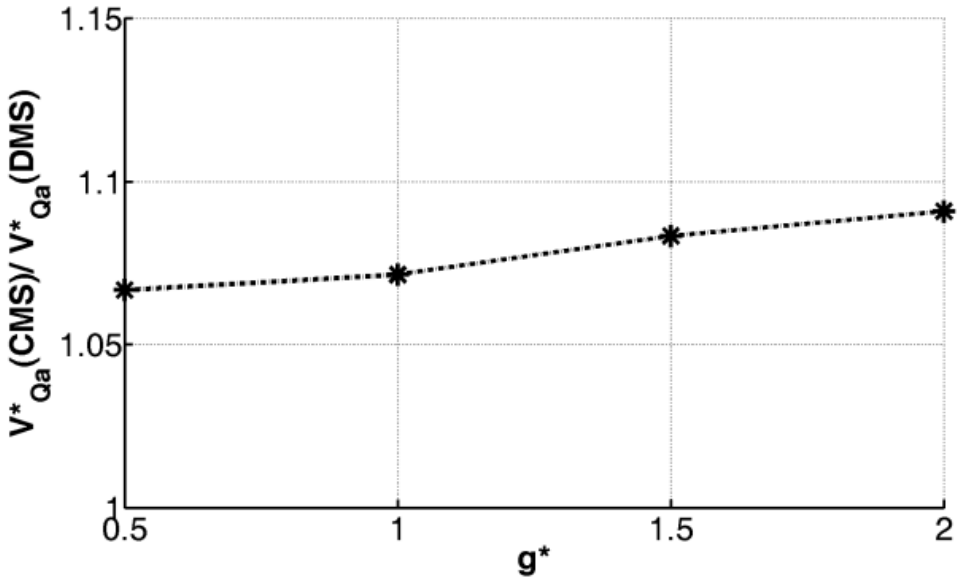


Fig. 54. Experimental efficiency of the DTCI for varying normalized peak phase-voltage gain obtained using DMS and CMS.

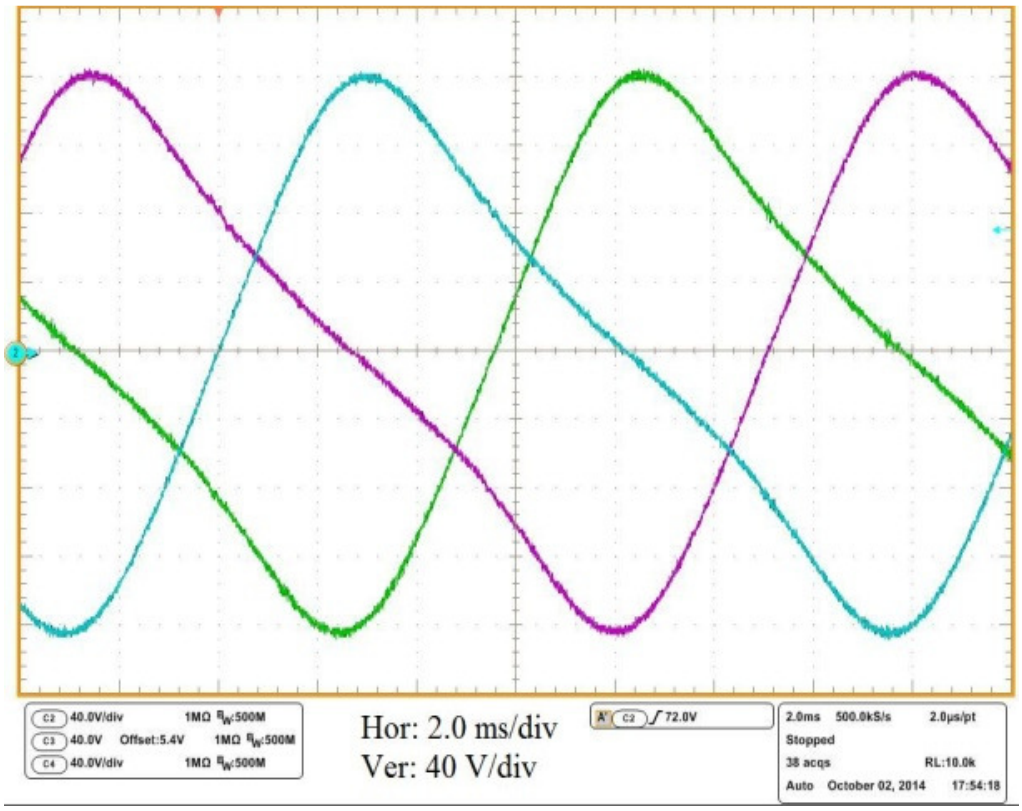


(a)

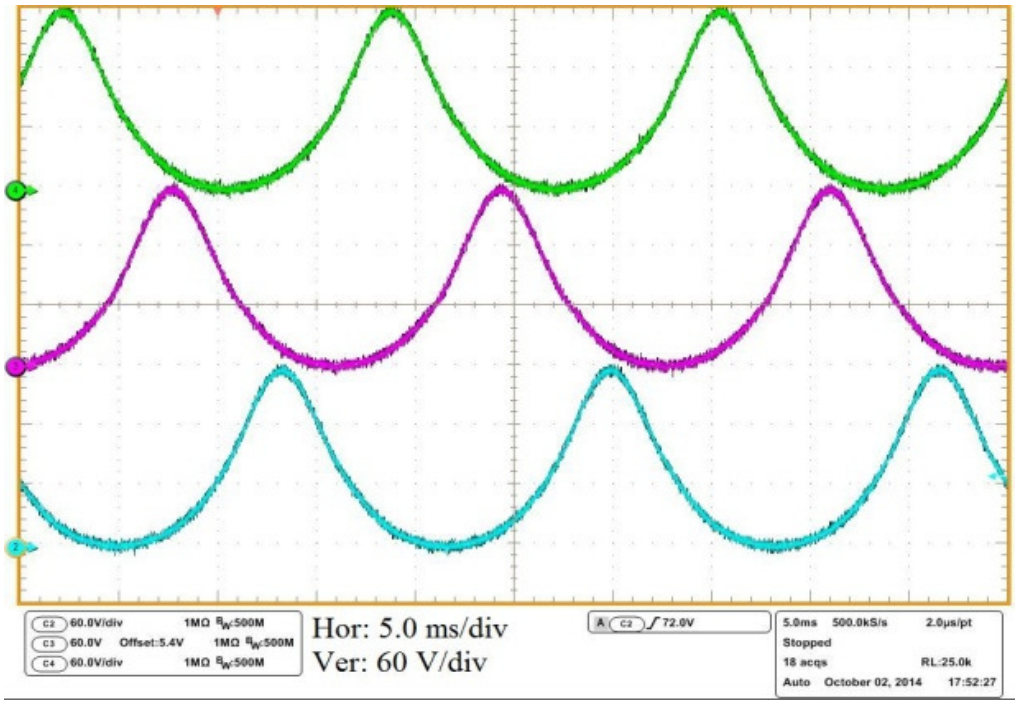


(b)

Fig. 55. (a) Experimentally-determined peak voltage of the primary-side switches of the DTCI with CMS (solid line) and DMS (dotted line). (b) Ratios of the two traces in (a).

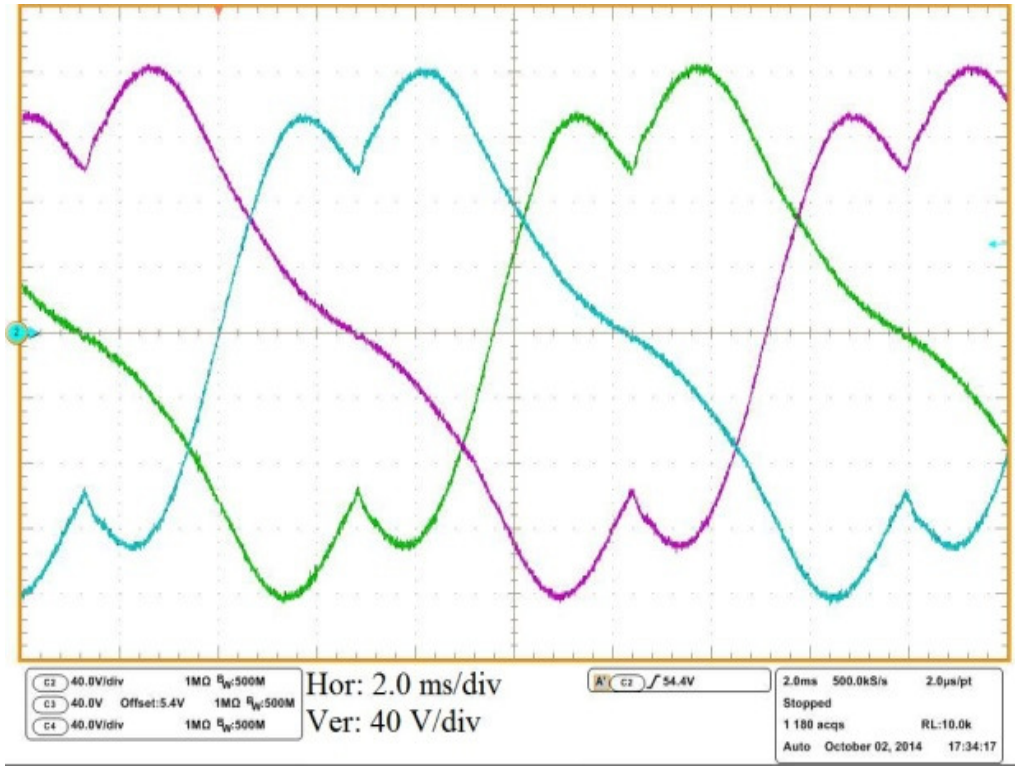


(a)

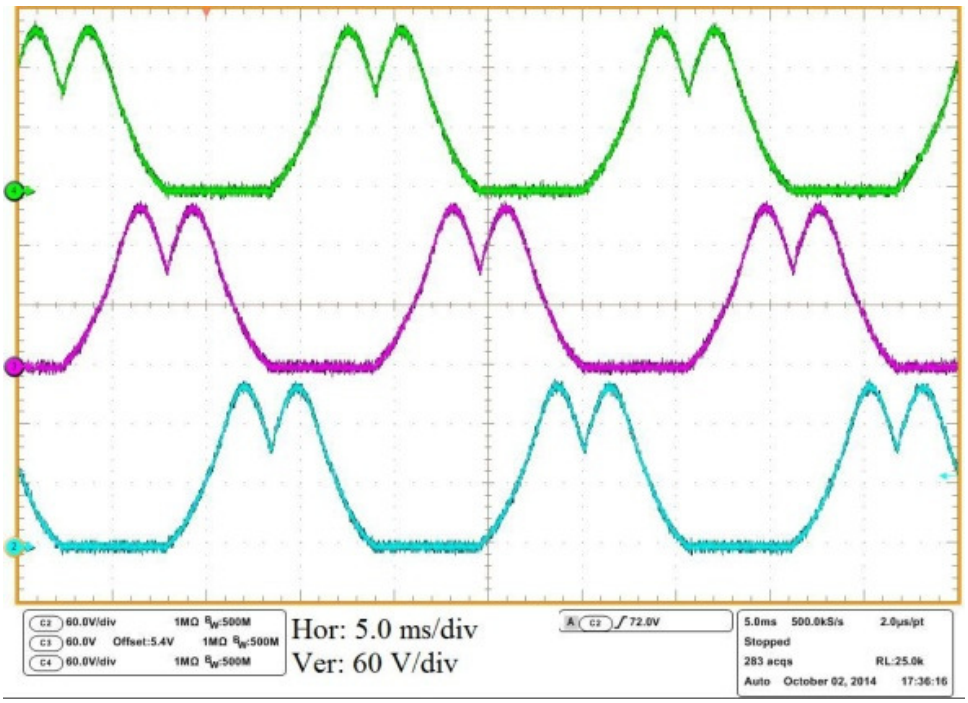


(b)

Fig. 56. The open-loop (a) line-voltages and (b) terminal voltages of DTCI, operating with CMS. The inverter is excited with sinusoidal signals without SLB.



(a)



(b)

Fig. 57. The open loop (a) line-voltages and (b) terminal voltages of DTCI, operating with DMS. The inverter is excited with sinusoidal signals without SLB.

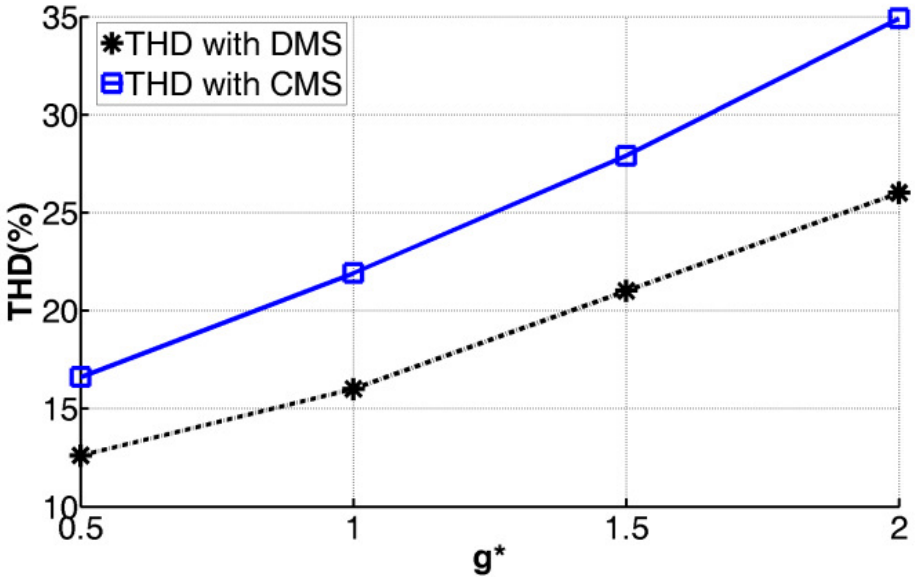
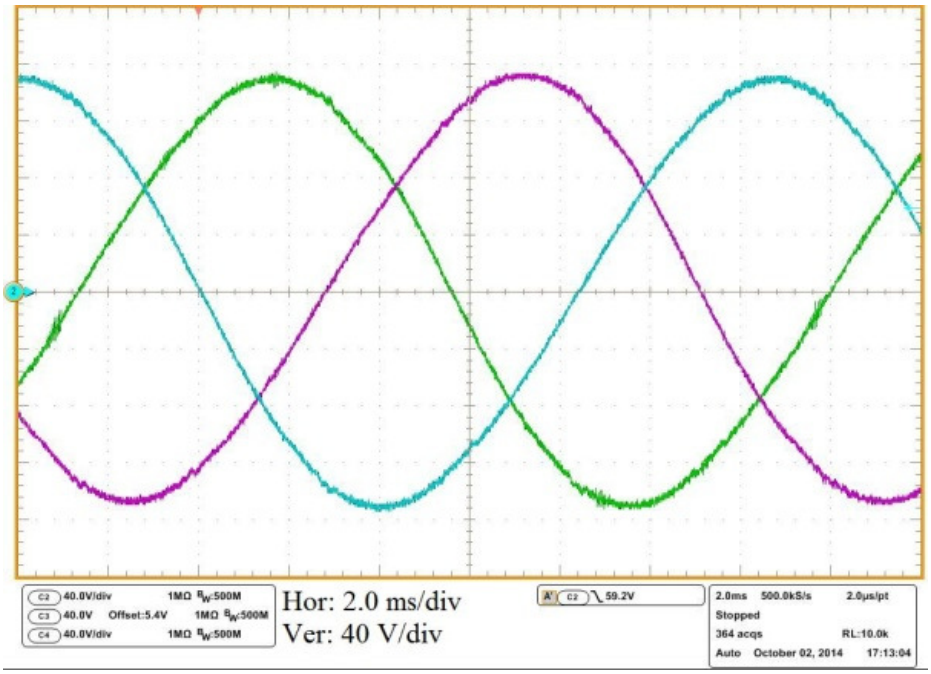


Fig. 58. The line-voltage THD results for open loop DTCI without SLB operating with CMS (solid line) and DMS (dotted line), versus peak line-voltage gain.

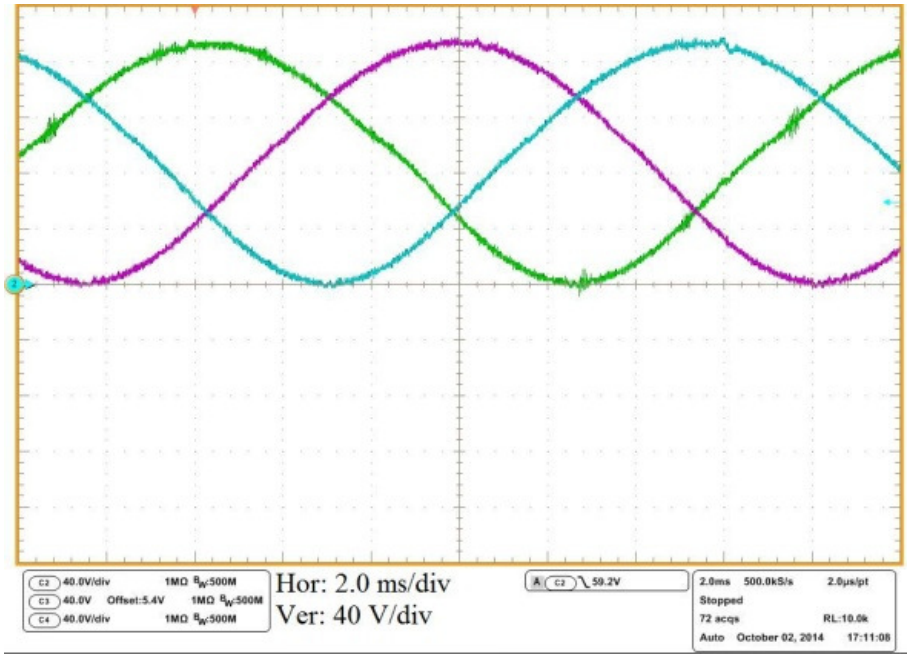
The static linearization method to overcome the distortion problem is discussed in Section C and static linearization method is proposed in Section D based on (41). The SLB is implemented for the experimental DTCI using a DSP controller. The experiments are carried out for open loop DTCI with SLB, under the identical operating condition used to carry out the experiments of Fig. 56 - Fig. 58. The line-voltages and phase-voltages of the DTCI operating with CMS are shown in Fig. 59 (a) and Fig. 59(b), respectively. Fig. 60 (a) and Fig. 60 (b) show the line-voltages and phase-voltages of DTCI operating using DMS, respectively. Both experiments are carried out with SLB; and DTCI is excited by three-phase sinusoidal signals ($Gain_A$ through $Gain_C$). A THD of about 5% is measured for this experiment with DMS, while the CMS-based DTCI yields a THD of 6% under similar operating conditions.

Further illustration of the problem is provided in Fig. 61, which compares the measured THD results for the open-loop DTCI with SLB operating with CMS (solid line) and DMS (dotted line) versus peak line-voltage gain. The significant reduction of THD by using SLB, proves effectiveness of the method. Also, it is evident that, DTCI with DMS yields even better THD results than that obtained using CMS in conjunction with SLB.

The remaining distortion after using static nonlinear compensation is primarily due to two factors; one is non-ideal practical static phase-voltage gain, which does not exactly follow (38). The reason is the dead-time effect on the voltage gain of modules. The other important factor of distortion is the dynamic behavior of DTCI. The improved THD of DTCI obtained using DMS (as compared to that obtained using CMS) is due to the second factor. Even though the identical hardware is used for implementing the two schemes, DMS obtains less voltage distortion. DMS eliminates almost one third of zeros and poles of DTCI transfer function by turning off one module a time. This results in reduced order dynamic of the system and leads to less voltage distortion of the DTCI.

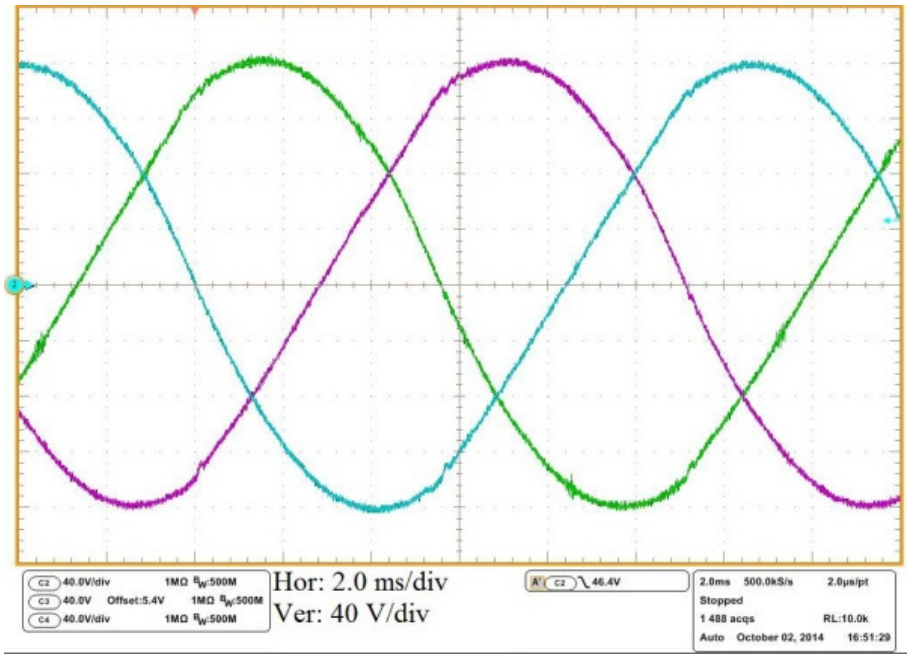


(a)

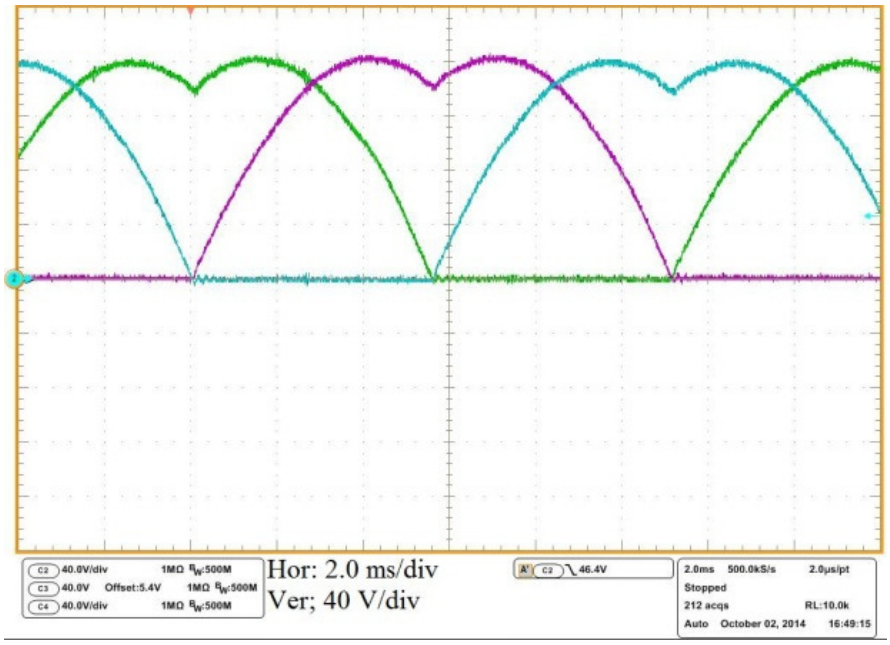


(b)

Fig. 59. The open-loop (a) line-voltages and (b) phase-voltages of DTCI, operating with CMS. The inverter is excited with sinusoidal signals applied to SLB.



(a)



(b)

Fig. 60. The open loop (a) line-voltages and (b) phase-voltages of DTCI, operating with DMS. The inverter is excited with sinusoidal signals applied to SLB.

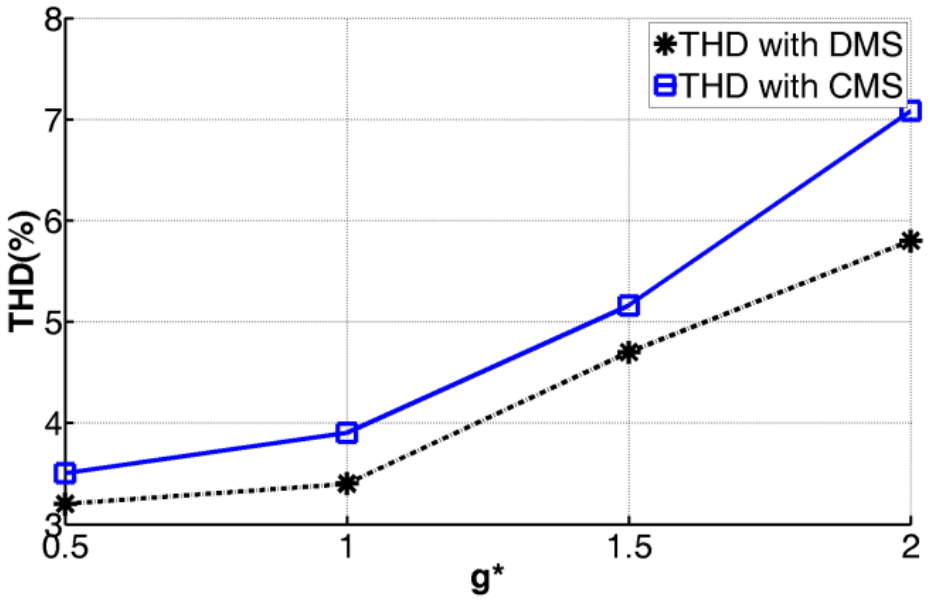
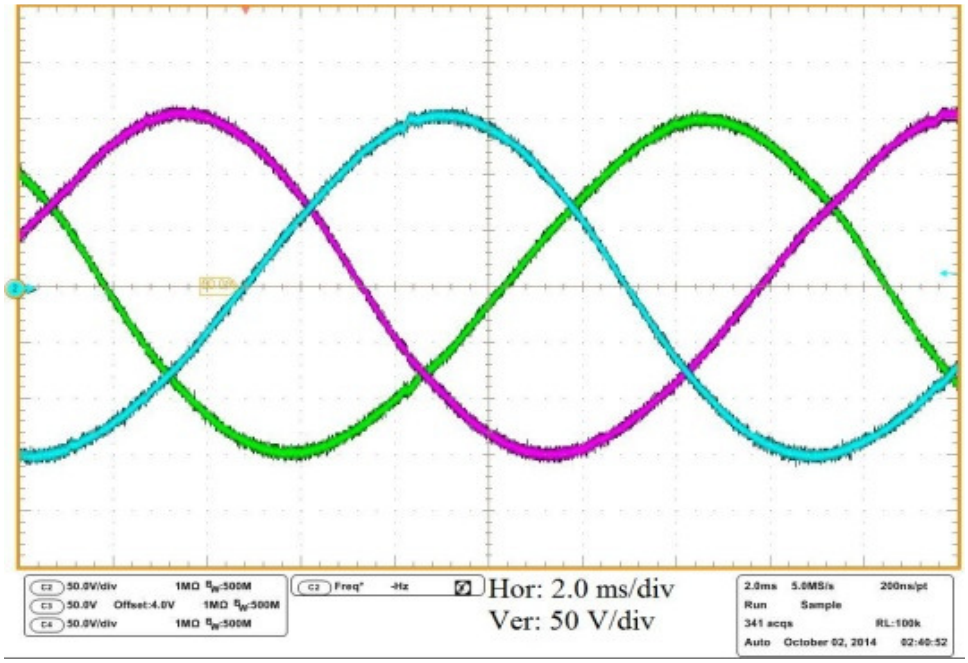
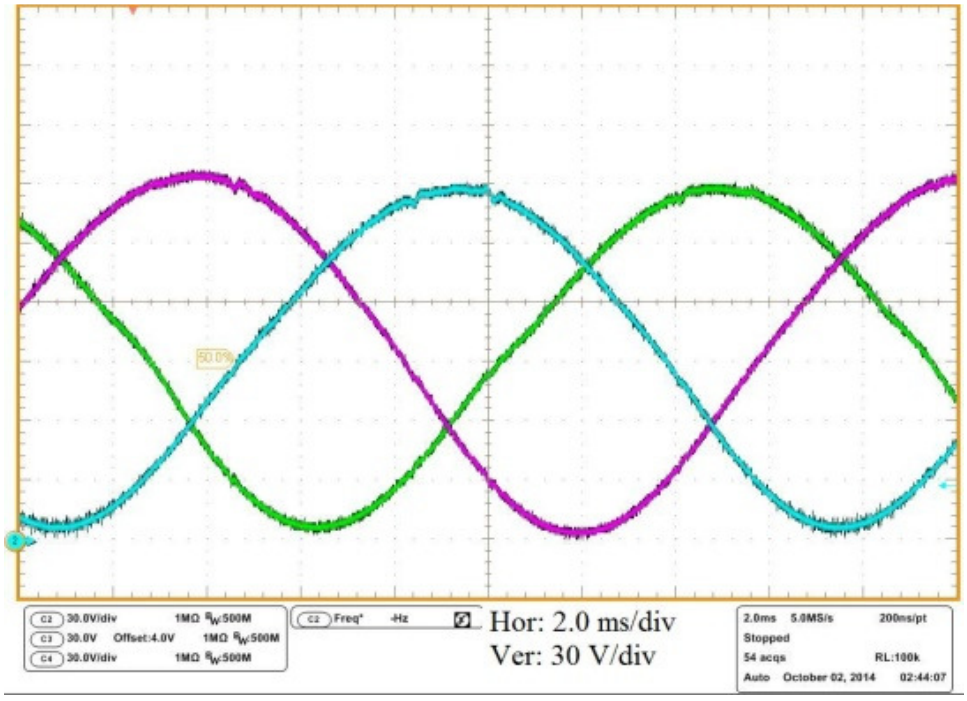


Fig. 61. The line-voltage THD results for the open-loop DTCI along with SLB. The DTCI operating with CMS is solid line and DMS-based DTCI is represented by dotted line, versus peak line-voltage gain. It shows a marked improvement in the THD of DTCI using SLB.

Subsequently, the closed-loop controllers, as illustrated in Fig. 52, are implemented and the steady-state and transient results are presented below. The PR compensator is tuned to keep a balance between satisfactory steady-state performance and acceptable transient response [56]. The closed loop line-voltages and phase-voltages of DTCI operating using CMS are shown in Fig. 62(a) and Fig. 62(b), respectively. The same waveforms are shown in Fig. 63 (a) and Fig. 63 (b) when DTCI is operated using DMS. The peak line-voltages for both experiments are set at 170 V (corresponding to 120-V RMS) while the input voltage and output power are set, respectively, at 33 V and 500 W. The DMS yields a THD of 1.6%, while THD of 5.5% obtained by operating the DTCI using CMS. Fig. 64 shows the THD of the line-voltage of the closed-loop DTCI as a function of the line-voltage gain when the DTCI is operated with DMS (dotted line) and CMS (solid line). By comparing the open- and closed-loop results of DTCI , as shown, respectively, in Fig. 61 and Fig. 64, one can observe that the (PR-based) HCs reduce the THD of the DMS-based and CMS-based closed-loop DTCI. In addition to achieve an acceptable THD, an additional goal is to achieve an acceptable transient performance for the DTCI. Consequently, the gains of the fundamental-frequency compensator have to be so chosen such that an optimal tradeoff between a lower harmonic distortion and a satisfactory transient response is achieved.

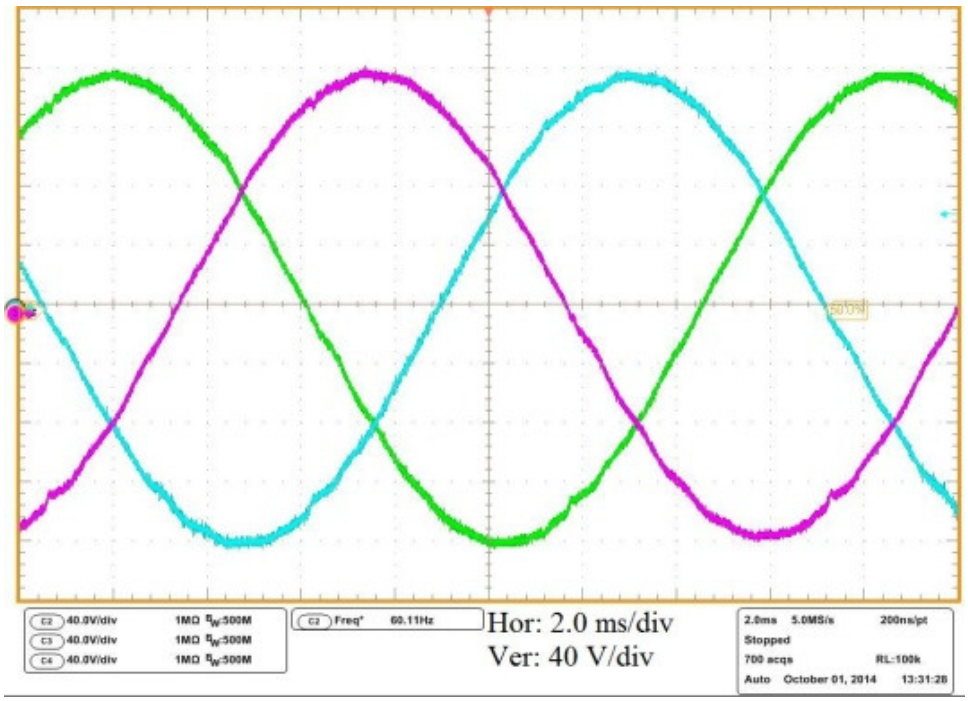


(a)

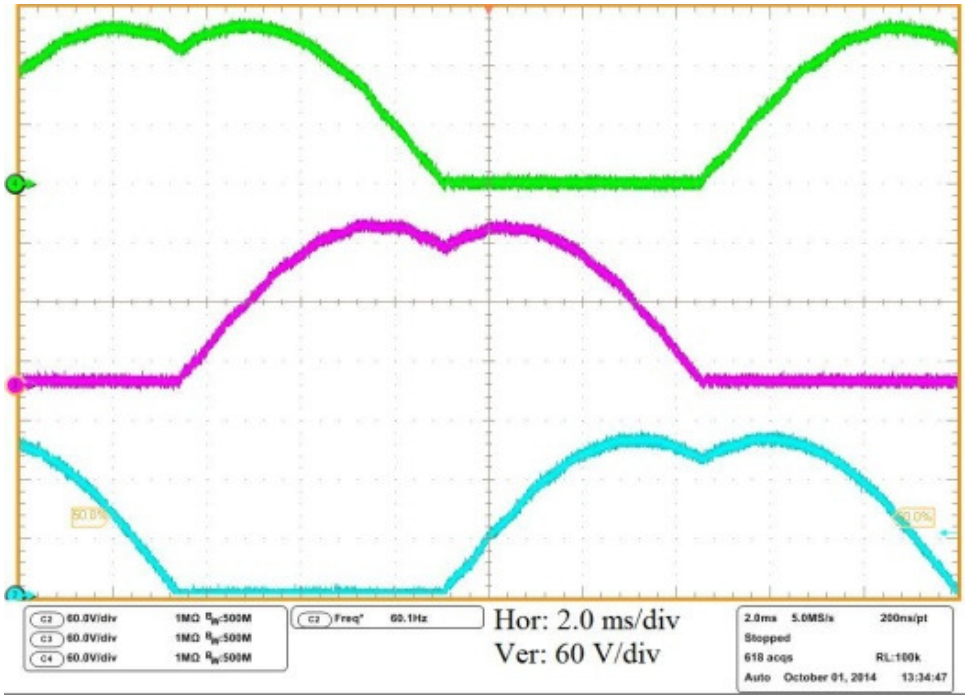


(b)

Fig. 62. Experimentally-obtained closed-loop (a) line-voltages and (b) phase-voltages of DTCI, operating with CMS. The implemented control scheme is illustrated in Fig. 52(a).



(a)



(b)

Fig. 63. Experimentally obtained closed loop (a) line-voltages and (b) phase-voltages of DTCI, operating with DMS. The implemented control scheme is illustrated in Fig. 52(b).

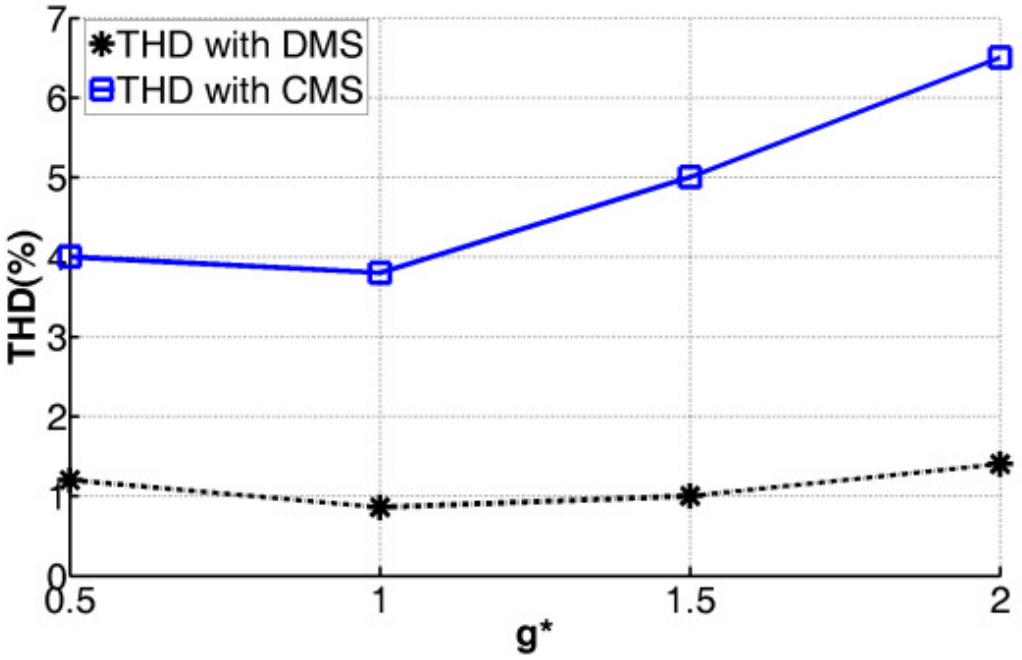
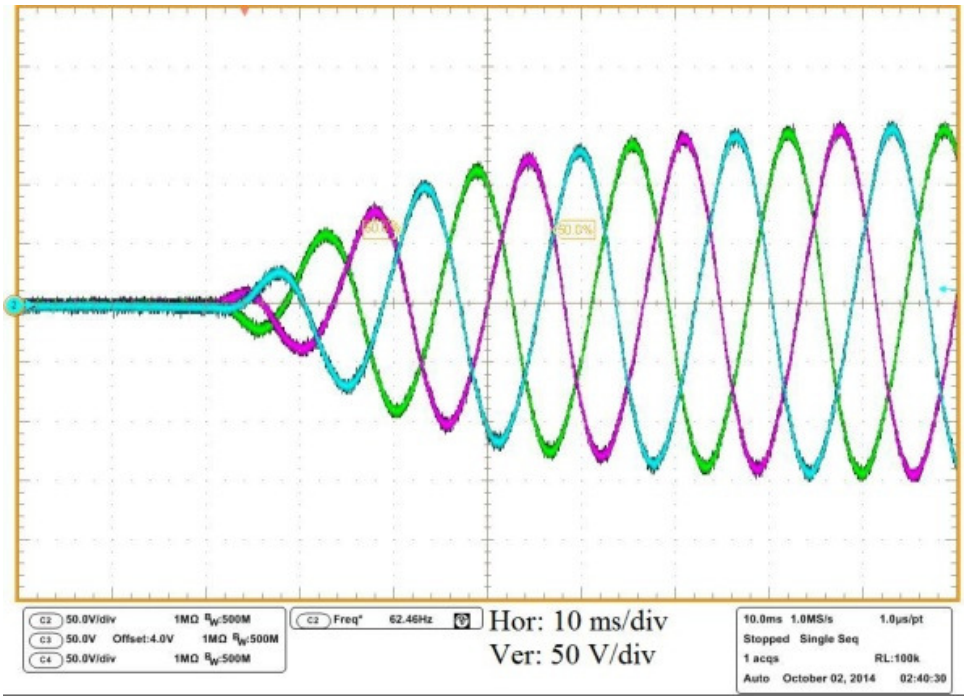
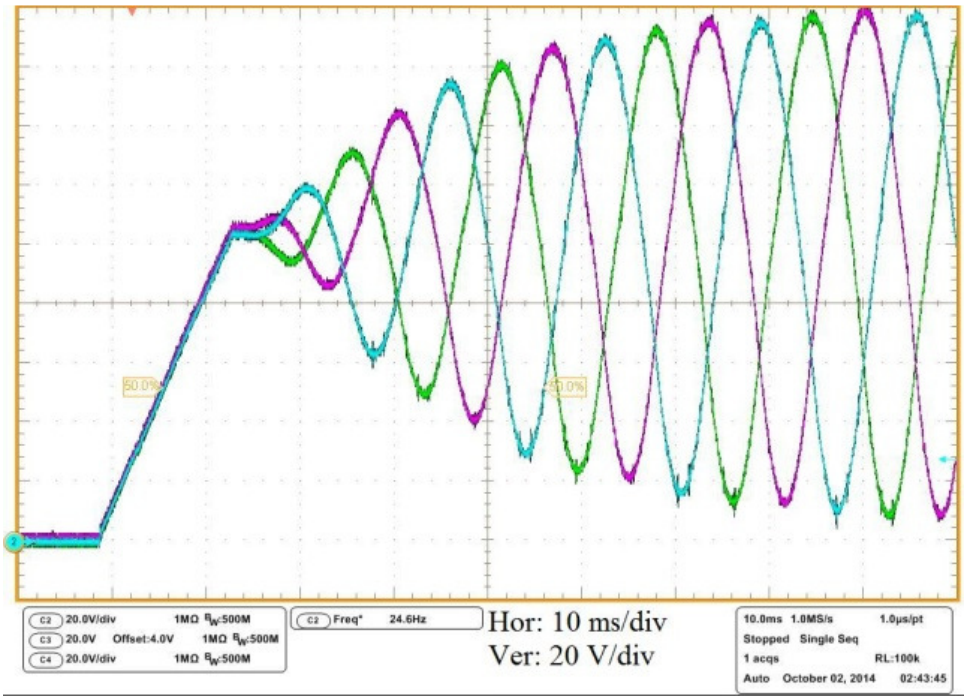


Fig. 64. Experimentally-obtained THD of the line voltage as a function of the normalized peak line-voltage gain of the closed-loop DTCI when it is operated using DMS (dotted line) and CMS (solid line).

The start-up response of the DTCI is used as a transient behavior of the system. The start-up waveforms of line voltages and phase voltages of DTCI operating with CMS are shown in Fig. 65 (a) and Fig. 65(b), respectively. The same waveforms for DMS-based DTCI are shown Fig. 66 (a) and Fig. 66 (b), respectively too. Transient responses found to be satisfactory and they do not exhibit any overshoot or undershoot. The CMS- and DMS-based DTCI exhibit convergence after the third and second cycle, respectively.

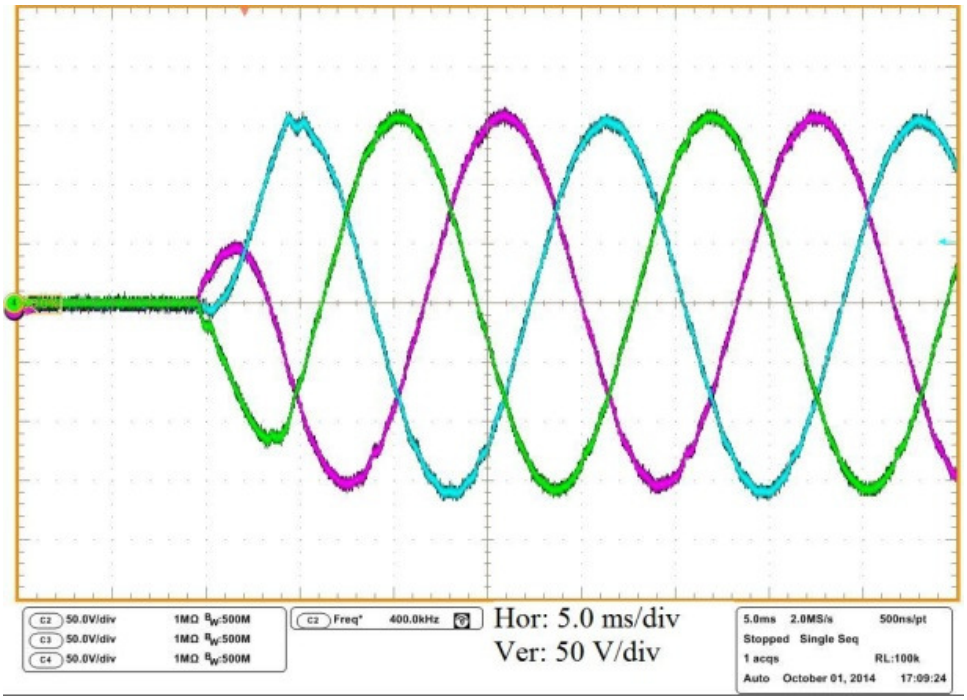


(a)

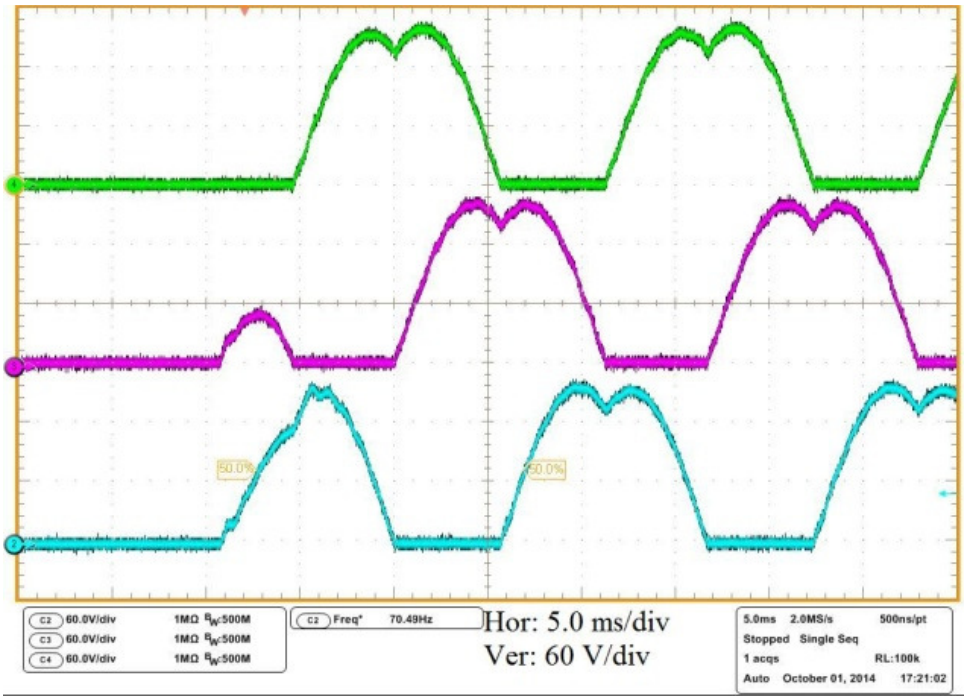


(b)

Fig. 65. Experimentally-obtained start-up (a) line and (b) phase-voltages of the closed-loop CMS-base DTCI.



(a)



(b)

Fig. 66. Experimentally-obtained start-up (a) line and (b) phase voltages of the DMS-based closed-loop DTCI.

Chapter 4

CONCLUSIONS AND FUTURE WORKS

A. Conclusions

The Dissertation describes a discontinuous modulation scheme (DMS) for a differential-mode Ćuk inverter (DMCI) and differential-mode three-phase Ćuk inverter (DTCI). Subsequently, the mechanism and performance of the DMS-based DTCI and DMCI are compared to that of a prior-art continuous-modulation scheme (CMS) based DTCI and DMCI. Two experimental hardware prototypes were developed for the DMCI and DTCI to validate and compare the results obtained operating with DMS and CMS with focus on energy-conversion efficiency, device rating, output-voltage distortion, and transient response of the inverter. It has been found that DMS, which leads to topological switching of the DMCI, yields significant improvement in efficiency of the inverter compared to that obtained using CMS. This is because DMS eliminates/reduce the pathway for circulating reactive power in the inverter. For the same reason, the reduction in the voltage rating of the DTCI and DMCI switches is also found to be significant using DMS.

With regard to the total harmonic distortion (THD) of the output voltage of the DMCI, CMS demonstrated better results compared to DMS for the inverter when it was operated under open-loop control. The DMS-based DMCI has a better dynamic response because of the reduced order of the topological control system; however, the DMS-based DMCI has wide range of nonlinearity in its dc-voltage gain, which yields higher THD. Consequently, a closed-loop control for the DMCI-based on harmonic compensation was designed and the experimental results obtained using DMS demonstrated a marked improvement in the THD of the inverter output voltage. The slightly slower response of the DMS-based DMCI is due to the fact that a higher-order proportional-resonant (PR) based harmonic compensation for the closed-loop controller is needed that reduces the control bandwidth.

The analysis shows the distorted output for open loop DTCI with both modulation schemes. The static linearization method is proposed for inverter as an effective method to reduce distortion. The effectiveness of method is proved by experimental THD results after and before addition of static linearization block for both

modulation techniques. Finally closed loop architecture is proposed and implemented. Experimental steady state and start up transient results are provided to show the effectiveness of linearization for both modulation schemes.

An overall qualitative comparison between the DMS- and CMS-based operations of the DMCI/DTCI, as implemented currently, indicates that the DMS based operation of the inverter has the potential to yield relatively higher saving in the power stage due to the reduced requirements of the device breakdown-voltage, heat-sinking, and power-handling.

B. Future Works

The focus on the following aspects of the work can be clue for future works:

- Control of DMCI and DTCI in grid connection mode. The inverters in grid connection mode tends more to instability, in comparison to stand alone operation;
- Explore the possibility of soft switching and/or active snubber for reducing the switching losses (which is dominant loss in DTCI and DMCI) to achieve higher efficiency;
- Exploring and implementing similar modulation schemes for other differential-mode inverters/rectifiers.

APPENDIX

Experimental Prototype Design

Initial specification of the inverter

f_{sw} = 250 kHz	T_{sw} = 4 µs	P_{nom} = 500 W(DC and AC Modes)	Transformer turns ratio: N = 1:2
Input ratings: 20 V < V_{DC} < 50 V 1 A < I_{in} < 25 A		Output ratings(AC mode): 100Vac < V_{out} < 120 V ac 0.41 ac < I_{out} < 5 A ac	

Design of the input filter of the converter

Input filter inductor (L_a and L_c)

$$L = \frac{V\Delta t}{\Delta I} \tag{A-1}$$

For input inductor or L_a we have

$$L_a \geq \frac{V_{in}\, DT}{\Delta I_{la}} \tag{A-2}$$

with assumption that all input current flows to inductor and considering the proper operation of circuit at $0.1P_{nom}$ it can be rewritten as follows:

$$L_a \geq \frac{V_{in}\left(\frac{1}{1+nV_{in}/V_{out}}\right)}{fsw\left(2\frac{P_{nom}/10}{V_{in}}\right)} = \frac{\left(\frac{V_{in}^{\,2}}{1+nV_{in}/V_{out}}\right)}{fsw(P_{nom}/5)} \tag{A-3}$$

L_a should be calculated for the worst case which is max V_{DC} and V_{out}:

$$L_a \geq 28.6\,\mu H \tag{A-4}$$

Thus; the following specification is roughly chosen for inductor design:

APPENDIX (continued)

L_a = 30 µH	f_{sw} = 250 kHz	$I_{rms} = P_{nom}/V_{in}$ (min) = 500/20 A = 25 A	$I_{peak} < 2*I_{rms}$ (in ac mode) = 50 A

core selection: 0R45050UG (R Material)

B_{max} = 0.35 T

μ_r = 2300

A_e = 328 mm^2

L_e = 113 mm

A_{window} = 32*10 mm*mm

With the inductor specifications and the selected core we have:

needed air gap = $g/2$ = 1.2 mm

Number of turns = 13

wire design(for j = 3.5Amm^{-1}): litz of (Ns = 140) wire of D = 0.255 mm; effective wire diameter D_e = 4 mm

needed wire length:

each turn in layer 1 $L_1 = \pi(D_{acc}+D_e) = \pi$(32mm+4mm) = 113 mm

each turn in second layer = $\pi(D_{acc}+3D_e) = \pi$(32 mm+12 mm) = 138 mm

L_{total} = 7*L_1+6*L_2 = 1619 mm

Input filter capacitor design:

In dc/dc mode this capacitor just filters out the 250 kHz. but in dc/ac mode there is also 120 Hz ripple too.

For dc/dc mode:

$$C = \frac{I\Delta t}{\Delta V} \tag{A-5}$$

Assuming that all input ripple current goes to the capacitor:

APPENDIX (continued)

$$\Delta I_a = \frac{V_{in}(\frac{1}{1+nV_{in}/V_{out}})}{L_a f_{sw}} = 1.9A \quad \text{(A-6)}$$

Thus:

$$C_{in} = 2.17\mu F \approx 2.2\mu F \quad \text{(A-7)}$$

The above value is needed for switching frequency. For dc/ac mode we have large ripple of 120 Hz on input current. Assuming that all 500 W ac comes to input without filtering we have 25 A ac on inductor current. If we design capacitor to confine input ac ripple current to %5 of V_{DC} we have:

$$C = \frac{I}{\omega V} = \frac{25A}{2\pi 60 \times 50V \times 0.05} = 26.5mF \quad \text{(A-8)}$$

Selected capacitor for input can be smaller than this value because we did not consider any other filtering in energy pass. So we have 6*3.3 mF = 19.8 mF capacitor installed on input. This capacitor may need precaution or pre-charger for installing battery on it.

Design of the output filter of the converter

Output filter inductor design and calculations

$$L = \frac{V\Delta t}{\Delta I} \quad \text{(A-9)}$$

for output inductor or L_b we have:

$$L_b = \frac{V_{out}(1-D)T}{\Delta I_{lb}} \quad \text{(A-10)}$$

with assumption that all output current flows to inductor and considering the proper operation of circuit at $0.1P_{nom}$ it can be rewritten as follows:

APPENDIX (continued)

$$L_b \geq \frac{V_{out}\left(\frac{nV_{in}/V_{out}}{1+nV_{in}/V_{out}}\right)}{fsw\left(2\frac{P_{nom}/10}{V_{out}}\right)} = \frac{\left(\frac{nV_{in}V_{out}}{1+nV_{in}/V_{out}}\right)}{fsw(P_{nom}/5)} \quad \text{(A-11)}$$

Inductance L_b should be calculated for the worst case which is max of V_{DC} and V_{out}:

$$L_b \geq 45.7\,\mu H \quad \text{(A-12)}$$

Thus, inductor specifications are as follows:

L_b = 50 μH	f_{sw} = 250kHz	$I_{rms} = P_{nom}/V_{DC}$(min) = 500/40 A = 12.5A	$I_{peak} < I_{rms}$ (in ac mode) = 17.7A

core selection: 0R44040UG (R Material)

B_{max} = 0.35 T	μ_r = 2300	A_e = 201 mm^2	L_e = 102mm	A_{window} = 27*10 mm*mm

With the inductor specifications and the selected core we have:

- needed air gap = $g/2$ = 0.4 mm
- Number of turns =13
- wire design(for j = 3.5 Amm^{-1}): litz of (N_s = 70) wire of D = 0.255mm; effective wire diameter D_e = 3 mm
- needed wire length:

  each turn in layer 1 $L_1 = \pi(D_{acc}+D_e) = \pi$(16 mm+3 mm)=60 mm

  each turn in second layer = $\pi(D_{acc}+3D_e) = \pi$(16 mm + 9 mm) =79 mm

  $L_{total} = 8*L_1+5*L_2$ = 875 mm

Output filter capacitance design

In dc/dc mode this capacitor just filters out the 250 kHz. and in dc/ac mode we do not want capacitor to block 60 Hz.

APPENDIX (continued)

$$C = \frac{I\Delta t}{\Delta V} \tag{A-13}$$

Assuming that all input ripple current goes to capacitor:

$$\Delta I_b = \frac{V_{out}(1-\frac{1}{1+nV_{in}/V_{out}})}{L_b f_{sw}} = 2.8A \tag{A-14}$$

So

$$C_{out} = 8\mu F \approx 10\mu F \tag{A-15}$$

Blocking capacitor design

Under steady-state condition, the average value of voltages on C_a and C_b are equal to V_{DC} and V_{out}, respectively. Since average value of voltage on inductor and transformer is zero and imposing KVL rule in loop containing L_a, C_a, input source and transformer, the mean value of voltage on C_a capacitor is equal to input voltage. The same evaluation is true for C_b. So, we have:

$$V_{ca} = V_{in} \tag{A-16}$$

$$V_{cb} = V_{out} \tag{A-17}$$

$$C_a = \frac{I_{la}(1-D)T}{\Delta V_{ca}} = \frac{I_{la}(1-\frac{1}{1+nV_{in}/V_{out}})T}{\Delta V_{ca}} \tag{A-18}$$

In the worst condition and for 20% ripple on voltage of the capacitor we have

$C_a = 7.1\ \mu H \approx 10\ \mu H$

$$C_b = \frac{I_{lb}(D)T}{\Delta V_{cb}} = \frac{I_{lb}(\frac{1}{1+nV_{in}/V_{out}})T}{\Delta V_{cb}} \tag{A-19}$$

In the worst condition and for 20% ripple on voltage on capacitor we obtain the following value for the blocking capacitor:

$C_a = 3.1\ \mu H \approx 10\ \mu H$

REFERENCES

[1] N. Tanaka, "Clean energy progress report," Paris, 2011.

[2] S. R. Bull, "Renewable energy today and tomorrow," *Proc. IEEE*, vol. 89, no. 8, pp. 1216–1226, 2001.

[3] "Office of Energy Efficiency & Renewable Energy." [Online]. Available: http://www.eren.doe.gov/repis.

[4] U.S. Dept. of Energy, "Dollars from sense—the economic benefits of renewable energy," 1997.

[5] "ABB web site." [Online]. Available: http://www.power-one.com/renewable-energy/efficient-power-solutions.

[6] S. Nowak, "Trends in photovoltaic application survey report of selected IEA countries between 1992 and 2004," 2005.

[7] A. Q. Jakhrani, A. Othman, A. R. H. Rigit, and S. R. Samo, "Life cycle cost analysis of a standalone PV system," in *2012 International Conference on Green and Ubiquitous Technology*, 2012, pp. 82–85.

[8] R. Naik, N. Mohan, M. Rogers, and A. Bulawka, "A novel grid interface, optimized for utility-scale applications of photovoltaic, wind-electric, and fuel-cell systems," *IEEE Trans. Power Deliv.*, vol. 10, no. 4, pp. 1920–1926, 1995.

[9] T. Erge, V. . Hoffmann, and K. Kiefer, "The German experience with grid-connected PV-systems," *Sol. Energy*, vol. 70, no. 6, pp. 479–487, Jan. 2001.

[10] Z. Ozkan and A. M. Hava, "A survey and extension of high efficiency grid connected transformerless solar inverters with focus on leakage current characteristics," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 3453–3460.

[11] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating Ground Current in a Transformerless Photovoltaic Application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.

[12] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[13] W. X. Shen, "Single-Phase Uninterruptible Power Supply Based on Z-Source Inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2997–3004, Aug. 2008.

[14] S. Roy and L. Umanand, "Integrated Magnetics-Based Multisource Quality AC Power Supply," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1350–1358, Apr. 2011.

[15] G. Franceschini, E. Lorenzani, and G. Buticchi, "Saturation Compensation Strategy for Grid Connected Converters Based on Line Frequency Transformers," *IEEE Trans. Energy Convers.*, vol. 27, no. 2, pp. 229–237, Jun. 2012.

[16] Y. Han, G. Cheung, A. Li, C. R. Sullivan, and D. J. Perreault, "Evaluation of Magnetic Materials for Very High Frequency Power Applications," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 425–435, Jan. 2012.

REFERENCES (continued)

[17] Young Roc Kim, Byung Hun Ra, Sung Hwon Kim, Young Hoon Son, and Seok Ki Kim, "Development of 10kW grid-connected photovoltaic inverter with high frequency transformer." pp. 346–348, 2007.

[18] R. O. Caceres and I. Barbi, "A boost DC-AC converter: analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, 1999.

[19] N. Vazquez, J. Almazan, J. Alvarez, C. Aguilar, and J. Arau, "Analysis and experimental study of the buck, boost and buck-boost inverters," in *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, 1999, vol. 2, pp. 801–806.

[20] N. Kasa, T. Iida, and H. Iwamoto, "An inverter using buck-boost type chopper circuits for popular small-scale photovoltaic power system," in *IECON'99. Conference Proceedings. 25th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.99CH37029)*, 1999, vol. 1, pp. 185–190.

[21] S. B. Kjaer and F. Blaabjerg, "A novel single-stage inverter for the ac-module with low frequency ripple penetration," in *in Proc. 10th EPE European Conf. Power Electronics and Applications*, 2001.

[22] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[23] C.-M. Wang, "A Novel Single-Stage Full-Bridge Buck-Boost Inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.

[24] M. Nagao and K. Harada, "Power flow of photovoltaic system using buck-boost PWM power inverter," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, 1997, vol. 1, pp. 144–149.

[25] M. Kusakawa, H. Nagayoshi, K. Kamisako, and K. Kurokawa, "Further improvement of a transformerless, voltage-boosting inverter for AC modules," *Sol. Energy Mater. Sol. Cells*, vol. 67, no. 1–4, pp. 379–387, Mar. 2001.

[26] T. J. Liang, Y. C. Kuo, and J. F. Chen, "Single-stage photovoltaic energy conversion system," *IEE Proc. - Electr. Power Appl.*, vol. 148, no. 4, p. 339, 2001.

[27] S. K. Mazumder, R. K. Burra, R. Huang, and V. Arguelles, "A low-cost single-stage isolated differential ĈCuk inverter for fuel-cell application," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4426–4431.

[28] S. K. Mazumder and S. Mehrnami, "A low-device-count single-stage direct-power-conversion solar microinverter for microgrid," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 725–730.

[29] R. Mechouma, B. Azoui, and M. Chaabane, "Three-phase grid connected inverter for photovoltaic systems, a review," in *2012 First International Conference on Renewable Energies and Vehicular Technology*, 2012, pp. 37–42.

[30] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-Phase Dual-Buck Inverter With Unified Pulsewidth Modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.

REFERENCES (continued)

[31] J.-J. Chen and C.-M. Kung, "A new on-chip all-digital three-phase full-bridge dc/ac power inverter with feedforward and frequency control techniques.," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 57, no. 9, pp. 1915–25, Sep. 2010.

[32] A. W. Burton, "Innovation drives for electric power-assisted steering," *IEEE Control Syst. Mag.*, vol. 23, no. 6, pp. 30–39, Dec. 2003.

[33] F. Gao, P. C. Loh, R. Teodorescu, F. Blaabjerg, and D. M. Vilathgamuwa, "Topological Design and Modulation Strategy for Buck–Boost Three-Level Inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1722–1732, Jul. 2009.

[34] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[35] J. A. Pomilio and G. Spiazzi, "High-precision current source using low-loss, single-switch, three-phase AC/DC converter," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 561–566, Jul. 1996.

[36] G. Bhuvaneswari, B. Singh, and S. Singh, "Three-phase single stage medium power supply using Cuk converter," in *2012 IEEE 5th India International Conference on Power Electronics (IICPE)*, 2012, pp. 1–6.

[37] U. Kamnarn, S. Yousawat, Y. Kanthaphayao, and V. Chunkag, "Redundant three-phase AC to DC converter using single-phase CUK rectifier module with minimized DC bus capacitance," in *2009 IEEE International Conference on Industrial Technology*, 2009, pp. 1–6.

[38] U. R. Prasanna and A. K. Rathore, "A Novel Single-Reference Six-Pulse-Modulation (SRSPM) Technique-Based Interleaved High-Frequency Three-Phase Inverter for Fuel Cell Vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5547–5556, Dec. 2013.

[39] K. Schenk and S. Cuk, "A simple three-phase power factor corrector with improved harmonic distortion," in *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*, 1997, vol. 1, pp. 399–405.

[40] N. Mohan and S. Gandikota, "High frequency ac-link transformer isolated three phase inverter with natural commutation of leakage energy," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, 2014, pp. 1.10.03–1.10.03.

[41] L. Wang, H. W. Chen, and D.-J. Lee, "Implementation of a DSP-based power converter for a wind induction generator," in *2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, 2008, pp. 1–6.

[42] A. K. Kaviani and B. Mirafzal, "Stability analysis of the three-phase single-stage boost inverter," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 918–923.

[43] M. Jang and V. G. Agelidis, "A Boost-Inverter-Based, Battery-Supported, Fuel-Cell Sourced Three-Phase Stand-Alone Power Supply," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6472–6480, Dec. 2014.

REFERENCES (continued)

[44] C. Cecati, A. Dell'Aquila, and M. Liserre, "A Novel Three-Phase Single-Stage Distributed Power Inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1226–1233, Sep. 2004.

[45] B. Mirafzal, M. Saghaleini, and A. K. Kaviani, "An SVPWM-Based Switching Pattern for Stand-Alone and Grid-Connected Three-Phase Single-Stage Boost Inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1102–1111, Apr. 2011.

[46] J. M. A. Myrzik, "Novel inverter topologies for single-phase stand-alone or grid-connected photovoltaic systems," in *4th IEEE International Conference on Power Electronics and Drive Systems. IEEE PEDS 2001 - Indonesia. Proceedings (Cat. No.01TH8594)*, 2001, vol. 1, pp. 103–108.

[47] J. M. A. Myrzik and M. Calais, "String and module integrated inverters for single-phase grid connected photovoltaic systems - a review," in *2003 IEEE Bologna Power Tech Conference Proceedings,* 2003, vol. 2, pp. 430–437.

[48] S. Cuk, "A new zero-ripple switching DC-to-DC converter and integrated magnetics," *IEEE Trans. Magn.*, vol. 19, no. 2, pp. 57–75, Mar. 1983.

[49] S. Mehrnami and S. K. Mazumder, "Modulation scheme of the differential-mode Ćuk inverter for loss mitigation," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 3419–3425.

[50] B. W. Williams, "DC-to-DC Converters With Continuous Input and Output Power," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2307–2316, May 2013.

[51] F. Barzegar and S. Cuk, "A new switched-mode amplifier produces clean three-phase power," in *ninth International Solid-state Power Electronics Conference*, 1982.

[52] A. Darwish, D. Holliday, S. Ahmed, A. Massoud, and B. Williams, "A Single-Stage Three-Phase Inverter Based on Cuk Converters for PV Applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2014.

[53] S. Mehrnami and S. K. Mazumder, "Harmonic-compensation based control of a nonlinear differential-mode Ćuk inverter," in *2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2013, pp. 1–3.

[54] S. Ćuk and R. Erickson, "A conceptually new high-frequency new zero-ripple switching dc-to-dc converter and integrated magnetics," in *5th nat. Solid-State Power Conv. Conf. (Powercon 5)*, 1978, p. G3.22.

[55] S. Mehrnami and S. K. Mazumder, "Discontinuous Modulation Scheme for a Differential-Mode Ćuk Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1242–1254, Mar. 2015.

[56] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.

[57] S. K. Mazumder, "High-frequency inverters: From photovoltaic, wind, and fuel-cell based renewable and alternative-energy DER/DG systems to battery-based energy-storage application," in *Power electronics handbook, Editor M.H. Rashid*, M. H. Rashid, Ed. Academic Press, Burlington, Massachusetts, 2010.

[58] S. K. Mazumder and P. T. Sivasubramanian, "A modular approach for current-source multi-phase inverter," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 5698–5701.

REFERENCES (continued)

[59] D. Chen and G. Wang, "Differential Buck DC–DC Chopper Mode Inverters With High-Frequency Link," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1444–1451, May 2011.

[60] J. Knight, S. Shirsavar, and W. Holderbaum, "An Improved Reliability Cuk Based Solar Inverter With Sliding Mode Control," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1107–1115, Jul. 2006.

[61] V. Valouch, Z. Muller, J. Svec, and J. Tlusty, "Evaluation of IRP, FBD, SD, and generalized non-active power theories," in *2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel*, 2012, pp. 1–5.

[62] S. Mehrnami and S. K. Mazumder, "A Control Mechanism to Compensate Nonlinearity of Discontinuous Modulation based Grid-Connected Differential-Mode Ćuk Inverter," in *IEEE Energy Conversion Congress Assotioation and Exposition*, 2014.

[63] Nam-Sup Choi and Yulong Li, "Modeling and analysis of AC line conditioner based on three-phase PWM cuk AC-AC converter," in *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004*, 2004, vol. 2, pp. 1646–1651.

VITA

NAME	Siamak Mehrnami
EDUCATION	B.Sc. Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran, 2006 M.Sc. Electrical and Computer Engineering, University of Tehran, Tehran, Iran, 2009 Ph.D. Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, Illinois, 2015
TEACHING	Department of Electrical and Computer Engineering, University of Tehran, Laboratory of Electrical Drives for Graduates, 2009 Department of Electrical and Computer Engineering, University of Illinois at Chicago, Power Electronic Laboratory for Undergraduates, Electronics Laboratory for Undergraduates, Energy Conversion Laboratory for Undergraduates, 2012-2014
HONORS	Best Paper Award in PEDG 2013
PROFESSIONAL MEMBERSHIP	IEEE Persian Gazelle II Solar Car Team Member and Contractor
PUBLICATION	S. Mehrnami and S. K. Mazumder, "Discontinuous Modulation Scheme for a Differential-Mode Ćuk Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1242–1254, Mar. 2015. S. Mehrnami and S.K. Mazumder, "Modulation scheme of the differential-mode Ćuk inverter for loss mitigation," in IEEE Energy Conversion Congr. and Expo. (ECCE), Sept. 2013, pp. 3419-3425. G. Farivar, B. Asaei, and S. Mehrnami, "An Analytical Solution for Tracking Photovoltaic Module MPP," IEEE Journal of Photovoltaics, vol.3, no.3, pp.1053-1061, July 2013. S. Mehrnami and S.K. Mazumder, "Harmonic-Compensation based Control of a Nonlinear Differential-Mode Ćuk Inverter," in IEEE 4rd Int. Symp. on Power Electron. for Distributed Generation Systems (PEDG), July 2013. S. K. Mazumder, and S. Mehrnami, "A low-device-count single-stage direct-power-conversion solar microinverter for microgrid," in IEEE 3rd Int. Symp. on Power Electron. for Distributed Generation Systems (PEDG), 25-28 Jun. 2012, pp.725-730. S. Mehrnami, and S. Farhangi, "Innovative Decision Reference Based Algorithm for Photovoltaic Maximum Power Point Tracking," Journal of Power Electron., no.5, pp.528-537, 2010. S. Mehrnami, and S. Farhangi, "A fast maximum power point tracking technique for PV powered systems," in IEEE 35th annu. Conf. Ind. Electron. (IECON), Nov. 2009, pp.42-46.