Thermal Transport and Power Dissipation in Two-Dimensional (2D) Materials and Interfaces

BY

Poya Yasaei
B.S., Sharif University of Technology, Tehran, Iran, 2012
M.S., University of Illinois at Chicago, Chicago, IL, USA, 2015

THESIS

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Defense Committee:

Amin Salehi-Khojin, Chair and Advisor
Kenneth Bresinsky
Farzad Mashayek
W.J. Minkowycz
Constantine M. Megaridis
Zlatan Aksamija, University of Massachusetts at Amherst

To parents,

To my loving wife, Nazanin

To my sister, Saba

and to my friends.

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CONTRIBUTION OF AUTHORS

Major parts of the results and discussions in this thesis are taken from my published or submitted papers with written permission from the journals (see Appendix). Below, the contributions of all the co-authors are listed:

Authors' contributions in chapter 2 (taken from reference [1]): A.Salehi-Khojin, R.Hantehzadeh, P.Yasaei, and F.Khalili-Araghi conceived the idea. A.Salehi-Khojin led the synthesis, fabrication, characterization, and experiments. F.Khalili-Araghi led the MD simulations. Z.Aksamija led the BTE modeling and calculations. C.D.Foster led the FE simulations. D.Estrada contributed on the fabrication and experimental procedures. P.Yasaei and R.Hantehzadeh synthesized graphene flakes and developed the fabrication process and experimental setup. P.Yasaei and R.Hantehzadeh fabricated final devices and performed the experiments. A.El-Ghandour developed the FE model and carried out the parameter optimization and data extraction process (with P.Yasaei). A.Fathizadeh performed the MD simulations. A.K.Majee carried out the BTE modeling and calculations. All authors contributed to the write up of the manuscript.

Authors' contributions in chapter 3 (taken from reference [2]): A.Salehi-Khojin and P.Yasaei conceived the idea. A.Salehi-Khojin led the synthesis, fabrication, characterization, and experiments. F.Khalili-Araghi led the MD simulations. Z.Aksamija led the BTE modeling and calculations. C.D.Foster led the FE simulations. P.Yasaei synthesized graphene flakes, developed the platform design, fabrication process, and experimental setup. A.Behranginia. synthesized MoS_2. P.Yasaei fabricated all the devices and performed the experiments. A.El-Ghandour developed the FE model and carried out the parameter optimization and data extraction process (with P.Yasaei). K.Karis and A.Fathizadeh performed the MD simulations. C.J.Foss and A.K.Majee carried out the BTE modeling and first principles calculations. All authors contributed to the write up of the manuscript.

Authors' contributions in chapter 4 (taken from reference [3]): A.Salehi-Khojin and P.Yasaei conceived the idea. A.Salehi-Khojin led the synthesis, fabrication, characterization, and experiments. C.D.Foster led the FE modeling. P.Yasaei, A.Behranginia, and Z.Hemmat synthesized the graphene flakes. P.Yasaei fabricated all the devices and performed the experiments. A.El-Ghandour developed the FE model and carried out the parameter optimization and data extraction process (with P.Yasaei). All authors contributed to the write up of the manuscript.

Authors' contributions in chapter 5 (taken from reference [4]): A.Salehi-Khojin A.Behranginia conceived the idea. A.Salehi-Khojin led the material synthesis, device fabrications, electrical measurements and device characterizations. A.Behranginia synthesized the MoS_2-graphene lateral heterostructure and performed electrical experiments. A.Behranginia and P.Yasaei carried out device fabrications and characterizations. P.Yasaei and T.Foroozan synthesized the CVD graphene. A.K.Majee performed band structure alignment, mobility, and interfacial resistance calculations. V.K.Sangwan performed 1/f noise and breakdown measurements and analysis. C.J.Foss carried out DFT and transmission coefficient calculations. Z.Aksamija conceived and supervised the calculations. M.C.Hersam supervised the 1/f noise and breakdown measurements and analysis. F.Long performed KPFM measurements and R.Shahbazian-Yassar supervised him. S.Fuladi helped in DFT calculations. M.R.Hantehzadeh helped in CVD MoS_2 and graphene synthesis.

SUMMARY

This dissertation presents the study of thermal and electrical transport phenomena in the systems based on atomically thin two-dimensional (2D) materials with a focus on the roles of heterogeneities such as grain boundaries (GBs), interfaces, and junctions. The studies are mainly focused on chemical vapor deposited (CVD) graphene and molybdenum disulfide (MoS_2) monolayers, while having implications in a wide range of 2D-material-based systems. The nanoscale thermal transport experiments are performed using custom-designed electrical thermometry platforms followed by 3D finite element (FE) analyses on models with the exact geometrical dimensions as in the fabricated devices. Electrical measurements are carried out in back-gated field effect transistor (FET) platform.

In particular, a simultaneous comparison of thermal transport was performed in supported single crystalline graphene and a bi-crystalline graphene having an individual GB. The experiments show that thermal conductance (per unit area) through an isolated GB can be up to an order of magnitude lower than the theoretically anticipated values for one ring of defects and depends on the crystalline mismatch angle. In collaboration with Prof. Aksamija (Boltzmann transport equation –BTE– modeling), it is uncovered that the boundary roughness scattering dominates the phonon transport in low-mismatch GBs, while for higher mismatch angles there must be an extra resistance caused by the formation of a disordered region at the GB. These results have major implications on the use of CVD graphene (which exhibits a polycrystalline structure) for thermal management of power dissipation in nanoelectronic devices.

The thermal transport is also studied in the through-plane direction which accounts for a major fraction of power dissipation from hot-spots in devices made of 2D materials with larger than ~100 nm characteristic length. First, the focus was on the interfacial thermal transport characterization of graphene and MoS_2 monolayers which may serve as the bottle-neck of dissipation in the through-plane direction. Despite the importance and implications

in many areas, there is an enormous discrepancy in the literature on the interfacial thermal transport characteristics of MoS_2 and other transition metal dichalcogenides (TMDs). The effect of interface coupling and metal encapsulation on thermal boundary conductance (TBC) across MoS_2 and graphene monolayers was also investigated.

Moreover, a system-level analysis of heat transport in the through-plane direction is also carried out to quantify the thermal dissipation limits in 2D-material-based structures on different technologically-viable substrates, e.g., diamond, aluminum nitride (AlN), sapphire, and silicon with different oxide types/thicknesses. It is demonstrated that the heat dissipation through graphene on AlN substrate near room temperature outperforms those of CVD diamond and other studied substrates, owing to its superior TBC.

Apart from the thermal transport characterization of 2D materials, a method is developed for reliable fabrication of high-quality lateral interfaces between graphene and MoS_2 monolayers through seed-free consecutive CVD processes. Their electronic properties are also comprehensively investigated through a combination of various experimental techniques and theoretical modeling. The results show that the MoS_2-graphene devices exhibit an order of magnitude higher mobility and lower noise metrics compared to the conventional MoS_2-metal devices as a result of energy band rearrangement and smaller Schottky barrier height at the contacts. These findings suggest that MoS_2-graphene in-plane heterostructures are promising materials for the scale-up of all-2D circuitry with superlative electrical performance.

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ΔT	temperature rise
2D	two-dimensional
3ω	3-Omega
AFM	atomic force microscopy
Al_2O_3	aluminum oxide
ALD	atomic layer deposition
AlN	aluminum nitride
AP-CVD	atmospheric pressure chemical vapor deposition
Ar	argon
Au	gold
BeO	beryllium oxide
BP	black phosphorus
BTE	Boltzmann transport equation
CI	charged-impurity
CLS	classical least square
Cu	copper
CVD	chemical vapor deposition
DFT	density functional theory
EBL	electron beam lithography
FDTR	frequency domain thermoreflectance
FE	finite element
FET	field-effect transistor
FFT	fast Fourier transform
G/A	thermal conductance per unit area
GB	grain boundary
GNR	graphene nano-ribbon
hBN	hexagonal boron nitride
HOPG	highly ordered pyrolytic graphite
HRTEM	high-resolution transmission electron microscopy
I_{2D}	intensity of the 2D Raman peak in graphene
I_d	drain current
I_G	intensity of the G Raman peak in graphene

IPA	isopropyl alcohol
IR	infra-red
K	bulk thermal conductivity
K/mW	Kelvin per milliwatt
KPFM	Kelvin probe force microscopy
MD	molecular dynamics
MoO_3	molybdenum trioxide
MoS_2	molybdenum disulfide
NEMD	non-equilibrium molecular dynamics
rms	root mean square
R_{square}	linear regression
R_{TH}	thermal resistance
RWM	Rayleigh wave mode
SAED	selected area electron diffraction
SEM	scanning electron microscopy
Si	silicon
SiN	silicon nitride
SiO_2	silicon dioxide
SJEM	scanning Joule expansion microscopy
SO	surface optical
SThM	scanning thermal microscopy
STM	scanning tunneling microscopy
TBC	thermal boundary conductance
TBR	thermal boundary resistance
TDTR	time domain thermoreflectance
TEM	transmission electron microscopy
Ti	titanium
TMD	transition metal dichalcogenides
V_{ds}	drain-source voltage
V_g	gate voltage
ZA	flexural (out-of-plane) acoustic
Φ_B	Schottky barrier height

CHAPTER 1

INTRODUCTION

1.1. Relevance of Thermal Transport in Two-Dimensional Materials

According to Moore's law, the transistor count per chip doubles every two years[5]. The continuing shrinkage in size is pushing the silicon-based industry toward its physical limitations. Numerous efforts are now being dedicated to the development of two-dimensional (2D) materials for future electronic/optoelectronic devices[6], [7]. Among 2D materials, graphene has the highest charge carrier mobility[8], but the absence of a band-gap restricts its applications[9]. Thus, efforts are focused on developing other 2D materials which can provide complementary properties absent in graphene[6], [10]. Transition metal dichalcogenides (TMDs) are a large family of layered materials with the formula MX_2, where M is a transition metal (such as Mo or W) and X is a chalcogenide (S, Se, or Te). Both monolayer and few-layer TMDs are opening the possibility of developing systems with reduced dimensionality and a range of unique properties[6]. For example, the spin-orbit coupling effects can range from virtually nonexistent in graphene to quite significant in TMDs[11]. Moreover, TMDs possess a tunable energy gap which allows them to have high on-off ratios[12] for low-power logic and switching applications[13]. Combined with graphene and hexagonal boron nitride (hBN), heterostructures of TMDs offer unique emergent electronic properties[14]. For example, tunneling field effect transistors formed by stacking of these atomically thin 2D materials can enable energy-efficient transistors

for digital and analog circuit applications[15]. These intrinsically 2D devices are also highly desirable in flexible electronics[16].

While 2D heterogeneous materials provide intriguing opportunities for future high-power/high-frequency electronics, thermal management in these devices can become a challenge. In almost all device platforms that include 2D materials, heterogeneous junctions of metal-semiconductor and insulator-semiconductor are unavoidably used as elementary bricks that form complex electronic architectures[17], [18]. As a result, prior to utilization of 2D heterogeneous materials in practice, a deeper understanding of the limits set by dissipation and heat removal through various junctions and interfaces must be developed. Recent studies of thermal transport in graphene has illustrated the importance of 2D phonon physics, and has implications for the performance and reliability of 2D-material-based devices[19], [20]. However, the mechanisms of thermal transport and the roles of in-plane and out-of-plane phonons in TMDs and their heterostructures still remain largely unexplored. Understanding dissipation through various junctions and interfaces will enable us to design new classes of 2D material candidates with superior thermal transport properties suitable for future ultra-scaled (having feature sizes below 10 nm) and low-power electronics (requiring on-off current ratios exceeding 10^8) [10].

In addition to the intrinsic limits of thermal dissipation, 2D materials grown by Chemical Vapor Deposition (CVD) are not single-crystalline, but exhibit a polycrystalline structure due to nucleated growth in the CVD process [21]–[25]. The presence of grain boundaries (GBs) poses additional challenges to the thermal transport and heat removal

from devices fabricated from CVD-grown samples due to the scattering of heat-carrying phonons at the GBs. GB scattering puts additional extrinsic limitations on the ability of 2D materials to conduct heat and manage dissipation [26].

On the other hand, since 2D materials at their limit of thinness are essentially "all-interface" their interactions with the underlying substrates and encapsulating layers can largely affect their performance. Thus far, the effects of these interactions have been carefully considered in the design of the electronic functionality of the devices made of 2D materials.[27] However, it is equally important to consider the interfacial thermal transport characteristics of 2D materials in the design criteria, if one is to benefit from their intriguing properties, especially for high-power/high-frequency applications.[28]–[37]

1.2. Literature Survey

In general, 2D materials are the atomically thin version of layered crystals which have in-plane tight covalent bonds are weak cross-plane Van der Waals bonds.[38]–[40] Since the discovery of graphene monolayer and its amazing properties, [41] 2D materials have received massive attention in research which has led to the discovery of a wide range of 2D materials such as TMDs[42], hBN[43], and black phosphorus (BP - phosphorene)[44]. After the realization of atomically thin 2D materials through mechanical exfoliation, efforts were dedicated to synthesizing 2D atomic layers through scalable techniques such as CVD [22], [42], [43], [45]–[47] and liquid phase exfoliation[42], [48]–[50]. Development of the process for clean transfer of the 2D atomic layers [51]–[56] has made it possible to make various heterostructures with advanced device functionality.

Over the past decade, there have been countless reports on the structural and electrical characterization of the 2D materials and utilization of them and their heterostructures for various device applications.[9], [10], [21]–[23], [42], [57]–[72] In particular, the effects of interfaces[58], [64], [73]–[79] and grain boundaries [22], [25], [80]–[100] on the electronic properties were studied to a great extent. There has been a pronounced research interest on all-2D devices enabled by 2D material heterostructures. [9], [18], [40], [57], [58], [63], [64], [69], [73], [76], [77], [79], [101]–[104], [104]–[116] In the earlier stage, the interest were on fabricating vertical (Van der Waals) heterostructures by stacking the atomic layers on top of each other.[9], [52], [57], [58], [77], [109] In particular, 2D transistors based on out-of-plane graphene contacted MoS_2 have been reported with an improved performance compared to metal-contacted MoS_2 device.[17], [103], [110], [113], [117] However, the heterogeneous MoS_2-Graphene devices made by such methods have usually been fabricated with a micrometer-scale contact area, possibly to preserve the device mobility. This requirement could seriously limit the number of devices per chip for future high performance integrated electronics. Moreover, such methods impose sophisticated transfer and fabrication techniques resulting in costly mass production. To by-pass the fabrication challenges and performance/size limitations imposed by the vertical interfaces, researchers were looking into the scalable fabrication of lateral interfaces between different 2D materials. So far, lateral interfaces have been synthesized for 2D material pairs with high crystal similarity such as hBN and graphene[79], [106] as well as different sets of TMDs[77], [118]. Most recently, lateral metallic/semiconducting interface has been

demonstrated through chemical phase conversion of semiconducting 2H MoS_2 to the metastable metallic 1T phase and improved device performances were achieved, but the stability of the 1T phase can limit the applications of such structures[119]. The reports are currently focused on the development of lateral junctions between graphene and different semiconducting 2D materials such as MoS_2.[120]–[125]

The widespread application of 2D materials and their heterostructures in various applications requires a system level characterization of thermal transport and power dissipation in the relevant 2D-based structures and interfaces to understand the limits of operation and failure thresholds. [126]–[133] For several years, researchers have investigated the energy dissipation, transport, and conversion phenomena at the nanoscale, and particularly in reduced-dimensional materials and their interfaces.[127], [129], [131], [134], [135] In particular, this area of research has great implications for the operation and lifetime of the electronic, optoelectronic, and energy conversion/storage systems based on 2D materials.[6], [7]

In the early years, the experimental research efforts had been focused on the development of thermal transport measurement techniques such as time domain thermoreflectance (TDTR), 3-Omega (3ω), suspended bridge, and Raman thermometry.[136], [137] TDTR is a pump-probe technique in which a laser beam is used to heat a metal transducer and another beam is used to measure the change in the reflectance of the metal surface and contain temperature information.[138]–[140] The TDTR method is widely used to probe the thermal conductance across various interfaces

and thermal conductivity of thin films.[33], [129], [131], [141], [142] In the 3ω technique, a microfabricated metal electrode is used to apply electrical (Joule) heating and measure the temperature by monitoring the changes in the resistance of the electrode.[142], [143] This method is capable of measuring both, in-plane and cross-plane transport in thin films and other nanostructures. The suspended bridge method works similar to the 3ω technique but utilizes a measurement geometry that confines the heat from propagation in the parasitic pathways (e.g., cross-plane direction) in order to improve the sensitivity for in-plane thermal measurements.[29], [144]–[155] Among the challenges associated with the micro-bridge technique are the cleanness of the fabrication process and additional scattering sources due to the presence of polymeric residues.[156] In the Raman thermometry, the dependence of Raman signal to temperature is used as the thermometer, while the optical heating by the laser or in-situ Joule heating in the device under electrical operation results in a temperature rise. [157]–[161] The thermometry probe can either be a shift in the frequency of the Raman peaks or a change in the ratio of stokes and anti-stokes. In principle, Raman technique is capable of measuring both in-plane conductivity and thermal boundary conductance (TBC) in reduced dimensional systems by comparing the Raman measurements on suspended and supported materials. On the downside, uncertainty in the absorbed laser power and Raman peak shift lead to significant errors in the extracted thermal parameters[142] and large disagreements in the literature data.[157], [162]

On top of the development of experimental methods, there have also been numerous developments in theoretical and computational techniques such as molecular dynamics (MD) simulations Boltzmann transport equation (BTE) modeling to cover the length scales from nanometers up to device-level.[129], [142] So far, the thermal transport studies have covered steady-state and transient thermal transport in various devices and structures.[131] Different carriers of heat, namely electrons and lattice vibrations (phonons) have widely been studied.[127], [129]

So far, the thermal transport in various 2D atomic layers such as graphene [1], [26], [29], [30], [155], [157], [163]–[176], MoS_2 [36], [37], [133], [158], [159], [165], [169], [177]–[179] hBN [160], [180], [181], and BP [152], [161], [182] have been characterized. Undoubtedly, graphene is the most-studied 2D material from a thermal transport perspective.[1], [26], [29], [30], [155], [157], [163]–[175] For suspended single-layer graphene, an in-plane thermal conductivity of ~5300 $W.m^{-1}.K^{-1}$ was first reported by Balandin *et al.* through Raman thermometry technique, which exceeds those of diamond and highly ordered pyrolytic graphite (HOPG).[157] Seol *et al.* later discovered that thermal conductivity of supported graphene on silicon oxide reduces down to ~600 $W.m^{-1}.K^{-1}$ due to scattering of out-of-plane flexural phonons at the interface with the substrate.[29] The effects of geometry [164], [171], [183], [184] and impurity [185]–[187] on thermal transport in graphene-based structures have also been investigated.

Thermal transport in selected members of TMD family such as MoS_2 has also been explored in the past few years. For the case of monolayer MoS_2, reported values for the

room temperature thermal conductivity vary from 34.5 $W.m^{-1}.K^{-1}$ to ~62 $W.m^{-1}.K^{-1}$ through Raman technique.[36], [159] For multilayer MoS_2, the room temperature thermal conductivity is found in the range of 44-52 $W.m^{-1}.K^{-1}$.[151] For the case of WS_2, this value for monolayer and bilayer materials are found to be 32 and 53 $W.m^{-1}.K^{-1}$ respectively. [188] The lowest thermal conductivity among TMD materials is observed for WSe_2 in the cross-plane direction which is ~0.05 $W.m^{-1}.K^{-1}$ at room temperature.[189]

Other than in-plane and cross-plane thermal conductivity in the 2D materials, the TBC between the 2D materials and the underlying substrate could remarkably affect the overall heat dissipation performance of the 2D-based systems. In this regard, there had been several reports on the TBC measurements between graphene and substrates from different methods.[34], [35], [166], [172], [190] For instance, Koh *et al.*[35] used TDTR method and reported TBC values of ~25 $MW.m^{-2}.K^{-1}$ and ~100 $MW.m^{-2}.K^{-1}$ for heat conduction across Au/Ti/n-layer-Gr/SiO_2/Si (n between 1 to 10) and Au/Ti/SiO_2/Si interfaces, respectively. Yang *et al.*[166] also used frequency domain thermoreflectance (FDTR) and reported a value of 22±2 $MW.m^{-2}.K^{-1}$ for TBC across Au/Ti/Gr/SiO_2/Si (monolayer) and similar values up to 7 atomic layers. They also reported a TBC of ~80 $MW.m^{-2}.K^{-1}$ for the control experiment. Another paper by Cai *et al.*[172] reports a value of 28+16/-9.2 $MW.m^{-2}.K^{-1}$ for TBC across monolayer graphene on Au/SiN_x substrate using Raman thermometry technique. Chen *et al.*[34] also measured the TBC for the heat transport across sandwiched graphene between SiO_2 layers (SiO_2/Gr/SiO_2) to be ~100 $MW.m^{-2}.K^{-1}$. In spite of the above experimental reports where integration of a graphene film reduces the TBC across

the interface, it is suggested that graphene may improve the TBC in strongly coupled interfaces[191], while experimental verification of such cases is yet to come.

Despite the importance and implications in many areas, there is an enormous discrepancy in the literature on the interfacial thermal transport characteristics of MoS_2 and other TMDs.[36], [37], [133], [165] Through Raman thermometry technique, Zhang *et al.*[37] reported thermal boundary conductance (TBC) values in the order of 0.1-1 $MW.m^{-2}.K^{-1}$ for MoS_2 or $MoSe_2$ with SiO_2 and gold-coated SiO_2 substrates, far smaller than the previously reported values on graphene[34], [35], [166], [172], [190]. Taube *et al.*[36] in another Raman-based study obtained a value of ~2 $MW.m^{-2}.K^{-1}$ for TBC of monolayer MoS_2 on Si/SiO_2 substrate at 300K. Yalon *et al.*[133] also employed the Raman spectroscopy technique and estimated the TBC between AlO_x-coated monolayer MoS_2 and Si/SiO_2 substrate to be in the range of 14 ± 4 $MW.m^{-2}.K^{-1}$ at room temperature.

The paper by Judek *et al.*[165] reports the TBC values across graphene and MoS_2 multilayers to be 1.7 ± 0.2 $MW.m^{-2}.K^{-1}$ and 2.6 ± 0.2 $MW.m^{-2}.K^{-1}$, respectively. These values are almost an order of magnitude smaller than the TBC results across graphene monolayers. The lower TBC values in this report can be due to the volumetric contribution of the multilayer flakes which reduces the lumped TBC. The interface and adhesion forces of a multilayer are also not necessarily similar to those of monolayers due to less conformity of the flakes with the substrate.

Apart from the above-discussed intrinsic and extrinsic thermal parameters associated with 2D materials, it is of an utmost importance to understand how the heat generates in

2D-based devices during an electrical operation. This study would shed light on different sources of scattering and could potentially enable one to identify the hot-spots under the operation which has implications on the failure modes of the devices.[131] The temperature rise in graphene-based electronic devices has been extensively studied by various methods such as Raman spectroscopy[192], infra-red (IR) microscopy [31], [132], [133], [193] and atomic force microscopy (AFM)-based techniques such as scanning thermal microscopy (SThM)[194] and scanning Joule expansion microscopy (SJEM).[126], [128], [193] Researchers have also looked at the high-power operation and energy dissipation in 2D materials beyond graphene such as MoS_2 [133], [195], [196]and BP atomic layers.[197]

1.3.Research Objectives

In the light of numerous research reports on the roles of heterogeneities and interfaces on the electrical, chemical, mechanical and thermal properties of the 2D materials, it is safe to conclude that in many cases the extrinsic limitations imposed by such imperfections limit the overall performance and functionality of such 2D-based systems.

Graphene has served as the model 2D system for over a decade, and the effects of GBs on its electrical and mechanical properties are very well investigated. However, no direct measurement of the correlation between thermal transport and graphene GBs has been reported. In the second chapter, the aim was to understand how individual graphene grain boundaries affect the overall thermal transport characteristics of the monolayer graphene films. Measurements on individual GBs enables us to identify the correlations between the

thermal resistance imposed by the GBs and the crystallographic mismatch across the GB. Benchmarking the experimental results against theoretical predictions (carried out through collaboration) and literature data allows us to identify the governing mechanisms of the phonon scattering across GBs with different mismatch angles and morphological details.

Heat generated in the hot-spots of 2D circuitry generally spreads within the plane of the 2D materials and ultimately dissipates through the substrate and the contact electrodes.[33] The contributions of in-plane and through-plane transport on the overall thermal resistance (R_{TH}) is determined by a combination of geometrical dimensions as well as thermal properties of the materials and interfaces.[33], [131] In many device architectures (e.g., devices with characteristic lengths>100nm), the through-plane thermal transport predominantly defines the R_{TH}.[33] In these cases, the interfacial thermal resistances can significantly restrain the heat dissipation and lead to overheating of the device. Despite its importance, there is an enormous discrepancy in the literature on the interfacial thermal transport characteristics of MoS_2 and other TMDs (0.1 to 15 $MW.m^{-2}.K^{-1}$).[36], [37], [198] This 1-2 orders of magnitude variation in the reported results demands a precise thermal transport study on MoS_2 in order to produce reliable data at different temperatures and to identify the possible sources of such disagreements. Particularly, if the values in the range of 1 $MW.m^{-2}.K^{-1}$ stand for the TBC of MoS_2 with the substrate, the MoS_2-based circuitry would face enormous heat removal and thermal management challenges. In the third chapter, the research objective is to carry out a direct comparison between the TBC across graphene and MoS_2 monolayers in identical

conditions and investigate the effects of interface coupling, substrate properties, and encapsulation on TBC across MoS_2 and graphene monolayers.

In the cases where through-plane transport is dominant, optimizing the overall thermal resistance (R_{TH}) of the device requires a high-conductance substrate on top of a good thermal interface. One major challenge is that the heat in high-conductance substrates such as diamond is usually carried by high-frequency phonons which transmit poorly through the Van der Waals interfaces that bind 2D materials.[141], [199] In other words, a practical trade-off seems to exist between the bulk thermal conductivity of existing substrates and the interfacial conductance at their junction with the 2D materials. On top of this criterion, the microscopic details of the interface such as coupling (adhesion) forces, surface roughness, and the presence of potential contaminants also affect the thermal boundary resistances (TBRs) and consequently the R_{TH}. Thus, it is necessary to consider all the thermal resistances and their decisive parameters simultaneously in the design of the 2D-based systems, in order to maximize overall thermal dissipation. In the fourth chapter, the scope is to quantify the limits of power dissipation in monolayer graphene, a representative of 2D materials, fabricated on various technologically-viable substrates in order to identify the best structures from a thermal management perspective.

Other than the challenges imposed by the heat dissipation, one major bottleneck of the performance in nano-electronic devices made of 2D semiconducting materials such as (MoS_2) is the formation of a Schottky barrier at the MoS_2 junction with the metal contact electrodes due to the Fermi level pinning phenomenon[200]. Moreover, miniaturization of

the metal/2D-material junctions usually results in even larger contact resistances due to the weak Van der Waals forces. Metals also do not have enough mechanical bendability for use in flexible structures. To simultaneously address all these challenges, one should replace the conventional metal electrodes with their 2D counterparts to fabricate intrinsically 2D devices. The scalability and possibility of forming atomically narrow junctions with improved electrical performance should be considered in the design/development of the alternative fabrication routes. This objective has been addressed in chapter five.

Finally, in chapter six, the results and discussions are summarize and the main conclusions are stated.

CHAPTER 2

THERMAL TRANSPORT MEASUREMENTS ACROSS INDIVIDUAL GRAPHENE GRAIN BOUNDARIES

(Some parts of this chapter are taken from the published paper with the following citation:

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Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

2.1. Introduction

Thermal management [26], [29]–[32], [154], [155], [157], [164], [170], [171] of power dissipation in nanoelectronic devices[31], [155] is among the recently emerged potential commercial applications of graphene. In order to realize this potential, extensive research efforts have focused on the high-volume manufacturing of graphene. One of the most practical approaches for large scale production of graphene is through CVD and roll-to-roll processing techniques[54], [201]. In this approach, the outcome is primarily a polycrystalline film, where single crystalline domains are joined by defective GBs[25]. GBs have been shown to largely alter the physical properties of CVD-grown graphene films[23], [25], [26], [80], [81], [95], [96], [99], [202], [203]. So far, a wide range of research studies has been dedicated on how the GBs affect the electronic properties of graphene[23], [25], [80], [81], [84], [91], [95], [96], [202]–[204]. In this regard, strong carrier scattering and suppressed electrical conductivity are reported at GBs as a result of

modified density of states and formation of potential barriers in the vicinity of the GBs[80], [95]. However, efforts on understanding the role of GBs in the thermal transport across the graphene lattice have been limited to theoretical works[26], [205]–[208] and a few indirect experimental measurements [128], [209]. This is mainly because the direct experimental thermal transport study of GBs requires a novel measurement platform capable of separating the contribution of the GB from the graphene lattice itself.

In this chapter, the temperature-dependent thermal transport results of supported CVD-grown graphene for a single crystalline flake as well as two merged flakes having an individual GB are presented. A symmetric electrical thermometry platform fabricated on an ultra-thin freely suspended silicon nitride (SiN) membrane was employed to extract the role of individual GBs having different crystalline mismatch angles between the grains. The results demonstrate an order of magnitude variation in the heat conductance per unit area through the GBs, depending on their crystallographic mismatch angle. For instance, a few-nanometer-wide GB with a 21^{o} mismatch angle adds a thermal resistance to the graphene lattice that is equivalent to a 3.25 μm length extension of the single crystalline region. In contrast, the equivalent length for a GB with a 3^{o} mismatch angle is only 380 nm. The phonon Boltzmann transport equation (pBTE) modelling (In collaboration with Prof. Aksamija's group) uncover that the significant drop in the thermal conductance at high mismatch angle GBs can only be a result of multiple phonon boundary scattering events, caused by formation of a disordered (amorphous) structure in the merging region of two adjacent flakes[80].

2.2. Graphene Synthesis and Characterization

The graphene used in this study is synthesized through atmospheric pressure CVD method, similar to previous reports[23], [99]. By precise control over the growth time, hexagonally shaped graphene domains grown from random nucleation points are merged together forming the GBs with the high quality of stitching in the coalescing region of the grains. In more details, Partial coverage graphene films with distinguishable GBs are synthesized by ambient pressure CVD process on copper foils (from Alfa Aesar, product no. 46365). At first, copper foils are initially cleaned by 10 minutes soaking in 10% hydrochloric acid, rinsed in acetone and IPA, dried under nitrogen flow, and loaded into the chamber. The CVD chamber is then evacuated (down to 1 mtorr) for and then purged with forming gas (5% hydrogen diluted in Argon) up to the atmospheric pressure. The graphene growth takes place at 1050° by introducing 20 ppm diluted methane (in argon) for ~30-50 minutes. The samples are then rapidly cooled down in the protection of forming gas.

There exist a number of different possibilities in the growth process due to the random nature of the CVD process. A combination of scanning electron microscopy (SEM) and AFM characterizations was performed on the grown graphene GB structures to examine possible overlapping and weak stitching of the grains (i.e. existence of a pronounced density of vacancies). In all cases, SEM images show a pretty uniform contrast in the merging region of the grains, indicating the uniform and well-stitched GB structure (Figure 1a-c). In some cases, AFM topography maps show a bump on the merging site of the grains

which is the characteristic of the wrinkles, as similarly observed on the wrinkles of single grain regions (Figure 1d-f). However, no step profile was observed on the AFM mapping for possible overlap regions.

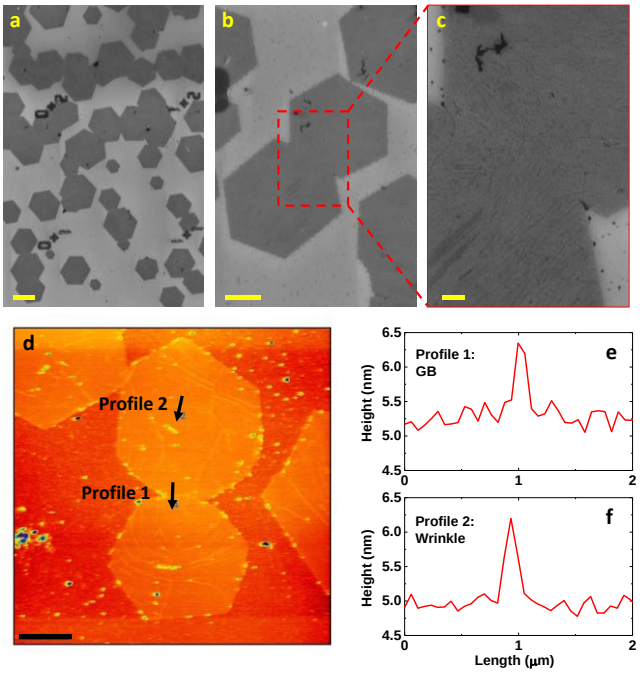

Figure 1. Topographic Characterization of Graphene GBs. (a-c) SEM images of the uniform and well-stitched graphene GBs. It is clear that overlapping or disconnection does not exist in the merging region of the flakes. Scale bars in (a), (b), and (c) are 20μm, 10μm, and 2μm, respectively. (d) The AFM topography image of two merged graphene GBs. The scale bar is 5μm. (e-f) the height profiles across the GB and across a wrinkle in the single crystalline grain.

Raman spectroscopy is also utilized to characterize the graphene and its GBs. Figure 2a shows the optical image of the coalesced graphene flakes. The Raman point spectra obtained from the graphene region and GB region are shown in Figure 2b. Apart from a small defect-induced D-peak at ~1350 cm^{-1} in the merging region of the flakes, the graphitic G and 2D peaks, respectively at 1580 and 2670 cm^{-1} with an intensity ratio

(I_{2D}/I_G) of >2 are observed in both spectra which correspond to monolayer graphene[23], [99], [210]. Figure 2c shows the spatially resolved Raman spectroscopy map obtained for the D-band (wavenumber ~1350 cm^{-1}). An intense I_D signal obtained in merging region of the grains provides a strong evidence for the defective nature of GB region. The occasional I_D signals at grains show some structural defects within the perfect lattice, which can be attributed to the nucleation points[23], [210]. The ratio of 2D-to G-band intensity (I_{2D}/I_G) is mapped where the high intensity ratio (> 2.5) all over the scanned area confirms the uniform existence of monolayer graphene (Figure 2d). The spatially resolved Raman maps were obtained using a Horiba JobinYvonXplora confocal Raman microscope equipped with a motorized sample stage from Marzhauser Wetzlar. The laser excitation wavelength was 532 nm and the maps were obtained for graphene GB samples transferred on SiO_2 substrate. The spectral resolution of the laser was 2.5 cm^{-1}, and pixel size of the map was 500 nm. D (~1350 cm^{-1}), G (~1580 cm^{-1}) and 2D-band (~2690 cm^{-1}) spatial maps were extracted.

Figure 2e shows selected area electron diffraction (SAED) patterns obtained from transmission electron microscopy (TEM) for both grains and GB regions. Identical and sharp hexagonal diffraction patterns recorded for the grains in different regions confirm their single crystalline nature[204]. However, a twofold diffraction pattern was observed when the aperture was located exactly at the merging region disclosing a crystallographic mismatch between the grains, another evidence for the existence of GBs.

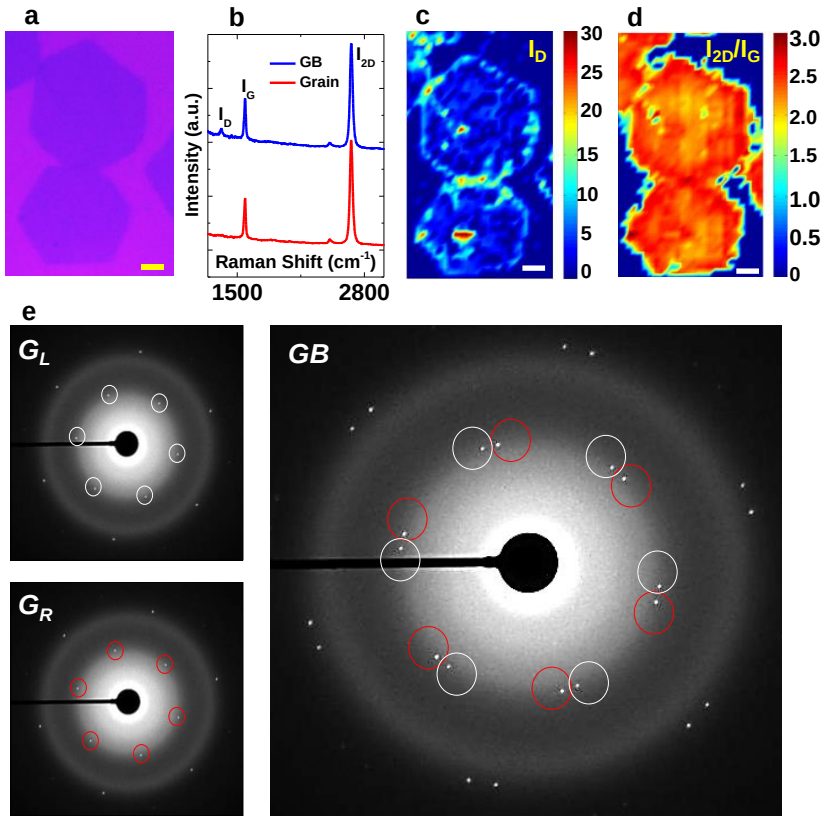

Figure 2. Structural Characterization of Graphene GBs. (a) Optical image of two merged hexagonal graphene grains, forming an individual GB (scale bar-5µm). (b) Raman spectra obtained from two points on graphene single crystalline grain and the vicinity of the GB. The spectra are normalized with the G-peak intensity at 1580 cm^{-1}. (c) D-band Raman mapping of the same graphene grains as shown in Figure 2a. The higher intensity in the merging region of the grains demonstrates the defective nature of the GBs. (c) 2D/G ratio mapping of the same region as shown in Figure 2a (Scale bars-5µm). The ratio in the range of 2.5 is associated with monolayer graphene. (d) Selected area electron diffraction (SAED) patterns obtained from left (G_L), right (G_R) grains and GB region. Sharp and single hexagonal shape evidences the single crystalline structure of grains. A pattern with two discrete sets of rotated spots appears in the merging region indicating the imperfect stitching of the two graphene grains which results in the origination of GB. This figure is reproduced from reference [99].

TEM images and diffraction patterns were acquired on an aberration-corrected JEOL JEM-ARM200CF, operated at 80 kV to avoid the beam damage effects. At first, graphene samples were transferred to a 30 nm thick Silicon Nitride membrane using a polymer assisted transfer technique. Further, samples were annealed at 350 °C for 3-4 hours in the presence of forming gas (5% H_2 in Argon) to clean the residual contamination and then samples grid was loaded into the microscope for characterization.

Based on the above characterization data, the GBs in the partially covered films can be distinguished by the geometry of the as grown hexagonal flakes. Due to a predominant zigzag edge preference in the growth process[23], [211], [212], the crystalline misorientation angle between the merged grains can be estimated by comparing the edge orientations of the flakes[23] (Figure 3). This is also consistent with our TEM analysis shown above [99].

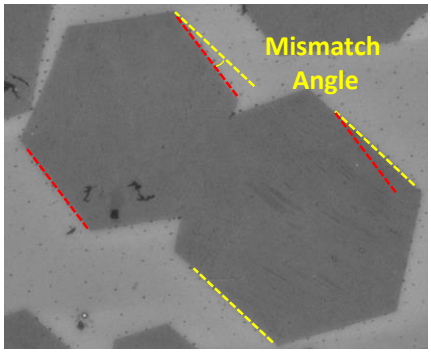

Figure 3. Estimating the Crystallographic Mismatch Angle from Morphology. SEM image of two merged hexagonally shaped single crystalline graphene grains forming an individual GB. The comparison of the edge orientations is used to estimate the crystallographic mismatch angle across the GB. The scale bar is 5 μm.

2.3. Design and Fabrication of the Electrical Thermometry Platform

To determine the role of GBs on thermal transport in graphene structures, a symmetric electrical thermometry platform was designed that allows for simultaneous examination of the thermal conductance through a single crystalline graphene flake (graphene region) and a bi-crystalline region, having an individual GB perpendicular to the direction of heat flow (GB region). To enhance the measurement sensitivity for in-plane thermal conduction, the platform is fabricated on a 100-nm thick suspended SiN membrane (500x500 μm^2), which practically confines the heat into a two-dimensional plane. Figure 4a shows a low-magnification optical image of the fabricated device under illumination from the top (reflection) and the bottom (transmission) of the membrane in order to produce maximum contrast. The targeted area for measurement is in the center of the window (within a 100 x 100 μm^2 square) to maintain the symmetry of the heat dissipation through the electrodes and the underlying substrate. Figure 4b magnifies the central part of the device by SEM, showing three thermometry metal electrodes and the graphene flakes, purposely colored for clarity. The central (red) electrode serves as the heater, while the right and left (yellow) electrodes serve as thermometers, operating at very low power with negligible joule heating. The inset of Figure 4b shows the as-grown flakes before oxygen plasma etching and electrode deposition. As indicated by dashed lines in Figure 4b, the electrodes are patterned in such a way that the role of an individual GB can be examined through a comparison between the left and right thermometers. The width of the graphene flakes are 11.5 μm and the distance between the electrodes are 5 μm. Figure 4c schematically shows

the cross section (side view) of the platform. The SiO_2 layer between the electrodes and graphene is essential for electrical insulation of the electrodes which are supposed to simultaneously operate without any interference.

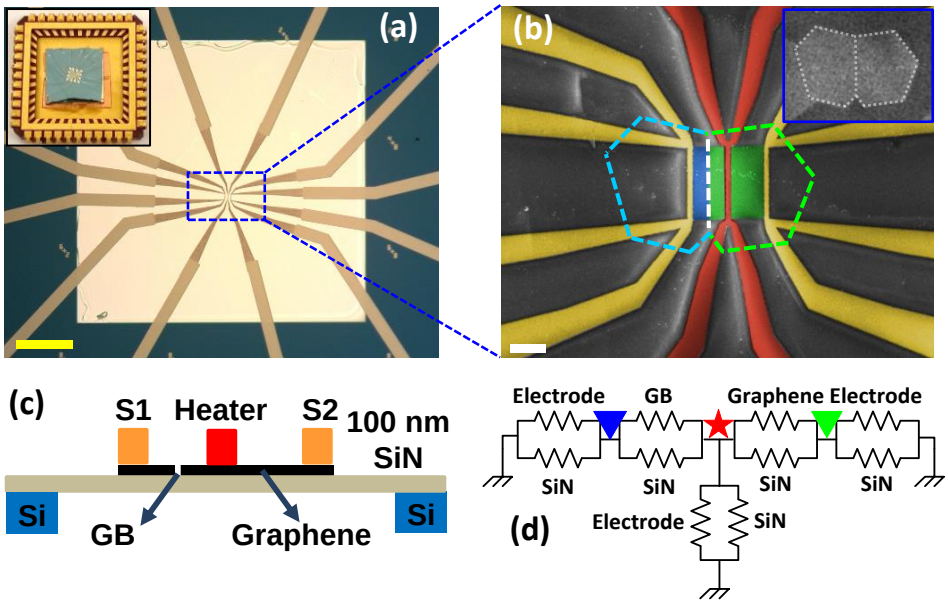

Figure 4. Electrical Thermometry Platform for Investigation of Individual Graphene GBs. (a) Low magnification optical microscopy image of a fabricated thermometry platform on a 100 nm thick silicon nitride (SiN) membrane. The scale bar is 100 μm. The inset shows the fabricated chip on a chip carrier with wire bonded electrical connections. (b) High magnification SEM image of a fabricated thermometry platform, comprised of a heater electrode in the center and two sensor electrodes on the sides having perfect symmetry. The scale bar is 5 μm. The inset shows the SEM image of the merged grains before oxygen plasma patterning and device fabrication. (c) Schematic side view of the thermometry platform. (d) A simple thermal resistance circuit that shows the paths of heat dissipation. The red star shows the heater position and the green and blue triangles show the position of the grain sensor and GB region sensor, respectively.

In more details, The graphene films (on Cu) were transferred to standard SiN membrane windows (from Silson Ltd.) using PMMA-assisted technique[53], followed by

an annealing process at 350°C for 90 minutes in the flow of forming gas (5% H_2 in Ar). The GBs are located by the geometrical shape of the merged flakes in the partially covered graphene film relative to predefined alignment marks. Electron beam lithography (EBL) followed by O_2 plasma cleaning is used to remove excess of graphene flakes and define the target flakes into a rectangle with desired geometry. In another step, electrode patterns are transferred onto the sample and SiO_2/Cr/Au (5/5/40 nm) electrodes are deposited using sputtering and electron beam evaporation systems. The devices are then annealed again to remove polymer residues by the fabrication process and are mounted on chip carriers by wire bonding. To carry out temperature-dependent thermal transport experiments, the devices are mounted on chip carriers using copper tape and thermally conductive grease (inset of Figure 2c). The devices are subsequently loaded in a cryostat system with a precise temperature controller. The simplified equivalent thermal circuit of the device is shown in Figure 4d, demonstrating two parasitic heat dissipation paths other than the graphene films.

2.4. Thermal Transport Experiments and Finite Element (FE) Analysis

In the cryostat, the thermal resistances associated with the chip-carrier and its contacts with the cold-finger on one side and with the sample on the other side causes a drift in the actual temperature of the chip below 100K, which is carefully corrected by using a reference cryogenic diode sensor. Heat flow measurements were performed at a temperature range of 44 to 305 K in an ultra-high vacuum (~10^{-7} mbar) on three devices, having GBs with mismatch angles of 3, 8, and 21º. Initially, the electrical resistances of all

electrodes are calibrated in a four-probe measurement configuration over the entire temperature range. This calibration enables us to accurately measure the temperature in the subsequent experiments by monitoring the changes in the resistance of the electrodes. Next, the ambient temperature is held constant and a range of electrical powers are dissipated into the heater. The temperature rises of the sensors are used to measure the temperature gradients as functions of the input thermal power. After carrying out the thermometry measurements, the graphene flakes are etched in low-power oxygen plasma and control experiments are repeated in identical conditions in order to determine the contribution of the underlying SiN membrane and the metal electrodes.

To accurately extract the thermal properties of the graphene single crystals and the GB regions, 3D Finite Element (FE) simulations were performed using the actual geometrical dimensions of the fabricated device (In collaboration with Prof. Foster's group). Initially, the data collected from the control experiments was used to find the temperature-dependent thermal conductivity of the SiN membrane. In more details, thermal conductivity values of the metal electrodes (using Wiedemann-Franz law)[32], [213] and the SiO_2 layer[214], [215] are introduced into the steady-state thermal analysis of FE model as known parameters, and the thermal conductivity of SiN membrane was found to match the experimental data. Next, the average thermal conductivities of the grain and the GB regions are fitted into the model in order to obtain the best match between the FE simulations and the experimental temperature gradients on the thermometers. In the FE analysis, a thermal interface resistance of 4×10^{-8} $m^2.K.W^{-1}$ is assumed between SiO_2-graphene and electrode-

SiO_2, which is in the range of typical values according to previous experimental reports[34], [35], [154]. It is worth noting that owing to the large contact areas in the designed platform, the extracted quantities are just slightly sensitive to the interface resistances. Modulating contact resistances in the range of 5×10^{-9} to 7.5×10^{-8} $m^2.K.W^{-1}$ (±87%) causes less than 3% change in the extracted thermal conductivities at 305K (details are provided below). This range is adequately wide to account for the temperature dependence of the contact resistances. The results of the FE simulations are plotted in Figure 5a-b. Figure 5a shows the vector plot of the thermal flux in a half-size FE model, clearly showing that more heat is being dissipated through the graphene region (right) compared with the GB region (left). The steady-state temperature distribution in the FE model is shown in Figure 5b.

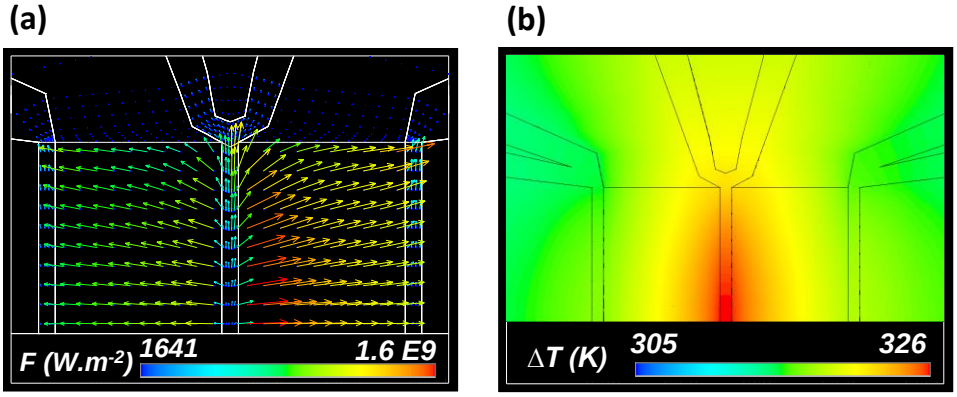

Figure 5. Finite Element (FE) Simulations and Analyses. (a) Vector plot of the thermal flux in a half-model FE simulation of the thermometry device, showing asymmetric heat dissipation through grain and GB regions. (b) Temperature distribution in the FE model.

2.4.1. Details of the Measurement Setup

An optical cryogenic refrigerator (from Janis, model: CCS-450) were used to carry out our temperature dependent thermometry experiments. The system provides a nominal temperature range of 10 to 500K using a closed loop Helium compressor and precise temperature controlling unit (Lakeshore 335). All the measurements are carried out in ultra-high vacuum (~10^{-7} mbar) to minimize the heat losses by convection. As shown in Figure 6a-b, the electrical connections are established through a chip-carrier/socket pair with thermally anchored wires. The chip carrier is mounted on top of the cold finger by applying sufficient vacuum compatible thermally conductive grease and is further fixed by a Teflon strip to provide normal force for a good contact. The Same grease is also used on top of the chip carrier to minimize thermal contact resistances between the silicon/SiN membrane chip and the chip carrier. The temperature drift between the sample position and the cold finger was tested all over the temperature range. The temperature difference between the cold finger (read by the cryostat) and top of the chip carrier (sample), was measured by a calibrated cryogenic temperature sensor (Omega model: CY7-SD7), mounted on the chip carrier. Figure 6c shows the temperature drift in temperatures lower than 100K. The corrected temperature profile has been used as the "sample temperature" throughout the manuscript.

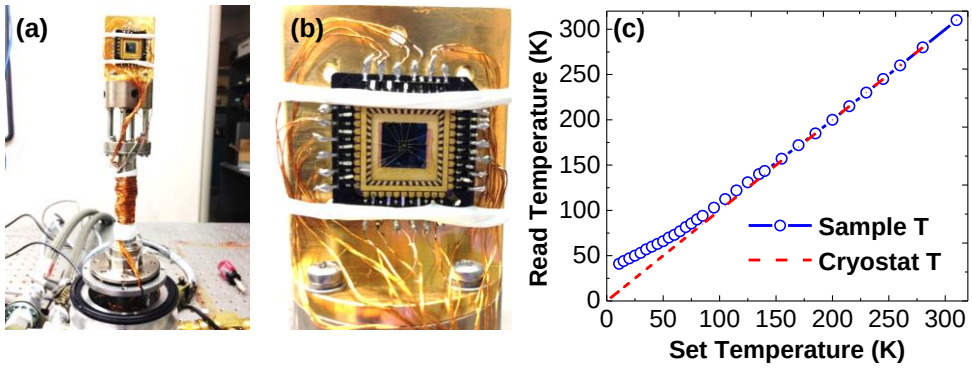

Figure 6. Details of Experimental Setup (a-b) Optical images of the measurement setup (c) Measured temperature drift between the sample and cold finger.

2.4.2. Details of the Measurement Process

To carry out the temperature dependent thermometry experiments, the electrical resistances of all electrodes are initially calibrated in four-probe measurement configuration over the entire temperature range, as shown in Figure 7a. Owing to the symmetric design, the electrodes have quite similar resistance values and follow similar trends. Figure 7b shows the current-voltage characteristics of the resistors at room temperature in multiple sweeps and also before and after a complete set of experiments. With a very good approximation, all of the trends are linear and overlapping, without hysteresis and drift. Calibration of the resistances with the temperature enables us to accurately measure the temperature in the subsequent experiments by monitoring the changes in the resistance of the electrodes. Next, the temperature is swept and at any of the desired temperature points, a range of electrical powers are dissipated into the heater, and the three resistances are monitored in 4-probe configuration. Figure 7c shows a representative signal obtained for the device with 3^{o} mismatch angle at 100K.

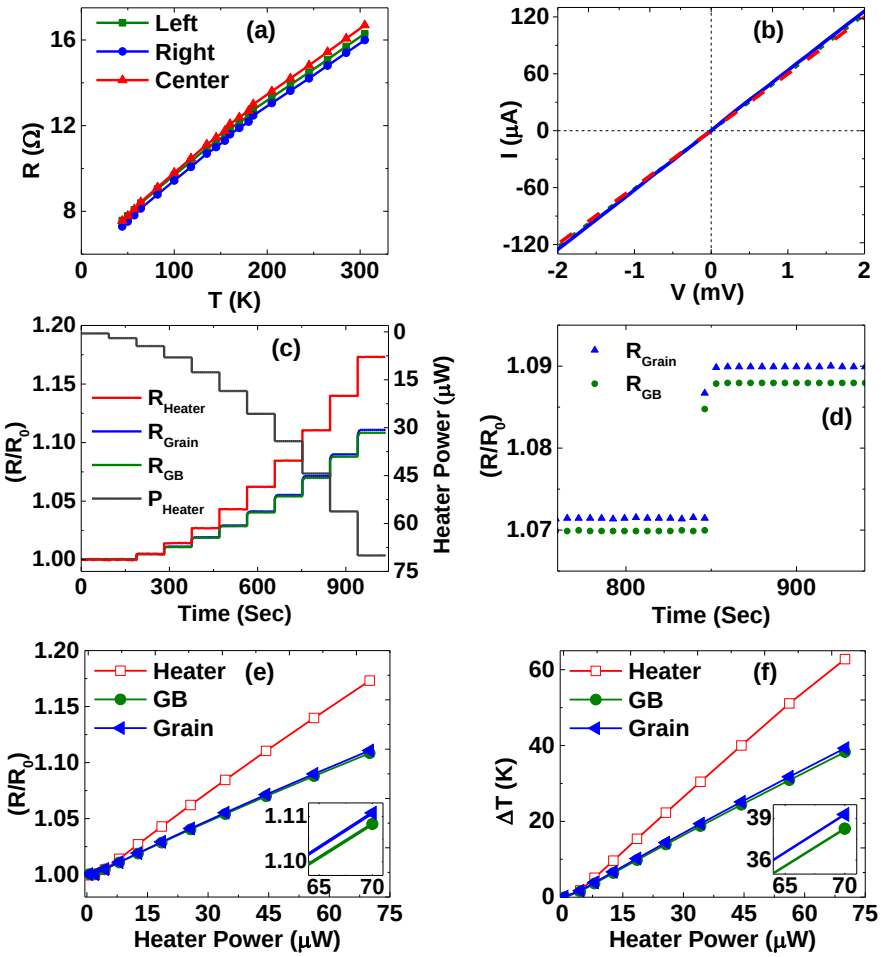

Figure 7. Details of the Thermal Transport Measurements. A representative set of data processing plots from the experiments for the device with 3º mismatch angle. (a) The resistance vs. temperature curves (calibration) for all the three electrodes (heater and sensors). (b) The I-V characteristics of the electrodes. (c) The time-dependent change in the normalized resistances of the electrodes at 100K. (d) Point plot of the normalized resistance as a function of time. The standard deviation of all the data point at each applied heater power is considered as the uncertainty of the measurement (4.9923×10^{-5}), which translated into a temperature resolution of 18mK. (e) The change in the normalized resistances of the three electrodes as functions of the heater input power. The inset shows the same curves. (f) The change in the temperatures of the electrodes as functions of applied power to the heater.

Owing to the ultra-thin structure of the platform and very small thermal capacity of the membrane, the transient time of the heat transfer is shorter than a second. The steady state heat conduction regime is reached immediately after changing the applied bias, as indicated in Figure 7c. The uncertainty of the measured R/R_0 based on the standard deviations of all the data points (an example is shown in Figure 7d) at that certain applied heater power (56.208 μW) is measured to be 4.9923×10^{-5}, which translates into 18mK fluctuations in the converted temperatures, according to its conversion slope which is:

$$\frac{\Delta T}{\Delta(\frac{R}{R_0})} = 363.0319K.$$

In the R-t trend of the three sensors, by eliminating the time, the changes in the resistance are plotted as a function of applied power, as shown in Figure 7e. Using the calibration curves, the temperature rises of the three electrodes as functions of applied power are obtained and plotted in Figure 7f. This final curve is used as the input for the FE analysis for all the devices in all temperature points.

2.4.3. Details of the FE Simulations

To extract the thermal properties of the graphene, GB region, and the SiN membrane, FE simulations were performed using the commercial ANSYS software. Considering the symmetrical design of the platform, the actual geometries of the fabricated devices are used to make a 3D half model in size of 500x250x0.1 μm^3 (Figure 8a). As shown in Figure 8b-c, the model consists of four layers of solid elements (Solid70), representing Gold, Chromium, SiO_2, and SiN from top to bottom, respectively. To model graphene flakes in

the model, shell elements (Shell57) are used to add a thin layer of 0.335 nm thick, on top of the SiN and underneath the electrodes. The swept mesh strategy is utilized to overcome the large aspect ratio of the elements. The mesh size is refined and the convergence of the results is tested.

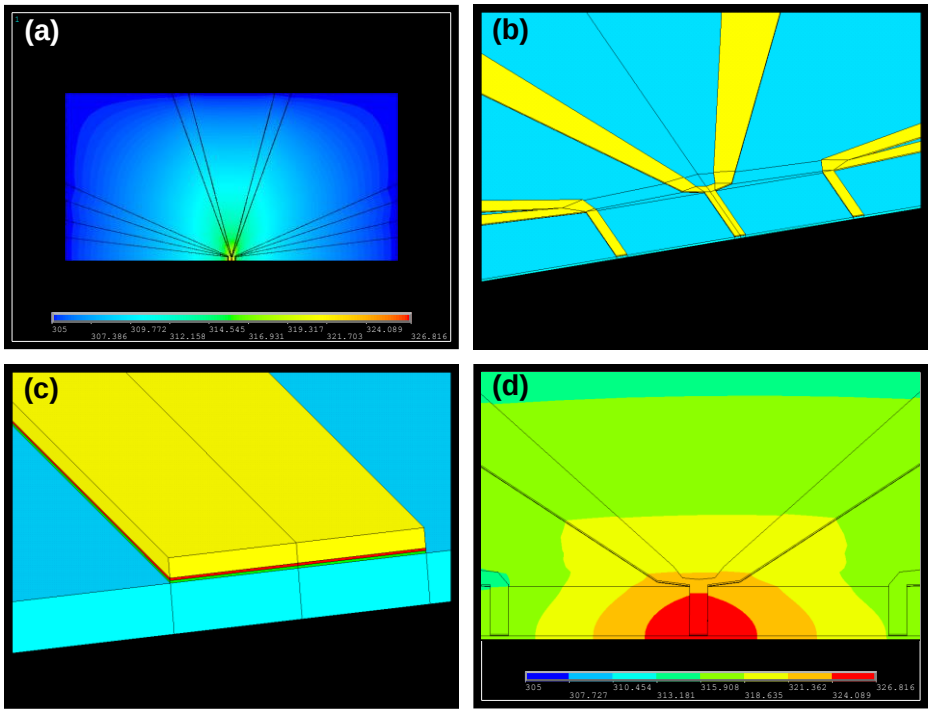

Figure 8. Details of In-Plane FE Analysis (a) The overview of the temperature distribution in the whole model. (b) Closer view of the central part of the model, which shows the electrodes in yellow and the SiN membrane in blue (c) Closer view of the electrodes, consisting of 3 layers of Au, Cr, and SiO_2, from top to bottom, shown in yellow, red, and green, respectively. (d) The temperature distribution in the central region of the model in a low number of color contours. The isothermal lines clearly demonstrate asymmetry in the temperature distribution.

To run the simulations, three boundaries of the membrane (all edges except the symmetry axis) are held at constant ambient temperature, and the symmetry boundary, as

well as the top and bottom surfaces, are isolated. Considering the geometry of the platform, applying a constant temperature to the borders of the membrane is a very reasonable assumption, as the membrane merges with a thick Si chip at those boundaries which practically is a heat sink. Negligible convection and radiation is also a reasonable assumption, as the temperature changes are small and the measurements are carried out in high vacuum. To mimic the joule heating of the heater electrode, a power density is applied to the heater which is inversely proportional to the width of the electrode. Solving the steady-state thermal analysis, the temperature distribution is found for several of the experimentally applied powers. The thermal properties of several of the materials that are well-characterized in the literature are input as known. Namely, the thermal conductivity of the metal electrodes is calculated from their electrical conductivity through Wiedemann-Franz law[32], [216], using an average Lorentz number $L = 2.7\times10^{-8}$ $W.\Omega.K^{-2}$. The temperature-dependent thermal conductivity of SiO_2 layer is also used according to former studies[29], [167], [214], [217]. A typical thermal contact resistance of 4×10^{-8} $m^2.K.W^{-1}$ was initially assumed to account for the SiO_2-graphene interface resistance[29], [32], [34], and the SiO_2-electrode interface resistance[35]. However, it was later noticed in the uncertainty analysis that even using much larger values in the range of $7.5\times10^{-8}m^2.K.W^{-1}$ only slightly changes the results (<3% at 305K and ~8% at 44K). This is due to the very weak sensitivity of the extracted quantities to this parameter, owing to the relatively large contact areas in the designed platform.

After developing the model, the data from the controlled experiment is first used to extract the temperature-dependent thermal conductivity of the underlying silicon nitride membrane. For this purpose, the SiN thermal conductivity is optimized to match the experimental temperature gradients on several of the applied powers. The optimization process stops when the errors in the temperature gradients between the simulations and experiments are smaller than 0.5%. Next, the experimental results of the graphene and GB region are used to match/extract the average thermal conductivity of the graphene region as well as the GB region. Figure 8d illustrates a set of temperature distribution which matches the experimental data. Intentionally, the distribution is indicated by only 8 contours in Figure 8d to demonstrate the asymmetry in the temperature distribution by the distinct isothermal lines.

2.4.4. Details of the Control Experiments

After carrying out the thermometry measurements and etching the graphene flakes in a low-power oxygen plasma, control experiments are performed in order to determine the thermal conductivity of the underlying SiN membrane. The thermal properties of the SiN thin films in the literature vary within a wide range, depending on the elemental composition of the film (i.e. X in SiN_x), deposition method and quality, thickness, and etc. Hence, direct extraction of its thermal conductivity in our devices is crucial. As shown in Figure 9, it is found the thermal conductivity of the SiN membrane through our control experiments and found its trend to be weakly dependent on the temperature, similar to the

previously observed trends[218].These values are used as the input for extraction of the thermal conductivity of graphene/GB-region.

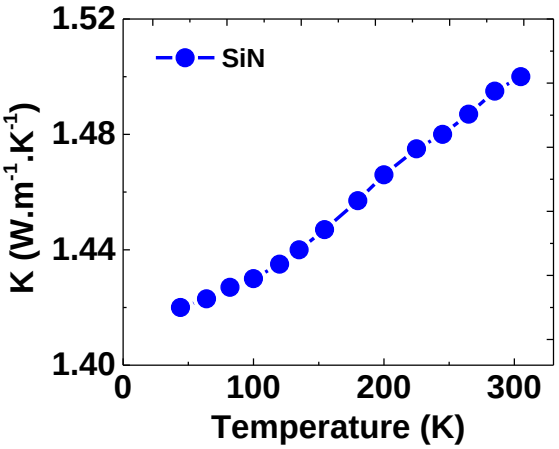

Figure 9. Extracted Thermal Conductivity of The SiN Membrane.

2.5. Analysis of the Experimental Thermometry Results

Figure 10a shows the extracted average thermal conductivity values of the graphene and GB regions for the three tested devices having misorientation angles of 3, 8, and 21º. The thermal conductivity of single crystalline graphene at room temperature is extracted to be 836±126 $W.m^{-1}.K^{-1}$. The error bars represent the overall uncertainties of the measurements and are fully discussed later in this manuscript. This Figure also reveals that a single GB can significantly decrease the thermal conductivity of the graphene structures, and its effect becomes more evident as the misorientation angle of the merged grains increases. To quantify the excessive thermal resistance caused by the GBs, the thermal resistance (*R*) of the measured films was calculated as a function of temperature in Figure

10b using a simple equation $R=L/(KWt)$ where L,W, and t are the length (5 μm), width (11.5 μm), and thickness (0.335 nm) of the graphene channel, and K is the average thermal conductivity values from Figure 10a. The resistance of the GB regions ($R_{GB\text{-}Region}$) can be thought as a superimposition of two components: (i) the isolated GB (R_{GB}) and (ii) it's adjacent graphene lattice (R_G). The contribution of the graphene lattice is directly found in the grain region of the device, hence, the contribution of the GB is obtained by subtracting the overall resistance of GB region from that of graphene region ($R_{GB}=R_{GB\text{-}Region}-R_G$).

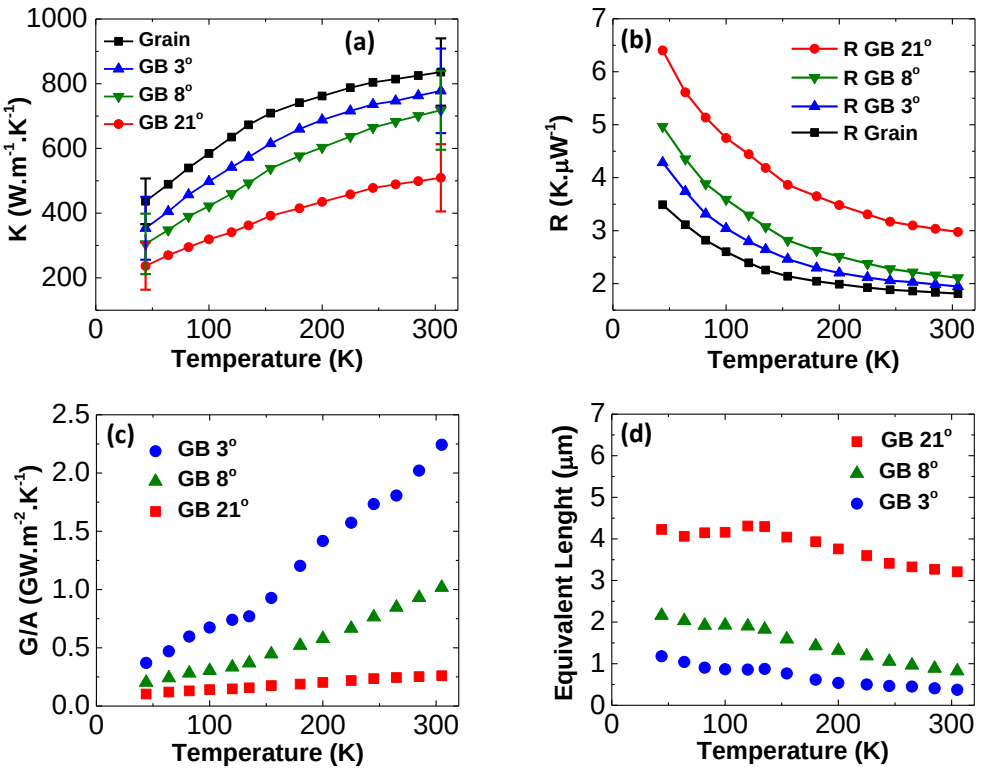

Figure 10. Extraction and Analysis of the Experimental Data. (a) Temperature-dependent extracted thermal conductivity of the single crystalline graphene and the GB region with different mismatch angles (3, 8, and 21 degrees). The error bars represent the overall uncertainty of the

measurements. (b) The thermal resistance of the GB regions and the single crystalline graphene grains. (c) The thermal conductance per unit area (*G/A*) of the different GBs. (d) The additional thermal resistance caused by an individual GB is shown as an equivalent extra length of the single grain with a similar width.

As a geometry-independent quantity, Figure 10c shows the thermal conductance per unit area (*G/A*) for the isolated GBs having different mismatch angles ($G=1/R_{GB}$). At room temperature, the measured *G/A* are 2.25, 1.02, and 0.26 $GW.m^{-2}.K^{-1}$, for the GBs with 3º, 8º, and 21º mismatch angles, respectively. A previous theoretical calculation predicted that thermal conductance through the GBs at room temperature varies 50% to 80% of the Ballistic limit (~4.2 $GW.m^{-2}.K^{-1}$), depending on the phonon transparency of the GB structure[26]. While the *G/A* for the GB with 3º mismatch angle lies within the predicted range (~53%), the results of the GBs with 8º and 21º mismatch are strikingly lower, in the range of 24% and 6% of the Ballistic limit, respectively.

Figure 10d shows the equivalent length of single crystalline graphene per unit width which causes the same thermal resistance as of the GBs. This representation reveals that a few-nanometer-wide GB with 21º mismatch angle imposes a huge thermal resistance, equivalent to 3.25 μm of single crystal CVD graphene, while this equivalent length is only 380 nm for a GB with 3º mismatch angle.

2.6. Uncertainty Analyses

The partial derivative method is used to calculate the sensitivity of the extracted quantities to different input parameters and to estimate the uncertainty of the analysis[32].

The sensitivities are calculated by perturbing each parameter with a small amount (∂x_i) around its typical value (x_i) and calculating the optimization/extraction process to find the corresponding change in the extracted conductivities (∂k). The dimensionless sensitivities are then calculated as follow:

$$s_i = \frac{x_i}{k}\frac{\partial k}{\partial x_i}$$

By knowing the sensitivity for each parameter, the overall uncertainty (u_k) in the extracted thermal conductivities can be calculated as follow:

$$\frac{u_k}{k} = \sqrt{\sum_i \left(s_i \times \frac{u_{x_i}}{x_i}\right)^2}$$

where u_{x_i} is the overall random and systematic uncertainty of the ith parameter around its typical value (x_i) and s_i is the sensitivity to that particular input.

Table 1. Uncertainty analysis for the device with 8º mismatch angle at 305K.

Input	Units	x_i (values)	u_{xi} (errors)	u_{xi}/x_i	$s_{i\text{-}Gr}$	$s_{i\text{-}GB}$	$c_{i\text{-}Gr} = \lvert s_{i\text{-}Gr}\rvert \times u_{xi}/x_i$	$c_{i\text{-}GB} = \lvert s_{i\text{-}Gr}\rvert \times u_{xi}/x_i$	$(c_{i\text{-}Gr})^2 / \Sigma(c_{i\text{-}Gr})^2$	$(c_{i\text{-}GB})^2 / \Sigma(c_{i\text{-}GB})^2$
K_{Metal}	W/m/K	252	10	3.97%	0.602	0.679	2.39%	2.69%	3.65%	4.70%
K_{SiN}	W/m/K	1.52	0.2	13.2%	0.904	0.895	11.9%	11.8%	90.4%	89.9%
K_{SiO2}	W/m/K	1.4	0.1	7.14%	0.017	0.017	0.12%	0.12%	0.01%	0.01%
$R_{contact}$	m^2.W/K	4×10^{-8}	3.5×10^{-8}	87.5%	0.034	0.032	3.01%	2.84%	5.8%	5.22%
δ_{Metal}	nm	45	2	4.44%	0.108	0.121	0.48%	0.54%	0.15%	0.19%
δ_{SiN}	nm	100	3	3%	0.014	0.014	0.04%	0.04%	0%	0%
δ_{SiO2}	nm	5	1	20%	<0.01	<0.01	0%	0%	0%	0%
$W_{Graphene}/2$	nm	5750	20	0.35%	n.a.	n.a.	0%	0%	0%	0%
$L_{Graphene}$	nm	5000	20	0.4%	n.a.	n.a.	0%	0%	0%	0%
$W_{Electrode}$	nm	500	5	1%	n.a.	n.a.	0%	0%	0%	0%

Table 1 summarizes the uncertainty analysis of different inputs, showing the typical values, errors, sensitivities, and the relative and absolute contributions of each parameter to the overall uncertainty at T=305K, for a representative device (8º mismatch angle). The overall uncertainties for all the data sets at the boundary points are shown as error bars in Figure 10a. The overall uncertainty ($\frac{u_k}{k}$) for the device with 8º mismatch angle is ~12.5% for both graphene region and the GB region at 305K. The errors have a ~90% relative contribution by the uncertainty of the measurement in the thermal conductivity of the SiN film (control experiments). These analysis also reveal than the extracted thermal conductivities at 305K are less than 3% affected by the interface resistances changing in the wide range of 5×10^{-9} to 7.5×10^{-8} $m^2.K.W^{-1}$. All the error bars shown in Figure 10a are calculated with same method. It should be mentioned that only the effect of thermal parameters and geometrical thicknesses were taken into account. Perturbing other dimensions of the device such as width and length of graphene and width of the electrodes was not feasible for us, as in each case the model need to be meshed from scratch. However, it is noted that the uncertainties of these parameters are all within 1%, and their sensitivities are also expected to be small. Hence their errors would minimally affect the overall results, and are considered to be zero in the analysis.

2.7. Theoretical Modelling (in collaboration with Prof. Aksamija's groups)

In order to explain the order of magnitude difference between our experiments and previous predictions[26], extensive theoretical modeling (in collaboration with Prof. Aksamija's groups) were carried out to elucidate the different phonon modes and their

scattering mechanisms involved in thermal transport across the graphene GBs. To calculate the in-plane thermal conductance across graphene GBs, the solution to pBTE is used in the presence of GBs.[219] The details can be found in the published paper.[1]

In general, thermal transport in supported graphene is characterized by the complex interplay between boundary roughness scattering and various internal scattering mechanisms (substrate, phonon-phonon, impurity, isotope scattering)[220]. It has been found that in wide supported graphene nanoribbons (GNRs), substrate scattering plays a dominant role over edge roughness scattering, while in narrow GNRs, edge roughness scattering plays a significant role. In the case of graphene GBs, it is crucial to determine the contribution of the phonon scattering at the GB compared to other scattering mechanisms[219]. It is also necessary to determine how different characteristics of the GBs affect the thermal transport. Direct imaging of graphene GBs has shown the atomic structure of the GBs can be comprised of a highly disordered and corrugated region[25], [80], [95], [96], which is in contrast to well-ordered and symmetric GB structures more commonly used in simulations. For a low angle of grain mismatch, this disordered region is narrow and can be treated as a thin GB (single ring wide) having a root mean square (rms) value of edge roughness Δ, whose value depends on the mismatch angle. When phonons encounter such GBs, they may scatter with the roughness, and the probability of this interaction depends on the direction of phonon propagation and its wavelength. Small wavelength phonons interact with the GB more strongly and are scattered randomly while large wavelengths can pass through the boundary unaffected. This interaction is captured

by the momentum-dependent specularity parameter, representing the fraction of incident phonons with wavevector $\vec{q}$ that will pass through the boundary unaffected, and is given by $p(\vec{q}) = \exp(-4\Delta^2 q^2 \cos^2\theta)$. As Δ increases, the specularity $p(\vec{q})$ rapidly tends to zero, indicating that all incident phonons will scatter diffusely once at the GB.

However, GB scattering is only one of several scattering mechanisms in supported graphene. Most notably, substrate scattering adds considerably to scattering of phonons in supported graphene[32]. The additional scattering from the thin GB can only reduce the total thermal conductivity from ~850 $W.m^{-1}.K^{-1}$ to ~750 $W.m^{-1}.K^{-1}$ due to the strong competing influence of the substrate. At higher angles of mismatch, atomic resolution images obtained from graphene GBs by scanning tunneling microscope (STM)[80] and TEM [25] show that a disordered boundary region can form, which can be wide enough to add a considerable amount of additional resistance to the heat flow.

The added thermal resistance due to the disordered graphene region of width W_D in the GBs is calculated from Cahill's minimum thermal conductivity model[221] by setting the scattering rate to the maximum value reached when the phonon lifetime equals one half of its period of vibration ($\tau_{max}^{-1} = \omega/\pi$). This model provides what is believed to be a lower bound on the thermal conductivity of the disordered region; hence the W_D calculated from the minimum thermal conductivity model can be thought of as a lower bound on the width of the disordered region at the GB.

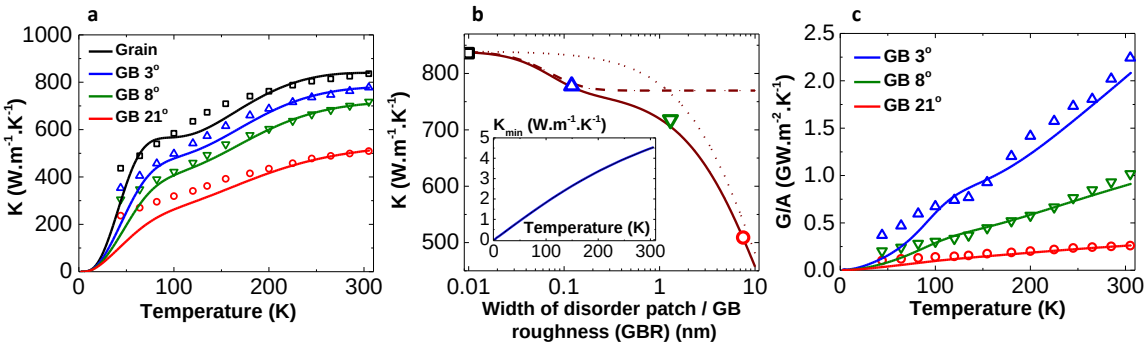

Figure 11. Boltzmann Transport Modelling Results. (a) Thermal conductivity vs. temperature calculated from the phonon Boltzmann transport model. The symbols in (a) and (c) represent experimental data from Figure 10 (a) and (c), while solid curves represent simulation results. (b) shows the thermal conductivity at room temperature vs. the GB roughness Δ and width of the disordered boundary region W_D. The solid curve shows total thermal conductivity plotted against both W_D and Δ, while dashed line shows thermal conductivity vs. Δ with W_D=0 and the dotted line shows thermal conductivity vs. W_D keeping Δ=0. Symbols represent experimental data at 300K. (c) Thermal conductance of the grain boundary vs. temperature.

Figure 11a shows the variation of thermal conductivity with temperature for various grain mismatch angles, including the one with no GB (single crystal). The total thermal conductivity in Figure 11a has been calculated as $K_{GB-Region} = W_G/(R_{GB-Region}.A)$, where $R_{GB-Region}$ is the total resistance due to graphene with GB and amorphous patch and is given by: $R_{GB-Region} = [(W_G - W_D)/(A.K_G)] + [W_D/(A.K_{min})]$. Here, W_G denotes the width of the graphene between heater and sensor (5μm), W_D is the width of the disordered region at the GB, and K_G denotes thermal conductivity of graphene without any GBs. K_{min} is the thermal conductivity of the disordered region from Cahill's minimum thermal conductivity model. Figure 8c shows the effective *G/A* through a GB as a function of temperature. The *G* is calculated as the reciprocal of the resistance arising due to GB

alone (R_{GB}) as $(G = 1/R_{GB})$, where $R_{GB} = [W_G/(A.K_{GB-Region})] - [W_G/(A.K_G)]$ and $K_{GB-Region}$ denotes total thermal conductivity in the GB region (as calculated above). It can be seen that the boundary conductance (*G/A*) results obtained from phonon BTE are in excellent agreement with the experimental data.

The effect of the GB on thermal conductivity due to different rms roughness (Δ) and the effect of disordered region due to its varying width (W_D) are complementary to each other because the effect of roughness saturates after Δ=0.25 nm. Figure 11b shows that for low values of Δ and W_D, the total thermal conductivity (solid curve) follows the thermal conductivity curve due to GB scattering alone (dashed curve), and for higher values of Δ and W_D, follows the thermal conductivity trend due to the width of disordered strip alone (dotted curve). Hence, for small values of Δ and W_D (up to 0.25nm), thermal conductivity is largely dominated by the GB scattering alone with negligible effect from the narrow disordered strip, in agreement with the experimental data for low mismatch angle. For higher values of Δ and W_D (beyond 0.25nm), GB scattering becomes completely diffuse (p=0), and the effect of boundary roughness saturates. There is a natural cross-over occurring at 1 nm, beyond which the thermal conductivity is governed dominantly by the additional resistance of the disordered region. This is in good agreement with the experimental data for large angle mismatch. Using the explained methodology, the experimental data for thermal conductance of the GB is well reproduced for the entire temperature range (Figure 11c). These results are also confirmed through MD simulation carried out by Prof. Khalili-Araghi's group.[1]

2.8. Summary and Conclusion

In summary, a symmetrical electrical thermometry technique was used to directly extract the temperature-dependent thermal resistance of graphene GBs with different crystalline mismatch angles. It was observed that the thermal resistance at highly misoriented GBs can be remarkably higher than previous theoretical predictions owing to the larger disorder found in the atomic structure of GBs in CVD grown graphene. BTE calculations indicate that a bimodal scattering mechanism governs the phonon transport through the GB: for small mismatch angles, the thermal resistance of the GB can be captured through phonon scattering from the GB roughness while for higher mismatch angles, the GB roughness effect is saturated. The lower thermal conductivity at higher mismatch angles can be explained by the presence of a narrow strip of disordered graphene at the GB. For the highest mismatch angle of 21^{o}, the width of the disordered region is calculated to be 7.5 nm based on the minimum thermal conductivity model. For intermediately misoriented GBs, thermal conductivity is affected by a complex interplay between the amount edge roughness and the amount of disorder in the disordered patch. Further study is required to probe the structure and morphology of the GB region.

CHAPTER 3

INTERFACIAL THERMAL TRANSPORT IN MONOLAYER MoS_2- AND GRAPHENE-BASED DEVICED

(Some parts of this chapter are taken from the published paper with the following citation:

Poya Yasaei, Cameron J. Foss, Klas Karis, Amirhossein Behranginia, Ahmed El-Ghandour, Arman Fathizadeh, Javier Olivares, Arnab K. Majee, Craig D. Foster, Fatemeh Khalili-Araghi, Zlatan Aksamija, Amin Salehi-Khojin, "Interfacial Thermal Transport in Monolayer MoS_2- and Graphene-Based Devices" *Advanced Materials Interfaces*, p. 1700334, Jul. 2017.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

3.1. Introduction

Since 2D materials at their limit of thinness (monolayer) are essentially "all-interface" their interactions with the underlying substrates and encapsulating layers can largely affect their performance. Thus far, the effects of these interactions have been carefully considered in the design of the electronic functionality of the devices made of 2D materials.[27] However, it is equally important to consider the interfacial thermal transport characteristics of 2D materials in the design criteria, if one is to benefit from their intriguing properties, especially for high-power/high-frequency applications.[28]–[37] Over-heating in 2D-based electronics could lead to chemical degradations and/or thermomechanical strains resulting in the failure of an operating device or deviation from the desired performance characteristics.[130]

Despite the importance and implications in many areas, there is an enormous discrepancy in the literature on the interfacial thermal transport characteristics of MoS_2

and other TMDs.[36], [37], [133], [165] Through Raman thermometry technique, Zhang *et al.*[37] reported TBC values in the order of 0.1-1 $MW.m^{-2}.K^{-1}$ for MoS_2 or $MoSe_2$ with SiO_2 and gold-coated SiO_2 substrates, far smaller than the previously reported values on graphene[34], [35], [166], [172], [190]. Taube *et al.*[36] in another Raman-based study obtained a value of ~2 $MW.m^{-2}.K^{-1}$ for TBC of monolayer MoS_2 on Si/SiO_2 substrate at 300K. Yalon *et al.*[133] also employed the Raman spectroscopy technique and estimated the TBC between AlO_x-coated monolayer MoS_2 and Si/SiO_2 substrate to be in the range of 14 ± 4 $MW.m^{-2}.K^{-1}$ at room temperature. This 1-2 orders of magnitude variation demands a precise thermal transport study on MoS_2 in order to produce reliable data at different temperatures and to identify the possible sources of such disagreements. Particularly, if the values in the range of 1 $MW.m^{-2}.K^{-1}$ stand for the TBC of MoS_2 with the substrate, the MoS_2-based circuitry would suffer from enormous heat removal and thermal management challenges. It is worth noting that these numbers are nearly 2 orders of magnitude smaller than the typical TBC values reported between graphene and substrates.[34], [35], [166], [172], [190]

In this chapter, the interfacial thermal transport across CVD MoS_2 and graphene monolayers is systematically studied using electrical thermometry experiments and 3D FE analyses (In collaboration with Prof. Foster's group). First, the results were validated on graphene with the well-established data in the literature obtained from different techniques (e.g., time domain thermoreflectance and Raman).[35], [166], [172] In identical measurement platform and experimental conditions, it is observed that the TBC across

MoS_2 remains in the same range as in graphene, far larger than the reports based on Raman thermometry with optical heating.[36], [37] To address the possible sources of discrepancy in the measured TBC values in the literature, the effect of processing quality and potential interface contaminants (affecting the interface couplings and adhesion forces) are studied on the measured TBC values through a comparison between direct-grown and transferred MoS_2 monolayers. The effects of the underlying substrate on the TBC across MoS_2 and graphene is also examined by performing identical experiments on two of the most technologically viable substrates, namely, Si/SiO_2 and c-plane sapphire. Finally, the effects of metal encapsulating layers on the TBC are investigated through a combination of MD simulations (in collaboration with Prof. Khalili's group) and BTE modeling (in collaboration with Prof. Aksamija's group) which reveal that that the emergence of Rayleigh wave modes (RWMs) dramatically contributes to the interfacial conductance across encapsulated 2D monolayers.

3.2. Synthesis and Characterization of Graphene and MoS_2

The MoS_2 and graphene used in this study were synthesized by atmospheric pressure CVD method with recipes described in our previous reports[99], [222]. The graphene flakes were synthesized by ambient pressure CVD process, similar to Chapter 2 of this dissertation and the previous reports.[1], [99] A typical PMMA-assisted[55], [56] method was used to transfer the graphene flakes to the desired substrates. For MoS_2 synthesis, a vapor phase CVD method[22], [223] was adopted, in which the sulfur flakes and molybdenum trioxide (MoO_3) powder are used as precursors. In this process, the target

substrates (Si/SiO_2 or sapphire) were placed upside-down in an alumina crucible having 2 mg of MoO_3 and then loaded in the center of a 3" quartz furnace. Another crucible having 1 g sulfur was also loaded in the upstream in a precisely calibrated location (to achieve the desired temperature profile). The furnace is then evacuated and purged with argon gas to reach to atmospheric pressure. The chamber temperature was then increased to 550 ^oC in 30 minutes and to 850 ^oC in the next 60 minutes under 70 sccm argon flow. The growth time was 10 minutes and the furnace was cooled down to the room temperature by natural cooling. MoS_2 flakes were either directly used for device fabrication or transferred using a PMMA-assisted method with KOH etching.[22] AFM and Raman spectroscopy revealed that the synthesized graphene and MoS_2 are highly crystalline monolayers, as evidenced by their sub-nanometer measured thickness and sharp Raman peaks. More specifically, Figure12a-b shows topographic AFM maps of MoS_2 and graphene single crystalline flakes with apparent thicknesses of 0.65 nm and 0.75nm, respectively. Raman spectroscopy is used to characterize the crystalline quality of the synthesized structures. For MoS_2, the signature peaks of E^1_{2g} and A_{1g} appear at ~384.6 and ~405.6 cm^{-1} which show a high-quality CVD MoS_2 which corresponds to a mono- or bilayer (Figure 12c).[22], [224] In case of graphene (Figure 12d), apart from a small defect-induced D-peak at ~1340-1350 cm^{-1}, the Raman spectra shows the graphitic G and 2D peaks, respectively at 1580 and 2670 cm^{-1} with an intensity ratio (I_{2D}/I_G) of >2, which correspond to monolayer graphene[23], [99], [210]. With the combination of Raman and AFM results, it is concluded that the MoS_2 and graphene samples are monolayers.

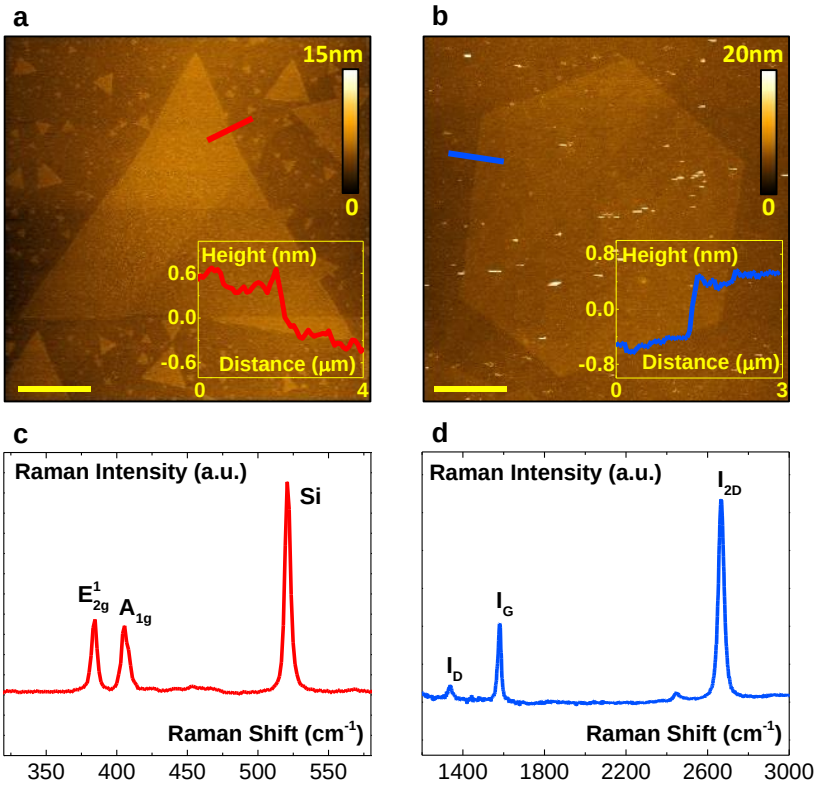

Figure 12. Characterization of MoS_2 and Graphene Flakes. (a-b) AFM topography maps of the direct-grown MoS_2 and transferred graphene flakes on Si/SiO_2 substrate. The scale bars are 5 μm. (c-d) Raman point spectra obtained from the synthesized MoS_2 (c) and graphene (d) flakes.

It is worth noting that the graphene flakes were synthesized on copper foils and then transferred to the target substrates via polymer-assisted wet transfer process.[225] The MoS_2 flakes were either directly synthesized on the target substrates or transferred via a similar polymer-assisted method.[22] This enables us to account for the contributions of interface contaminants and coupling forces on the interfacial thermal characteristics of MoS_2 with the substrate.

3.3. Design and Fabrication of Through-Plane Thermometry Platform

To measure the thermal transport across MoS_2 and graphene, a symmetrical serpentine-shape four-probe electrical thermometry platform was designed which simultaneously serves as the heater and the temperature sensor. Figure 13 shows different steps of the fabrication process for the thermometry platform. After the transfer processes, the samples are annealed at 300 in °C for 3 hours in presence of argon (for MoS_2) or forming gas (for graphene). The selected flakes are then patterned into a symmetrical (octagonal) shape through a standard EBL process followed by oxygen plasma etching. The resist is then dissolved in remover PG and the surface is then annealed again, as explained above, to remove the solvent residues and obtain a clean surface. In the second EBL process the electrode patterns are transferred onto the sample and metal (5/50 nm Ti/Au) is deposited. Finally, the excess of the flake is etched away in another oxygen plasma process to prevent in-plane thermal and current cross-talking.

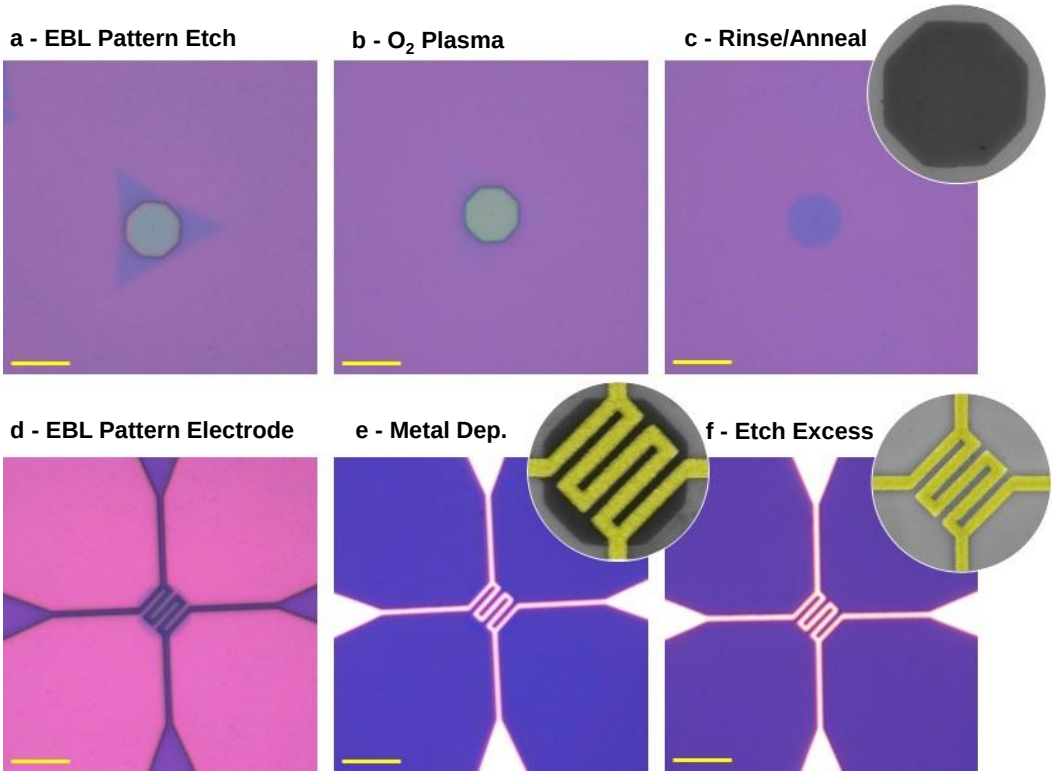

Figure 13. Different Steps of The Fabrication Process. The scale bars are 10 µm.

3.4. Through-Plane Thermometry Experiments

For temperature-dependent thermometry experiments, the devices were mounted on chip carriers using conductive epoxy and loaded into the cryogenic system with a precise temperature controller. The experiments are performed in high vacuum (~10^{-7} mbar) to minimize the heat losses by convection. The temperature rise was always kept under 40K which results in a negligible heat loss through radiation. The temperature of the cold finger is used as the cold source temperature (T_C) in all the measurements, while the hot source temperature (T_H) is measured at the heater/sensor through electrical thermometry. The chip carrier is mounted on the cold finger by applying sufficient vacuum compatible thermally

conductive grease and is further fixed by a Teflon strip to provide normal force for a good contact. The test substrate is fixed on the chip carrier with conductive epoxy, which provides an improved conductance compared to our previously used method by double-sided copper tape and thermal grease. In this modified configuration, the temperature drift in the system is negligible down to ~35 K, but to assure a minimal error for precise TBR extractions, only the data above 85 K is used in the analyses.

In the thermometry experiments, the temperature of the cryostat is swept from 25 K to 295 K and kept constant at desired temperature points. At each point, the temperature is regulated for 1 hour to assure thermal stabilization with a uniform temperature distribution in the entire chip carrier/substrate structure. Next, a range of electrical powers are dissipated into the heater, and the resistance is monitored in 4-probe configuration, as shown in Figure 14a. In small applied powers, the resistance of the heater does not change, revealing that the temperature rise due to Joule heating is approximately zero. This resistance can be correlated to the temperature of the cold finger, enabling the calibration of the heater electrode for temperature sensing (Figure 14b). Calibration of the resistance with the temperature allows for accurate temperature measurements in the higher applied powers where the temperature increases due to Joule heating (Figure 14c). The small size of the heater electrode results in a small thermal capacity in which the transient time of the heat transfer is in the order of few seconds. Hence, running the measurement for ~ 100s is long enough to obtain a steady-state response in the platform. Figure 14d shows the temperature rise of the electrode as a function of applied power which is used to obtain the

overall thermal dissipation resistance to the environment (R_{TH}). In other words, the R_{TH} represents the average temperature rise of the serpentine shape electrode when the unit power (e.g., 1mW) is being dissipated between the voltage leads of the platform. The small non-linearity in the Temperature-Power data at high dissipated powers - especially for low-temperature data - originates from the temperature dependence of thermal conductivity of the substrate materials (i.e., SiO_2). To avoid such issues, the data around 1mW dissipated power is used for extraction of thermal resistances throughout the manuscript where the temperature rise is less than 20 K over the entire temperature range.

In our thermometry experiments, the uncertainty of the measured resistance based on the standard deviations of all the data points in the lowest applied power (14.454μW @ 295K – worst case) is measured to be 1.2916×10^{-3}, which translates to ~45mK fluctuations in the converted temperatures, according to the calibration curve. The sample numbers and plots provided in this section are based on the control experiment on the Si/SiO_2 (270 nm) substrate as a representative of all other measurements.

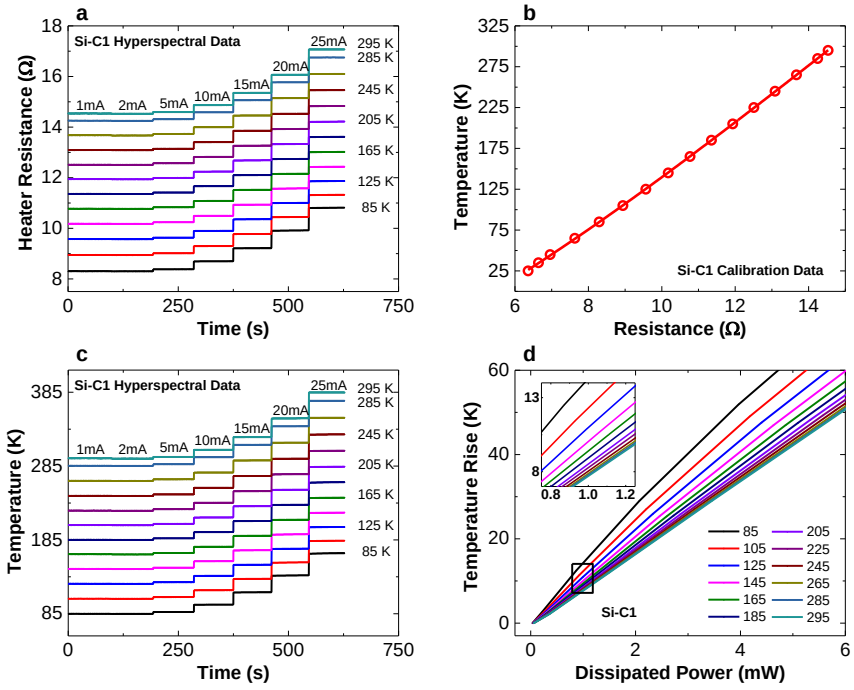

Figure 14. A representative Set of Data Processing Plots for One of The Control Experiments on Si/SiO_2 Substrate. (a) The resistance vs. time at different temperatures and applied powers. (b) The calibration curve for temperature vs. resistance. The data is fitted by a 3rd order polynomial. (c) Converted temperature vs. time at different base temperatures and applied powers. (d) The temperature rise of the electrode as a function of applied power at different base temperatures.

Figure 15a-b shows the thermometry platform and the FE model used for analysis of the experimental data. Figure 15c shows the temperature-dependent R_{TH} of the devices based on transferred graphene, direct-grown and transferred MoS_2 in K/mW (Kelvin per milliwatt). The R_{TH} values of the devices without 2D materials (control experiment) on Si/SiO_2 (270 nm) substrate tested under identical experimental conditions is also shown in Figure 15c. All the tested structures show a similar descending trend for R_{TH} versus temperature which is mainly dictated by the thermal resistance of the Si/SiO_2 substrate.

The difference in the R_{TH} values is associated with the difference in the TBR caused by the presence of the graphene or MoS_2 monolayer. It is worth noting that for all the tested structures herein, at least 3 different devices were tested to assure repeatability of the measurements and the standard deviations of the measured values are shown as error bars in the R_{TH} versus Temperature plots.

To quantify the contribution of each component (e.g., metal electrodes, interfaces, and substrate) on R_{TH}, the experimental data was analyzed in a 3D FE model using the actual geometrical dimensions of the fabricated devices. Figure 15b show the top and cross-sectional view of the temperature distribution in the Au/Ti/MoS_2/SiO_2/Si stack (270nm SiO_2 thickness) at 1mW applied power at 295 K base temperature. The results indicate a sharp temperature gradient around the interface and the oxide layer due to their large and localized resistance. In the FE model, the temperature-dependent thermal conductivity of the substrate materials (presented in the next subsection)[32], [226], [227] and the metal electrodes (obtained using Wiedemann-Franz law)[32], [213] were used as known parameters in the steady-state thermal analysis. The modeled lumped TBR between the metal electrode and the substrate (in presence or absence of the 2D material) was then iteratively found to match the experimental data.

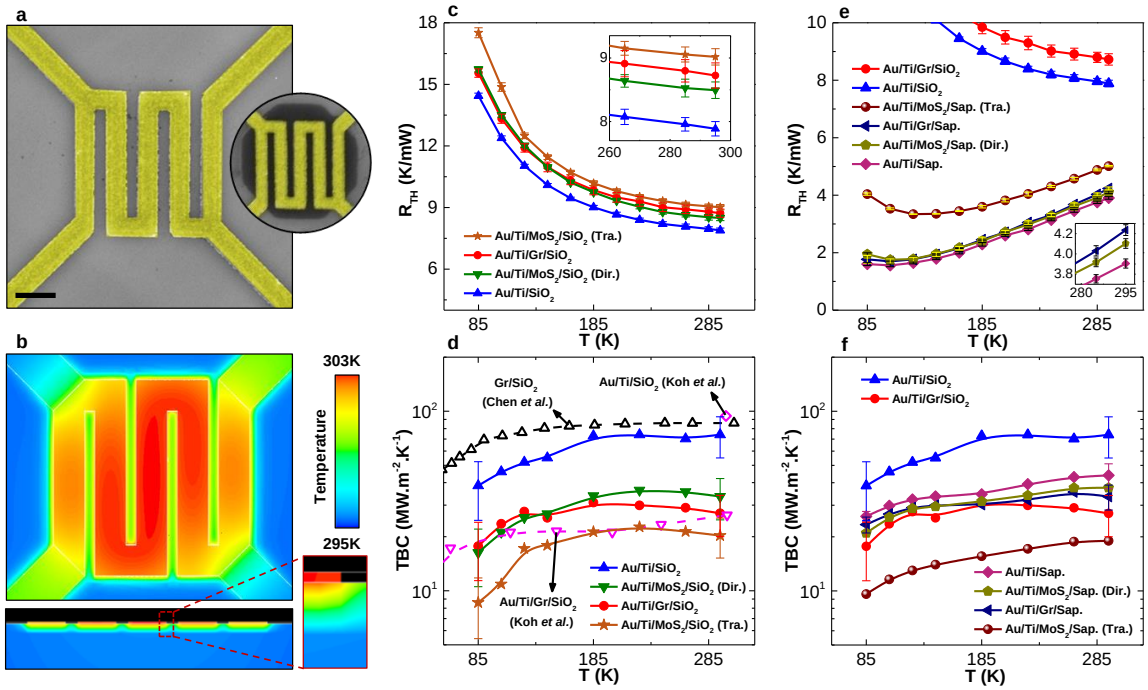

Figure 15. Through-Plane Thermometry Experiments and FE Analyses (a) Colored SEM image of the electrical thermometry platform fabricated on a symmetrically patterned MoS_2 flake. The scale bar is 2μm. The inset shows the same device before oxygen plasma etching. (b) Temperature distribution in the FE model for the Au/Ti/MoS_2/SiO_2/Si stack at 1mW applied power and at 295 K base temperature. The cross-sectional side view of the FE model along the black dashed line is also shown. (c) Temperature-dependent overall thermal resistance to the environment (R_{TH}) of all the tested structures on Si/SiO_2 (270nm SiO_2 thickness). The inset magnifies the same curves. The error bars indicate the standard deviation of at least 3 experiments in identical conditions. (d) Temperature-dependent TBC for the tested structures extracted from the FE analyses plotted against the data from Koh *et al.*[35] and Chen *et al.*[34] reports. The error bars represent the overall uncertainty of the measurements, as discussed in the following subsections. (e) R_{TH} versus T, and (f) TBC versus T for the tested structures on sapphire.

As a geometry-independent quantity, the TBC values (reciprocal of TBR) extracted from the FE analyses are shown in Figure 15d for graphene, MoS_2 (direct-grown and

transferred), and control experiment on Si/SiO_2 substrate over the entire temperature range (85-295K). The temperature dependence of TBC follows the heat capacity of the as flexural acoustic (ZA) branch[228] and nearly flattens at room temperature, in accordance with earlier work.[35] The results are plotted along with the data by Koh *et al.*[35] for heat conduction across $Au/Ti/Gr/SiO_2/Si$ and $Au/Ti/SiO_2/Si$ interfaces as well as the data by Chen *et al.*[34] for the heat transport across sandwiched graphene between SiO_2 layers ($SiO_2/Gr/SiO_2$). The error bars represent the overall uncertainties of the measurements and are fully discussed in the following subsections. For the case of $Au/Ti/Gr/SiO_2/Si$ and $Au/Ti/SiO_2/Si$, the TBCs at 295K are 27 and 74 $MW.m^{-2}.K^{-1}$, respectively, consistent with the results obtained by Koh *et al.* on the very similar structures using time domain thermoreflectance (TDTR) method.[35] The values are also in agreement with the report by Yang *et al.*[166] which shows a TBC of 22±2 $MW.m^{-2}.K^{-1}$ for the $Au/Ti/Gr/SiO_2$ interface and 80 $MW.m^{-2}.K^{-1}$ for the control experiment ($Au/Ti/SiO_2$). The TBC at 295K for $Au/Ti/MoS_2/SiO_2/Si$ stack is also found to be 33.5 and 20.3 $MW.m^{-2}.K^{-1}$ for the direct-grown and transferred MoS_2, respectively. This difference is likely due to the presence of interface contaminants in the transferred structure resulting in a weaker interface coupling (adhesion forces) or an additional series resistance in the path of phonon transmission across the interface. Here it is noted that the TBC in both MoS_2 cases are in the same order as in graphene, but they are remarkably larger than the previous reports by Zhang *et al.*[37] (0.1-1 $MW.m^{-2}.K^{-1}$) and Taube *et al.*[36] (~2 $MW.m^{-2}.K^{-1}$). However, our results agree better with the data by Yalon *et al.* where the TBC for the monolayer CVD MoS_2 encased

between an AlO_x layer and a SiO_2/Si substrate was estimated to be 14±4 $MW.m^{-2}.K^{-1}$ at room temperature.[198] The disagreement among these results can be partly due to the presence/absence of an encapsulating layer. The samples in this study are encased by a metal and the report by Yalon *et al.*[133], [198] is on AlO_x-coated samples, while the reports by Zhang *et al.*[37] and Taube *et al.*[36] do not have any encapsulating layer on the 2D material. The discrepancy could also be due to better interface quality in our tested structures. The samples were annealed at 300 in °C for 3 hours in vacuum which is known to remove the polymeric residue[229] and increase the adhesion of the 2D monolayers with the substrate. Our extracted TBCs are also an order of magnitude larger than the reported values by Judek *et al.*[165] on multilayer graphene and MoS_2 which are 1.7±0.2 $MW.m^{-2}.K^{-1}$ and 2.6±0.2 $MW.m^{-2}.K^{-1}$, respectively.

The same measurements was also performed on sapphire substrate (c-plane, average roughness: Ra<1nm) which has already proven as a viable substrate for many applications involving 2D materials.[230], [231] Figures 15e-f show the full data set for sapphire along with the selected data on Si/SiO_2 for comparison. Unlike the Si/SiO_2 substrates with 270nm oxide thickness, the R_{TH} plots in all the sapphire experiments show an ascending trend as the temperature increases from 85 to 295K (Figure 15e). More specifically, the R_{TH} at 295K for Au/Ti/sapphire and Au/Ti/Gr/Sapphire stacks are 3.9 and 4.23 K/mW, respectively, which decrease to 1.6 and 1.76 K/mW at 85K, suggesting the suitability of sapphire for 2D-based cryogenic applications. The FE analyses on the sapphire thermometry data show a TBC value of 44 $MW.m^{-2}.K^{-1}$ at 295K for the control experiment

on sapphire which is smaller than that of Si/SiO_2 substrate (74 $MW.m^{-2}.K^{-1}$). This can be explained by the larger mismatch in the Debye temperature of Ti (~420K) to that of sapphire (1000K) compared with SiO_2 (550K).[141], [199], [232] For Au/Ti/Gr/Sapphire and Au/Ti/MoS_2/sapphire (direct-grown and transferred), the values of TBC at 295K are 33.5, 37.5, and 19 $MW.m^{-2}.K^{-1}$, respectively (Figure 15f).

3.4.1. Temperature Dependence of Thermal Conductivities of The Materials

The temperature-dependent thermal conductivities of all the materials used in the fabricated structures are well-characterized in the literature and are input as known parameters in the FE analyses. For the metal electrodes (Au/Ti), the effective thermal conductivity is calculated from the electrical conductivity through Wiedemann-Franz law[32], [216], using an average Lorentz number $L = 2.7\times10^{-8}$ $W.\Omega.K^{-2}$ (Figure 16a). The temperature-dependent thermal conductivity of SiO_2 layer is used from the report by Bae *et al.*[32] which is shown in Figure 16b. For sapphire and silicon single crystals, the data reported by Dobrovinskaya *et al.*[227] and Glassbrenner *et al.*[226] are respectively used in the analyses (Figure 16c-d).

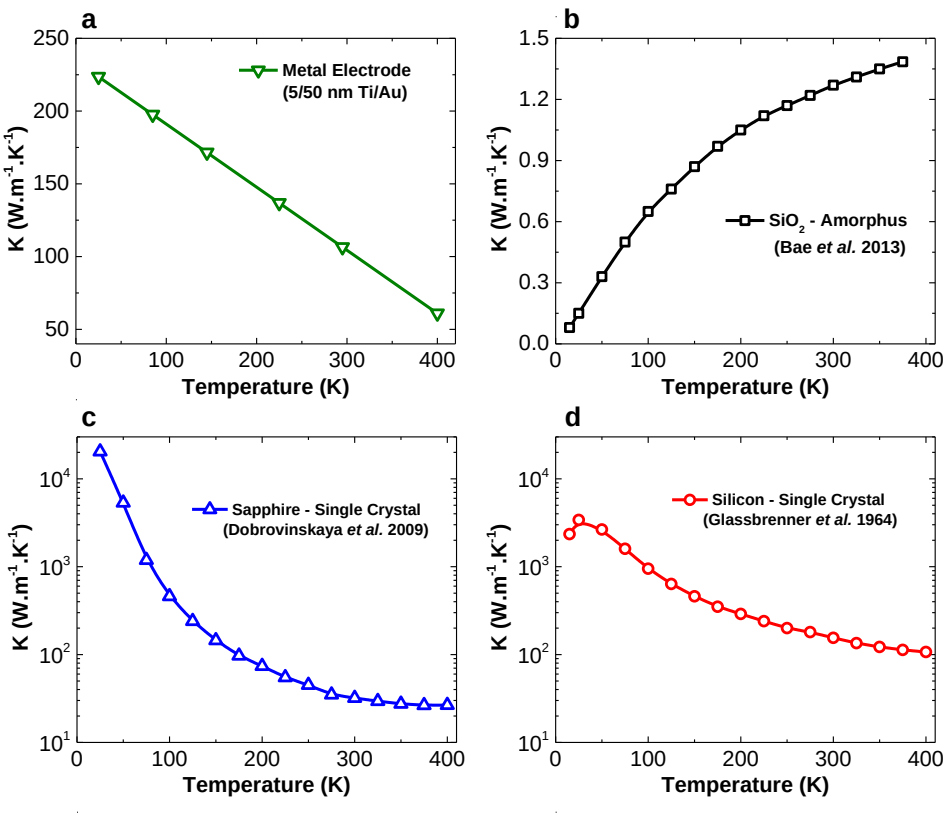

Figure 16. Thermal Conductivities of The Materials vs. Temperature. (a) Metal electrode through Wiedemann-Franz law[32], [216], (b) Silicon oxide (SiO_2), (c) Sapphire single crystal, (d) Silicon single crystal.

3.4.2. Details of the Through-Plane Finite Element (FE) Simulations

A 3D FE model in lateral size of 100x100x μm^2 with a varying depth between 50.056 to 50.326 μm (depending on the dielectric thickness), consisting of ~$2x10^5$ elements is built in commercial software ANSYS (See the full model in Figure 17a-b). In the model, solid elements (Solid70) are used to represent all the five layers in the experimental thermometry platforms. From bottom to top, the layers and their corresponding thicknesses are: (I) Si (50μm), (II) SiO_2 (270nm thickness), (III) a 1nm-thick layer representing the lumped TBR,

(IV) Titanium (5nm), and (V) Gold (50nm) (Figure 17c). The mesh size is refined and the convergence of the results is tested. The geometrical dimensions of the model are obtained from the SEM images of the actual fabricated devices within 5% error. The temperature-dependent thermal conductivities of all the known materials are input as known to the model. The back and side surfaces of the model are held at a constant (ambient) temperature (the temperature of the cold finger in the cryogenic refrigerator). The top surface is isolated which is a reasonable assumption due to a negligible convection (vacuum ~10^{-7} mbar) and radiation (temperature changes < 20K). A volumetric heat generation is applied to the current-carrying metal electrodes (gold) to resemble the Joule heating which is inversely proportional to the width of the electrode.

By solving the steady-state thermal transport at different applied powers, the average nodal temperature rises of the serpentine shape electrode (between the voltage leads) are extracted and compared to that of the experiment. The thermal conductivity of the 1nm TBR layer is then optimized in several iterations until the temperature rise in the model matches that of the experiment (within 0.5% error). Figure 17d-f show few cross-sectional view of the temperature distributions for the Au/Ti/Gr/SiO_2/Si stack with 270 nm oxide thickness at 295K and at 1mW.

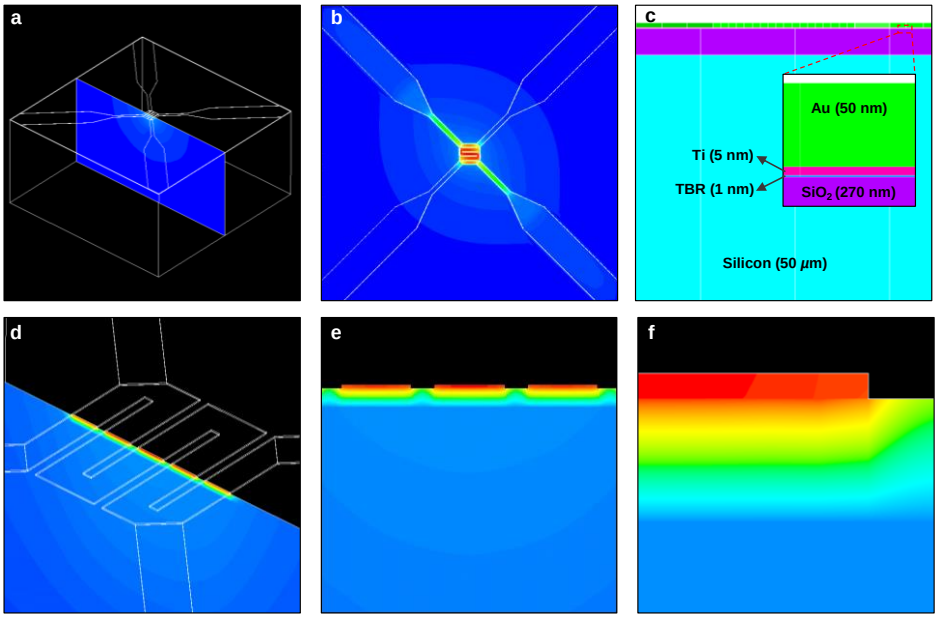

Figure 17. Details of The FE Model for Through-Plane Thermometry Platform. (a) Full view of the FE model, showing the temperature distribution on a cross-sectional plane for the Au/Ti/Gr/SiO_2/Si stack with 270 nm oxide thickness at 295K and at 1mW. (b) Top view of the temperature distribution for the simulation shown in (a). (c) The actual distribution of the layers in the cross-sectional view. (d-f) More temperature distribution plots at higher magnification for the simulation shown in (a).

3.5. Uncertainty Analysis

To calculate the uncertainty of the extracted TBCs, sensitivity analyses were performed using the partial derivative method, similar to the analyses in Chapter 2.[1], [32] In this analyses, each of the input parameters are perturbed (∂x_i) around its typical value (x_i) and the corresponding change in the TBC (∂TBC) is calculated through FE simulation. The dimensionless sensitivities are then calculated as follow:

$$s_i = \frac{x_i}{TBC}\frac{\partial TBC}{\partial x_i}$$

The overall uncertainty (u_{TBC}) in the extracted TBCs is then calculated as follow:

$$\frac{u_{TBC}}{TBC} = \sqrt{\sum_i \left(s_i \times \frac{u_{x_i}}{x_i}\right)^2}$$

where u_{x_i} is the overall random and systematic uncertainty of the ith parameter around its typical value (x_i) and s_i is the sensitivity to that particular input. Due to the heavy load of the uncertainty analyses, this process is carried out for selected data points as shown in Figure 15d and 15f. Table 2 summarizes a set of uncertainty analysis of different inputs on the extracted TBC of the Au/Ti/MoS_2/SiO_2/Si stack (270nm oxide thickness – direct-grown).

Table 2. Uncertainty analysis for the TBC of Au/Ti/MoS_2/SiO_2/Si stack (direct-grown) at 295K.

Input	Units	x_i (values)	u_{xi} (errors)	u_{xi}/x_i (%)	s_i	$c_i = \lvert s_i \times u_{xi}/x_i \rvert$	$(c_i)^2 / \Sigma(c_i)^2$ (%)
R_{TH}	K/mW	8.493	0.16	1.88%	7.463	0.019766	29.58
K_{Metal}	W/m/K	106.49	5	4.70%	0.207	0.000428	0.64
K_{SiO2}	W/m/K	1.26	0.03	2.38%	5.744	0.014318	21.42
K_{Si}	W/m/K	149	5	3.36%	0.527	1.73×10^{-5}	0.026
TBR (Metal-SiO_2)	m^2.K/W	7.4×10^{-8}	2.5×10^{-8}	33.78%	0.0098	1.11×10^{-5}	0.017
δ_{Metal}	nm	55	2	3.64%	1.556	0.003202	4.791
δ_{SiO2}	nm	270	10	3.7%	4.605	0.02909	43.53
$W_{electrode}$	nm	950	20	2.11%	Neglected	N.A.	N.A.
$L_{electrode}$	nm	6850	20	0.29%	Neglected	N.A.	N.A.

The table shows the typical values, errors, sensitivities, and the relative and absolute contributions of each parameter to the overall uncertainty of the TBC at T=295K. The error in the R_{TH} is obtained from the standard deviation of at least 3 experiments in identical conditions. The TBR (Metal-SiO_2) is the TBR between the metal and substrate on the outer

regions of the platform in the FE model (extension of the electrodes) which has a negligible contribution to the overall uncertainty.

The overall uncertainty ($\frac{u_{TBC}}{TBC}$) is 25.85% for the Au/Ti/MoS_2/SiO_2/Si stack at 295K. In higher conductance substrates like sapphire, the uncertainty becomes smaller due to lower contributions of the in-plane dissipation and substrate resistances.

3.6. Theoretical Modelling and Simulations (in collaboration)

In extracting the experimentally measured values, all interfacial resistances including the metal/2D-material and 2D-material/substrate were considered as a lumped TBR value in the FE model. Next, we collaborated with Prof. Khalili-Araghi and Prof. Aksamija's groups to deconvolute the contributions of these resistances and to gain more insight into the governing physics of the interfacial thermal transport in these structures.

MD simulations were used to calculate the through-plane thermal conductivity of a stacked system consisting of a single layer of MoS_2 sandwiched between Ti on one side and SiO_2 on the other side (Ti/MoS_2/SiO_2). The TBC (Kapitza conductance) at each interface was extracted from a series of NEMD as outlined in Figure 18. The details of the MD simulations can be found in reference [2].

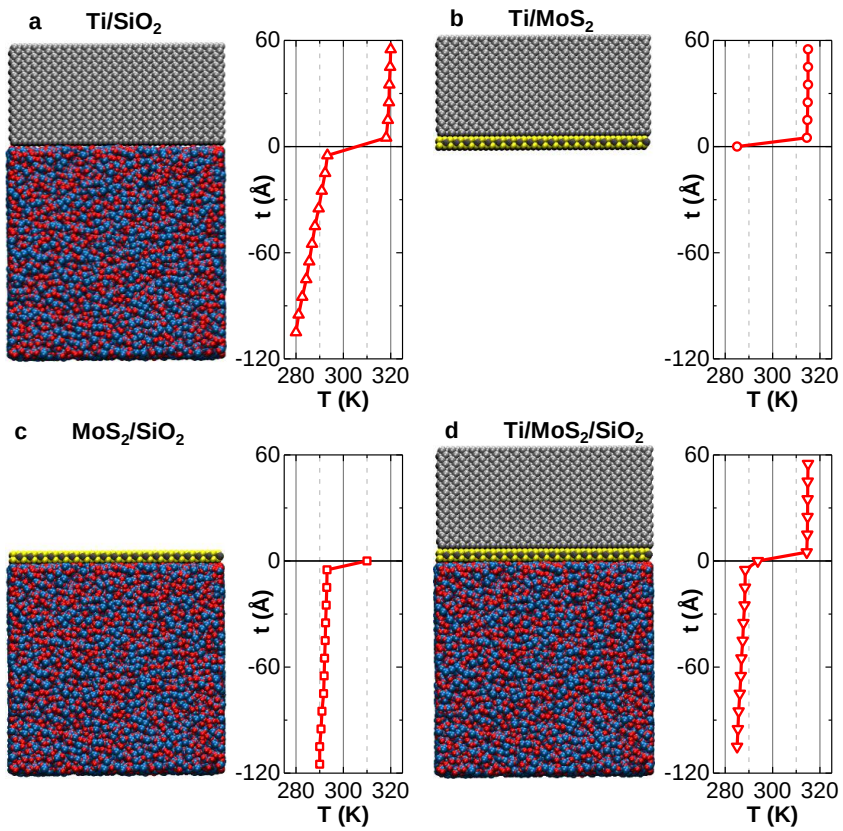

Figure 18. Snapshots of The Four MD Simulation Systems Consisting of Ti, MoS_2, and SiO_2. For each system, the temperature profile normal to the plane of MoS_2 obtained from the NEMD simulations is shown. The temperature profiles are used to calculate the TBC at each boundary.

In addition to obtaining the TBC between MoS_2 and substrates (Ti or SiO_2) in the triple stacked (double interface) system (Figure 18d) two other simulations were performed to calculate the TBC between MoS_2 and Ti as well as MoS_2 and SiO_2 directly from double stacked systems (single interface), as shown in Figure 18b-c. A control simulation on Ti-SiO_2 stack without the MoS_2 layer was also performed (Figure 18a).

The thermal conductivity of Ti and SiO_2 are found to be 2.6 $W.m^{-1}.K^{-1}$ and 0.9 $W.m^{-1}.K^{-1}$, respectively. It has to be noted that while the finite size of the system is not expected

to affect the TBC of the boundaries, it may affect the bulk conductivity of the substrates calculated from the simulations. The deviation in the thermal conductivity of Ti from MD simulations and experimental measurements (~21.9 $W.m^{-1}.K^{-1}$)[233] comes from the fact that classical MD does not account for the electronic contribution to the thermal conductivity. Using Wiedemann-Franz law, the electronic thermal conductivity can be estimated as ~19.44 $W.m^{-1}.K^{-1}$, assuming an electrical conductivity of 2.4×10^{6} S/m[233] and an average Lorenz number of 2.7×10^{-8} $W.\Omega.K^{-2}$ for Ti.[32], [234] This suggests a lattice thermal conductivity of 2.46 $W.m^{-1}.K^{-1}$ which is in good agreement with the MD value (2.6 $W.m^{-1}.K^{-1}$). It should be noticed that only phonons contribute to the interfacial thermal transport across the 2D material interfaces with the insulating substrates[35], thus the conclusion based on the MD simulations is valid at the interface area. For the above-mentioned structures, the TBC of each interface was calculated from the simulations and is summarized in Table 3.

Table 3. TBCs from the MD simulations along with the experimental data. The top three rows are from single interface systems and the bottom three rows are values from the stacked system (two interfaces). Individual interface values of the stacked system were calculated using the temperature drops between the two sides of the interface. (*) shows the extracted values from triple-stack simulations.

	TBC–MD ($MW.m^{-2}.K^{-1}$)	TBC–Experiment ($MW.m^{-2}.K^{-1}$)
MoS_2/SiO_2	15.6	
Ti/MoS_2	7.9	
Ti/SiO_2	57.7	56-74
$Ti/MoS_2/SiO_2$	10.9	20.3-33.5
MoS_2/SiO_2 (*)	54.6	
Ti/MoS_2 (*)	13.7	

The control simulation shows a TBC of 57.7 $MW.m^{-2}.K^{-1}$ between the SiO_2 substrate and the Ti layer, comparable to the experimentally measured value of 74 (Figure 15d). The results show that adding a MoS_2 layer between Ti and SiO_2 decreases the TBC from 57.7 $MW.m^{-2}.K^{-1}$ in the control simulation to 10.9 $MW.m^{-2}.K^{-1}$. A similar decrease from 74 $MW.m^{-2}.K^{-1}$ to 20.3-33.5 $MW.m^{-2}.K^{-1}$ was observed in our experiments once the MoS_2 layer is introduced in the device. Interestingly, the simulations reveal that the TBC between MoS_2 and Ti or between MoS_2 and SiO_2 cannot be calculated independently. The TBC between MoS_2 and Ti calculated in the double stacked system increases by 70% once the Ti-MoS_2 system is placed on the SiO_2 substrate. On the other hand, the MoS_2-SiO_2 TBC increases by a factor of 3.5 once the Ti is added to the system. Our MD simulation results clearly indicate that a full system analysis is required to precisely deduce the TBC values in multi-interface systems.

In collaboration with Prof. Aksamija's group, through ab initio calculations and BTE modeling, the TBCs were calculated for the double stacked and triple stacked systems to quantify the effects caused by encapsulation on the thermal transport across the tested monolayers (both MoS_2 and graphene). The model includes two effects that impact the TBCs: (i) the coupling forces between the monolayer and the environment (substrate and encapsulating layer) that modify the phonon dispersion of the monolayer, including gapping of the flexural branch and emergence of hybridized Rayleigh wave modes (RWMs),[235] and (ii) the vibrational modes in the monolayer couple to the modes in the substrate through the van der Waals interaction forces, treated in our model as a harmonic

spring with constant K_a[29], and thus transfer heat between them. These calculations yield the TBC values, which agree with the experimental values quite closely and allow us to break the total TBC into the key components, showing that hybridization of phonon modes leads to higher TBC when the monolayer is encapsulated.

3.7. Summary and Conclusion

In summary, the thermal dissipation was studied across CVD MoS_2 and graphene monolayers through a coupled combination of experiments, simulations, and modeling. In contrast with previous estimations[36], [37], our comparative experiments and 3D FE analyses reveal that the TBC across MoS_2 is in the same order as in the case of graphene on both Si/SiO_2 and sapphire substrates. Remarkably, our MD results unveil that the TBC of a 2D material with the substrate can be largely different in presence of an encapsulating layer. First principles BTE calculations explain this effect as being due to hybridization of the phonon modes and emergence of Rayleigh waves. This finding opens up an additional pathway for interfacial thermal transport in 2D-based devices through deposition of an engineered encapsulating layer (i.e., contact metals or gate dielectrics).

CHAPTER 4

QUANTIFYING THE LIMITS OF THROUGH-PLANE THERMAL DISSIPATION IN 2D-MATERIAL-BASED SYSTEMS

(Some parts of this chapter are taken from the published paper with the following citation:

Poya Yasaei, Amirhossein Behranginia, Zahra Hemmat, Ahmed El-Ghandour, Craig D. Foster, Amin Salehi-Khojin "Quantifying the Limits of Through-Plane Thermal Dissipation in 2D-Material-Based Systems" *2D Mater.*, vol. 4, no. 3, p. 35027, Aug. 2017.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

4.1. Introduction

As discussed in the previous chapters, heat dissipation and thermal management are crucial for the design and operation of 2D nano-devices, in which overheating could lead to premature failure. While 2D materials offer excellent intrinsic thermal properties, the heat dissipation performance of devices based on these materials will be affected by the thermal characteristics of the enabling infrastructures, such as interconnects and substrates as well as their junctions and interfaces. Thus, a system-level analysis is essential to quantify the thermal dissipation limits in 2D material-based structures to realize their competitive advantage over their 3D counterparts.[28]–[35], [155], [157]

Heat generated in the hot-spots of 2D circuitry generally spreads within the plane of the 2D materials and ultimately dissipates through the substrate and the contact electrodes.[33] The contributions of in-plane and through-plane transport on the overall thermal resistance (R_{TH}) is determined by a combination of geometrical dimensions as well

as thermal properties of the materials and interfaces.[33], [131] In many device architectures (e.g., devices with characteristic lengths>100nm), the through-plane thermal transport predominantly defines the R_{TH}.[33] In these cases, optimizing the R_{TH} requires a high-conductance substrate as well as a good thermal interface. One major challenge is that the heat in high-conductance substrates such as diamond is usually carried by high-frequency phonons which transmit poorly through the Van der Waals interfaces that bind 2D materials.[141], [199] In other words, a practical trade-off seems to exist between the bulk thermal conductivity of existing substrates and the interfacial conductance at their junction with the 2D materials. On top of this criterion, the microscopic details of the interface such as coupling (adhesion) forces, surface roughness, and presence of potential contaminants also affect the TBRs and consequently the R_{TH}. Thus, it is necessary to consider all the thermal resistances and their decisive parameters simultaneously in the design of the 2D-based systems, in order to maximize overall thermal dissipation.

4.2. Through-Plane Thermal Transport Measurements

In this chapter, the same electrical thermometry platform was utilized which was developed in the previous chapter to measure through-plane thermal transport in representative 2D-based devices fabricated on the substrates with the highest available thermal conductances, e.g., CVD diamond (K~1500 $W.m^{-1}.K^{-1}$ at room temperature), tape-casted (sintered) aluminum nitride (AlN - K~170 $W.m^{-1}.K^{-1}$), and single crystalline c-plane sapphire (K~31 $W.m^{-1}.K^{-1}$). It is noted that beryllium oxide (BeO) (K~250 $W.m^{-1}.K^{-1}$) is another high-conductance substrate, but we declined to test it due to its toxicity, which has

caused a ban on its use in many industries.[236], [237] The Si/SiO_2 (270nm oxide thickness) was also tested as a reference point for comparison, as it is the most frequently used substrate for devices based on 2D materials. The Si/SiO_2 and sapphire substrates are single crystalline with a surface roughness of <1nm. Commercially available CVD diamond and tape-casted AlN substrates were used with an advertised roughness of <10nm and <1µ-in (~25.4nm), respectively. Optical images of the as-received diamond and AlN substrates are respectively shown in Figure 19a-b. The AFM images of diamond and AlN are also respectively shown in Figure 19c-d and a representative height profile is shown in the insets. Surface analyses show that diamond has a root mean square (rms) roughness of R_q=5.21nm and R_q=3.72nm before and after waviness removal, respectively. AlN is more wavy than rough, as evidenced by R_q=24.6nm and R_q=2.3nm before and after waviness removal, respectively.

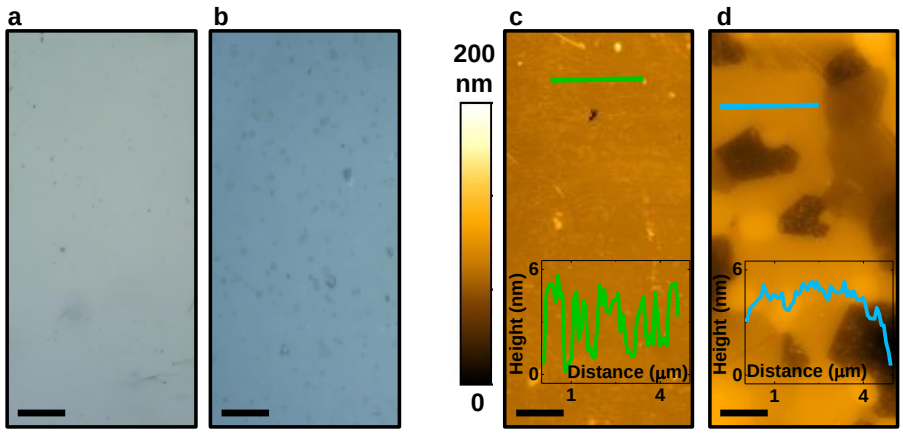

Figure 19. Morphological Characterization of Diamond and AlN Substrates. (a-b) Optical image of an as-received diamond and AlN substrates, respectively. The scale bars are 15 µm. (c-d) AFM images of the diamond and AlN substrates, respectively. The scale bars are 2 µm. The inset shows the height profile along the green and blue lines.

Detailed analyses were performed to quantify the limits of through-plane heat dissipation in the tested devices and to identify the best structure from a thermal management perspective. Monolayer CVD graphene is used as a model for 2D materials throughout this study. The graphene growth process and characterization can be found in the previous chapters and in the previous reports.[23], [99], [222] After the synthesis of graphene on copper foils, a typical polymer-assisted wet etching process was used to transfer the monolayer flakes to the target substrates.[225]

For the through-plane thermal transport measurements, the same serpentine-shape electrical thermometry platform is employed which was developed in the previous chapter, as shown in Figure 20a. The resistance of the four-probe heater/sensor electrode, which is patterned on a monolayer graphene (or a bare substrate for control experiments), was initially calibrated at different temperatures (25K to 295K) in the cryogenic refrigerator (inset of Figure 20b). The base temperature is then held constant and different levels of electrical power (Joule heating) were applied to the platform, while the resistance was being monitored (Figure 20b shows a representative dataset for graphene on SiO_2/Si with 270nm oxide thickness). Using the calibration data in Figure 20b, the change in the resistance was used to precisely measure the temperature rise (ΔT) of the platform at different applied powers (P) (Figure 20c). The slope of the ΔT versus P plot represents the R_{TH} to the environment. The R_{TH} characterizes the temperature rise of the device at a given applied power and determines how efficiently a certain structure can dissipate the heat from the electrode.

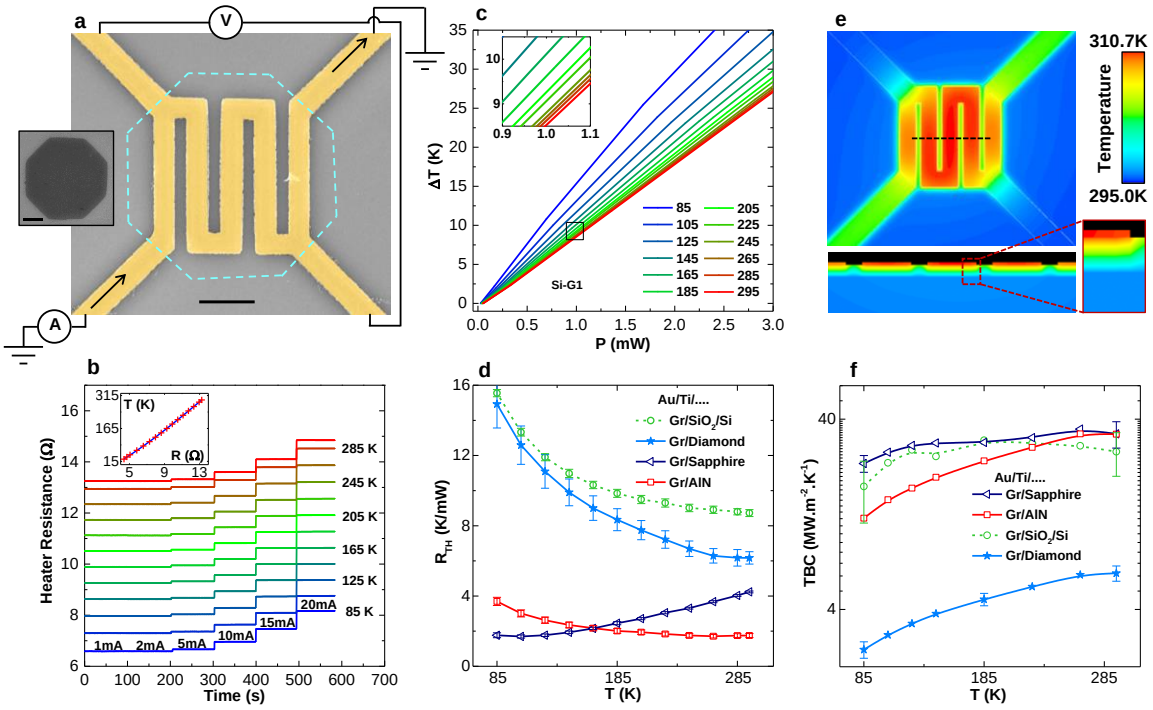

Figure 20. Thermometry Measurements on Different Technologically-Viable Substrates. (a) False-Colored SEM image of the thermometry platform. The inset shows the graphene flake defined into a symmetric octagon before electrode patterning/deposition and plasma etching. The dashed lines indicate the graphene borders under the metal electrodes. The scale bar is 2µm. (b) Hyperspectral data for the electrical resistances of the heater versus time at different temperatures and applied powers. The inset shows the calibration curve with a 3rd order polynomial fitting. (c) The temperature rise (ΔT) versus applied power (P) at different base temperatures. (d) Temperature-dependent overall thermal resistance to the environment (R_{TH}) of the tested structures. The error bars indicate the standard deviation of at least 3 experiments in identical conditions. (e) The top- and side-view of the temperature distribution of the Au/Ti/Gr/SiO_2/Si stack (270nm SiO_2 thickness) in the FE model at 2mW applied power and at 295K base temperature. (f) TBC of the tested structures at different temperatures extracted from the FE analyses. The error bars represent the overall uncertainty of the measurements.

In the measurements, the structure consists of a monolayer graphene sheet capped with an Au/Ti (50/5 nm) electrode and supported by different substrates. For all the substrates, The R_{TH} was also tested for a directly deposited metal electrode on the substrates without any graphene layer (control experiments). The temperature-dependent R_{TH} values of these structures with graphene are shown in Figure 20d (Unit: K/mW - Kelvin per milliwatt). The full dataset along with the control experiment results (Au/Ti/Substrate stacks) are presented in Figure 21. The error bars in Figure 20d represent the standard deviations of at least 3 measurements in identical conditions (same in all R_{TH}-T plots hereafter). As shown in Figure 21d, the highest R_{TH} throughout the temperature range is obtained for the Au/Ti/Gr/SiO_2/Si (270nm oxide) structure, which increases from 8.72 K/mW at 295K to 15.55 K/mW at 85K. Remarkably, the lowest R_{TH} values near the room temperature are recorded for the Au/Ti/Gr/AlN structure (1.75 K/mW at 295K). At low temperatures, the Au/Ti/Gr/Sapphire stack provides the lowest R_{TH} (1.77 K/mW at 85K).

It is noteworthy that the R_{TH} for the Au/Ti/Gr/Diamond structure is quite large, despite the very high lattice thermal conductivity of diamond. For the Au/Ti/Diamond stack (control experiment – in Figure 21), the R_{TH} at 295K is ~1.78 K/mW, which increases to 5.41 K/mW at 85K. For the Au/Ti/Gr/Diamond stack, the R_{TH} is 6.17 K/mW and 14.93 K/mW at 295K and 85K, respectively. This enormous surge in the R_{TH} upon incorporating the graphene monolayer in the stack implies that the TBR significantly contributes to the R_{TH} of the Au/Ti/Gr/Diamond structure.

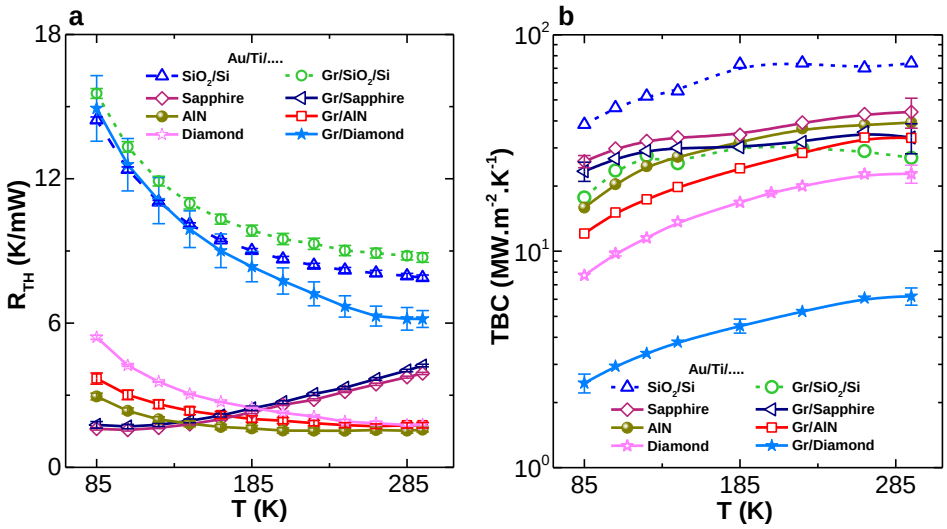

Figure 21. Full Dataset for (a) R_{TH} and (b) TBC for the Diamond, Sapphire, AlN, and Si/SiO_2 (270nm) Substrates.

To extract the interfacial thermal properties of these structures, the thermometry results are analyzed in a 3D FE model with the exact geometrical dimensions of the fabricated platform (In collaboration with Prof. Foster's group). In the FE model, the previously measured thermal conductivity of the materials[32], [213], [226], [227], [238] were used as input parameters and iteratively matched the lumped TBR between the metal electrode and the substrate. For Si, SiO_2, sapphire, and metal electrode, the thermal conductivity data is presented in chapter 3.4. For diamond, and aluminum nitride, this data is presented in the next sub-chapter. Figure 20e shows the temperature distribution of a representative FE model for the Au/Ti/Gr/SiO_2/Si stack (270nm SiO_2 thickness) at 2mW applied power at 295 K. Figure 20f exhibits the extracted TBC values for the tested structures (Full dataset in Figure 21). For the case of Au/Ti/Gr/SiO_2/Si the TBC at 295K is 27 $MW.m^{-2}.K^{-1}$, nearly half of the TBC for the Au/Ti/SiO_2/Si stack (74 $MW.m^{-2}.K^{-1}$). These values are consistent

with the well-established results by Koh *et al.* on the same structures using TDTR technique.[35] The values are also consistent with the report by Yang *et al*.[166] which shows a TBC of 22±2 $MW.m^{-2}.K^{-1}$ for the Au/Ti/single-layer graphene/SiO_2 interface and a TBC of 80 $MW.m^{-2}.K^{-1}$ for the control experiment (Au/Ti/SiO_2). In our measurements, the highest TBC at 295K was obtained for the sapphire and AlN substrates (~33.5 $MW.m^{-2}.K^{-1}$). Sapphire also exhibits the highest TBC at low temperatures (23.4 $MW.m^{-2}.K^{-1}$ at 85K). The lowest values of TBC in the tested temperature range were obtained for the Au/Ti/Gr/Diamond stack (6.2 $MW.m^{-2}.K^{-1}$ at 295K and 2.46 $MW.m^{-2}.K^{-1}$ at 85K). The TBC for the Au/Ti/diamond stack is also the lowest among the tested control samples (22.78 $MW.m^{-2}.K^{-1}$ at 295 and 7.74 $MW.m^{-2}.K^{-1}$ at 85K – see Figure 21). This is in agreement with the previously reported metal/diamond TBC values.[131], [141] The low TBC in diamond interfaces is attributed to the very high Debye temperature of diamond (2200K), which is highly mismatched with most of the metals and the 2D materials (in the out-of-plane direction).[141], [199], [239] This imposes serious challenges for the use of diamond for thermal management in 2D-based applications. In Figure 20f, the error bars of the selected data points represent the overall uncertainty of the extracted TBCs, obtained through an analysis based on the partial derivative method,[1], [32] similar to chapter 3.

4.3. Identifying The Bottlenecks of Heat Dissipation

To better identify the bottlenecks of heat dissipation in these structures, the thermometry platform was modeled with an equivalent thermal circuit, as shown in Figure 22a along with the schematic side view of the device (Figure 22b). The structure is

modeled as an in-plane resistance through the metal electrodes (R_M) acting in parallel to the through-plane overall dissipation resistance. In the through-plane direction, the TBR (here noted as R_B), the dielectric resistance (R_D - if present), and the substrate resistance (R_S) act in series. It is worth noting that the serpentine-shape thermometry platform is designed in such a way that the in-plane conduction through the voltage leads (low-power electrodes) accounts for <2% of the overall heat dissipation ($R_M >> R_B+R_D+R_S$). Thus, the generated heat in the electrode predominantly transfers across the interface and through the substrate, and the in-plane dissipation through the electrodes can be neglected. Knowing the geometry and the bulk/interfacial thermal properties in the tested devices, the values of R_B, R_D, and R_S are calculated and shown in Figure 22c.

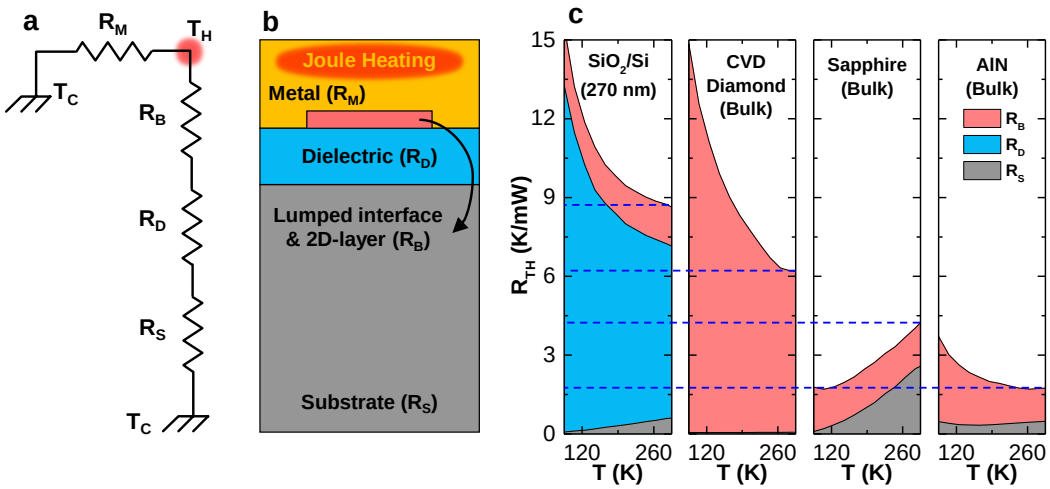

Figure 22. Thermal Circuit Analyses for The Tested Structures. (a) The equivalent thermal circuit of the fabricated platform. The metal resistance (R_M) is parallel to the through-plane resistance which consists of the TBR (R_B), dielectric resistance (R_D - if present), and substrate resistance (R_S). (b) Schematic side view of the test structure. (c) Accumulative plots of R_{TH} for the tested structures. The dashed lines provide eye guidance for a comparison of R_{TH} at 295K.

For the Au/Ti/Gr/SiO_2/Si stack, the R_{TH} at 295K is comprised of 17% R_B, 76% R_D, and 7% R_S. At 85K, the values for R_B, R_D, and R_S are 14.5%, 85%, and 0.5%, respectively. For the Au/Ti/Gr/Diamond stack, the R_S is negligible and the R_{TH} is mainly contributed by the R_B (~99%). In the sapphire stack, the R_S at 295K is the largest among other stacks, but the R_{TH} remains relatively small owing to a decent interface conductance. The results for the AlN stack are remarkable because it provides the lowest R_{TH} among the tested structures.

4.4. Optimizing The Dielectric Layer on Silicon for Better Thermal Dissipation

It should be noted that the applicability of the AlN substrate is limited to devices that do not require a back-gate for operation. Moreover, the fabrication process on AlN substrate is more difficult (due to a poor metal adhesion) compared to the substrates with sub-nanometer roughness such as Si/SiO_2 and sapphire. Silicon substrate is also preferred in many industries due to its abundance, low cost, and availability of developed fabrication recipes. From a thermal transport perspective, Figure 22c shows that R_S for the silicon substrate (with K~150 $W.m^{-1}.K^{-1}$) is a tiny fraction of R_{TH}, while a major contribution comes from the R_D. A prospective approach to improving the overall heat dissipation is to reduce the thickness of SiO_2 or deposit dielectric thin films with higher thermal conductivity. There is a wide range of different dielectric materials that can be reliably deposited on silicon wafers to potentially deliver desirable thermal and electrical properties.[240] Finding the best choice of the dielectrics for a given 2D material requires an extensive survey of materials, which lies beyond the scope of this work. Here, the possibility of reducing the R_{TH} is investigated by using thinner dielectrics of highest

practicality. The thermally grown SiO_2 (thickness of 22 and 29nm) and atomic layer deposited (ALD) aluminum oxide (Al_2O_3) (thickness: 12 and 25nm) thin films were selected. SiO_2 has proven to form an excellent insulator with a high-quality interface with silicon.[240], [241] Al_2O_3 is also a widely used alternative to SiO_2 with higher permittivity.[242]

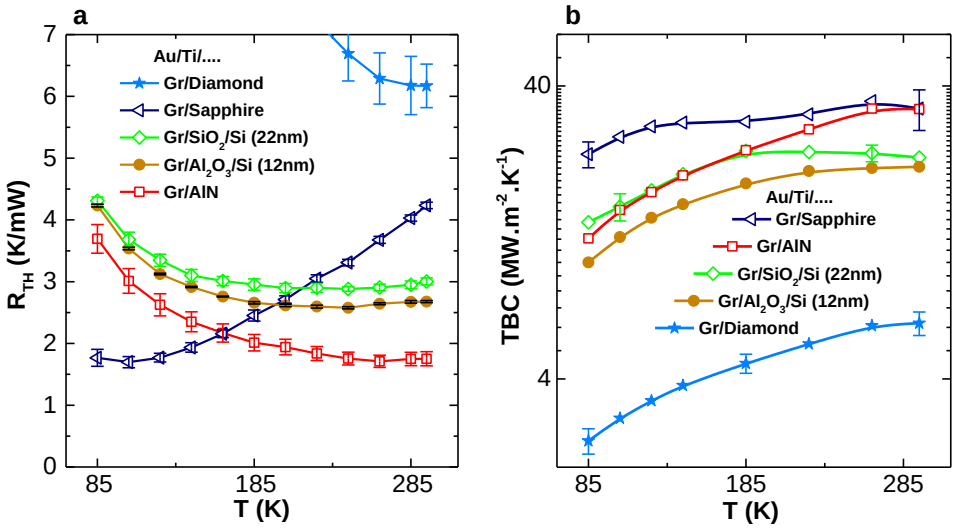

Figure 23. Thermometry Results of Graphene Stacks on Silicon Substrate with Thin Oxides. (a) R_{TH} and (b) TBC versus Temperature results of Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) stacks along with the graphene stack results on sapphire, AlN, and diamond substrates. The error bars in (a) indicate the standard deviation of >3 experiments in identical conditions. The error bars in (b) shows the uncertainty of the extracted TBC values.

Figure 23 shows the R_{TH} measurements and TBC extractions for the Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) stacks at different temperatures along with the graphene-stack results on diamond, AlN, and sapphire. The R_{TH} of Au/Ti/Gr/SiO_2/Si (22nm) and Au/Ti/Gr/Al_2O_3/Si (12nm) structures at 295K are 3.00 K/mW and 2.68 K/mW,

respectively (Figure 23). The values are still higher than those of AlN structure but are far lower than the case of diamond and Si/SiO_2 (270nm).

Figure 23b shows the extracted TBC values of the graphene stacks on silicon substrates. At 295K, the TBC for $Au/Ti/Gr/SiO_2/Si$ (22nm) and $Au/Ti/Gr/Al_2O_3/Si$ (12nm) structures are respectively 22.8 and 21.2 $MW.m^{-2}.K^{-1}$, which reduce to 13.7 and 10 $MW.m^{-2}.K^{-1}$ at 85K. These values are also lower than the TBC on AlN and sapphire substrates. Overall, these results suggest that thin oxide substrates provide a competitive thermal dissipation performance for devices that require a back-gate. However, AlN shows the best through-plane heat dissipation performance near room temperature among the tested structures. The full data set for different oxide thicknesses along with the data for control experiments are presented in Figure 24.

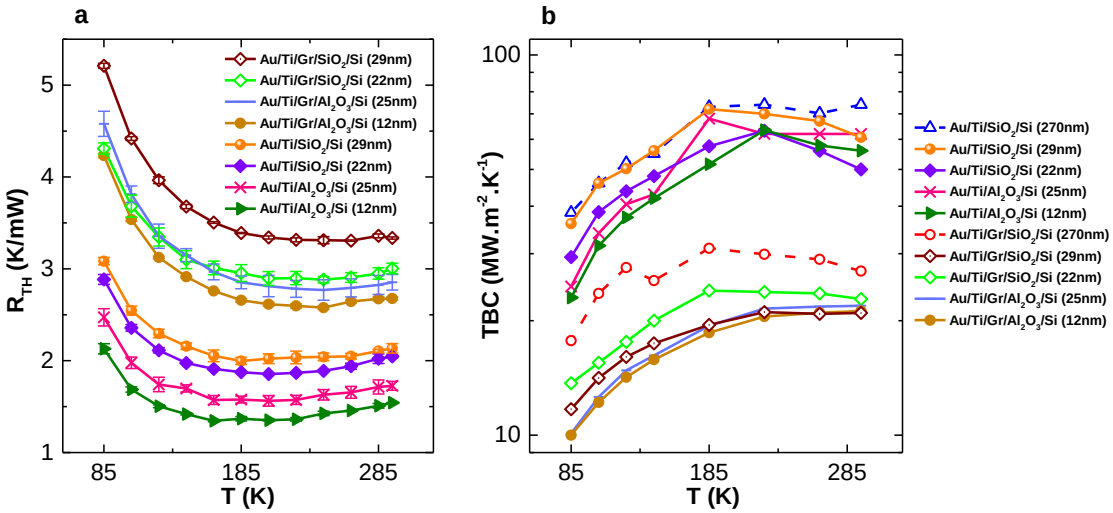

Figure 24. The Full Dataset for The Thermometry Results on Silicon Substrate with Thin Oxides. (a) R_{TH} and (b) TBC for different test structures on thin oxides at the temperature range of 85-295K. The TBC curves are plotted against the data for Si/SiO_2 (270nm) for comparison.

4.5. Establishing The Trend of R_{TH} Versus TBC in The Tested Structures

In a different presentation, Figure 25 demonstrates the R_{TH} values at 295K with respect to TBC. The solid lines show the trends predicted by the FE analyses and the symbols indicate the experimentally obtained data points. This figure demonstrates the importance of substrate conductance and TBC on the R_{TH} in the tested structures. It is observed that for high-conductance substrates (i.e., thin oxides on silicon, AlN, and diamond), the TBC is the bottle-neck of dissipation. This implies that further improvement of the substrate thermal conductance would not lead to a significant reduction in the R_{TH} unless the TBC is improved. For instance, the AlN substrate provides lower R_{TH} than diamond due to a superior TBC where the impact of substrate conductance is insignificant. This figure also visualizes the shift in the TBC upon incorporation of a graphene monolayer in the stack. For instance, although the control experiment TBC for AlN is lower than those of thin oxides, the TBC after addition of a graphene is greater, leading to a lower R_{TH}.

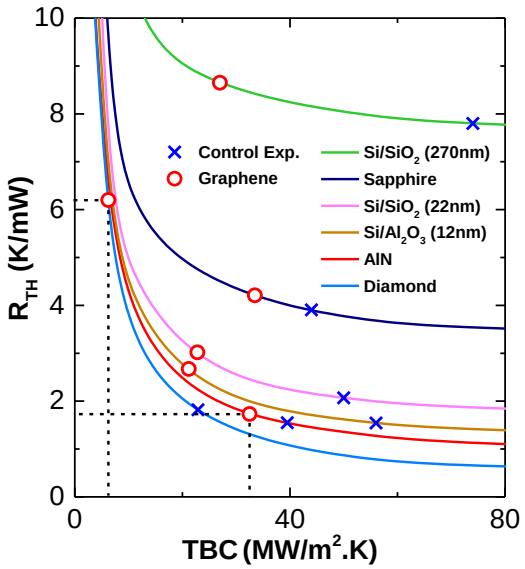

Figure 25. Dependence of R_{TH} on TBC for All The Tested Structures. The solid lines show the trends obtained from FE analyses and the symbols represent the experimental data. The dashed lines compare the R_{TH} and TBC between the Au/Ti/Gr/Diamond and Au/Ti/Gr/AlN stacks.

4.6. Thermal Conductivity Values for Other Materials Used in the Platform

The thermal conductivities of the materials used in the fabricated structures are obtained from literature or our direct measurements and are used as known parameters in the FE analyses. For the CVD diamond (Figure 26a), the thermal conductivity data from Hebei Co. (manufacturer of the diamond substrates used in this study) in the range of 298 – 433 K is extrapolated down to 200 K using the trends in the report by Vandersande *et al.* (1994)[238] for diamond with the closest thermal conductivities. It worth noting that the sensitivity of the extracted TBCs for diamond experiments to the thermal conductivity of the diamond are found to be very low (weak function) because the diamond substrate resistance has a minor contribution on the overall R_{TH}. Hence, the error in the extrapolation

would not notably affect the extracted TBC values. This allowed us to further extrapolate the trends down to 75K (Orange) and still the overall uncertainty in the extracted TBC values remain less than 3%, considering ±500 $W.m^{-1}.K^{-1}$ uncertainty for the diamond thermal conductivity at low temperatures.

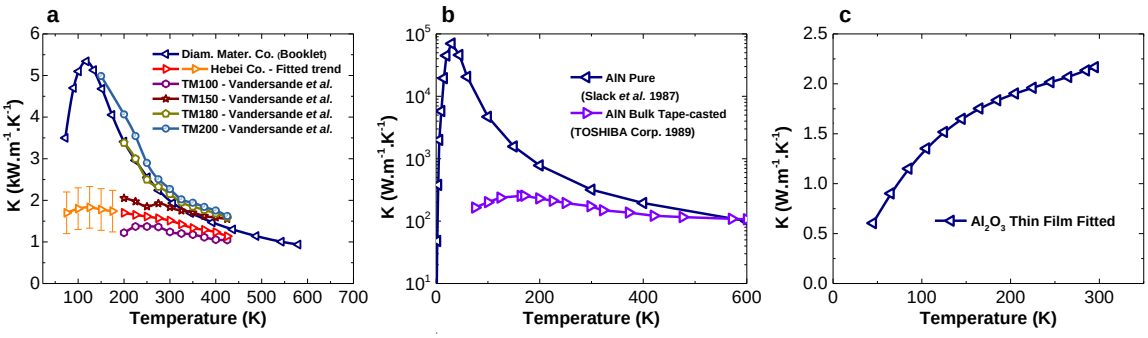

Figure 26. Thermal Conductivities of The Materials vs. Temperature. (a) Diamond[238], (b) AlN[243], (c) Al_2O_3 thin film.

Regarding the bulk AlN, Figure 26b shows the available data for pure AlN by Slack *et al.*[243] as well as the data for AlN-170 (used in this study) by Toshiba Corp. published in 1989. For aluminum oxide thin films by ALD, since a reliable temperature-dependent data was not found in the literature, the experiments were directly carried out to estimate the thermal conductivity. In more details, the difference in the R_{TH} of the control experiment data on Si/Al_2O_3 (12nm) and Si/Al_2O_3 (25nm) were attributed to the 13nm difference in the oxide thickness. Knowing the geometry of the device, the K at different temperatures are calculated and shown in Figure 26c. These values are slightly higher than the sputtered amorphous Al_2O_3 thin films measured by Lee *et al.*,[244] but the temperature-dependent trends are very consistent.

4.7. Summary and Conclusion

In summary, the thermal dissipation is investigated across monolayer CVD graphene, as a representative 2D materials on different technologically-viable substrates having a wide range of thermal conductances and interfacial properties. The contributions of the interfaces and substrate resistances were systematically quantified on the overall thermal dissipation resistance to the environment (R_{TH}), which is essential for the design of electronic circuitry from a thermal management perspective. The results indicate that the overall thermal dissipation performance of monolayer graphene on AlN substrate can rival that of diamond and silicon substrate (even with thin oxides) as a result of a superior TBC. This study reveals that the TBC of monolayer 2D materials on high-conductance substrates is the bottle-neck of power dissipation, while the role of substrate conductance is insignificant.

CHAPTER 5

SYNTHESIS AND ELECTRONIC CHARACTERIZATION OF LATERAL MoS_2-GRAPHENE HETEROSTRUCTURES

(Some parts of this chapter are taken from the published paper with the following citation:

Amirhossein Behranginia, Poya Yasaei, Arnab K. Majee, Vinod K. Sangwan, Fei Long, Cameron J. Foss, Tara Foroozan, Shadi Fuladi, Mohammad Reza Hantehzadeh, Reza Shahbazian-Yassar, Mark C. Hersam, Zlatan Aksamija, Amin Salehi-Khojin "Direct Growth of High Mobility and Low Noise Lateral MoS_2-Graphene Heterostructure Electronics" Small, 2017.

Please refer to the authors' contributions in page iv in the beginning of this document for details of the contributions)

5.1. Introduction

According to Moore's law, the transistor count per chip doubles every two years.[245] The continuing shrinkage in size is pushing the silicon-based industry toward its physical limitations. Numerous efforts are now being dedicated to the development of 2D materials for future electronic/optoelectronic devices.[7], [22], [42], [47], [50], [231], [246] TMDs are opening the possibility of developing systems with reduced dimensionality and a range of unique properties.[42] The most abundant member of this family, MoS_2, has shown interesting semiconducting properties[247], [248] that make it a promising candidate for digital electronic circuitry applications. On the downside, the electrical performance of MoS_2 field-effect transistors (FETs) has been limited by the performance of the MoS_2 junction with the metal contact electrodes.[200] In particular, due to Fermi level pinning, nearly all metals form a Schottky barrier upon contact with MoS_2, which results in large contact resistances on the extrinsic (2-probe) performance of MoS_2-based devices.[200]

Additionally, metals do not possess sufficient mechanical bendability for use in flexible structures. Thus, significant research has been invested in finding a replacement for conventional metal electrodes that will allow the fabrication of intrinsically 2D devices with improved device metrics.[17], [103], [110], [113], [117], [119]

Recently, 2D transistors based on out-of-plane graphene contacted MoS_2 have been reported with an improved performance compared to metal-contacted MoS_2 devices[17], [103], [110], [113], [117]. However, the heterogeneous MoS_2/Gr devices made by such methods have usually been fabricated with a micrometer-scale contact area, possibly to preserve the device mobility. This requirement could seriously limit the number of devices per chip for future high performance integrated electronics. Moreover, such methods impose sophisticated transfer and fabrication techniques resulting in costly mass production. To by-pass the fabrication challenges and performance/size limitations imposed by the vertical interfaces in stacked heterostructures, there has been a pronounced interest in scalable fabrication of lateral interfaces between different 2D materials. So far, lateral interfaces have been synthesized for 2D material pairs with high crystal similarity such as hBN and graphene[79], [106] as well as different sets of TMDs[77], [118]. Among the possible 2D lateral interfaces, one of the most interesting types is the semiconducting/conducting junction as it addresses long-standing challenges on the compactness of high-performance all 2D electronics. Recently, lateral metallic/semiconducting interface has been demonstrated through chemical phase conversion of semiconducting 2H MoS_2 to the metastable metallic 1T phase and improved

device performances were achieved, but the stability of the 1T phase can limit the applications of such structures[119].

In this study, seed-free consecutive CVD processes are utilized to synthesize lateral MoS_2-graphene interfaces with large crystal domain sizes and high interface quality. Device-level experiments reveal that the extrinsic mobility of MoS_2-graphene FETs is improved by an order of magnitude compared with the MoS_2-metal FETs because of energy band rearrangement and smaller Schottky barrier height at the contacts, especially in the accumulation region (large positive gate voltages). For direct verification of the device-level measurements and to gain more insight into the role of the interface on the overall resistance of the device, Kelvin probe force microscopy (KPFM) is employed to map the surface potential distribution of a biased MoS_2-graphene heterojunction under applied gate potentials. Low-frequency 1/f noise metrics of the MoS_2-graphene FETs are also extensively studied in both subthreshold and accumulation regions to identify the origins of signal fluctuations in lateral MoS_2-graphene devices. The results show that the mobility fluctuations are the dominant origin of the noise in the accumulation region, while the overall noise amplitude is an order of magnitude lower than MoS_2-metal FETs. Additionally, electrostatic breakdown measurements are performed on both MoS_2-graphene and MoS_2-metal devices to study the failure modes of the devices under high-power operation. Overall, the research efforts presented in this chapter establishes the superlative electronic properties of directly grown MoS_2-graphene lateral heterostructures.

5.2. Synthesis and Characterization of MoS_2-Graphene Lateral Heterostructures

In this method, a graphene film with partial (or full) coverage is initially synthesized on a copper substrate in an AP-CVD process and then transferred to a silicon (SiO_2/Si) substrate, similar to the previous chapters and the earlier reports.[1], [99] The samples are then transferred to another AP-CVD chamber to synthesize MoS_2 through the reaction of sulfur and molybdenum trioxide (MoO_3) precursors. Figure 27a shows the optical image of the CVD grown MoS_2 film, making a lateral junction with partially covered Gr flakes. Interestingly, it was observed that the growth of MoS_2 is more favorable on bare oxide substrate compared to graphene films. This can be due to the scarcity of the nucleation sites on the sp^2 hybridized carbon atoms of the graphene as opposed to the SiO_2 surface which has many oxygen terminated bonds that can turn into dangling bonds in high temperatures. This can result in selective deposition of MoS_2 on SiO_2 compared to graphene, as long as the concentrations of precursors are not too high. This preference (selective deposition) causes the growth of MoS_2 film to stop right at the edge of the graphene films, making a sharp lateral (in-plane) junction. With shorter growth times a partially covered MoS_2 film (consisting of discrete MoS_2 flakes) is formed next to graphene domains (Figure 27b). It is noted that the respective hexagonal and triangular shapes of the graphene and MoS_2 domains are due to an edge preference in the CVD growth processes, confirming high crystalline quality with quite large grain sizes[21], [22], [211], [249]. SEM imaging of the samples (Figure 27c) shows high-quality MoS_2-graphene lateral heterojunctions with no visible gap or overlap. However, due to the

relatively large (25%) mismatch between the lattice parameters in graphene and MoS_2, it is believed that covalent lateral bonding at an atomically sharp interface is not likely to happen without major crystalline distortion. Such a distortion is less significant in covalent lateral interfaces with higher lattice similarity such as MoS_2-WS_2 or graphene-hBN. As discussed earlier, the lateral MoS_2-graphene interfaces are formed due to the self-limiting growth process (deposition selectivity) which leads to a very narrow overlapping region. The paper by Ling *et al.*[120] has also shown that MoS_2-graphene interfaces exhibit a 2-30 nm wide overlapping region. However, no distortion is observed in the lattice parameters of graphene or MoS_2 in the overlapping region, as evidenced by high-resolution transmission electron microscopy (HRTEM) images and their corresponding Fast Fourier Transform (FFT) diffractograms. To directly evaluate the overlapping region in the samples, atomic force microscopy was also performed on the MoS_2-graphene interfaces. Figure 27d-e show the AFM images of the interface. Particularly, Fig 27e shows that the overlapping region is narrower than 30 nm.

In the next phase, fully-covered graphene samples were fabricated on Si/SiO_2 substrates and were patterned into arbitrary shapes using the standard photolithography and oxygen plasma etching processes. The patterned graphene samples were then loaded into the CVD chamber for MoS_2 growth and the gaps were filled with MoS_2 films while the graphene film remained nearly unaffected (Figure 27f).

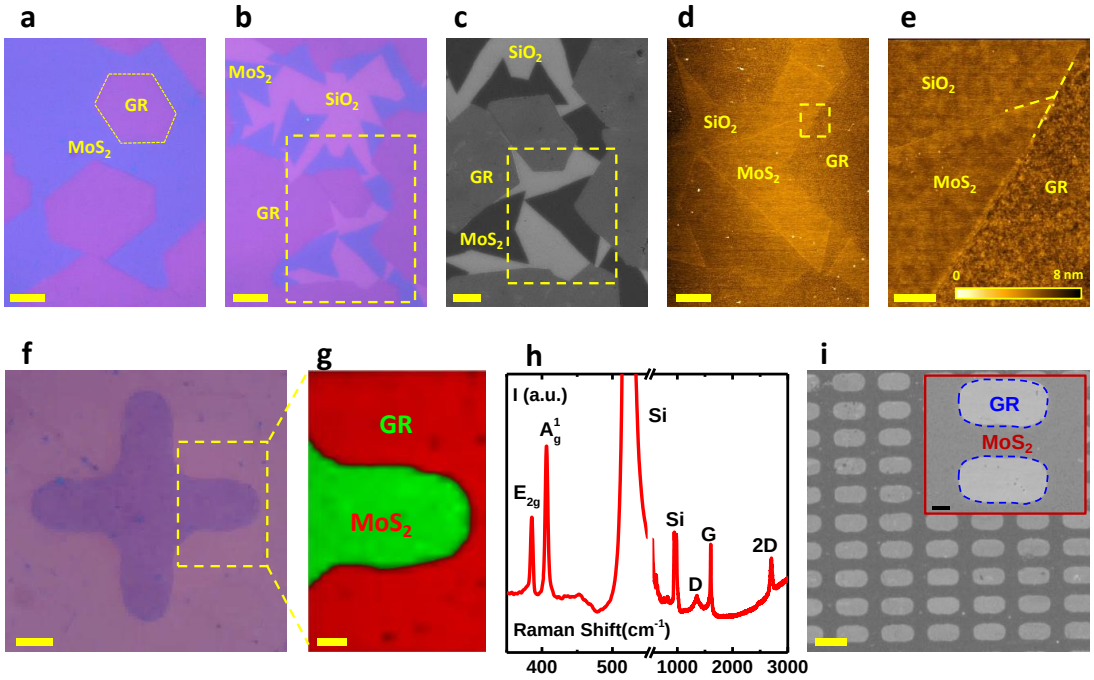

Figure 27. Microscopy and Characterization of MoS_2-Graphene In-Plane Heterostructure. Optical image of (a) the fully covered MoS_2 film (b) partially covered MoS_2 flakes next to the partially covered graphene flakes (scale bars 10 µm). (c) SEM image of the MoS_2-graphene in-plane heterostructure from the selected area in (b) (scale bar 5 µm). (d) AFM image of the selected area of (c) (scale bar 5 µm). (e) Higher magnification AFM image of the selected area in (d), showing the interface between MoS_2 and graphene (scale bar 300 nm). (f) Optical image of a cross-shape patterned graphene film which is filled with MoS_2 in a second CVD growth (scale bar 5 µm). (g) Raman mapping of a selected area shown in (f) (scale bar is 2 µm). (h) Representative Raman point spectra from the MoS_2-graphene interface area. (i) SEM image of a large scale MoS_2-graphene in-plane heterostructure (scale bar 10 µm) the inset magnifies the same image (Scale bar in inset 2 µm).

Raman spectroscopy is used to characterize the structure of the grown materials and the lateral interface. Figure 27g shows the spatial distributions of the graphene and MoS_2 Raman peaks in the selected area of the cross-shaped MoS_2-graphene heterojunction shown in Figure 27f. The classical least square (CLS) fitting was used to analyze the

obtained hyper-spectra, including the E^2_g and A^1g peaks of the MoS_2 (coded as green in Figure 27g) and the G peak of the graphene (coded as red). These results show that a uniform MoS_2 film has fully filled the etched-away gap of graphene and formed a lateral interface without any evidence of overlaps or gaps. These images also show that MoS_2 has not grown on top of the graphene film except for few tiny nucleation sites that are believed to form on the graphene defects. It is worth noting that the optimized growth condition is crucial to avoid MoS_2 formation on the graphene films in the form of small islands or multilayer structures[222]. The Raman point spectra obtained from the border (Figure 27h) shows the presence of representative graphene peaks next to the MoS_2 and the silicon substrate peaks. To demonstrate the scalability of the direct CVD method for fabrication of MoS_2-graphene heterostructures, a large-scale fully covered graphene film was patterned into small squares to serve as electrodes and synthesized a uniform MoS_2 film to fill the gaps (Figure 27i).

5.2.1. Details of the Growth Process for CVD MoS_2 on Graphene

The oxygen plasma treatment is performed on SiO_2/Silicon substrate for two minutes to make the substrate hydrophilic, which helps with the transfer of the graphene film and the growth of MoS_2 on the substrate. After transferring the partial coverage graphene film onto the SiO_2/Silicon substrate, the substrate is annealed at 400 ºC for 8 hours. The 5% diluted hydrogen in argon gas was also continuously supplied during the annealing process to remove the residue of the transfer process. Then, the substrate is placed inside of the MoS_2 CVD chamber together with 2 milligrams of Molybdenum trioxides (MoO_3) and 1

gram of sulfur as precursors for the MoS_2 growth. The chamber temperature increased to 550 ^oC in 30 minutes and then it was increased to 850 ^oC in 60 minutes. The growth time was 10 minutes and then furnace was cooled down to the room temperature by natural cooling. It is worth mentioning that increasing the time of the MoS_2 growth or the amount of the MoO_3 powder will result in the growth of the MoS_2 film on top of the graphene film.[250]

5.2.2. Details of the Raman Mapping

The Swift mode Raman mapping with a 500 nm scanning step size is performed for two different ranges with the total number of 1824 collected spectrums. The first range was from 100 cm^{-1} to 900 cm^{-1} and the second one was from 800 cm^{-1} to 1700 cm^{-1}.The CLS fitting was used to analyze the Raman data, which includes the E^2_g and A^1g peaks of the MoS_2 and the G peak of the graphene.

5.3. Electrical Characterization of MoS_2-Graphene Field-Effect Transistors (FETs)

Next, back-gated FETs were fabricated by patterning metal electrodes on the graphene films rather than on the MoS_2 channel (Figure 28a-b). Initially, two-probe current-voltage (I_d-V_{ds}) measurements were performed at a back-gate voltage (V_g) of 60 V (which turns on the devices) at different temperatures. We noticed almost an order of magnitude higher current and a more linear trend for the MoS_2-graphene devices compared with the MoS_2-metal ones.

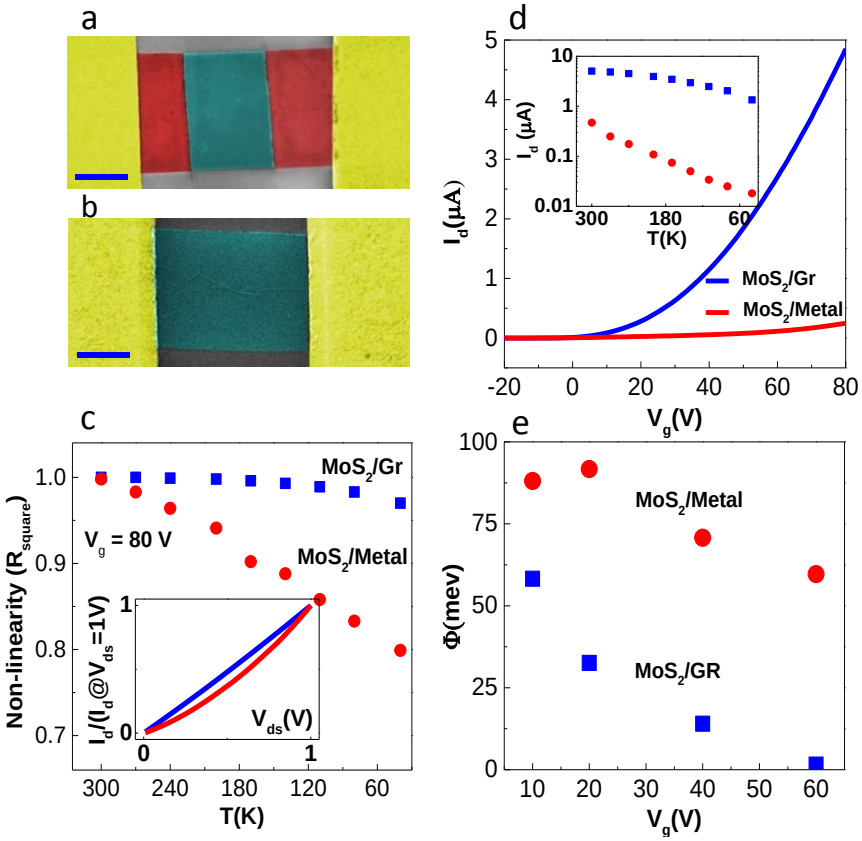

Figure 28. Electrical Characterization of MoS_2-Graphene and MoS_2-Metal Devices (a-b) SEM images of the MoS_2-graphene and MoS_2-metal FETs, respectively (scale bars 2 μm and 1 μm, respectively). (c) The linear regression (R_{square}) of the I_d-V_{sd} at different temperatures for the MoS_2-graphene and MoS_2-metal FETs (The inset shows normalized I_d-V_{sd} characteristics of the both devices – normalized with their respective I_d at V_{sd}=1V). (d) I_d-V_g characteristics of the MoS_2-graphene and MoS_2-metal FETs at 270 K (the inset shows the drain current at V_g=80V with respect to temperature). (e) Schottky barrier height - extracted from Arrhenius measurements - as a function of V_g for the MoS_2-graphene and MoS_2-metal FETs.

To compare the linearity of the I_d-V_{ds} trends, the normalized I_d-V_{ds} trends (Y axis: $I_d/I_{d@Vsd=1V}$) at temperature 270 K are shown as an inset to Figure 28c. Unlike the MoS_2-metal device, the MoS_2-graphene FET shows a linear behavior. The correlation coefficient

of the linear regression (R_{square}) in the I_d-V_{ds} is also calculated for both devices at different temperatures (see Figure 28c). The R_{square} of the MoS_2-graphene FET starts from 1 at room temperature and goes to 0.970 at 40 K. However, the R_{square} of the MoS_2-metal transistor shows greater temperature dependence (0.998 to 0.799). The larger non-linearity in the I_d-V_{ds} curve of the MoS_2-metal device compared to the MoS_2-graphene device – especially at low temperatures – suggests that a larger Schottky barrier is present for the metal-contacted MoS_2 device.

The I_d-V_g results at 270 K (Figure 28d) indicate that the current density ($I_d \times \frac{L}{W}$) at V_g = 80 V for the MoS_2-graphene FET is 20 times higher than the MoS_2-metal FET. This ratio becomes even larger at low temperatures and approaches ~74 times at 40 K (Figure 28d inset), which is attributed to a smaller barrier for thermally induced charge carriers in the MoS_2-graphene in-plane heterostructure. The extrinsic field-effect mobility is also calculated for both structures at room temperature and different back gate voltages. Both transistors are completely turned OFF at large negative gate biases and turned ON at a threshold voltage of 55 V and 40 V with an ON/OFF ratio of 10^4 and 10^5 for MoS_2-metal and MoS_2-graphene, respectively. The linear field-effect mobility is calculated as ~11.5 $cm^2/V.S$ for MoS_2-graphene and ~1.5 $cm^2/V.S$ for MoS_2-metal at V_g = 80 V. It should be noted that the field-effect mobility of the MoS_2-metal devices is consistent with the previously reported mobility of monolayer CVD MoS_2 without top-gate dielectrics.[113] However, higher extrinsic mobility values can be achieved by using multilayer MoS_2[251] or using high-k dielectric substrates/overcoats.[252] The temperature-dependent

measurements show that the mobility of the MoS_2-metal FET is reduced by 95% as the temperature is decreased to 40 K, while the MoS_2-graphene FET shows almost constant mobility down to 160 K and then 30% reduction in the mobility at 40 K. This temperature dependence is also demonstrated in the inset of Figure 28d in which the drain current of the MoS_2-graphene device reduces by ~4 times, while that of the MoS_2-metal device decreases by ~26 times.

To gain better insight concerning the Schottky barrier height, a 2D thermionic model is used to analyze the data (Arrhenius measurements).[253] Figure 29 shows the logarithmic plots of ($I_d/T^{3/2}$) versus (1000/T) for the MoS_2-graphene and MoS_2-metal interfaces at different V_{ds} and +40V back gate bias. To study the Schottky barrier height of the devices, a 2D thermionic equation $I_d=AT^{3/2}\exp\left(\frac{-q(\Phi_B-\frac{V_{ds}}{n})}{K_BT}\right)$ is used in which I_d is source-drain current, T is temperature, q is electron charge, K_B is Boltzmann constant, Φ_B is Schottky barrier height, V_{ds} is Source-drain current, n is Schottky diode non-ideality factor, and A is Richardson's constant[253], [254].

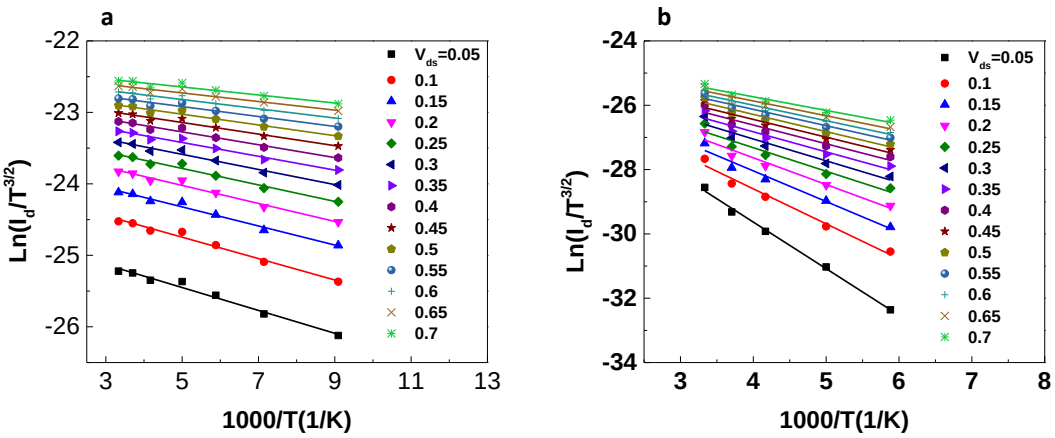

Figure 29. Arrhenius Measurements at V_g=40V for Different Applied V_{ds} for (a), MoS_2/Gr (b), MoS_2/Metal transistors

The slope of figure 29a ($\frac{-q(\Phi_B-\frac{V_{ds}}{n})}{K_BT}$) at each source-drain bias for V_g=40 V is derived and plotted in Figure 30 for the MoS_2-graphene in-plane heterostructure. Finally, the Schottky barrier height (Φ_B) is calculated at the intercept of Figure 30 with the Y axis, where the V_{ds} is zero[253].

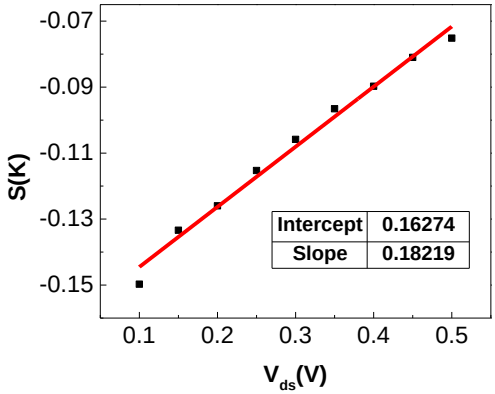

Figure 30. Slope of the Arrhenius graph as a function of the V_{ds} at gate 40 V.

In Figure 31, the Arrhenius graphs are also plotted at constant V_{sd} for different applied gate voltages at room temperature. Changing the slope of the Figure 31a from minus value

at V_g=50 V to about zero at V_g=60 V and positive value at V_g=70 V also confirms the absence of the Schottky barrier for the MoS_2-graphene in-plane contact at gate biases close to the 60 V and above. Figure 28e further shows the derived Schottky barrier height of both structures at room temperature for different applied gate voltages. The Schottky barrier height for the MoS_2-metal structure is about 88 meV at V_g = 10 V and decreases to 60 meV for V_g = 60 V, while the MoS_2-graphene in-plane heterostructure starts at ~58 meV at V_g = 10 V and fades to zero at V_g = 60 V.

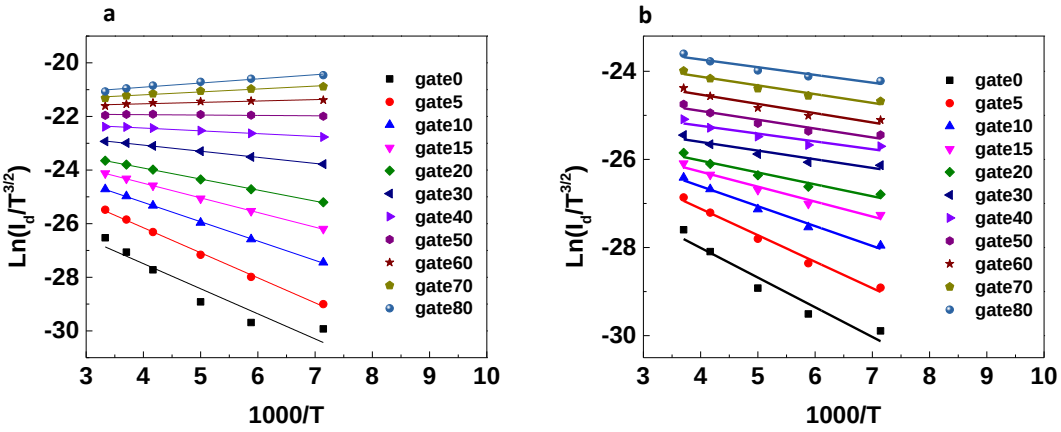

Figure 31. Arrhenius Measurements at V_{sd} = 1V for Different Applied V_g for (a) MoS_2-graphene (b) MoS_2-metal transistors.

5.3.1. Details for the Fabrication Process for the MoS_2-Graphene FETs

After the graphene film was transferred onto the SiO_2 substrate, it was patterned into rectangles by a photolithography process followed by oxygen plasma etching. Next, MoS_2-graphene heterostructure was synthesized, and the metal electrodes were patterned on the MoS_2-graphene FETs and on the MoS_2 FETs by an electron beam lithography method.

Finally, 10 nm Titanium and 60 nm Gold were deposited on the devices by an electron beam evaporation process.

5.4. Kelvin Probe Force Microscopy (KPFM)

KPFM experiments were also performed to map the surface potential distribution across the MoS_2-graphene interface under applied source-drain and gate voltages. Schematic of the setup is shown in Figure 32.

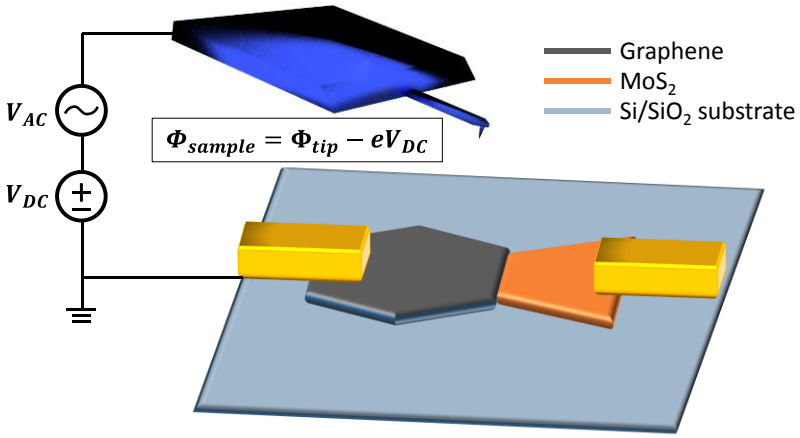

Figure 32. Schematic of Kelvin Probe Force Microscopy (KPFM) Setup.

This technique enables us to spatially map the local potential drops in the MoS_2-graphene lateral heterojunction and in the MoS_2 and graphene films under device operational conditions to gain insight into their relative contributions to the overall resistance of the device. Figure 33a shows the KPFM mapping of the device at V_{ds} = 0 V and V_g = 0 V. The change in the surface potential was also mapped along the entire length of the device at V_{ds} = 1V and at different gate voltages (Figure 33b-c). As the gate voltage increases from -20 V to +20 V, the potential drop across the interface decreases from 455

mV to 201 mV (Figure 33d). This observation implies that the contribution of the resistive potential drop across the interface relative to the total resistance of the device decreases as one increases the gate voltage. In other words, the MoS_2-graphene contact resistance has a negligible contribution to the overall device resistance at larger gate voltages.

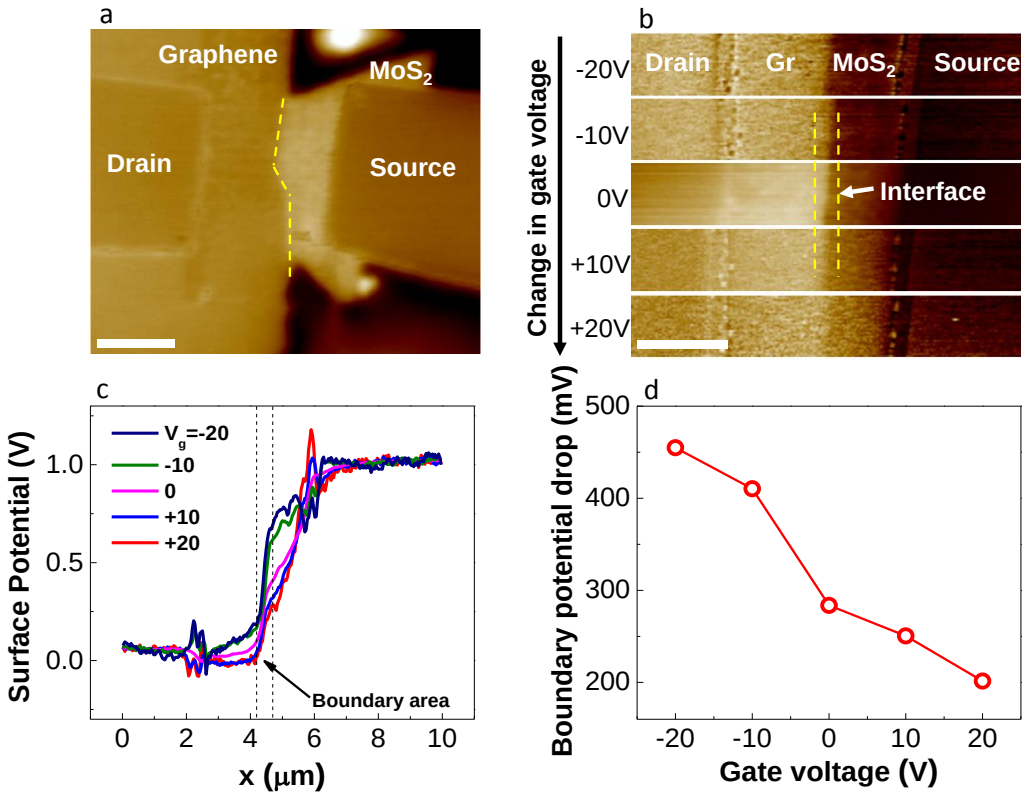

Figure 33. KPFM Measurements Under Operation. (a) KPFM mapping of the MoS_2-graphene transistor with $V_{gate} = 0\,V$ and $V_{sd} = 0\,V$. The interface between graphene and MoS_2 is highlighted with yellow dashed line (scale bar 2 μm). (b) KPFM mapping of the interface area from a selected region shown in (a) by keeping $V_{sd} = 1\,V$ and changing V_{gate} from $-20\,V$ to $+20\,V$ with $10\,V$ increments (Scale bar 2 μm). The dashed lines show the interface area. (c) Corresponding surface potential profiles across the interface area. (d) The potential drop at the interface area as a function of the applied gate voltages.

5.4.1. Details of the KPFM Measurements

All AFM experiments were carried out with a Dimension ICON system (Bruker, CA) in ambient conditions. PFQNE-AL cantilevers (Bruker, CA) were selected for improved spatial resolution in surface potential measurements. The nominal spring constant is 0.8 N/m and the resonant frequency is 300 kHz. Two-pass technique (also known as 'lift mode') was applied in KPFM experiments. During scanning, the sample was grounded, while a bias $\Delta V = V_{DC} + V_{AC}$ was applied to the AFM cantilever, where the V_{DC} and V_{AC} are the DC and AC component, respectively. The frequency of V_{AC} was chosen at the resonant frequency of the cantilever. The AFM controller nulled the cantilever amplitude due to periodic electrostatic force by adjusting V_{DC}. If the work function of the cantilever tip Φ_{tip} is known, then the sample work function Φ_s can be given as $\Phi_s = \Phi_{tip} - eV_{DC}$. Φ_s and V_{DC} are opposite in sign, so the work function Φ_s has inverse contrast with KPFM mapping. All AFM data were analyzed with Nanoscope Analysis software (Bruker, CA).

5.5. Low Frequency 1/f Noise Measurements

Next, a systematic study of 1/f noise was performed in the MoS_2-graphene and MoS_2-metal devices in a vacuum (pressure < 10^{-5} Torr) in a collaboration with Prof. Hersam's group. Low frequency 1/f noise has the potential to severely limit the performance of nanoscale materials because 1/f noise increases with decreasing number of carriers (i.e., device size). Recently, it has been shown that metal contacts can play a significant role in 1/f noise in CVD-grown MoS_2. Thus, 1/f noise is an important metric to gauge the quality

and viability of lateral graphene-MoS_2 heterojunctions. Extensive details of the noise measurements can be found in reference [4]. In summary, the normalized noise amplitude (A ~ 1/N) with the total number of carriers (i.e., channel area L × W) for all measured MoS_2-graphene and MoS_2-metal devices is shown in Figure 34. V_g dependence of normalized noise amplitude shows overall decreased noise in MoS_2-graphene. Furthermore, channel area-scaling results in a tighter distribution of noise metrics for MoS_2-graphene devices (Figure 34), suggesting MoS_2-metal has a larger contribution of noise from the contacts. Furthermore, the overall V_g dependence is more well-defined (A ~ $1/V_g$) in MoS_2-graphene devices, again corroborating the dominance of channel resistance fluctuations compared to contact resistance fluctuations.

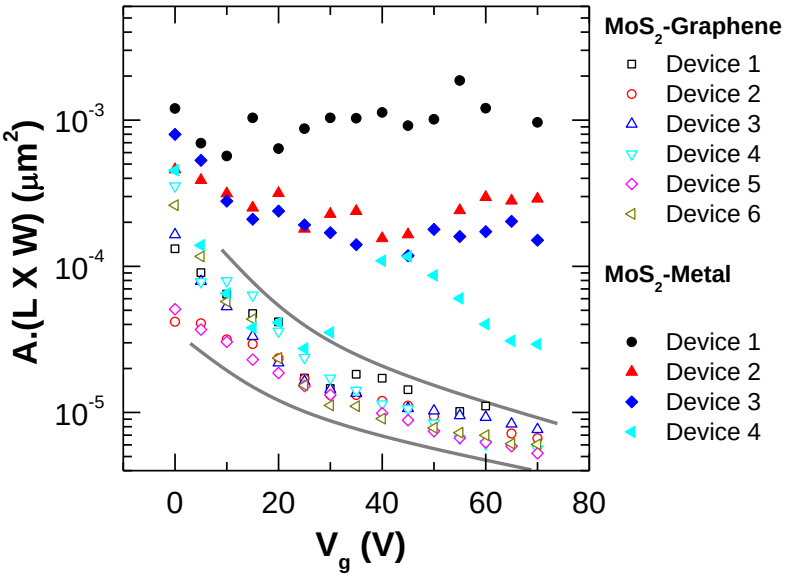

Figure 34. Comparison of Area-Normalized Noise Amplitude of MoS_2-Graphene and MoS_2-Metal FETs as a Function of V_g. Two gray lines show upper and lower bounds of noise amplitude for MoS_2-graphene devices.

5.6. Electrostatic Break-Down Tests

For reliable electronics, it is also critical to achieve mechanically and electrostatically robust contacts. The present MoS_2-graphene devices have essentially a 1D interface between two 2D materials. Thus far, electrostatic breakdown of a lateral heterojunction of this type has not been probed. Figure 35a,b shows current-voltage characteristics of a MoS_2-graphene and a MoS_2-metal device for V_d = 75 to -75 V (sweep rate = 1 V/s) under vacuum (pressure < 10^{-5} torr) which are carried out through a collaboration with Prof. Hersam's group. Both devices show qualitatively similar behavior of electrostatic breakdown. In particular, the current decreases irreversibly by more than 2 orders of magnitude within 1 V. Interestingly, both MoS_2-graphene and MoS_2-metal devices show comparable maximum width-normalized drain current (~40 μA/μm) just before breakdown, roughly an order of magnitude lower current density than high quality exfoliated monolayer MoS_2.[195] The breakdown field of the two devices is also comparable (~38 MV/m). SEM of the broken devices was conducted to probe morphological evidence of the failure mode (inset of Figure 35a-b). A significant portion of CVD MoS_2 was found missing near the drain contacts in both of the devices. This suggests a similar failure mechanism irrespective of metal or lateral graphene contacts. Thus, direct growth of the MoS_2-graphene heterojunction does not significantly affect the electrostatic breakdown characteristics of the devices.

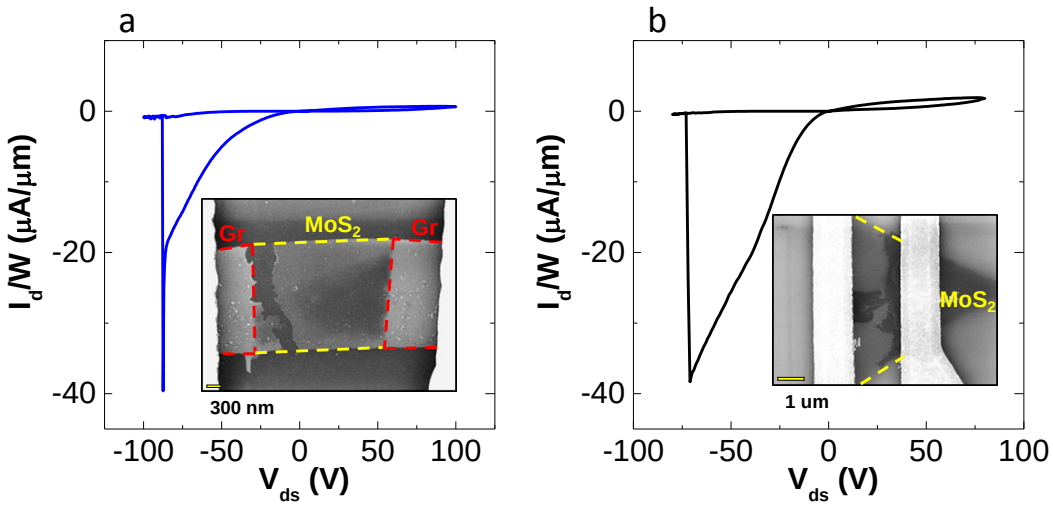

Figure 35. Breakdown Study of MoS_2-Graphene and MoS_2-Metal FETs. (a), (b) Current-voltage characteristics of a MoS_2-graphene and MoS_2-metal FET, respectively, at $V_g = 0$ V showing irreversible breakdown at large V_d. The current was normalized to the channel width. The insets of (a) and (b) show scanning electron microscopy micrographs of the MoS_2-graphene and MoS_2-metal FETs after the breakdown, respectively.

5.7. Summary and Conclusion

In conclusion, seed-free synthesis of graphene and MoS_2 lateral heterojunctions is reported through the CVD method, which exhibit improved electrical performance compared to conventional metal-contact MoS_2 devices. This method makes in-plane MoS_2-graphene heterostructures promising for the large-scale production of electronic and logic circuits from all-2D materials for next generation device applications. Temperature-dependent electrical characterization shows Ohmic behavior for the MoS_2-graphene FET devices at back-gate voltages above 60 V, verifying a high-quality lateral interface between MoS_2 and graphene. KPFM results also visualize the reduction of the MoS_2-graphene in-plane junction resistance at positive gate voltages. Moreover, MoS_2-graphene devices

show up to an order of magnitude lower noise amplitude in comparison to MoS_2-metal devices fabricated under similar conditions. The first electrostatic breakdown study of lateral MoS_2-graphene heterojunctions are also conducted. In this case, MoS_2-graphene and MoS_2-metal devices showed comparable current density, breakdown fields, and similar failure modes through microscopic visualization.

CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

In conclusion, this dissertation demonstrates the importance of different types of heterogeneities such as grain boundaries and interfaces on the thermal and electrical characteristics of 2D-material-based systems.

In the case of monolayer graphene synthesized by CVD technique, the results show that the thermal resistance of the GBs with large mismatch angles is almost an order of magnitude higher than those of GBs with small mismatch angles. The BTE modeling shows that this is only possible of an amorphous carbon region form at the coalescing region of two adjacent grains which accounts for the additional resistance observed in the highly mismatched GBs. This is due to the fact that such a large resistance cannot be caused by a single scattering event, considering the other scattering sources such as the ones at the interface with the substrate. For intermediately misoriented GBs, the average thermal conductivity of the polycrystalline film is determined by a complex interplay between the amount edge roughness and width of the amorphous region at the GB. Further study is required to probe the structure and morphology of the GB region to precisely determine its thermal properties. If one is to benefit from the outstandingly high thermal conductivity of graphene for thermal management and heat dissipation applications, the results suggest that a modified synthesis process which yields aligned graphene grains should be used.[255], [256] The results also highlight the important structure-property-processing

correlations of 1D defects on thermal transport in 2D crystals, emphasizing the importance of engineering such correlations in emerging 2D materials and devices.[1]

One of the main goals in this dissertation was to systematically study the interfacial thermal transport across CVD MoS_2 monolayers and compare the results to those of graphene in identical experimental conditions in order to identify the possible sources of disagreement in the literature. If the values in the range of 1 $MW.m^{-2}.K^{-1}$ stand for the TBC of MoS_2 with the substrate, the MoS_2-based circuitry would face enormous heat removal and thermal management challenges (10-20 times higher thermal resistance compared with an equivalent graphene device). To address this goal, the results were first validated on graphene with the well-established data in the literature obtained from different techniques (e.g., thermoreflectance and Raman).[35], [166], [172] In identical measurement platform and experimental conditions, it was then found that the TBC across MoS_2 remains in the same range as in graphene, far larger than the reports based on Raman thermometry with optical heating.[36], [37] The parameters which could potentially cause the above-discussed discrepancy in the measured TBC values in the literature was also investigated. Moreover, the effect of processing quality and potential interface contaminants (affecting the interface couplings and adhesion forces) were studied on the measured TBC values through a comparison between direct-grown and transferred MoS_2 monolayers. The results show that the TBC is highly dependent on the processing quality, as indicated by a TBC of ~19 $MW.m^{-2}.K^{-1}$ for transferred MoS_2 and ~37 $MW.m^{-2}.K^{-1}$ for direct-grown MoS_2 on sapphire. The effects of metal encapsulating layers on the TBC were investigated through

a combination of MD simulations and BTE modeling which reveal that the emergence of RWMs dramatically contributes to the interfacial conductance across encapsulated 2D monolayers.

In the cases that the through-plane thermal transport is the dominant pathway of heat removal, the heat dissipation capability of the system is defined by the substrate conductance as well as the TBC across the 2D materials. One major challenge is that the heat in high-conductance substrates such as diamond is usually carried by high-frequency phonons which transmit poorly through the Van der Waals interfaces that bind 2D materials. This implies that a practical trade-off exists between the bulk thermal conductivity of existing substrates and the interfacial conductance at their junction with the 2D materials. Another main finding of this dissertation was to quantify the limits of through-plane power dissipation in monolayer graphene, a representative of 2D materials, fabricated on the substrates with the highest available thermal conductances, e.g., CVD diamond, tape-casted (sintered) AlN, single crystalline sapphire, and silicon with different oxide layers. In the tested structures, the weights of the contributing thermal resistances were quantified in the through-plane direction, namely TBRs, dielectric resistance (if present), and bulk substrate resistance. The results demonstrate that the heat dissipation through graphene on AlN substrate near room temperature outperforms those of CVD diamond and other studied substrates, owing to its superior TBC. This study highlights that in a broader perspective, a system-level analysis is essential to quantify the thermal

dissipation limits in 2D material-based structures to realize their competitive advantage over their 3D counterparts.

Last, but not least, the creation of high-quality heterojunctions between conducting and semiconducting 2D materials were investigated, which are known to be an essential step to enable fabrication of all-2D electronic circuitry with competitive device performance. This is particularly important in MoS_2-based devices, as the performance and applications of typical metal-contacted MoS_2-based electronics are constrained by their contact electrodes due to the presence of huge contact resistances. In particular, due to the Fermi level pinning phenomenon, nearly all the metals form a Schottky barrier upon contact with MoS_2 which imposes large contact resistances on the extrinsic (2-probe) performance of the MoS_2-based devices. To address this issue, an all-CVD-based process is developed to synthesize nearly perfect lateral (in-plane) MoS_2-Graphene heterojunctions without noticeable gap or overlap. The fabricated FETs with graphene contacts exhibit an order of magnitude improved mobility and lower noise metrics over the metal-contacted MoS_2 FETs. This is attributed to the Ohmic behavior at the MoS_2-Graphene interface which is confirmed through various experimental results.

The results presented in this dissertation provide a comprehensive understanding of system-level thermal transport in graphene- and MoS_2-based nanoelectronic devices. The main assumption of such analyses is the formation of uniform heat sources in the system which is not true in the devices under operation. For the future works, one should investigate the temperature rise of the relevant 2D-based devices under operational

conditions to probe the power dissipation phenomena and identify the formation of localized hit-spots. Another pathway for future works is to investigate the materials which can form improved TBC with 2D materials. Obviously, improving TBC should take place on substrates with high thermal conductance. Another potential pathway for improving the TBC is through engineering of the encapsulating dielectrics. It may be possible to preserve the electronic functionality of a given device, meanwhile improve the TBC by depositing given dielectrics on top.

CITED LITERATURE

[1] P. Yasaei, A. Fathizadeh, R. Hantehzadeh, A. K. Majee, A. El-Ghandour, D. Estrada, C. Foster, Z. Aksamija, F. Khalili-Araghi, and A. Salehi-Khojin, "Bimodal Phonon Scattering in Graphene Grain Boundaries," *Nano Lett.*, vol. 15, no. 7, pp. 4532–4540, Jun. 2015.

[2] P. Yasaei, C. J. Foss, K. Karis, A. Behranginia, A. I. El-Ghandour, A. Fathizadeh, J. Olivares, A. K. Majee, C. D. Foster, F. Khalili-Araghi, Z. Aksamija, and A. Salehi-Khojin, "Interfacial Thermal Transport in Monolayer MoS 2 - and Graphene-Based Devices," *Adv. Mater. Interfaces*, p. 1700334, Jul. 2017.

[3] P. Yasaei, A. Behranginia, Z. Hemmat, A. I. El-Ghandour, C. D. Foster, and A. Salehi-Khojin, "Quantifying the limits of through-plane thermal dissipation in 2D-material-based systems," *2D Mater.*, vol. 4, no. 3, p. 35027, Aug. 2017.

[4] A. Behranginia, P. Yasaei, A. K. Majee, V. K. Sangwan, F. Long, C. J. Foss, T. Foroozan, S. Fuladi, M. R. Hantehzadeh, R. Shahbazian-Yassar, M. C. Hersam, Z. Aksamija, and A. Salehi-Khojin, "Direct Growth of High Mobility and Low-Noise Lateral MoS 2 -Graphene Heterostructure Electronics," *Small*, p. 1604301, Jun. 2017.

[5] G. Moore, "Progress in Digital Integrated Electronics," in *IEEE, IEDM Tech Digest*, 1975, p. pp.11-13.

[6] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides.," *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012.

[7] F. Xia, H. Wang, and Y. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics.," *Nat. Commun.*, vol. 5, p. 4458, Jan. 2014.

[8] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, no. 9–10, pp. 351–355, Jun. 2008.

[9] K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene.," *Nature*, vol. 490, no. 7419, pp. 192–200, Oct. 2012.

[10] B. Radisavljevic, a Radenovic, J. Brivio, V. Giacometti, and a Kis, "Single-layer MoS2 transistors.," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 147–50, Mar. 2011.

[11] D. Xiao, G.-B. Liu, W. Feng, X. Xu, and W. Yao, “Coupled Spin and Valley Physics in Monolayers of MoS_{2} and Other Group-VI Dichalcogenides,” *Phys. Rev. Lett.*, vol. 108, no. 19, p. 196802, May 2012.

[12] C. Shih, Q. H. Wang, Y. Son, Z. Jin, D. Blankschtein, and M. S. Strano, “Tuning On À O ff Current Ratio and Field-E ff ect Mobility in a MoS 2 À Graphene Heterostructure,” no. 6, pp. 5790–5798, 2014.

[13] S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, “High-mobility and low-power thin-film transistors based on multilayer MoS2 crystals.,” *Nat. Commun.*, vol. 3, p. 1011, Jan. 2012.

[14] S. Das, R. Gulotty, A. V Sumant, and A. Roelofs, “All two-dimensional, flexible, transparent, and thinnest thin film transistor.,” *Nano Lett.*, vol. 14, no. 5, pp. 2861–6, May 2014.

[15] A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches.,” *Nature*, vol. 479, no. 7373, pp. 329–37, Nov. 2011.

[16] S. Das, R. Gulotty, A. V Sumant, and A. Roelofs, “All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor,” *Nano Lett.*, vol. 14, no. 5, pp. 2861–2866, 2014.

[17] J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee, and H. C. Ko, “Highly flexible and transparent multilayer MoS2 transistors with graphene electrodes.,” *Small*, vol. 9, no. 19, pp. 3295–300, Oct. 2013.

[18] G.-H. Lee, Y. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, “Flexible and transparent MoS2 field-effect transistors on hexagonal boron nitride-graphene heterostructures.,” *ACS Nano*, vol. 7, no. 9, pp. 7931–6, Sep. 2013.

[19] A. D. Liao, J. Z. Wu, X. Wang, K. Tahy, D. Jena, H. Dai, and E. Pop, “Thermally Limited Current Carrying Ability of Graphene Nanoribbons,” *Phys. Rev. Lett.*, vol. 106, no. 25, p. 256801, Jun. 2011.

[20] M. M. Sadeghi, I. Jo, and L. Shi, “Phonon-interface scattering in multilayer graphene on an amorphous support,” *Proc. Natl. Acad. Sci.*, vol. 110, no. 41, pp. 16321–16326, 2013.

[21] A. M. van der Zande, P. Y. Huang, D. a Chenet, T. C. Berkelbach, Y. You, G.-H.

Lee, T. F. Heinz, D. R. Reichman, D. a Muller, and J. C. Hone, “Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide.,” *Nat. Mater.*, vol. 12, no. 6, pp. 554–61, Jun. 2013.

[22] S. Najmaei, Z. Liu, W. Zhou, X. Zou, G. Shi, S. Lei, B. I. Yakobson, J.-C. Idrobo, P. M. Ajayan, and J. Lou, “Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers.,” *Nat. Mater.*, vol. 12, no. 8, pp. 754–9, Aug. 2013.

[23] Q. Yu, L. a Jauregui, W. Wu, R. Colby, J. Tian, Z. Su, H. Cao, Z. Liu, D. Pandey, D. Wei, T. F. Chung, P. Peng, N. P. Guisinger, E. a Stach, J. Bao, S.-S. Pei, and Y. P. Chen, “Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition.,” *Nat. Mater.*, vol. 10, no. 6, pp. 443–9, Jun. 2011.

[24] I. Vlassiouk, M. Regmi, P. Fulvio, S. Dai, P. Datskos, G. Eres, and S. Smirnov, “Role of hydrogen in chemical vapor deposition growth of large single-crystal graphene.,” *ACS Nano*, vol. 5, no. 7, pp. 6069–76, Jul. 2011.

[25] P. Y. Huang, C. S. Ruiz-Vargas, A. M. van der Zande, W. S. Whitney, M. P. Levendorf, J. W. Kevek, S. Garg, J. S. Alden, C. J. Hustedt, Y. Zhu, J. Park, P. L. McEuen, and D. a Muller, “Grains and grain boundaries in single-layer graphene atomic patchwork quilts.,” *Nature*, vol. 469, no. 7330, pp. 389–92, Jan. 2011.

[26] A. Y. Serov, Z.-Y. Ong, and E. Pop, “Effect of grain boundaries on thermal transport in graphene,” *Appl. Phys. Lett.*, vol. 102, no. 3, p. 33104, 2013.

[27] Y. Jung, J. Shen, and J. J. Cha, “Surface effects on electronic transport of 2D chalcogenide thin films and nanostructures,” *Nano Converg.*, vol. 1, no. 1, p. 18, 2014.

[28] A. L. Moore and L. Shi, “Emerging challenges and materials for thermal management of electronics,” *Mater. Today*, vol. 17, no. 4, pp. 163–174, 2014.

[29] J. H. Seol, I. Jo, A. L. Moore, L. Lindsay, Z. H. Aitken, M. T. Pettes, X. Li, Z. Yao, R. Huang, D. Broido, N. Mingo, R. S. Ruoff, and L. Shi, “Two-dimensional phonon transport in supported graphene.,” *Science*, vol. 328, no. 5975, pp. 213–6, Apr. 2010.

[30] Z.-Y. Ong and E. Pop, “Effect of substrate modes on thermal transport in supported graphene,” *Phys. Rev. B*, vol. 84, no. 7, p. 75471, Aug. 2011.

[31] E. Pop, V. Varshney, and A. K. Roy, “Thermal properties of graphene: Fundamentals and applications,” *MRS Bull.*, vol. 37, no. 12, pp. 1273–1281, Nov.

2012.

[32] M.-H. Bae, Z. Li, Z. Aksamija, P. N. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, and E. Pop, “Ballistic to diffusive crossover of heat flow in graphene ribbons.,” *Nat. Commun.*, vol. 4, p. 1734, Jan. 2013.

[33] D. G. Cahill, P. V. Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson, P. Keblinski, W. P. King, G. D. Mahan, A. Majumdar, H. J. Maris, S. R. Phillpot, E. Pop, and L. Shi, “Nanoscale thermal transport. II. 2003?2012,” *Appl. Phys. Rev.*, vol. 1, no. 1, p. 11305, Mar. 2014.

[34] Z. Chen, W. Jang, W. Bao, C. N. Lau, and C. Dames, “Thermal contact resistance between graphene and silicon dioxide,” *Appl. Phys. Lett.*, vol. 95, no. 16, p. 161910, Oct. 2009.

[35] Y. K. Koh, M. H. Bae, D. G. Cahill, and E. Pop, “Heat conduction across monolayer and few-layer graphenes,” *Nano Lett.*, vol. 10, no. 11, pp. 4363–4368, 2010.

[36] A. Taube, J. Judek, A. Łapińska, and M. Zdrojek, “Temperature-dependent thermal properties of supported MoS2 monolayers,” *ACS Appl. Mater. Interfaces*, vol. 7, no. 9, pp. 5061–5065, 2015.

[37] X. Zhang, D. Sun, Y. Li, G. H. Lee, X. Cui, D. Chenet, Y. You, T. F. Heinz, and J. C. Hone, “Measurement of Lateral and Interfacial Thermal Conductivity of Single- and Bilayer MoS2 and MoSe2 Using Refined Optothermal Raman Technique,” *ACS Appl. Mater. Interfaces*, vol. 7, no. 46, pp. 25923–25929, 2015.

[38] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V Khotkevich, S. V Morozov, and a K. Geim, “Two-dimensional atomic crystals.,” *Proc. Natl. Acad. Sci. U. S. A.*, vol. 102, no. 30, pp. 10451–10453, 2005.

[39] M. Xu, T. Liang, M. Shi, and H. Chen, “Graphene-Like Two-Dimensional Materials,” *Chem. Rev.*, vol. 113, 2013.

[40] S. Z. Butler, S. M. Hollen, L. Cao, Y. Cui, J. A. Gupta, H. R. Guti??rrez, T. F. Heinz, S. S. Hong, J. Huang, A. F. Ismach, E. Johnston-Halperin, M. Kuno, V. V. Plashnitsa, R. D. Robinson, R. S. Ruoff, S. Salahuddin, J. Shan, L. Shi, M. G. Spencer, M. Terrones, W. Windl, and J. E. Goldberger, “Progress, challenges, and opportunities in two-dimensional materials beyond graphene,” *ACS Nano*, vol. 7, no. 4, pp. 2898–2926, 2013.

[41] J. M. Raimond, M. Brune, Q. Computation, F. De Martini, C. Monroe, D. L. Moehring, P. L. Knight, M. B. Plenio, V. Vedral, E. S. Polzik, C. Variables, S. L.

Braunstein, A. K. Pati, M. D. Lukin, I. J. Cirac, P. Zoller, C. Han, P. Xue, G. C. Guo, S. V Polyakov, A. Kuzmich, H. J. Kimble, J. I. Cirac, T. A. B. Kennedy, P. Horodecki, R. Horodecki, D. P. Divincenzo, J. A. Smolin, A. Beige, L. C. Kwek, P. Kok, J. A. Sauer, L. You, A. Zangwill, M. S. Chapman, and M. Nielsen, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, pp. 20–23, 204AD.

[42] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides.," *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012.

[43] Y. Shi, C. Hamsen, X. Jia, K. K. Kim, A. Reina, M. Hofmann, A. L. Hsu, K. Zhang, H. Li, Z. Y. Juang, M. S. Dresselhaus, L. J. Li, and J. Kong, "Synthesis of few-layer hexagonal boron nitride thin film by chemical vapor deposition," *Nano Lett.*, vol. 10, pp. 4134–4139, 2010.

[44] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, and P. D. Ye, "Phosphorene: an unexplored 2D semiconductor with a high hole mobility.," *ACS Nano*, vol. 8, no. 4, pp. 4033–41, Apr. 2014.

[45] K. K. Kim, A. Hsu, X. Jia, S. M. Kim, Y. Shi, M. Hofmann, D. Nezich, J. F. Rodriguez-Nieva, M. Dresselhaus, T. Palacios, and J. Kong, "Synthesis of monolayer hexagonal boron nitride on Cu foil using chemical vapor deposition," *Nano Lett.*, vol. 12, pp. 161–166, 2012.

[46] W. Ge, K. Kawahara, M. Tsuji, and H. Ago, "Large-scale synthesis of NbS2 nanosheets with controlled orientation on graphene by ambient pressure CVD.," *Nanoscale*, vol. 5, no. 207890, pp. 5773–8, 2013.

[47] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils.," *Science*, vol. 324, no. 5932, pp. 1312–1314, 2009.

[48] V. Nicolosi, M. Chhowalla, M. G. Kanatzidis, M. S. Strano, and J. N. Coleman, "Liquid Exfoliation of Layered Materials," *Science*, vol. 340, no. 6139, pp. 1226419–1226419, Jun. 2013.

[49] J. N. Coleman, M. Lotya, A. O'Neill, S. D. Bergin, P. J. King, U. Khan, K. Young, A. Gaucher, S. De, R. J. Smith, I. V Shvets, S. K. Arora, G. Stanton, H.-Y. Kim, K. Lee, G. T. Kim, G. S. Duesberg, T. Hallam, J. J. Boland, J. J. Wang, J. F. Donegan, J. C. Grunlan, G. Moriarty, A. Shmeliov, R. J. Nicholls, J. M. Perkins, E. M. Grieveson, K. Theuwissen, D. W. McComb, P. D. Nellist, and V. Nicolosi,

"Two-dimensional nanosheets produced by liquid exfoliation of layered materials.," *Science*, vol. 331, no. 6017, pp. 568–71, Feb. 2011.

[50] L. Exfoliation, P. Yasaei, B. Kumar, T. Foroozan, C. Wang, M. Asadi, D. Tuschel, J. E. Indacochea, R. F. Klie, and A. Salehi-khojin, "High-Quality Black Phosphorus Atomic Layers by Liquid-Phase Exfoliation," *Adv. Mater.*, vol. 27, no. 11, pp. 1887–1892, 2015.

[51] G. F. Schneider, V. E. Calado, H. Zandbergen, L. M. K. Vandersypen, and C. Dekker, "Wedging Transfer of Nanostructures," *Nano Lett.*, vol. 10, no. 5, pp. 1912–1916, May 2010.

[52] H. Li, J. M. T. Wu, X. Huang, Z. Y. Yin, J. Q. Liu, and H. Zhang, "A Universal, Rapid Method for Clean Transfer of Nanostructures onto Various Substrates," *ACS Nano*, vol. 8, no. 7, pp. 6563–6570, 2014.

[53] J. W. Suk, A. Kitt, C. W. Magnuson, Y. Hao, S. Ahmed, J. An, A. K. Swan, B. B. Goldberg, and R. S. Ruoff, "Transfer of CVD-grown monolayer graphene onto arbitrary substrates," *ACS Nano*, vol. 5, no. 9, pp. 6916–6924, 2011.

[54] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. Il Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes.," *Nat. Nanotechnol.*, vol. 5, no. August, pp. 574–578, 2010.

[55] X. Liang, B. a. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, H. Yuan, A. R. Hight Walker, Z. Liu, L. M. Peng, and C. a. Richter, "Toward clean and crackless transfer of graphene," *ACS Nano*, vol. 5, no. 11, pp. 9144–9153, 2011.

[56] A. Reina, H. Son, L. Jiao, B. Fan, M. S. Dresselhaus, Z. Liu, and J. Kong, "Transferring and identification of single- and few-layer graphene on arbitrary substrates," *J. Phys. Chem. C*, vol. 112, no. 46, pp. 17741–17744, 2008.

[57] a K. Geim and I. V Grigorieva, "Van der Waals heterostructures.," *Nature*, vol. 499, no. 7459, pp. 419–25, 2013.

[58] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V Gorbachev, S. V Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. a Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS2 heterostructures for flexible and transparent electronics.," *Nat. Nanotechnol.*, vol. 8, no. 2, pp. 100–3, 2013.

[59] J. Halim, S. Kota, M. R. Lukatskaya, M. Naguib, M. Q. Zhao, E. J. Moon, J.

Pitock, J. Nanda, S. J. May, Y. Gogotsi, and M. W. Barsoum, “Synthesis and Characterization of 2D Molybdenum Carbide (MXene),” *Adv. Funct. Mater.*, vol. 26, no. 18, pp. 3118–3127, 2016.

[60] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, and Y. Zhang, “Black phosphorus field-effect transistors.,” *Nat. Nanotechnol.*, vol. 9, no. 5, pp. 372–7, May 2014.

[61] M. C. Lemme, L. Li, T. Palacios, and F. Schwierz, “Two-dimensional materials for electronic applications,” *Mater. Res. Soc.*, vol. 39, no. August, pp. 711–718, 2014.

[62] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, “Electronics based on two-dimensional materials,” *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 768–779, 2014.

[63] C. Huang, S. Wu, A. M. Sanchez, J. J. P. Peters, R. Beanland, J. S. Ross, P. Rivera, W. Yao, D. H. Cobden, and X. Xu, “Lateral heterojunctions within monolayer semiconductors,” *Nat. Mater.*, vol. 13, no. December, p. 14, 2014.

[64] H. Coy Diaz, J. Avila, C. Chen, R. Addou, M. C. Asensio, and M. Batzill, “Direct observation of interlayer hybridization and dirac relativistic carriers in Graphene/MoS2 van der waals heterostructures,” *Nano Lett.*, vol. 15, no. 2, pp. 1135–1140, 2015.

[65] D. Akinwande, N. Petrone, and J. Hone, “Two-dimensional flexible nanoelectronics.,” *Nat. Commun.*, vol. 5, p. 5678, 2014.

[66] J.-S. Kim, Y. Liu, W. Zhu, S. Kim, D. Wu, L. Tao, A. Dodabalapur, K. Lai, and D. Akinwande, “Toward Air-Stable Multilayer Phosphorene Thin-Films and Transistors,” *Arxiv*, vol. 1412.0355, 2014.

[67] C. R. Dean, a F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone, “Boron nitride substrates for high-quality graphene electronics.,” *Nat. Nanotechnol.*, vol. 5, no. 10, pp. 722–726, 2010.

[68] Z. Sun, A. Martinez, and F. Wang, “Optical modulators with two-dimensional layered materials,” *Nat. Photonics*, vol. 10, no. 4, pp. 227–238, 2016.

[69] G. R. Bhimanapati, Z. Lin, V. Meunier, Y. Jung, J. Cha, S. Das, D. Xiao, Y. Son, M. S. Strano, V. R. Cooper, and Others, “Recent advances in two-dimensional materials beyond graphene,” *ACS Nano*, vol. 9, no. 12, pp. 11509–11539, 2015.

[70] A. Lipatov, M. Alhabeb, M. R. Lukatskaya, A. Boson, Y. Gogotsi, and A. Sinitskii, "Effect of Synthesis on Quality, Electronic Properties and Environmental Stability of Individual Monolayer Ti3C2 MXene Flakes," *Adv. Electron. Mater.*, 2016.

[71] M. Chhowalla, H. S. Shin, G. Eda, L.-J. Li, K. P. Loh, and H. Zhang, "The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets," *Nat. Chem.*, vol. 5, no. 4, pp. 263–275, Mar. 2013.

[72] H. Zhang, "Ultrathin Two-Dimensional Nanomaterials," *ACS Nano*, vol. 9, no. 10, pp. 9451–9469, Oct. 2015.

[73] J. a. Miwa, M. Dendzik, S. S. Grønborg, M. Bianchi, J. V. Lauritsen, P. Hofmann, and S. Ulstrup, "Van der Waals Epitaxy of Two-Dimensional MoS_2–Graphene Heterostructures in Ultrahigh Vacuum," *ACS Nano*, vol. 9, no. 6, pp. 6502–6510, 2015.

[74] J. M. Woods, Y. Jung, Y. Xie, W. Liu, Y. Liu, H. Wang, and J. J. Cha, "One-Step Synthesis of MoS2/WS2 Layered Heterostructures and Catalytic Activity of Defective Transition Metal Dichalcogenide Films," *ACS Nano*, vol. 10, no. 2, pp. 2004–2009, Feb. 2016.

[75] K. S. Novoselov and a H. Castro Neto, "Two-dimensional crystals-based heterostructures: materials with tailored properties," *Phys. Scr.*, vol. T146, p. 14006, 2012.

[76] Y. Lin, C. S. Chang, R. K. Ghosh, J. Li, H. Zhu, B. Diaconescu, T. Ohta, X. Peng, N. Lu, M. J. Kim, J. T. Robinson, R. M. Wallace, T. S. Mayer, S. Datta, L. Li, and J. A. Robinson, "Atomically Thin Heterostructures Based on Single-Layer Tungsten Diselenide and Graphene," no. 1, pp. 1–6, 2014.

[77] Y. Gong, J. Lin, X. Wang, G. Shi, S. Lei, Z. Lin, X. Zou, G. Ye, R. Vajtai, B. I. Yakobson, H. Terrones, M. Terrones, B. K. Tay, J. Lou, S. T. Pantelides, Z. Liu, W. Zhou, and P. M. Ajayan, "Vertical and in-plane heterostructures from WS2/MoS2 monolayers," *Nat. Mater.*, vol. 13, no. September, 2014.

[78] M. C. Hersam, "Functional Nanomaterial Heterostructures," 2014.

[79] M. P. Levendorf, C.-J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. a. Muller, and J. Park, "Graphene and boron nitride lateral heterostructures for atomically thin circuitry," *Nature*, vol. 488, no. 7413, pp. 627–632, 2012.

[80] J. C. Koepke, J. D. Wood, D. Estrada, Z.-Y. Ong, K. T. He, E. Pop, and J. W. Lyding, "Atomic-scale evidence for potential barriers and strong carrier scattering

at graphene grain boundaries: a scanning tunneling microscopy study.," *ACS Nano*, vol. 7, no. 1, pp. 75–86, Jan. 2013.

[81] J. Zhang, J. Gao, L. Liu, and J. Zhao, "Electronic and transport gaps of graphene opened by grain boundaries," *J. Appl. Phys.*, vol. 112, no. 5, p. 53713, 2012.

[82] S. B. Kumar and J. Guo, "Strain-induced conductance modulation in graphene grain boundary," *Nano Lett.*, vol. 12, no. 3, pp. 1362–1366, 2012.

[83] Y. Liu and B. I. Yakobson, "Cones, pringles, and grain boundary landscapes in graphene topology," *Nano Lett.*, vol. 10, no. 6, pp. 2178–2183, 2010.

[84] A. W. Tsen, L. Brown, M. P. Levendorf, F. Ghahari, P. Y. Huang, R. W. Havener, C. S. Ruiz-Vargas, D. a Muller, P. Kim, and J. Park, "Tailoring electrical transport across grain boundaries in polycrystalline graphene.," *Science*, vol. 336, no. 6085, pp. 1143–6, Jun. 2012.

[85] O. V. Yazyev and S. G. Louie, "Topological defects in graphene: Dislocations and grain boundaries," *Phys. Rev. B*, vol. 81, no. 19, p. 195420, May 2010.

[86] Y. Zhang, Y. Zhang, Q. Ji, J. Ju, H. Yuan, J. Shi, T. Gao, D. Ma, M. Liu, Y. Chen, X. Song, H. Y. Hwang, Y. Cui, and Z. Liu, "Controlled growth of high-quality monolayer WS2 layers on sapphire and imaging its grain boundary.," *ACS Nano*, vol. 7, no. 10, pp. 8963–71, Oct. 2013.

[87] K. Kim, Z. Lee, W. Regan, C. Kisielowski, M. F. Crommie, and a. Zettl, "Grain boundary mapping in polycrystalline graphene," *ACS Nano*, vol. 5, no. 3, pp. 2142–2146, 2011.

[88] M. Ahmad, H. An, Y. S. Kim, J. H. Lee, J. Jung, S.-H. Chun, and Y. Seo, "Nanoscale investigation of charge transport at the grain boundaries and wrinkles in graphene film," *Nanotechnology*, vol. 23, no. 28, p. 285705, 2012.

[89] a. Mesaros, S. Papanikolaou, C. F. J. Flipse, D. Sadri, and J. Zaanen, "Electronic states of graphene grain boundaries," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 82, no. 20, pp. 1–8, 2010.

[90] I. a. Ovid'ko, "Review on grain boundaries in graphene. Curved poly- and nanocrystalline graphene structures as new carbon allotropes," *Rev. Adv. Mater. Sci.*, vol. 30, no. 3, pp. 201–224, 2012.

[91] J. Červenka and C. Flipse, "Structural and electronic properties of grain boundaries in graphite: Planes of periodically distributed point defects," *Phys. Rev. B*, vol. 79, no. 19, p. 195429, May 2009.

[92] S. Malola, H. Häkkinen, and P. Koskinen, “Structural, chemical, and dynamical trends in graphene grain boundaries,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 81, no. 16, pp. 1–6, 2010.

[93] T. H. Ly, M. Chiu, M. Li, J. Zhao, D. J. Perello, M. O. Cichocka, H. M. Oh, S. H. Chae, H. Y. Jeong, F. Yao, L. Li, and Y. H. Lee, “Observing Grain Boundaries in CVD-grown Monolayer Transition Metal Dichalcogenides,” 2014.

[94] L. P. Biró and P. Lambin, “Grain boundaries in graphene grown by chemical vapor deposition,” *New J. Phys.*, vol. 15, 2013.

[95] L. Tapasztó, P. Nemes-Incze, G. Dobrik, K. Jae Yoo, C. Hwang, and L. P. Biró, “Mapping the electronic properties of individual graphene grain boundaries,” *Appl. Phys. Lett.*, vol. 100, no. 5, p. 53114, 2012.

[96] K. W. Clark, X.-G. Zhang, I. V Vlassiouk, G. He, R. M. Feenstra, and A.-P. Li, “Spatially resolved mapping of electrical conductivity across individual domain (grain) boundaries in graphene.,” *ACS Nano*, vol. 7, no. 9, pp. 7956–66, Sep. 2013.

[97] a. W. Tsen, L. Brown, M. P. Levendorf, F. Ghahari, P. Y. Huang, R. W. Havener, C. S. Ruiz-Vargas, D. a. Muller, P. Kim, and J. Park, “Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene,” *Science*, vol. 336, no. 6085, pp. 1143–1146, 2012.

[98] R. Grantab, V. B. Shenoy, and R. S. Ruoff, “Anomalous strength characteristics of tilt grain boundaries in graphene.,” *Science*, vol. 330, no. November, pp. 946–948, 2010.

[99] P. Yasaei, B. Kumar, R. Hantehzadeh, M. Kayyalha, A. Baskin, N. Repnin, C. Wang, R. F. Klie, Y. P. Chen, P. Král, and A. Salehi-Khojin, “Chemical sensing with switchable transport channels in graphene grain boundaries,” *Nat. Commun.*, vol. 5, p. 4911, Sep. 2014.

[100] G.-H. Lee, R. C. Cooper, S. J. An, S. Lee, A. van der Zande, N. Petrone, A. G. Hammerberg, C. Lee, B. Crawford, W. Oliver, J. W. Kysar, and J. Hone, “High-strength chemical-vapor-deposited graphene and grain boundaries.,” *Science*, vol. 340, no. 6136, pp. 1073–6, May 2013.

[101] X. Hong, J. Kim, S.-F. Shi, Y. Zhang, C. Jin, Y. Sun, S. Tongay, J. Wu, Y. Zhang, and F. Wang, “Ultrafast charge transfer in atomically thin MoS2/WS2 heterostructures,” *Nat. Nanotechnol.*, vol. 9, no. August, pp. 1–5, 2014.

[102] L. a. Ponomarenko, a. K. Geim, a. a. Zhukov, R. Jalil, S. V. Morozov, K. S.

Novoselov, I. V. Grigorieva, E. H. Hill, V. Cheianov, V. Falko, K. Watanabe, T. Taniguchi, and R. V. Gorbachev, "Tunable metal-insulator transition in double-layer graphene heterostructures," *Nat. Phys.*, vol. 7, no. 12, pp. 958–961, 2011.

[103] X. Cui, G.-H. Lee, Y. D. Kim, G. Arefe, P. Y. Huang, C. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, F. Pizzocchero, B. S. Jessen, K. Watanabe, T. Taniguchi, D. A. Muller, T. Low, P. Kim, and J. Hone, "Multi-terminal transport measurements of MoS2 using a van der Waals heterostructure device platform," *Nat. Nanotechnol.*, vol. 10, no. 6, pp. 534–540, 2015.

[104] S. Tongay, W. Fan, J. Kang, J. Park, U. Koldemir, J. Suh, D. S. Narang, K. Liu, J. Ji, J. Li, R. Sinclair, and J. Wu, "Tuning interlayer coupling in large-area heterostructures with CVD-grown MoS2 and WS2 monolayers," *Nano Lett.*, vol. 14, no. 6, pp. 3185–3190, 2014.

[105] J. Zhang, W. Xie, J. Zhao, and S. Zhang, "Band alignment of two-dimensional lateral heterostructures," *2D Mater.*, vol. 4, no. 1, p. 15038, Dec. 2016.

[106] Z. Liu, L. Ma, G. Shi, W. Zhou, Y. Gong, S. Lei, X. Yang, J. Zhang, J. Yu, K. P. Hackenberg, A. Babakhani, J.-C. Idrobo, R. Vajtai, J. Lou, and P. M. Ajayan, "In-plane heterostructures of graphene and hexagonal boron nitride with controlled domain sizes.," *Nat. Nanotechnol.*, vol. 8, no. 2, pp. 119–24, 2013.

[107] C. Shih, Q. H. Wang, Y. Son, Z. Jin, D. Blankschtein, and M. S. Strano, "Tuning On–Off Current Ratio and Field-Effect Mobility in a MoS 2 –Graphene Heterostructure via Schottky Barrier Modulation," *ACS Nano*, vol. 8, no. 6, pp. 5790–5798, Jun. 2014.

[108] M. S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. H. Lee, P. Kim, J. Hone, and W. J. Yoo, "Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices.," *Nat. Commun.*, vol. 4, p. 1624, 2013.

[109] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, a. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, a. K. Geim, K. S. Novoselov, and L. a. Ponomarenko, "Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures," *Science*, vol. 335, no. 6071, pp. 947–950, 2012.

[110] W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang, and X. Duan, "Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters," *Nat. Mater.*, vol. 12, no. 3, pp. 246–252, 2012.

[111] X. Hong, J. Kim, S.-F. Shi, Y. Zhang, C. Jin, Y. Sun, S. Tongay, J. Wu, Y. Zhang, and F. Wang, "Ultrafast charge transfer in atomically thin MoS2/WS2

heterostructures," *Nat. Nanotechnol.*, vol. 9, no. August, pp. 1–5, 2014.

[112] F. Xia, H. Wang, D. Xiao, M. Dubey, and A. Ramasubramaniam, "Two-dimensional material nanophotonics," *Nat. Photonics*, vol. 8, no. 12, pp. 899–907, 2014.

[113] L. Yu, Y. H. Lee, X. Ling, E. J. G. Santos, Y. C. Shin, Y. Lin, M. Dubey, E. Kaxiras, J. Kong, H. Wang, and T. Palacios, "Graphene/MoS2 Hybrid technology for large-scale two-dimensional electronics," *Nano Lett.*, vol. 14, no. 6, pp. 3055–3063, 2014.

[114] X. Ling, Y. Lin, Q. Ma, Z. Wang, Y. Song, L. Yu, S. Huang, W. Fang, X. Zhang, A. L. Hsu, Y. Bie, Y.-H. Lee, Y. Zhu, L. Wu, J. Li, P. Jarillo-Herrero, M. S. Dresselhaus, T. Palacios, and J. Kong, "Parallel Stitching of Two-Dimensional Materials," p. 30, 2015.

[115] X. X. Duan, C. Wang, J. C. Shaw, R. Cheng, Y. Chen, H. Li, X. Wu, Y. Tang, Q. Zhang, A. Pan, J. Jiang, R. Yu, Y. Huang, and X. X. Duan, "Lateral epitaxial growth of two-dimensional layered semiconductor heterojunctions," *Nat. Nanotechnol.*, vol. 9, no. 12, pp. 1024–1030, 2014.

[116] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, "Electronics based on two-dimensional materials," *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 768–779, 2014.

[117] Y. Liu, H. Wu, H.-C. Cheng, S. Yang, E. Zhu, Q. He, M. Ding, D. Li, J. Guo, N. O. Weiss, Y. Huang, and X. Duan, "Toward Barrier Free Contact to Molybdenum Disulfide Using Graphene Electrodes," *Nano Lett.*, vol. 15, no. 5, pp. 3030–3034, 2015.

[118] X. Duan, C. Wang, J. C. Shaw, R. Cheng, Y. Chen, H. Li, X. Wu, Y. Tang, Q. Zhang, A. Pan, J. Jiang, R. Yu, Y. Huang, and X. Duan, "Lateral epitaxial growth of two-dimensional layered semiconductor heterojunctions," *Nat Nanotechnol*, vol. 9, no. 12, pp. 1024–1030, 2014.

[119] R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, and M. Chhowalla, "Phase-engineered low-resistance contacts for ultrathin MoS2 transistors," *Nat. Mater.*, vol. 13, no. 12, pp. 1128–1134, 2014.

[120] X. Ling, Y. Lin, Q. Ma, Z. Wang, Y. Song, L. Yu, S. Huang, W. Fang, X. Zhang, A. L. Hsu, Y. Bie, Y. H. Lee, Y. Zhu, L. Wu, J. Li, P. Jarillo-Herrero, M. Dresselhaus, T. Palacios, and J. Kong, "Parallel Stitching of 2D Materials," *Adv. Mater.*, vol. 28, no. 12, pp. 2322–2329, 2016.

[121] Q. Qiao, R. F. Klie, S. Ogut, and J. C. Idrobo, “Atomic and electronic structures of SrTiO3/GaAs heterointerfaces: An 80-kV atomic-resolution electron energy-loss spectroscopy study.,” *Phys. Rev. B*, vol. 85, no. 16, p. 165406, Apr. 2012.

[122] K. Chen, X. Wan, and J. Xu, “Epitaxial Stitching and Stacking Growth of Atomically Thin Transition-Metal Dichalcogenides (TMDCs) Heterojunctions,” *Adv. Funct. Mater.*, vol. 27, no. 19, p. 1603884, May 2017.

[123] H. Yu, A. Kutana, and B. I. Yakobson, “Carrier Delocalization in Two-Dimensional Coplanar p–n Junctions of Graphene and Metal Dichalcogenides,” *Nano Lett.*, vol. 16, no. 8, pp. 5032–5036, Aug. 2016.

[124] X. Chen, Y. J. Park, T. Das, H. Jang, J.-B. Lee, and J.-H. Ahn, “Lithography-free plasma-induced patterned growth of MoS 2 and its heterojunction with graphene,” *Nanoscale*, vol. 8, no. 33, pp. 15181–15188, 2016.

[125] M. H. D. Guimarães, H. Gao, Y. Han, K. Kang, S. Xie, C.-J. Kim, D. A. Muller, D. C. Ralph, and J. Park, “Atomically Thin Ohmic Edge Contacts Between Two-Dimensional Materials,” *ACS Nano*, vol. 10, no. 6, pp. 6392–6399, Jun. 2016.

[126] K. L. Grosse, M.-H. Bae, F. Lian, E. Pop, and W. P. King, “Nanoscale Joule heating, Peltier cooling and current crowding at graphene-metal contacts.,” *Nat. Nanotechnol.*, vol. 6, no. 5, pp. 287–290, 2011.

[127] D. G. Cahill, P. V. Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson, P. Keblinski, W. P. King, G. D. Mahan, A. Majumdar, H. J. Maris, S. R. Phillpot, E. Pop, and L. Shi, “Nanoscale thermal transport. II. 2003–2012,” *Appl. Phys. Rev.*, vol. 1, no. 1, p. 11305, Mar. 2014.

[128] K. L. Grosse, V. E. Dorgan, D. Estrada, J. D. Wood, I. Vlassiouk, G. Eres, J. W. Lyding, W. P. King, and E. Pop, “Direct observation of resistive heating at graphene wrinkles and grain boundaries,” *Appl. Phys. Lett.*, vol. 105, no. 14, p. 143109, Oct. 2014.

[129] D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris, R. Merlin, and S. R. Phillpot, “Nanoscale thermal transport,” *J. Appl. Phys.*, vol. 93, no. 2, pp. 793–818, 2003.

[130] E. Pop, S. Sinha, and K. E. Goodson, “Heat generation and transport in nanometer-scale transistors,” *Proc. IEEE*, vol. 94, no. 8, pp. 1587–1601, 2006.

[131] E. Pop, “Energy dissipation and transport in nanoscale devices,” *Nano Res.*, vol. 3, no. 3, pp. 147–169, 2010.

[132] M. H. Bae, Z. Y. Ong, D. Estrada, and E. Pop, “Imaging, simulation, and electrostatic control of power dissipation in graphene devices,” *Nano Lett.*, vol. 10, no. 12, pp. 4787–4793, 2010.

[133] E. Yalon, C. J. McClellan, K. K. H. Smithe, M. Mu?oz Rojo, R. (Lily) Xu, S. V. Suryavanshi, A. J. Gabourie, C. M. Neumann, F. Xiong, A. B. Farimani, and E. Pop, “Energy Dissipation in Monolayer MoS 2 Electronics,” *Nano Lett.*, vol. 17, no. 6, pp. 3429–3433, Jun. 2017.

[134] G. Chen, *Nanoscale Energy Transport and Conversion*. 2005.

[135] Y. Yue, J. Zhang, X. Tang, S. Xu, and X. Wang, “Thermal transport across atomic-layer material interfaces,” *Nanotechnol. Rev.*, vol. 4, no. 6, Jan. 2015.

[136] A. Weathers and L. Shi, “THERMAL TRANSPORT MEASUREMENT TECHNIQUES FOR NANOWIRES AND NANOTUBES,” *Annu. Rev. Heat Transf.*, vol. 16, no. 1, pp. 101–134, 2013.

[137] Q. Y. Li, W. G. Ma, and X. Zhang, “Laser flash Raman spectroscopy method for characterizing thermal diffusivity of supported 2D nanomaterials,” *Int. J. Heat Mass Transf.*, vol. 95, pp. 956–963, 2016.

[138] G. L. Eesley, B. M. Clemens, and C. A. Paddock, “Generation and detection of picosecond acoustic pulses in thin metal films,” *Appl. Phys. Lett.*, vol. 50, no. 12, pp. 717–719, Mar. 1987.

[139] W. S. Capinski and H. J. Maris, “Improved apparatus for picosecond pump-and-probe optical measurements,” *Rev. Sci. Instrum.*, vol. 67, no. 8, pp. 2720–2726, Aug. 1996.

[140] B. Bonello, B. Perrin, and C. Rossignol, “Photothermal properties of bulk and layered materials by the picosecond acoustics technique,” *J. Appl. Phys.*, vol. 83, no. 6, pp. 3081–3088, Mar. 1998.

[141] H.-K. Lyeo and D. G. Cahill, “Thermal conductance of interfaces between highly dissimilar materials,” *Phys. Rev. B*, vol. 73, no. 14, p. 144301, Apr. 2006.

[142] Y. Wang, N. Xu, D. Li, and J. Zhu, “Thermal Properties of Two Dimensional Layered Materials,” *Adv. Funct. Mater.*, vol. 27, no. 19, p. 1604134, May 2017.

[143] D. G. Cahill, “Thermal conductivity measurement from 30 to 750 K: The 3ω method,” *Rev. Sci. Instrum.*, vol. 61, no. 2, pp. 802–808, 1990.

[144] J. Tang, H.-T. Wang, D. H. Lee, M. Fardy, Z. Huo, T. P. Russell, and P. Yang, “Holey Silicon as an Efficient Thermoelectric Material,” *Nano Lett.*, vol. 10, no.

10, pp. 4279–4283, Oct. 2010.

[145] A. Mavrokefalos, M. T. Pettes, F. Zhou, and L. Shi, “Four-probe measurements of the in-plane thermoelectric properties of nanofilms,” *Rev. Sci. Instrum.*, vol. 78, no. 3, p. 34901, Mar. 2007.

[146] J. Zhu, K. Hippalgaonkar, S. Shen, K. Wang, Y. Abate, S. Lee, J. Wu, X. Yin, A. Majumdar, and X. Zhang, “Temperature-Gated Thermal Rectifier for Active Heat Flow Control,” *Nano Lett.*, vol. 14, no. 8, pp. 4867–4872, Aug. 2014.

[147] C. W. Chang, D. Okawa, H. Garcia, A. Majumdar, and A. Zettl, “Breakdown of Fourier’s Law in Nanotube Thermal Conductors,” *Phys. Rev. Lett.*, vol. 101, no. 7, p. 75903, Aug. 2008.

[148] M. Fardy, A. I. Hochbaum, J. Goldberger, M. M. Zhang, and P. Yang, “Synthesis and Thermoelectrical Characterization of Lead Chalcogenide Nanowires,” *Adv. Mater.*, vol. 19, no. 19, pp. 3047–3051, Oct. 2007.

[149] L. Shi, D. Li, C. Yu, W. Jang, D. Kim, Z. Yao, P. Kim, and A. Majumdar, “Measuring Thermal and Thermoelectric Properties of One-Dimensional Nanostructures Using a Microfabricated Device,” *J. Heat Transfer*, vol. 125, no. 5, p. 881, 2003.

[150] Z. Wang, R. Xie, C. T. Bui, D. Liu, X. Ni, B. Li, and J. T. L. Thong, “Thermal Transport in Suspended and Supported Few-Layer Graphene,” *Nano Lett.*, vol. 11, no. 1, pp. 113–118, Jan. 2011.

[151] I. Jo, M. T. Pettes, E. Ou, W. Wu, and L. Shi, “Basal-plane thermal conductivity of few-layer molybdenum disulfide,” *Appl. Phys. Lett.*, vol. 104, no. 20, p. 201902, May 2014.

[152] S. Lee, F. Yang, J. Suh, S. Yang, Y. Lee, G. Li, H. Sung Choe, A. Suslu, Y. Chen, C. Ko, J. Park, K. Liu, J. Li, K. Hippalgaonkar, J. J. Urban, S. Tongay, and J. Wu, “Anisotropic in-plane thermal conductivity of black phosphorus nanoribbons at temperatures higher than 100 K,” *Nat. Commun.*, vol. 6, p. 8573, Oct. 2015.

[153] X. Xu, L. F. C. Pereira, Y. Wang, J. Wu, K. Zhang, X. Zhao, S. Bae, C. Tinh Bui, R. Xie, J. T. L. Thong, B. H. Hong, K. P. Loh, D. Donadio, B. Li, and B. Özyilmaz, “Length-dependent thermal conductivity in suspended single-layer graphene,” *Nat. Commun.*, vol. 5, Apr. 2014.

[154] J. H. Seol, A. L. Moore, L. Shi, I. Jo, and Z. Yao, “Thermal Conductivity Measurement of Graphene Exfoliated on Silicon Dioxide,” *J. Heat Transfer*, vol. 133, no. 2, p. 22403, 2011.

[155] A. a Balandin, “Thermal properties of graphene and nanostructured carbon materials.,” *Nat. Mater.*, vol. 10, no. 8, pp. 569–81, Aug. 2011.

[156] M. T. Pettes, I. Jo, Z. Yao, and L. Shi, “Influence of polymeric residue on the thermal conductivity of suspended bilayer graphene,” *Nano Lett.*, vol. 11, no. 3, pp. 1195–1200, 2011.

[157] A. a Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, “Superior thermal conductivity of single-layer graphene.,” *Nano Lett.*, vol. 8, no. 3, pp. 902–7, Mar. 2008.

[158] S. Sahoo, A. P. S. Gaur, M. Ahmadi, M. J.-F. Guinel, and R. S. Katiyar, “Temperature-Dependent Raman Studies and Thermal Conductivity of Few-Layer MoS 2,” *J. Phys. Chem. C*, vol. 117, no. 17, pp. 9042–9047, May 2013.

[159] R. Yan, J. R. Simpson, S. Bertolazzi, J. Brivio, M. Watson, X. Wu, A. Kis, T. Luo, A. R. Hight Walker, and H. G. Xing, “Thermal Conductivity of Monolayer Molybdenum Disulfide Obtained from Temperature-Dependent Raman Spectroscopy,” *ACS Nano*, vol. 8, no. 1, pp. 986–993, Jan. 2014.

[160] H. Zhou, J. Zhu, Z. Liu, Z. Yan, X. Fan, J. Lin, G. Wang, Q. Yan, T. Yu, P. M. Ajayan, and J. M. Tour, “High thermal conductivity of suspended few-layer hexagonal boron nitride sheets,” *Nano Res.*, vol. 7, no. 8, pp. 1232–1240, Aug. 2014.

[161] Z. Luo, J. Maassen, Y. Deng, Y. Du, R. P. Garrelts, M. S. Lundstrom, P. D. Ye, and X. Xu, “Anisotropic in-plane thermal conductivity observed in few-layer black phosphorus,” *Nat. Commun.*, vol. 6, p. 8572, Oct. 2015.

[162] J.-U. Lee, D. Yoon, H. Kim, S. W. Lee, and H. Cheong, “Thermal conductivity of suspended pristine graphene measured by Raman spectroscopy,” *Phys. Rev. B*, vol. 83, no. 8, p. 81419, Feb. 2011.

[163] E. Pop, V. Varshney, and A. K. a. K. Roy, “Thermal properties of graphene: Fundamentals and applications,” *MRS Bull.*, vol. 37, no. 12, pp. 1273–1281, 2012.

[164] S. Ghosh, W. Bao, D. L. Nika, S. Subrina, E. P. Pokatilov, C. N. Lau, and A. a Balandin, “Dimensional crossover of thermal transport in few-layer graphene.,” *Nat. Mater.*, vol. 9, no. 7, pp. 555–8, Jul. 2010.

[165] J. Judek, A. P. Gertych, M. Świniarski, A. Łapińska, A. Dużyńska, and M. Zdrojek, “High accuracy determination of the thermal properties of supported 2D materials,” *Sci. Rep.*, vol. 5, p. 12422, 2015.

[166] J. Yang, E. Ziade, C. Maragliano, R. Crowder, X. Wang, M. Stefancich, M. Chiesa, A. K. Swan, and A. J. Schmidt, "Thermal conductance imaging of graphene contacts," *J. Appl. Phys.*, vol. 116, no. 2, p. 23515, Jul. 2014.

[167] M.-H. Bae, Z. Li, Z. Aksamija, P. N. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, and E. Pop, "Ballistic to diffusive crossover of heat flow in graphene ribbons.," *Nat. Commun.*, vol. 4, p. 1734, Jan. 2013.

[168] J. Yang, E. Ziade, C. Maragliano, R. Crowder, X. Wang, M. Stefancich, M. Chiesa, A. K. Swan, and A. J. Schmidt, "Thermal conductance imaging of graphene contacts," *J. Appl. Phys.*, vol. 116, no. 2, pp. 0–9, 2014.

[169] Y. Liu, Z.-Y. Ong, J. Wu, Y. Zhao, K. Watanabe, T. Taniguchi, D. Chi, G. Zhang, J. T. L. Thong, C.-W. Qiu, and K. Hippalgaonkar, "Thermal Conductance of the 2D MoS2/h-BN and graphene/h-BN Interfaces," *Sci. Rep.*, vol. 7, no. February, p. 43886, 2017.

[170] S. Chen, Q. Wu, C. Mishra, J. Kang, H. Zhang, K. Cho, W. Cai, A. a Balandin, and R. S. Ruoff, "Thermal conductivity of isotopically modified graphene.," *Nat. Mater.*, vol. 11, no. 3, pp. 203–7, Mar. 2012.

[171] X. Xu, L. F. C. Pereira, Y. Wang, J. Wu, K. Zhang, X. Zhao, S. Bae, C. Tinh Bui, R. Xie, J. T. L. Thong, B. H. Hong, K. P. Loh, D. Donadio, B. Li, and B. Özyilmaz, "Length-dependent thermal conductivity in suspended single-layer graphene," *Nat. Commun.*, vol. 5, pp. 1–6, Apr. 2014.

[172] W. Cai, A. L. Moore, Y. Zhu, X. Li, S. Chen, L. Shi, and R. S. Ruoff, "Thermal transport in suspended and supported monolayer graphene grown by chemical vapor deposition.," *Nano Lett.*, vol. 10, no. 5, pp. 1645–51, May 2010.

[173] J. Chen, G. Zhang, and B. Li, "Substrate coupling suppresses size dependence of thermal conductivity in supported graphene.," *Nanoscale*, vol. 5, no. 2, pp. 532–6, 2013.

[174] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on SiO2.," *Nat. Nanotechnol.*, vol. 3, no. 4, pp. 206–9, Apr. 2008.

[175] M. M. Sadeghi, M. T. Pettes, and L. Shi, "Thermal transport in graphene," *Solid State Commun.*, vol. 152, no. 15, pp. 1321–1330, Aug. 2012.

[176] K. Khanafer and K. Vafai, "Analysis of the anomalies in graphene thermal properties," *Int. J. Heat Mass Transf.*, vol. 104, pp. 328–336, Jan. 2017.

[177] I. Jo, M. T. Pettes, E. Ou, W. Wu, and L. Shi, “Basal-plane thermal conductivity of few-layer molybdenum disulfide,” *Appl. Phys. Lett.*, vol. 104, no. 20, p. 201902, May 2014.

[178] P. Yuan, C. Li, S. Xu, J. Liu, and X. Wang, “Interfacial thermal conductance between few to tens of layered-MoS2 and c-Si: Effect of MoS2 thickness,” *Acta Mater.*, vol. 122, pp. 152–165, 2017.

[179] Z. Zhang, Y. Xie, Y. Ouyang, and Y. Chen, “A systematic investigation of thermal conductivities of transition metal dichalcogenides,” *Int. J. Heat Mass Transf.*, vol. 108, pp. 1–17, 2016.

[180] I. Jo, M. T. Pettes, J. Kim, K. Watanabe, T. Taniguchi, Z. Yao, and L. Shi, “Thermal conductivity and phonon transport in suspended few-layer hexagonal boron nitride,” *Nano Lett.*, vol. 13, no. 2, pp. 550–554, 2013.

[181] C. Wang, J. Guo, L. Dong, A. Aiyiti, X. Xu, and B. Li, “Superior thermal conductivity in suspended bilayer hexagonal boron nitride,” *Sci. Rep.*, vol. 6, no. 1, p. 25334, Jul. 2016.

[182] H. Jang, J. D. Wood, C. R. Ryder, M. C. Hersam, and D. G. Cahill, “Anisotropic Thermal Conductivity of Exfoliated Black Phosphorus,” *Adv. Mater.*, vol. 27, no. 48, pp. 8017–8022, Dec. 2015.

[183] W.-R. Zhong, W.-H. Huang, X.-R. Deng, and B.-Q. Ai, “Thermal rectification in thickness-asymmetric graphene nanoribbons,” *Appl. Phys. Lett.*, vol. 99, no. 19, p. 193104, Nov. 2011.

[184] D. L. Nika, A. S. Askerov, and A. A. Balandin, “Anomalous Size Dependence of the Thermal Conductivity of Graphene Ribbons,” *Nano Lett.*, vol. 12, no. 6, pp. 3238–3244, Jun. 2012.

[185] J. Y. Kim, J.-H. Lee, and J. C. Grossman, “Thermal Transport in Functionalized Graphene,” *ACS Nano*, vol. 6, no. 10, pp. 9050–9057, Oct. 2012.

[186] J. Wang, L. Zhu, J. Chen, B. Li, and J. T. L. Thong, “Suppressing Thermal Conductivity of Suspended Tri-layer Graphene by Gold Deposition,” *Adv. Mater.*, vol. 25, no. 47, pp. 6884–6888, Dec. 2013.

[187] Q.-X. Pei, Z.-D. Sha, and Y.-W. Zhang, “A theoretical analysis of the thermal conductivity of hydrogenated graphene,” *Carbon N. Y.*, vol. 49, no. 14, pp. 4752–4759, Nov. 2011.

[188] N. Peimyoo, J. Shang, W. Yang, Y. Wang, C. Cong, and T. Yu, “Thermal

conductivity determination of suspended mono- and bilayer WS2 by Raman spectroscopy," *Nano Res.*, vol. 8, no. 4, pp. 1210–1221, Apr. 2015.

[189] C. Chiritescu, D. G. Cahill, N. Nguyen, D. Johnson, A. Bodapati, P. Keblinski, and P. Zschack, "Ultralow Thermal Conductivity in Disordered, Layered WSe2 Crystals," *Science*, vol. 315, no. 5810, pp. 351–353, Jan. 2007.

[190] K. F. Mak, C. H. Lui, and T. F. Heinz, "Measurement of the thermal conductance of the graphene/ SiO2 interface," *Appl. Phys. Lett.*, vol. 97, no. 22, pp. 95–98, 2010.

[191] M. Hu and D. Poulikakos, "Graphene mediated thermal resistance reduction at strongly coupled interfaces," *Int. J. Heat Mass Transf.*, vol. 62, pp. 205–213, Jul. 2013.

[192] M. Freitag, M. Steiner, Y. Martin, V. Perebeinos, Z. Chen, J. C. Tsang, and P. Avouris, "Energy Dissipation in Graphene Field-Effect Transistors," *Nano Lett.*, vol. 9, no. 5, pp. 1883–1888, May 2009.

[193] M. H. Bae, S. Islam, V. E. Dorgan, and E. Pop, "Scaling of high-field transport and localized heating in graphene transistors," *ACS Nano*, vol. 5, no. 10, pp. 7936–7944, 2011.

[194] D. Choi, N. Poudel, S. B. Cronin, and L. Shi, "Effects of basal-plane thermal conductivity and interface thermal conductance on the hot spot temperature in graphene electronic devices," *Appl. Phys. Lett.*, vol. 110, no. 7, p. 73104, 2017.

[195] D. Lembke and A. Kis, "Breakdown of high-performance monolayer MoS2 transistors," *ACS Nano*, vol. 6, no. 11, pp. 10070–10075, 2012.

[196] R. Yang, Z. Wang, and P. X. Feng, "Electrical breakdown of multilayer MoS2 field-effect transistors with thickness-dependent mobility," *Nanoscale*, vol. 6, no. 21, pp. 12383–12390, 2014.

[197] M. Engel, M. Steiner, S.-J. Han, and P. Avouris, "Power Dissipation and Electrical Breakdown in Black Phosphorus," *Nano Lett.*, vol. 15, no. 10, pp. 6785–6788, Oct. 2015.

[198] E. Yalon, C. J. Mcclellan, K. K. H. Smithe, Y. C. Shin, R. Xu, and E. Pop, "Direct observation of power dissipation in monolayer MoS 2 devices," in *2016 74th Annual Device Research Conference (DRC)*, 2016, vol. 16, no. 6, pp. 1–2.

[199] H. Wang, Y. Xu, M. Shimono, Y. Tanaka, and M. Yamazaki, "Computation of Interfacial Thermal Resistance by Phonon Diffuse Mismatch Model," *Mater.*

Trans., vol. 48, no. 9, pp. 2349–2352, 2007.

[200] S. Das, H. Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS2 transistors with scandium contacts," *Nano Lett.*, vol. 13, pp. 100–105, 2013.

[201] A. N. Obraztsov, "Chemical vapour deposition: Making graphene on a large scale.," *Nat. Nanotechnol.*, vol. 4, no. 4, pp. 212–3, Apr. 2009.

[202] Z. Fei, A. S. Rodin, W. Gannett, S. Dai, W. Regan, M. Wagner, M. K. Liu, A. S. McLeod, G. Dominguez, M. Thiemens, A. H. Castro Neto, F. Keilmann, A. Zettl, R. Hillenbrand, M. M. Fogler, and D. N. Basov, "Electronic and plasmonic phenomena at graphene grain boundaries.," *Nat. Nanotechnol.*, vol. 8, no. 11, pp. 821–5, Nov. 2013.

[203] O. V Yazyev and S. G. Louie, "Electronic transport in polycrystalline graphene.," *Nat. Mater.*, vol. 9, no. 10, pp. 806–9, Oct. 2010.

[204] K. Kim, Z. Lee, W. Regan, C. Kisielowski, M. F. Crommie, and A. Zettl, "Grain boundary mapping in polycrystalline graphene.," *ACS Nano*, vol. 5, no. 3, pp. 2142–6, Mar. 2011.

[205] S. Tang and Y. Kulkarni, "The interplay between strain and size effects on the thermal conductance of grain boundaries in graphene," *Appl. Phys. Lett.*, vol. 103, pp. 2011–2015, 2013.

[206] A. Bagri, S. P. Kim, R. S. Ruoff, and V. B. Shenoy, "Thermal transport across twin grain boundaries in polycrystalline graphene from nonequilibrium molecular dynamics simulations," *Nano Lett.*, vol. 11, no. 9, pp. 3917–3921, 2011.

[207] H.-Y. Cao, H. Xiang, and X.-G. Gong, "Unexpected large thermal rectification in asymmetric grain boundary of graphene," *Solid State Commun.*, vol. 152, no. 19, pp. 1807–1810, Oct. 2012.

[208] P. K. Schelling, S. R. Phillpot, and P. Keblinski, "Kapitza conductance and phonon scattering at grain boundaries by simulation," *J. Appl. Phys.*, vol. 95, no. 2004, pp. 6082–6091, 2004.

[209] I. Vlassiouk, S. Smirnov, I. Ivanov, P. F. Fulvio, S. Dai, H. Meyer, M. Chi, D. Hensley, P. Datskos, and N. V Lavrik, "Electrical and thermal conductivity of low temperature CVD graphene: the effect of disorder.," *Nanotechnology*, vol. 22, p. 275716, 2011.

[210] A. C. Ferrari and D. M. Basko, "Raman spectroscopy as a versatile tool for

studying the properties of graphene.," *Nat. Nanotechnol.*, vol. 8, no. 4, pp. 235–46, Apr. 2013.

[211] Z. Shi, R. Yang, L. Zhang, Y. Wang, D. Liu, D. Shi, E. Wang, and G. Zhang, "Patterning graphene with zigzag edges by self-aligned anisotropic etching.," *Adv. Mater.*, vol. 23, no. 27, pp. 3061–5, Jul. 2011.

[212] V. I. Artyukhov, Y. Liu, and B. I. Yakobson, "Equilibrium at the edge and atomistic mechanisms of graphene growth.," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 109, no. 38, pp. 15136–40, Sep. 2012.

[213] G. S. Kumar, G. Prasad, and R. O. Pohl, "Experimental determinations of the Lorenz number," *J. Mater. Sci.*, vol. 28, no. 16, pp. 4261–4272, 1993.

[214] D. G. Cahill, "Thermal conductivity measurement from 30 to 750 K: the 3ω method," *Rev. Sci. Instrum.*, vol. 61, no. 2, p. 802, 1990.

[215] D. G. Cahill, "Erratum: 'Thermal conductivity measurement from 30 to 750 K: The 3ω method' [Rev. Sci. Instrum. 61, 802 (1990)]," *Rev. Sci. Instrum.*, vol. 73, no. 10, p. 3701, 2002.

[216] G. S. Kumar, G. Prasad, and R. O. Pohl, "Experimental determinations of the Lorenz number," *Journal of Materials Science*, vol. 28. pp. 4261–4272, 1993.

[217] D. G. Cahill, K. Goodson, and A. Majumdar, "Thermometry and Thermal Transport in Micro/Nanoscale Solid-State Devices and Structures," *Journal of Heat Transfer*, vol. 124. p. 223, 2002.

[218] a. Sikora, H. Ftouni, J. Richard, C. Hébert, D. Eon, F. Omnès, and O. Bourgeois, "Erratum: 'Highly sensitive thermal conductivity measurements of suspended membranes (SiN and diamond) using a 3ω-Völklein method' [Rev. Sci. Instrum. 83, 054902 (2012)]," *Rev. Sci. Instrum.*, vol. 84, no. 2, p. 29901, 2013.

[219] Z. Aksamija and I. Knezevic, "Lattice thermal transport in large-area polycrystalline graphene," *Phys. Rev. B*, vol. 90, no. 3, p. 35419, Jul. 2014.

[220] B. Qiu and X. Ruan, "Reduction of spectral phonon relaxation times from suspended to supported graphene," *Appl. Phys. Lett.*, vol. 100, no. 19, p. 193101, 2012.

[221] D. Cahill, S. Watson, and R. Pohl, "Lower limit to the thermal conductivity of disordered crystals," *Phys. Rev. B*, vol. 46, no. 10, pp. 6131–6140, Sep. 1992.

[222] A. Behranginia, M. Asadi, C. Liu, P. Yasaei, B. Kumar, P. Phillips, T. Foroozan, J. C. Waranius, K. Kim, J. Abiade, R. F. Klie, L. A. Curtiss, and A. Salehi-Khojin,

"Highly Efficient Hydrogen Evolution Reaction Using Crystalline Layered Three-Dimensional Molybdenum Disulfides Grown on Graphene Film," *Chem. Mater.*, vol. 28, no. 2, pp. 549–555, Jan. 2016.

[223] A. M. van der Zande, P. Y. Huang, D. a Chenet, T. C. Berkelbach, Y. You, G.-H. Lee, T. F. Heinz, D. R. Reichman, D. a Muller, and J. C. Hone, "Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide.," *Nat. Mater.*, vol. 12, pp. 554–61, 2013.

[224] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, and D. Baillargeat, "From bulk to monolayer MoS2: Evolution of Raman scattering," *Adv. Funct. Mater.*, vol. 22, no. 7, pp. 1385–1390, 2012.

[225] L. De Arco and Y. Zhang, "Synthesis, transfer, and devices of single-and few-layer graphene by chemical vapor deposition," *Ieee Trans. Nanotechnol.*, vol. 8, no. 2, pp. 135–138, 2009.

[226] C. J. Glassbrenner and G. A. Slack, "Thermal Conductivity of Silicon and Germanium from 3K to the Melting Point," *Phys. Rev.*, vol. 134, no. 4A, pp. A1058--A1069, May 1964.

[227] E. R. Dobrovinskaya, L. A. Lytvynov, and V. Pishchik, "Properties of Sapphire," in *Sapphire*, Boston, MA: Springer US, 2009, pp. 55–176.

[228] G. C. Correa, C. J. Foss, and Z. Aksamija, "Interface thermal conductance of van der Waals monolayers on amorphous substrates," *Nanotechnology*, vol. 28, no. 13, p. 135402, 2017.

[229] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nat. Nanotechnol.*, vol. 3, no. 8, pp. 491–495, 2008.

[230] E. Pallecchi, C. Benz, a. C. Betz, H. V. Lhneysen, B. Plaais, and R. Danneau, "Graphene microwave transistors on sapphire substrates," *Appl. Phys. Lett.*, vol. 99, no. 11, pp. 199–201, 2011.

[231] Y. Zhang, Y. Zhang, Q. Ji, J. Ju, H. Yuan, J. Shi, T. Gao, D. Ma, M. Liu, Y. Chen, X. Song, H. Y. Hwang, Y. Cui, and Z. Liu, "Controlled Growth of High-Quality Monolayer WS 2 Layers on Sapphire," *ACS Nano*, vol. 7, no. 10, pp. 8963–8971, 2013.

[232] G. R. Stewart, "Measurement of low-temperature specific heat," *Rev. Sci. Instrum.*, vol. 54, no. 1, pp. 1–11, Jan. 1983.

[233] D. R. Lide, Ed., *CRC Handbook of Chemistry and Physics*, 84th ed. Boca Raton,

Florida: CRC Press, 2003.

[234] G. S. Kumar, G. Prasad, and R. O. Pohl, “Experimental determinations of the Lorenz number,” *J. Mater. Sci.*, vol. 28, no. 16, pp. 4261–4272, 1993.

[235] B. Amorim and F. Guinea, “Flexural mode of graphene on a substrate,” *Phys. Rev. B*, vol. 88, no. 11, p. 115418, Sep. 2013.

[236] M. Kettner, P. Biebersmith, N. Roldan, and B. K. Sharma, “Aluminum Nitride Vs. Beryllium Oxide for High Power Resistor Products.(Technical Feature),” *Microw. J.*, vol. 44, no. 11, pp. 104–111, 2001.

[237] D. V Matthew, “ADVANCED MATERIALS AND POWDERS HANDBOOK. ALUMINIUM NITRIDE(AIN),” *Am. Ceram. Soc. Bull.*, vol. 78, no. 6, pp. 69–71, 1999.

[238] J. W. Vandersande, *Properties and Growth of Diamond*. London: INSPEC, the Institution of Electrical Engineers, 1994.

[239] J. Krumhansl and H. Brooks, “The Lattice Vibration Specific Heat of Graphite,” *J. Chem. Phys.*, vol. 21, no. 10, p. 1663, 1953.

[240] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, “Alternative dielectrics to silicon dioxide for memory and logic devices,” *Nature*, vol. 406, no. 6799, pp. 1032–1038, 2000.

[241] E. M. Vogel, “Electrical Characterization of Defects in High-k Gate Dielectrics,” in *2005 International Semiconductor Device Research Symposium*, 2009, pp. 209–210.

[242] H. C. Lin, P. D. Ye, and G. D. Wilk, “Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al2O3 on GaAs,” *Appl. Phys. Lett.*, vol. 87, no. 18, p. 182904, Oct. 2005.

[243] G. A. Slack, R. A. Tanzilli, R. O. Pohl, and J. W. Vandersande, “The intrinsic thermal conductivity of AIN,” *J. Phys. Chem. Solids*, vol. 48, no. 7, pp. 641–647, 1987.

[244] S. M. Lee, D. G. Cahill, and T. H. Allen, “Thermal conductivity of sputtered oxide films,” *Phys. Rev. B*, vol. 52, no. 1, pp. 253–257, 1995.

[245] G. E. Moore, “Progress in digital integrated electronics [Technical literaiture, Copyright 1975 IEEE. Reprinted, with permission. Technical Digest. International Electron Devices Meeting, IEEE, 1975, pp. 11-13.],” *Solid-State Circuits Soc. Newsletter, IEEE*, vol. 20, no. 3, pp. 36–37, 2006.

[246] Y. Zhan, Z. Liu, S. Najmaei, P. M. Ajayan, and J. Lou, “Large-area vapor-phase growth and characterization of MoS 2 atomic layers on a SiO 2 substrate,” *Small*, vol. 8, no. 7, pp. 966–971, 2012.

[247] R. Ganatra and Q. Zhang, “Few-layer MoS2: A promising layered semiconductor,” *ACS Nano*, vol. 8, no. 5, pp. 4074–4099, 2014.

[248] B. Radisavljevic, a Radenovic, J. Brivio, V. Giacometti, and a Kis, “Single-layer MoS2 transistors.,” *Nat. Nanotechnol.*, vol. 6, pp. 147–150, 2011.

[249] Q. Yu, L. a Jauregui, W. Wu, R. Colby, J. Tian, Z. Su, H. Cao, Z. Liu, D. Pandey, D. Wei, T. F. Chung, P. Peng, N. P. Guisinger, E. a Stach, J. Bao, S.-S. Pei, and Y. P. Chen, “Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition.,” *Nat. Mater.*, vol. 10, no. 6, pp. 443–449, 2011.

[250] A. Behranginia, M. Asadi, C. Liu, P. Yasaei, B. Kumar, P. Phillips, T. Foroozan, J. C. Waranius, K. Kim, J. Abiade, R. F. Klie, L. a. Curtiss, and A. Salehi-Khojin, “Highly Efficient Hydrogen Evolution Reaction Using Crystalline Layered Three-Dimensional Molybdenum Disulfides Grown on Graphene Film,” *Chem. Mater.*, vol. 28, no. 2, pp. 549–555, 2016.

[251] S. Jin-Hong Park, S. Lee, J. Jeon, S. Kyu Jang, S. Min Jeon, G. Yoo, Y. Hee Jang, and J.-H. Park, “Layer-controlled CVD growth of large-area two-dimensional MoS 2 fi lms As featured in: Layer-controlled CVD growth of large-area two-dimensional MoS 2 films,” *Nanoscale*, vol. 7, no. 5, pp. 1688–1695, 2015.

[252] H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, and P. D. Ye, “Statistical Study of Deep Sub-Micron Dual-Gated Field-Effect Transistors on Monolayer CVD Molybdenum Disulfide Films.,” *Nano Lett.*, vol. 13, pp. 2640–6, 2013.

[253] J. R. Chen, P. M. Odenthal, A. G. Swartz, G. C. Floyd, H. Wen, K. Y. Luo, and R. K. Kawakami, “Control of Schottky barriers in single layer MoS2 transistors with ferromagnetic contacts,” *Nano Lett.*, vol. 13, pp. 3106–3110, 2013.

[254] E. Kaxiras, J. Kong, and H. Wang, “Graphene/MoS 2 Hybrid Technology for Large-Scale Two- Dimensional Electronics,” *Nano Lett.*, vol. 14, no. Cvd, pp. 3055–3063, 2014.

[255] L. Brown, E. B. Lochocki, J. Avila, C.-J. Kim, Y. Ogawa, R. W. Havener, D.-K. Kim, E. J. Monkman, D. E. Shai, H. I. Wei, M. P. Levendorf, M. Asensio, K. M. Shen, and J. Park, “Polycrystalline Graphene with Single Crystalline Electronic Structure,” *Nano Lett.*, vol. 14, no. 10, pp. 5706–5711, Oct. 2014.

[256] Z. Yan, G. Liu, J. M. Khan, and A. A. Balandin, “Graphene quilts for thermal management of high-power GaN transistors,” *Nat. Commun.*, vol. 3, p. 827, May 2012.

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Summary

- 5 years of research experience in synthesis, characterization, nanofabrication, experimentation, and analysis in systems based on Nano- and 2D-materials
- 14 journal publications including two in ***Nano Letters***, one in ***Advanced Materials***, one in ***Nature Communications***, two in ***ACS Nano***, and one in ***Science*** (>500 citations – Google Scholar)
- Recipient of several awards including ***Materials Research Society (MRS)*** **Graduate Student Silver Award**
- More than 400 research highlights in the news including **Department of Energy (DOE)** front page, **National Science Foundation (NSF)**, ScienceDaily, NanoWerk, ChemEurope, Phys.org, etc.
- Contributed to the development of a **$2M awarded NSF proposal** "EFRI 2DARE: Thermal Transport in 2D Materials for Next Generation Nanoelectronics- from Fundamentals to Devices" and few submitted proposals
- Teaching and mentoring experience as laboratory instructor, teaching assistant, and research trainer

Education

- **Ph.D.**, University of Illinois at Chicago (UIC), Mechanical Engineering, 2015- 2017 (GPA: 4/4)
- **M.Sc.,** University of Illinois at Chicago (UIC), Mechanical Engineering, 2012- 2015 (GPA: 4/4)
- **B.Sc.,** Sharif University of Technology (SUT), Mechanical Engineering, 2008- 2012 (GPA: 17.11/20)

Awards and Honors

- **Graduate Student Silver Award** for the 2015 **Materials Research Society (MRS)** Fall Meeting ($200)
- **Dean's Scholar Fellowship** for the 2016-2017 Academic Year at UIC ($54,142)
- **Faydor Litvin Graduate Award** for the 2016-2017 Academic Year at UIC ($1500)
- **Chicago Consular Corps Scholarship** for the 2015-2016 Academic Year ($1000)
- **Provost's Graduate Research Award** at UIC for the 2015-2016 Academic Year ($2500)

Skills

Nano-fabrication and characterization techniques:

- EBL, contact aligner and direct-write (mask-less) lithography,
- CVD, ALD, PECVD, PVD (evaporation and sputtering), Plasma etching, Wet etching and processing
- AFM, SEM, Raman spectroscopy, PL, XPS, EDS, EBSD, UV-vis-NIR spectroscopy, DLS, Profilometry
- Sonication, centrifugation, filtration, film processing

Experimental techniques:

- Wire bonding and packaging, Electrical characterization, Impedance spectroscopy (IS)
- Electrical thermometry at nanoscale, Design of thermometry platforms, Uncertainty analyses
- Electrochemical characterization: EIS, Cyclic voltammetry, Gas chromatography
- Dynamic and static chemical sensing in nanoscale devices, Device calibration

Software: AutoCAD, Matlab, Solidworks, MechSoft **Languages:** English (Proficient), Farsi (Native)

Patents and Publications

Filed Patent Applications

1. A. Salehi-Khojin, **P. Yasaei**, B. Kumar, "Graphene Based Chemical Sensing Devices and Methods for Chemical Sensing" U.S. Provisional Patent Application serial no. 62/018,006, 2014
2. A. Salehi-Khojin, **P. Yasaei**, F. Khalili-Araghi, "Stable and Selective Humidity Detection Using Randomly Stacked Black Phosphorus Flakes" U.S. Provisional Patent Application serial no. 62/203,440, 2015
3. A. Salehi-khojin, A. Behraginia, M. Asadi, **P. Yasaei**, "Three Dimensional Structured Transition Metal Dichalcogenides for Electrochemical Reactions" U.S. Provisional PCT/US16/55939, 2016.

4. A. Salehi-Khojin, M. Asadi, A. Monticelli, B. Kumar, **P. Yasaei**, "Artificial Leaves for Solar Energy Storage" Patent disclosure no. DH167, 2014.

Published/Submitted Journal Articles

1. **P. Yasaei**, A. Fathizadeh, R. Hantehzadeh, A. K. Majee, A. El-Ghandour, D. Estrada, C. Foster, Z. Aksamija, F. Khalili-Araghi, and A. Salehi-Khojin, "Bimodal Phonon Scattering in Graphene Grain Boundaries" ***Nano Letters***, 2015 (Link)
2. **P. Yasaei,** C. J. Foss, K. Karis, A. Behranginia, A. El-Ghandour, A. Fathizadeh, A. K. Majee, C. Foster, F. Khalili-Araghi, Z. Aksamija, A. Salehi-Khojin, "Interfacial Thermal Transport in Monolayer Graphene- and MoS_2-Based Devices" ***Advanced Materials Interfaces***, 2017 (Link)
3. **P. Yasaei,** A. Behranginia, Z. Hemmat, A. El-Ghandour, C. Foster, A. Salehi-Khojin, "Quantifying the Limits of Through-Plane Thermal Dissipation in 2D-Material-Based Systems" ***2D Materials***, 2017 (Link)
4. **P. Yasaei**, B. Kumar, T. Foroozan, C. Wang, M. Asadi, D. Tuschel, J. E. Indacochea, R. F. Klie, and A. Salehi-khojin, "High-Quality Black Phosphorus Atomic Layers by Liquid-Phase Exfoliation" ***Advanced Materials***, 2015 (Link)
5. **P. Yasaei,** A. Behranginia, T. Foroozan, M. Asadi, K. Kim, F. Khalili-Araghi, A. Salehi-Khojin, "Stable and Selective Humidity Sensing Using Stacked Black Phosphorus Flakes" ***ACS Nano***, 2015 (Link)
6. **P. Yasaei,** B. Kumar, R. Hantehzadeh, M. Kayyalha, A. Baskin, N. Repnin, C. Wang, R. F. Klie, Y. P. Chen, P. Král, and A. Salehi-Khojin, "Chemical sensing with switchable transport channels in graphene grain boundaries" ***Nature Communications***, 2014 (Link)
7. A. Behranginia, **P. Yasaei**, A. K. Majee, V. K. Sangwan, F. Long, C. Foss, T. Foroozan, S. Fuladi, M. Hantehzadeh, R. Shahbazian-Yasar, M. C. Hersam, Z. Aksamija, A. Salehi-Khojin, "Direct Growth of High Mobility and Low Noise Lateral MoS_2 -Graphene Heterostructure Electronics" ***Small,*** 2017 (Link)
8. M. Asadi, K. Kim, C. Liu, A. V. Addepalli, P. Abbasi, **P. Yasaei**, P. Phillips, A. Behranginia, J. M. Cerrato, R. Haasch, P. Zapol, B. Kumar, R. F. Klie, J. Abiade, L. A. Curtiss, A. Salehi-Khojin, "Nanostructured Transition Metal Dichalcogenide Electrocatalysts for CO_2 Reduction in Ionic Liquid" ***Science***, 2016 (Link)
9. F. Long, **P. Yasaei**, S. Sanoj, W. Yao, P. Král, A. Salehi-Khojin, R. Shahbazian-Yassar, "Characteristic Work Function Variations of Graphene Line Defects" ***ACS Applied Materials & Interfaces***, 2016
10. A. Nie, Y. Cheng, S. Ning, T. Foroozan, **P. Yasaei**, W. Li, B. Song, Y. Yuan, L. Chen, A. Salehi-Khojin, F. Mashayek, R. Shahbazian-Yassar,"Selective Ionic Transport Pathways in Phosphorene" ***Nano Letters***, 2016
11. A. Behranginia, M. Asadi, C. Liu, **P. Yasaei**, B. Kumar, P. Phillips, T. Foroozan, J. C. Waranius, K. Kim, J. Abiade, R. F. Klie, L. A. Curtiss, A. Salehi-Khojin, "Highly Efficient Hydrogen Evolution Reaction Using Crystalline Layered Three Dimensional Molybdenum Disulfides Grown On Graphene Film" ***Chemistry of Materials,*** 2015
12. M. Asadi, B. Kumar, C. Liu, P. Phillips, **P. Yasaei**, A. Behranginia, P. Zapol, R. F. Klie, L. A. Curtiss, A. Salehi-Khojin, "A Cathode based on Molybdenum Disulfide Nanoflakes for Lithium–Oxygen Batteries" ***ACS Nano***, 2015
13. B. Kumar, K. Min, M. Bashirzadeh, A. B. Farimani, M.-H. Bae, D. Estrada, Y. D. Kim, **P. Yasaei**, Y. D. Park, E. Pop, N. R. Aluru, and A. Salehi-Khojin, "The role of external defects in chemical sensing of graphene field-effect transistors" ***Nano Letters***, 2013
14. F. Long, **P. Yasaei**, W. Yao, A. Salehi-Khojin, R. Shahbazian-Yassar, "Anisotropic Friction of Wrinkled Graphene Grown by Chemical Vapor Deposition" ***ACS Applied Materials & Interfaces***, 2017
15. K. Kim, M. Asadi, P. Abbasi, A. V. Addepalli, **P. Yasaei**, B. Sayahpour, A. Salehi-Khojin "Electrochemical Artificial Leaf for Carbon Dioxide Conversion to Energy-Rich Chemicals" ***Advanced Energy Materials,*** 2017 (Minor revisions requested)
16. B. Sayahpour, P. Abbasi, M. Asadi, C. Liu, J. Jokisaari, K. Karis, A. Ngo, K. C. Lau, B. Narayanan, P. Yasaei, M. Gerard, A. Mukherjee, X. Hu, F. Khalili-Araghi, R. Klie, L. A. Curtiss, A. Salehi-Khojin "Long Life Lithium-Air Battery Operating in a Realistic Atmosphere", ***Nature***, 2017 (Revisions requested)
17. X. Hu, **P. Yasaei**, J. R. Jokisaari, S. Ögüt, A Salehi-khojin, R. Klie "Mapping Thermal Expansion Coefficients in Free-Standing 2D Materials at the Nanometer Scale" ***PRL***, 2017 (Under review)

Books

1. **P. Yasaei**, M. Eslami, "Fundamentals of Thermodynamics: Comprehensive Test Book for the Graduate-Level Entrance Exam of Iran Universities" ***Mahan Higher Education Institute****, 2011*, ISBN: 978-964-164-493-4

Conference Proceedings

1. **P. Yasaei**, A. Behranginia, A. El-Ghandour, C. D. Foster, A. Salehi-Khojin "Roles of Interface and Substrate Properties on Through-Plane Heat Dissipation in 2D-Material-Based Devices" ***MRS*** Spring Meeting, Phoenix, AZ, 2017
2. X. Hu**, P. Yasaei,** J. Jokissari, A. Salehi-Khojin, R. Klie "Nanoscale Thermometer for Different 2D Materials" ***MRS*** Spring Meeting, Phoenix, AZ, 2017
3. A. Behranginia**, P. Yasaei,** F. Long, R. Shahbazian-Yassar, A. Salehi-Khojin "MoS_2/Graphene In-Plane Heterostructure—Synthesize, Electronic Properties and Interface Characteristics" ***MRS*** Spring Meeting, Phoenix, AZ, 2017
4. **P. Yasaei**, A. Fathizadeh, R. Hantehzadeh, A. K. Majee, A. El-Ghandour, D. Estrada, C. Foster, Z. Aksamija, F. Khalili-Araghi, and A. Salehi-Khojin "Thermal Transport across Individual Graphene Grain Boundaries" ***MRS*** Fall Meeting, Boston, MA, 2015
5. **P. Yasaei**, B. Kumar, T. Foroozan, M. Asadi, A. Salehi-Khojin "Large-scale production of Black Phosphorus Atomic Layers by Liquid Phase Exfoliation" ***MRS*** Spring Meeting, San Francisco, CA, 2015
6. **P. Yasaei**, B. Kumar, A. Baskin, N. Repnin, P. Král, A. Salehi-Khojin "Molecular Sensing at Graphene Grain Boundaries" ***AIChE*** Annual Meeting, Atlanta, GA, USA, 2014
7. **P. Yasaei**, B. Kumar, A. Baskin, N. Repnin, P. Král, A. Salehi-Khojin "Chemical Sensing at Graphene Grain Boundaries" ***NSS-8***, Chicago, IL, 2014
8. M. Purahmad, J. Huang, M. Plakhotnyuk, X. Zhang, J. Lee, A. Behranginia, **P. Yasaei**, T. Durowade, K. Spratt, M. Silvestri, M. Gouk, X. Cui, S. Chang, K. Maamari, M. Mathur, A. Solat, H. Tahiru, N. Krzyzanowski, A. Meyer, J. Counts, E. Tsang, N. Strach, I. Mohedano, M. Valencia, A. Raghunathan, T. Dankovic, A. Feinerman, H. Busta "A MEMS-based resistive vacuum gauge with voltage readout" *26th **IVNC***, Roanoke, Va, 2013

Research Highlights

_ *"Graphene heat-transfer riddle unraveled"* Highlighted in **ScienceDaily**, **Phys.org**, **ChemEurope**, **NanoWerk**, etc.

_ *"Graphene flaws key to creating hypersensitive electronic nose"* Highlighted in National Science Foundation (**NSF**), Department of Energy **(DOE) front page**, DOE Twitter account, **ScienceDaily**, **NanoWerk**, etc.

_ *"Engineers fine-tune the sensitivity of nano-chemical sensor"* Highlighted in **ScienceDaily**, **NanoWerk**, Science Codex, **Science Newsline**, **Phys.org**, **AZO Nano**, etc.

Technical Experience

- **Research assistant,** *"Nanomaterials and Energy Systems Lab"* Aug. 2012- Present
- **Reviewing board member**, Applied Physics Letter, Scientific Reports, Light: Science and Applications
- **Teaching assistant & lab supervisor,** *"Introduction to Heat Transfer"* UIC, 4 semesters
- **Teaching assistant,** *"Introduction to Thermodynamics"* UIC, 2 semesters
- **Teaching assistant,** *"Automatic Control"* and *"Applied Electronics"* SUT, 1 semester each
- **Project Engineer**, *"Design and Fabrication of a four-passenger gasoline-electric hybrid car for University of Tehran's Omid team",* in 3rd Iranian Machine Design Competition, Aug. 2011, SUT

Associations

- Member of Mechanical and Industrial Engineering (MIE) Graduate Students Council (GSC), UIC
- Member of professional communities: ASME, MRS, AIChE