High-Frequency Link Power Electronics Interface for Discrete Power and Data Transfer

BY

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THESIS

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Dedicated to my family

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AG

PREFACE

This dissertation is an original intellectual product of the author, A. Gupta. All the work presented here was conducted in the Laboratory for Energy and Switching-Electronics Systems (LESES) at the University of Illinois at Chicago.

The results of our research have been previously published as journal, conference, and workshop articles in:

- IEEE Transactions on Industrial Electronics (Gupta et al., 2018)
- IEEE Transactions on Industrial Informatics (Gupta and Mazumder, 2018)
- IEEE Transactions on Power Electronics (Kulkarni et al., 2018)
- IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA'18) (Gupta et al., 2018)
- IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA'17) (Gupta et al., 2017)
- IEEE Energy Conversion Congress and Exposition (ECCE'15) (Gupta et al., 2015)

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Ankit Gupta

March 7, 2019

CONTRIBUTION OF AUTHORS

Major parts of the results and discussions in this thesis are taken from my published or submitted papers with written permission from the journals (see Appendix A). Below, the contributions of all the co-authors are listed:

Authors' contributions in IEEE Transactions on Industrial Electronics, ECCE'15: A. Gupta, N. Kumar, and S. K. Mazumder conceived the main ideas and led the investigations. A. Gupta undertook the simulations and experimental study. N. Kumar contributed to the analytical analysis. A. Gupta, N. Kumar, and S. k. Mazumder contributed to the write-up of the manuscripts.

Authors' contributions in IEEE Transactions on Industrial Informatics, WiPDA'17, and WiPDA'18: A. Gupta, and S. K. Mazumder conceived the main idea and led the investigation. A. Gupta undertook the circuit design and performed the experimental analysis. A. Gupta and S. k Mazumder contributed to the review and write-up of the manuscript.

Authors' contributions in IEEE Transactions on Power Electronics: A. Kulkarni, A. Gupta, and S. K. Mazumder conceived the main idea and led the investigation. Analysis and experiments about issues with low-frequency harmonics in a grid-connected inverter were done by A. Kulkarni. A. Gupta undertook the study of high-frequency harmonics and designed a GaN-based 500 W grid connected DMCI. A. Kulkarni, A. Gupta, and S. K. Mazumder contributed to the review and write-up of the manuscript.

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LIST OF ABBREVIATIONS

ASK	Amplitude Shift Keying
CMOS	Complementary Metal–Oxide–Semiconductor
DER	Distributed Energy Resources
DMCI	Differential Mode Ćuk Inverter
DMS	Discontinuous Modulation Scheme
DPS	Distributed Power System
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EMS	Energy Management System
ePWM	Enhanced Pulse Width Modulator
FET	Field Effect Transistor
FSK	Frequency Shift Keying
GaN	Gallium Nitride
HF	High Frequency
HFDPS	High-Frequency Distributed Power System
HFDT	High-Frequency Data Transfer
LPES	Load-end Power Electronics System
LF	Low Frequency
LFPT	Low-Frequency Power Transfer
MAC	Media Access Control
NRZ	Non-Return-to-Zero
OEEN	Open-Electric-Energy-Network
EER	Electric Energy Routers

LIST OF ABBREVIATIONS (Continued)

OFDM	Orthogonal Frequency-Division Multiplexing
PCB	Plastic Circuit Board
PES	Power Electronics System
PLC	Power Line Communication
POE	Power Over Ethernet
PWM	Pulse Width Modulation
RF	Radio Frequency
Rx	Receiver
SCADA	Supervisory Control and Data Acquisition
SCI	Serial Communications Interface
SISO	Single-Input-Single-Output
SIMO	Single-Input-Multi-Output
SPDT	Single-Pole, Double-Throw
SPES	Source-end Power Electronics System
TCS	Transient Current Suppressor
TDM	Time Division Multiplexing
TVS	Transient Voltage Suppressor
Tx	Transmitter
WBG	Wide-bandgap

SUMMARY

In this dissertation, an approach for sequential transmission of high-frequency (HF) power and data signals over a common HF channel (i.e., co-transmission) is outlined. The proposed method is in contrast to conventional power-line communication (PLC), where the power and data co-transmission is simultaneous. Sequential co-transmission avoids data corruption by temporally distributing power and data signals over an HF channel and limiting their overlap. In this dissertation, a communication data-transfer architecture mechanism required to realize the sequential co-transfer approach has been outlined. Simple transmitter and receiver circuits, synthesized without the use of any analog-filtering circuitry, are designed, and an asynchronous serial-communication-interface (SCI) protocol is implemented. The sequential HF power and data co-transmission is experimentally achieved and validated on a single-input-single-output (SISO) and a single-input-multi-output (SIMO) power electronics system. Various applications encompassing packetized power delivery empowered by the sequential co-transfer scheme are envisioned and experimentally verified. Additionally, an in-depth analysis of GaN-based power electronics system required for generating the HF power signals is undertaken, and specific design guidelines for reducing HF noise in the circuit are discussed.

Chapter 1

Introduction

Parts of this chapter, including figures and text, are based on my following papers:

- A. Gupta, N. Kumar, and S. K. Mazumder, "Frequency-dependent criterion for mitigation of transmission-line effects in a high-frequency distributed power system," in *2015 IEEE Energy Conversion Congress and Exposition*, ECCE 2015, 2015, pp. 4624–4631.
- A. Gupta and S. K. Mazumder, "Sequential Co-transmission of High-Frequency Power and Data Signals," in *IEEE Transactions on Industrial Informatics*, vol. 14, no. 10, pp. 4440–4445, 2018.
- A. Gupta, N. Kumar, and S. K. Mazumder, "Generalized Input Impedance Modeling of TL-Network-Based HFDPS for Validating Frequency-Dependent Criteria for Power-Signal Integrity," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 5, pp. 4114–4124, May 2018.

A. Background

Distributed power systems (DPSs) can be considered as a combination of distributed energy resources (DER) and distributed energy storage that are used for feeding power to load centers. They can range in size from as few as a couple of nodes to a system with a large number of distributed nodes. They have an ability to work off-grid and integrate communication network for information exchange. Which results in improved system efficiency, higher reliability, environmental benefits, harnessing untapped energy resources and enhanced system security. This has led to their increased interest in various flexible applications ranging from VLSI, smart buildings, electric vehicles to a tethered network of drones, etc., as are shown in Figure 1 [1]–[4]. However, these applications are coupled with an increase in size and complexity of DPSs and have resulted in a growing need for developing smart means of resource allocation and power delivery. For instance, as predicted by Moore's law, the number of transistors on an integrated circuit chip is on the rise, and so are their power requirements [5]. The existing power supplies and power distribution architecture might not be able to follow this rising trend. Thus, in this dissertation, a new scheme for transferring discrete power and data packets in a DPS is proposed.

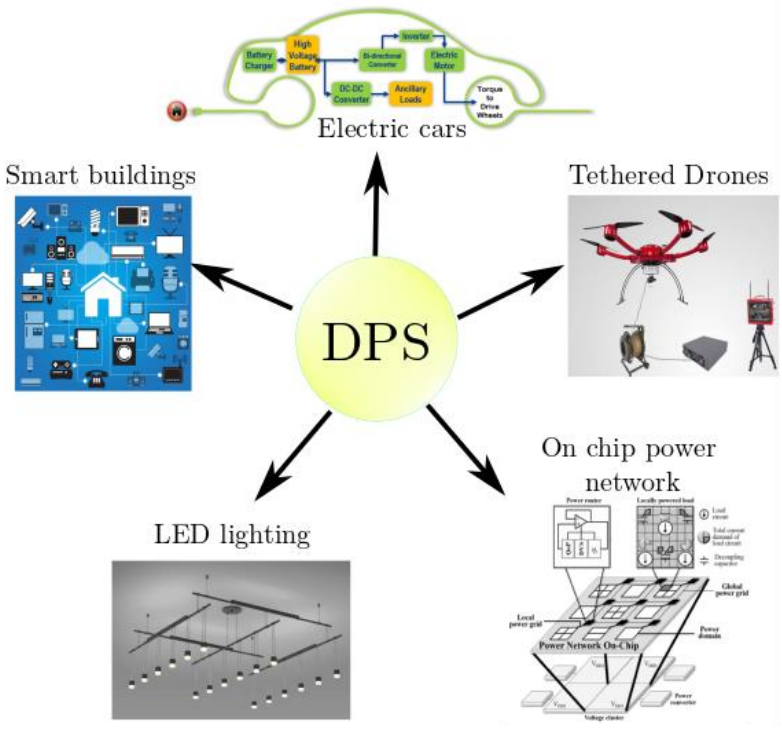


Figure 1. Various type of distributed power systems (DPS's).

As will be discussed in the later sections, transferring power and data in discrete packets can address the manifold requirements of the DPS in the following ways,

- A higher number of loads can be managed (increase network utilization)
- Size of the energy storage can be reduced (high-speed power delivery)
- The efficiency of the DPS can be increased (reduce standby power consumption)
- Power can be delivered based on load demand (integration of information and power delivery)

B. Overview of Distributed Power Systems

Distributed power systems (DPSs) have gained widespread acceptance over the conventional power system in several flexible applications owing to its modularity, flexibility, scalability, resilience and reliable operation [6], [7]. Figure 2 illustrates various DPS mechanisms available for transferring power from the distributed energy resources (DERs) to the load(s). As outlined in Figure 2, a DPS usually comprises three functional stages. First, the energy from DER (mostly dc) is converted to slow-scale ac/dc or HF ac using source end power-electronics system (SPES). The second stage comprises of an ac/dc transmission link, which is used to transmit the power to the load(s) and also serves as an energy buffer due to the continuous availability of power. The final stage culminates in the application load(s) typically interfaced with a set of preceding power-electronics system (PES)-based active front-end(s), load end power-electronics system (LPES). However, unlike the conventional low-frequency ac or dc DPS's shown in Figure 2 (a) and Figure 2 (b), HF DPS (HFDPS) shown in Figure 2 (c) and Figure 2 (d) uses a HF link for power transmission and provides significant advantages over the latter with regard to system compactness, design simplicity, dynamic performance, lower cost, and enhanced system efficiency and reliability [8]–[12]. Because of the advantages as mentioned above, HFDPS architectures have been widely studied, and some of the proposed designs for space, telecommunication, automotive and microgrid applications are captured in Figure 3.

Although, all the DPS mechanisms outlined in Figure 2 follow the same basic structure; they mostly differ in their power delivery methodology. While, low-frequency ac, dc, and HFDPS as shown in Figure 2 (a) - Figure 2 (c) transmit continuous power, discrete HFDPS is shown in Figure 2 (d) can incorporate discontinuous power flow. This is because, unlike in the conventional HFDPS, in a discrete HFDPS modulation scheme can be discontinuous and guided

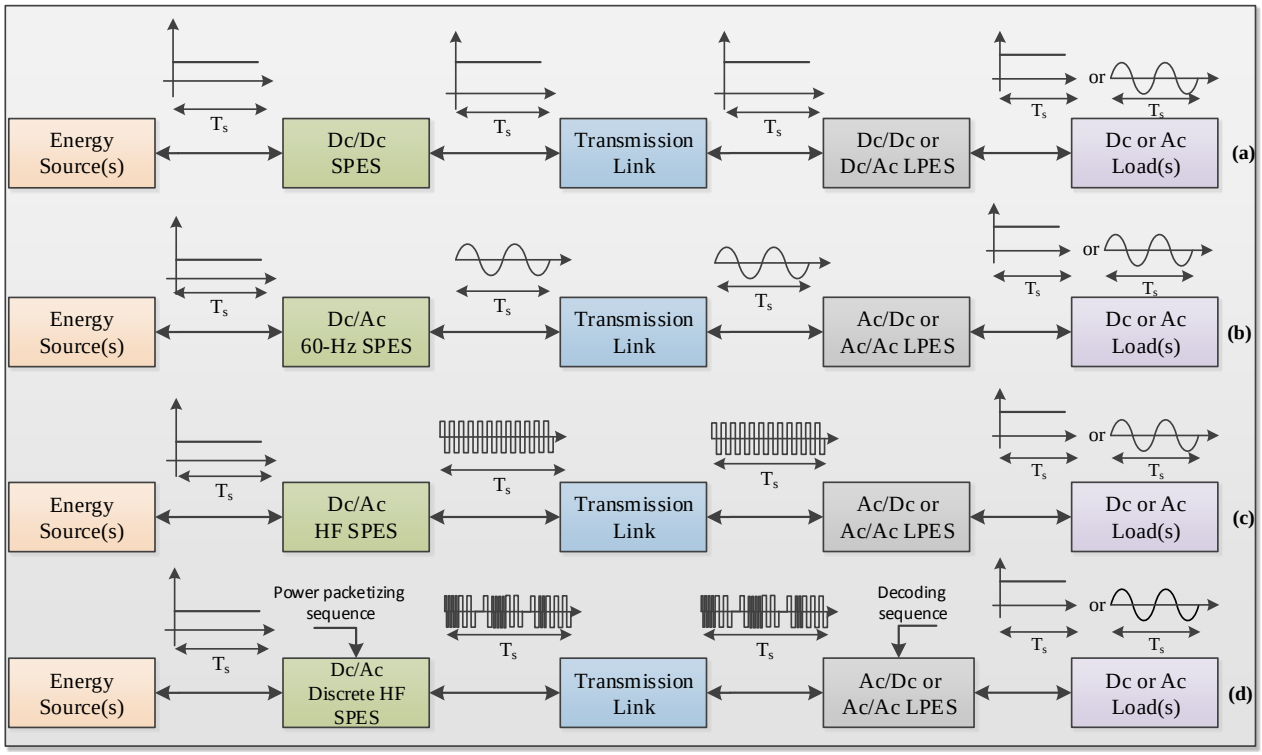


Figure 2. Illustration of (a) dc, (b) low-frequency ac, (c) HFDPS and (d) discrete HF DPSs architectures. The difference between (a), (b), (c) and (d) pertains to how the power signals are transmitted. (d) Can incorporate discontinuous power transfer whereas the rest incorporates continuous power transfer [11]**, ©2015 IEEE.**

by network protocols which are dynamically determined based on existing load/source demand and dynamic priority assigned to each load/source by the energy management system (EMS) [13]. One of the critical advantages of incorporating a discrete HFDPS over the conventional HFDPS is that, in a discrete HFDPS, the utilization of the network can be optimized by addressing a higher number of loads/sources proficiently in an event-driven fashion guided by the dynamic-priority assigned to each load/source through the EMS [14]. The assigned dynamic priority can be based on the severity, amount and frequentness of the power required by the load. Additionally, a discrete HFDPS can also be used for shaping individual discrete HF power packets based on load requirement to reduce switching requirement at the LPES and enhance system efficiency. Moreover, by transferring power in discrete HF power packets, HFDPS can support a wide variety of sources and loads and thus can result in increased network utilization. Benefits of such a discrete HFDPS are realizable in applications ranging from nanogrids, picogrids, smart-buildings, electric vehicles, and telecommunication and are also extendable to micro and macrogrids.

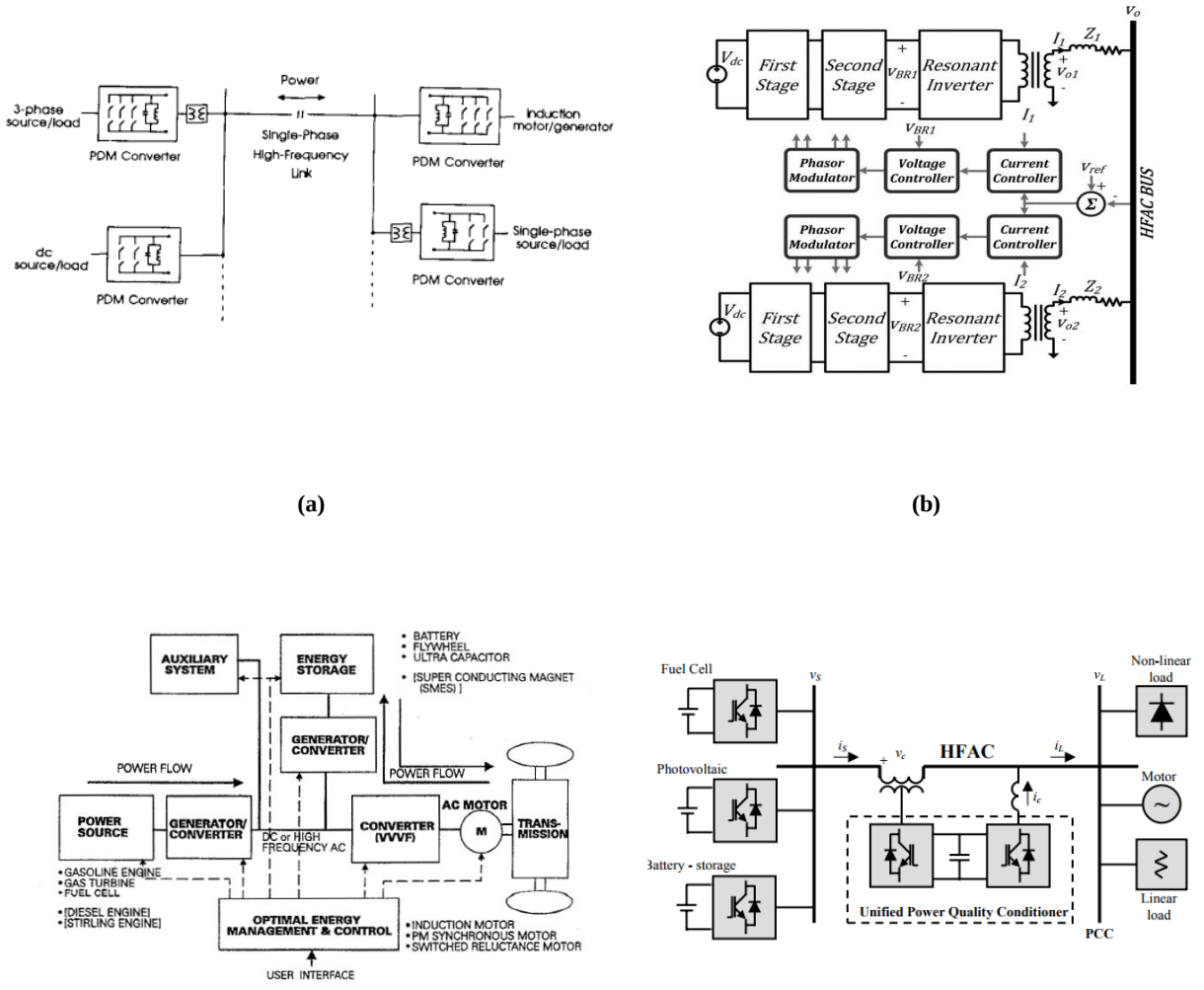


Figure 3. HFDPS architectures proposed in literature for (a) space station [15] **©1988 IEEE, (b) telecommunication applications** [8] **©2014 IEEE, (c) automotive application** [16] **©1996 IEEE, and (d) microgrid** [17] **©2003 IEEE.**

C. Overview of Communication Networks in an HFDPS

To realize the full potential of an HFDPS, a fast, reliable, and secure communication network is required to work alongside the HF power transfer network. Such a communication network can be used for implementing advanced network control algorithms by exchanging status information, control commands and sensor feedback between various

PES located in the network. The present communication architecture used in the conventional power system is limited to small pockets and is mainly used for basic monitoring and surveillance tasks. Communication schemes like power line communication (PLC) and supervisory control and data acquisition (SCADA) systems, prevalent in the conventional power system, handle low data rate and use protocols designed to operate with large data overheads. Hence, they might not be capable of catering to the communication demands of an HFDPS. Typically, an HFDPS comprises of a wide variety of PESs located far from each other and connected through an HF transmission link. Thus, they will require a communication network capable of handling a high volume of real-time bi-directional data transfer between many PESs connecting various DERs to loads.

As per the above discussion, power and data network can be identified as the two main building blocks of an HFPDS. While the role of HF power network is to provide a mechanism for fast and reliable power delivery, a high-speed communication network provides flexibility and enable intelligent management of the available resources. In the past, a lot of work has been done in designing data networks that can assist in HF power delivery. They can majorly be subdivided into two categories, wireless and wire-based communication network.

1. Wireless Communication Network

In a wireless communication network for an HFDPS, data is commonly transferred through a radio-frequency (RF) medium, while the power is transferred simultaneously using power transmission lines [18]–[21] or wirelessly through inductive or capacitive links [22], [23]. Wireless communication provides both flexibilities in terms of location of the data transmitter and receiver units and cost saving in deployment and maintenance. Sensors with wireless transceivers are low on maintenance and can function for an extended period using internal battery storage in harsh environments. Furthermore, wireless communication remains unaffected in case of faults on the power transmission line and serves as an excellent candidate for communication under such circumstances.

Advantages of employing wireless communication network in an HF distributed power converter have widely been explored. In [18], control of a parallel dc/dc buck converter has been demonstrated under transient and steady-state conditions using an RF-based communication network at a distance of 15 ft. As is shown in Figure 4, PWM

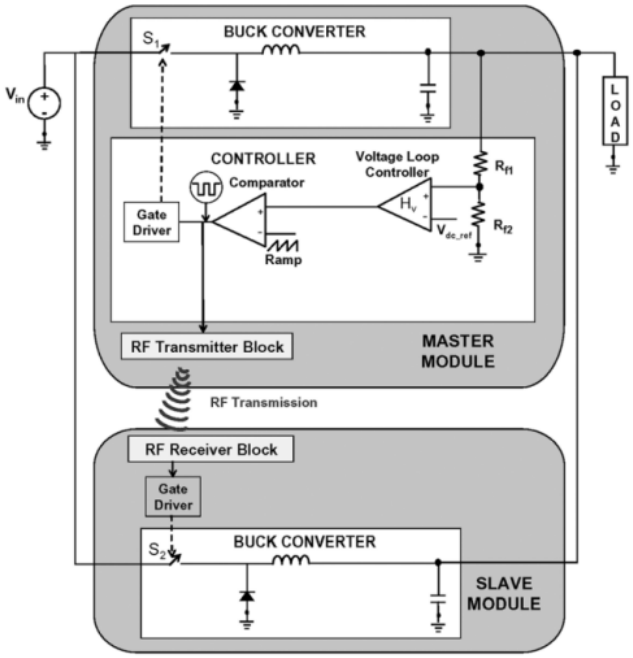
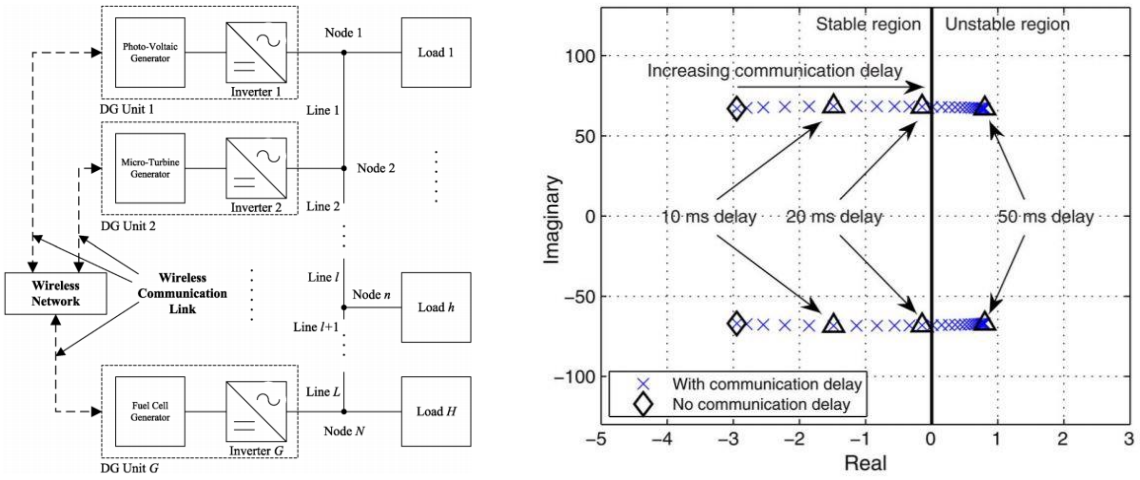


Figure 4. The wireless control scheme for parallel dc/dc converter [18] **©2008 IEEE.**

control signals were transmitted from the master to the slave module wirelessly, ensuring equal load sharing between the two modules. Additionally, a bound on the maximum time delay in communication that the system can tolerate while ensuring system stability and performance is also provided.

Next, as shown in Figure 5 (a), a wireless communication architecture has been proposed for enhancing the stability of a droop based decentralized inverter control scheme [21]. Wireless network with the configurable delay has been used for transferring information related to real and reactive power generated at the distributed generation units. Authors in [21], reported the movement of low-frequency modes towards instability with increased delay. Further, a complete loss of stability has been reported for a communication delay higher than 20 ms. Numerical result outlining this finding are shown in Figure 5 (b).

Lately, there have been significant efforts in developing methods for transmitting simultaneous wireless power and data efficiently using inductive links [22], [23]. In [22], an approach for integrating wireless bi-directional power and data transfer system has been outlined. Using the circuit shown in Figure 6, the authors reported achieving a maximum data rate of 20 $k$bps for a 500 W of power transfer between inductive coils with 7.5 cm. separation.



(a) **(b)**

Figure 5. The configuration of a microgrid with wireless communication network between distributed generation units [21]**, and (b) Impact of communication delay on the location of different modes** [21]**, ©2013 IEEE.**

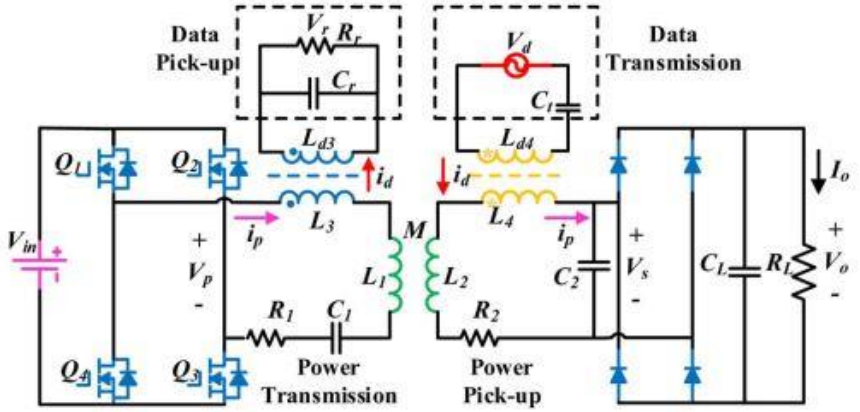


Figure 6. Schematic design of a circuit used for wireless power and data transfer [22]**, ©2015 IEEE.**

Although attractive, integrating wireless communication network on power transmission system highly depends on its communication delay, bandwidth, environmental interference, scalability, and security [24]. Communication delay is the total of time incurred in modulating, transmitting, receiving and demodulating the data. Maximum delay handling capability of a DPS sets the communication network scheme that it can work with. For instance, in [19], the author reports that because of the delay incurred in communication, operating the parallel dc/dc converter with a 20 *k*Hz switching frequency was not achievable. Next, the information transfer capacity of the channel is defined as

its bandwidth. The rated bandwidth of a wireless network can be very different from the observed network throughput [25], due to various sources of environmental interference and cross coupling. Though wireless network may be able to provide reliable data transfer using re-transmission and error-correction coding, this may add to the communication delay and affect the overall network throughput. Moreover, there can be scenarios where setting up a wireless network is not physically possible. Lastly, one of the major concerns associated with the use of the wireless network for communication is related to its security. Since in a HFDPS large volume of application-critical information will be transferred wirelessly between various PESs. It is essential to develop robust cybersecurity protocols to protect the wireless communication network against such threats. As a result of all the aforementioned issues, while wireless communication networks can provide an easy and reliable communication solution, they are mainly used for short distance connection with comparatively low data rates [26].

2. Wire-Based Communication Network

A wire-based communication network for an HFDPS can be further subdivided as simultaneous and sequential power and data delivery networks. In a simultaneous power and data delivery network, power and data signals are transferred together through a common waveguided medium. However, in a sequential power and data transfer network, power and data are distributed temporally.

- *Simultaneous Power and Data Transfer*

One of the most prevalent and widely researched wire-based technique for simultaneous data transmission in a DPS is the power line communication (PLC) [27]–[29]. In PLC, low voltage HF data signals are transmitted over a high voltage power transmission network which generally operates at a frequency of 50/60 Hz. Figure 7 illustrates the coupled HF data and LF power signals which are being transmitted simultaneously over the power lines. Conventional PLC architecture comprises of 4 essential components, line traps, modulator/demodulator, line couplers, and the transmission link. Figure 8 outlines the underlying architecture of a PLC-based sequential power and data transfer network. First, data to be transmitted is modulated to an HF signal using one of the various modulation techniques (FSK, ASK, OFDM, etc.) in a modulator unit. Later, inductive or capacitive line couplers are used to couple the HF modulated data to the high voltage power signals which are being transmitted over the power line. At the receiving end, line couplers and demodulator unit act as a receiver and are used to extract HF data from the power lines. Line

traps in the form of parallel resonant circuits are placed in the power lines to provide a high impedance to the HF modulated data signals and prevent them from traveling to unwanted locations.

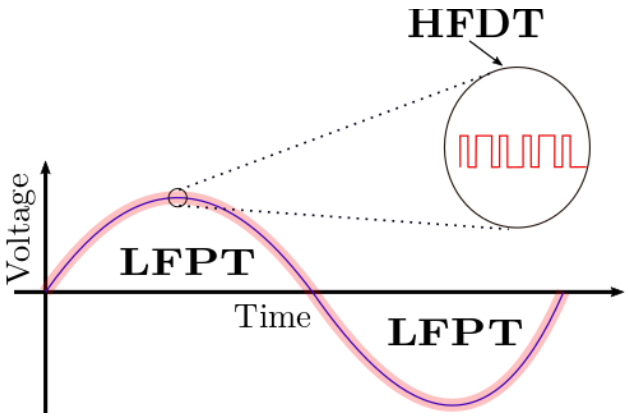


Figure 7. Illustration of a conventional PLC technique with simultaneous low-frequency power transfer (LFPT) and HF data transfer (HFDT) [30]**, ©2018 IEEE.**

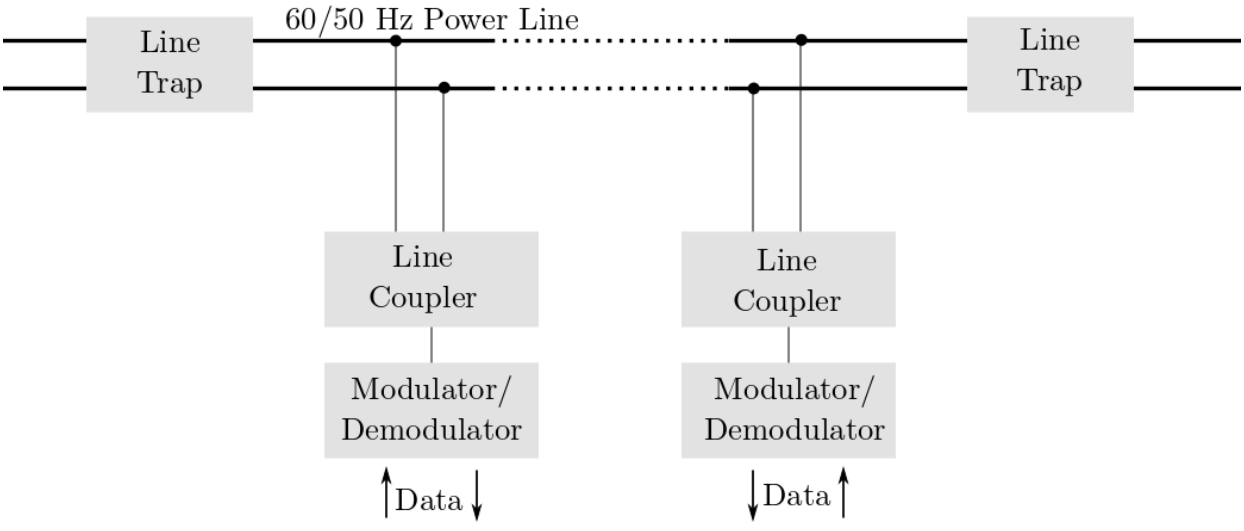


Figure 8. The underlying architecture of a PLC-based simultaneous power and data transfer network.

PLC is widely used over LF sinusoidal network, this can mainly be attributed to the fact that the wide separation between the frequency spectrums of the two signals (LF power signals and HF data signals) being transmitted over the power line enables the construction of simple but large reactive couplers, line traps, and low-order analog-filtering circuitry. Furthermore, networking features like Power Over Ethernet (POE) have surfaced using PLC technology, which uses an ethernet cable for supplying power to network devices over the existing data connection. However, the power delivery capacity of a POE network is limited to 51 Watt by IEEE 802.3at-2009 [31]. This enables the integration of the PLC receivers and transmitters in small-sized packages for networked devices.

Recently, the use of PLC has been proposed for applications involving HF power transfer. Significant research efforts have been placed in application focusing on the design of a PLC network for PWM-inverter fed electric machines [30], [32]–[37]. Transmission characteristics of PWM-inverter-fed power lines are entirely different from that of a 50/60 Hz power transmission line. This is because the output voltage of a PWM inverter consist of pulses or square waves having sharp edges with variable frequency and duration. Thus, the power carried by such signal is distributed across a much broader frequency spectrum. For instance, the output voltage spectrum of a typical sinusoidal PWM inverter operating at a switching frequency of 12 *k*Hz is provided in Figure 9 [35]. As evident from Figure 9, in comparison to the output of a 60 Hz power line, which only has the power transfer at the fundamental frequency, the output of a PWM inverter has a large amount of switching frequency harmonics which extend up to the *k*Hz range. Although, the power residing in the high-frequency components is low, it can be enough to corrupt the low-voltage data signals that are being transmitted in the communication band. Thus, the focus of the past research has mainly been on designing new PLC modems that can facilitate coupling/decoupling of the HF low-voltage data signals on the HF high-voltage power signals with high slew rates effectively.

In [35] Chen et al. proposed a PLC-based approach for monitoring the winding temperature of a PWM-inverter fed induction motor. Schematic diagram of the developed motor condition monitoring system and reported experimental results are provided in Figure 10. A passive line coupling circuit consisting of HF transformer and capacitors was used to block the low-frequency PWM waves in the PWM-inverter fed power line from entering the data circuit. While at the same time coupling circuit provided a low impedance path for the HF communication carriers to the PWM-inverter fed power line. In the designed data circuit, Class B amplifier was used as a booster circuit for

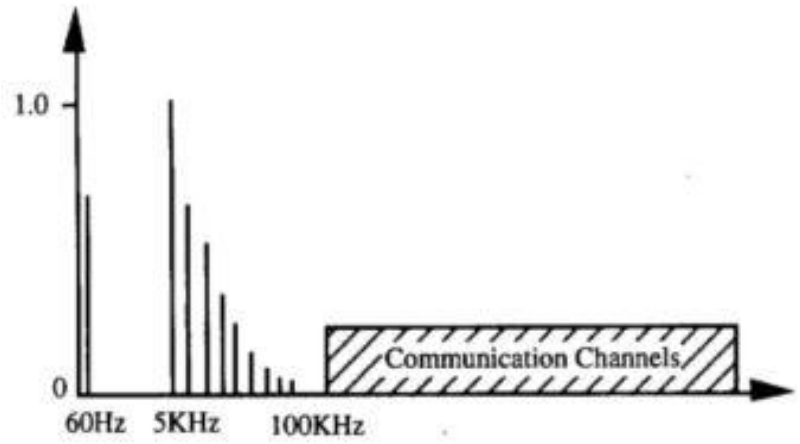


Figure 9. Transmission characteristics of a typical PWM-inverter fed power line [35]**, ©1993 IEEE.**

amplifying the low voltage FSK modulated data signals. A high order (ten poles) Butterworth bandpass filter centered at the communication frequency was employed at the receiver side to extract the HF data from the noisy power line. As can be seen from the experimental results of [35] provided in Figure 10 (b) and Figure 10 (c), for every PWM switching action, impulse noise was introduced in the data signals and caused data corruption. Finally, it has been reported that using a modified high-order low-pass filtering circuit and digital data recovery techniques; the authors were able to establish a satisfactory PLC network operating with a maximum data rate of 9600 bps (bauds per second) over power line feeding PWM signals to the motor. Similar observations were reported in [38], where the authors were able to achieve a maximum data rate of 40 kbps by avoiding data transfer during the event of switch transitions.

Further, in [33], [34], the authors presented a scheme for realizing PLC over HF PWM network using OFDM modulated data signals. Effect of PWM switching frequency, output voltage magnitude and length of power cable on PLC data transfer rate were studied. In this study, up to 90 % reduction in data rate was reported at a higher noise level and long transmission lengths. The main reason for the reduced data rate was reported as the increased magnitude of HF switching noise at higher voltage levels and attenuation of the HF data signals. The experimental setup and obtained results in [34] are shown in Figure 11 (a) and Figure 11 (b), respectively. Moreover, the authors reported that even with an LCL low-pass filter connected to the inverter output terminal (used for reducing PWM-inverter output voltage slope), significant voltage spikes were observed in the communication circuit.

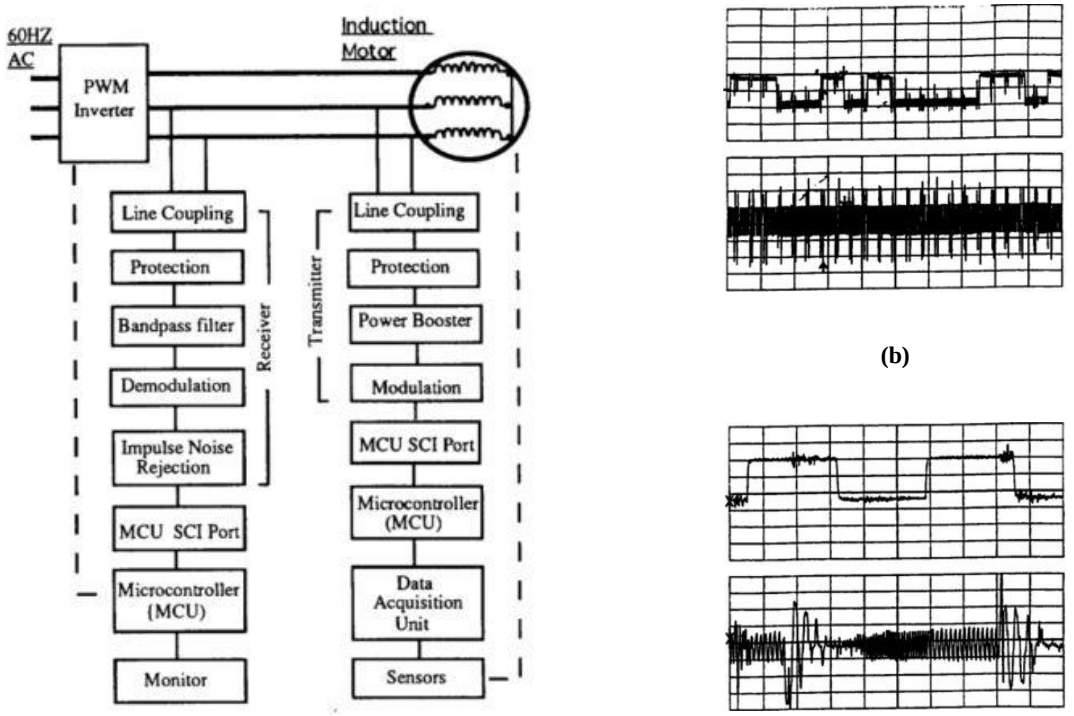


Figure 10. (a) Schematic of the motor condition monitoring system using PLC as proposed in [35]**. (b) Experimental plots of the transmitted data signal at the data input pin and signals at the primary terminal of the coupling transformer. (c) zoomed in version of the waveforms provided in (b), ©1993 IEEE.**

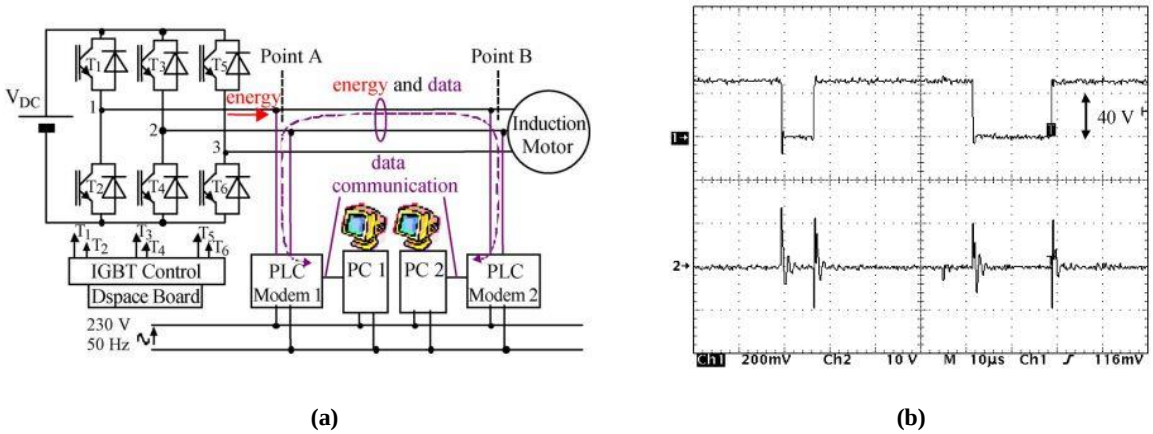


Figure 11. (a) Developed experimental setup for realizing PLC over PWM in [34]**, and (b) obtained experimental results showing PWM inverter output voltage and injected HF noise in the data circuit at every switching instant, ©2010 IEEE.**

- *Sequential Power and Data Transfer*

Another technique for power and data transfer through a wired-medium is the sequential transmission of power and data signals which is mainly employed in DPSs using packetized energy transfer [30], [39]–[42]. In this scheme, power and data signals are transmitted sequentially (as shown in Figure 12.), thereby ideally eliminating any spectral overlap between the two [30]. Sequential transfer of power and data was first conceptualized by Toyoda and Saitoh in terms of an open-electric-energy-network (OEEN) [43], [44]. In an OEEN, electric power was treated as a mail packet with its source and destination information attached to it in the form of data tags. Further, a network of multiple electric-energy-routers (EER's) was conceptualized to distribute the energy packets from various DER's to loads based on the tagged information. However, details about the shape, size, and frequency of the energy packets and the data tags were not discussed. Additionally, the research was ahead of its time, and the technological limitations restricted the practical realization of the mechanism required for generating these energy packets, data tags, and EER.

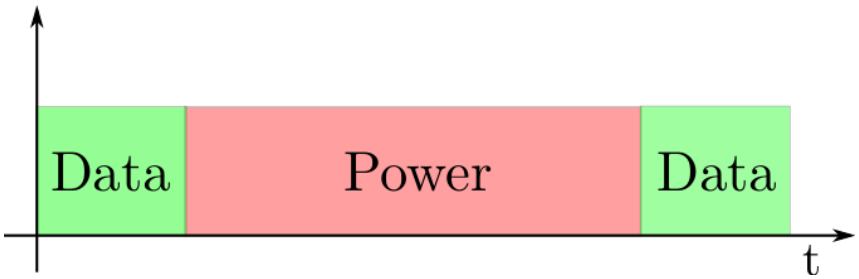


Figure 12. The basic structure of a power and data signal in a sequential power and data transfer scheme.

Owing to the advancements in the semiconductor industry, recently, sequential transfer of power and data signals has been proposed for HFDPS. In it, in contrast to a conventional DPS, where energy flow is constant, energy is transferred in the form of small energy packets along with information tags. In some applications, the attached information tag is used for ensuring system safety [39], while in others it is used for routing the energy packets through a network of energy routers from their source to destination [40]–[42]. Packetized energy transfer gives rise to multiple possibilities concerning how energy and information can be exchanged in an HFDPS. It forms the cornerstone for the research in digital grids, where the packetized energy transfer in a power network is envisioned as the data packet transfer in a computer network [45]. Additionally, packetized power transfer makes it possible for controlling the shape, size, and frequency of the power packets, which can now be tailor-made to cater to various time/event-driven

applications. However, the realization of such a system requires the development of highly sophisticated power and communication architecture that can coordinate and optimize the flow of energy and data packets in an HFDPS.

In recent days, various architectures for HFDPS supporting packetized power transfer have surfaced. Voltserver came up with the concept of "Digital Electricity" [39], [46], where power and data are transferred in packetized format from a transmitter unit to a receiver unit at a rate of 700 packets per second through a pair of conductor cables [46]. Although minimal information is available about the transmitter and receiver units, it is stated that the transmitter unit can be connected to any source with ac or dc output and transmit energy packets in the form of high-voltage dc signals over the conductor cable [39]. Once the high-voltage dc energy packets arrive at the receiver unit, they are converted back to an analog format at the correct voltage and power level required by the load. Data packets transmitted sequentially with the energy packets are used for monitoring system safety, by ensuring proper delivery of each energy packet from the transmitter to the receiver units. Each transmitter unit is said to have 24 line-cards that can support up to 24 receiver units in a single-input-single-output (SISO) configuration [46]. Though beneficial, "Digital Electricity" fails to realize the full potential of packetized power transfer concerning an HFDPS. This is because the developed system requires a dedicated transmitter for a dedicated receiver which as in a conventional HFDPS needs devoted power cables that leads to an increase in overall system cost and restricts the possibility of energy packet routing from multiple sources to multiple loads.

To enable the routing of energy packets in an HFDPS between various DER's and loads, in [40], [41] designs for power packet mixer and router units were provided. In the arrangement presented in [40], multiple DERs and loads were connected through the mixer, transmission line, and a router. Mixer unit had the role of connecting various DERs to a common transmission line, while, the router unit which was connected to the same transmission line, was used to connect/disconnect the loads. Information tags were physically attached to the power packet and contained information about the address of its source and destination load [40]. A pictorial representation of the prototype system as provided in [40], is presented in Figure 13. Additionally, circuit representation of the proposed mixer and router units in [40] are provided in Figure 14 (a) and Figure 14 (b), respectively.

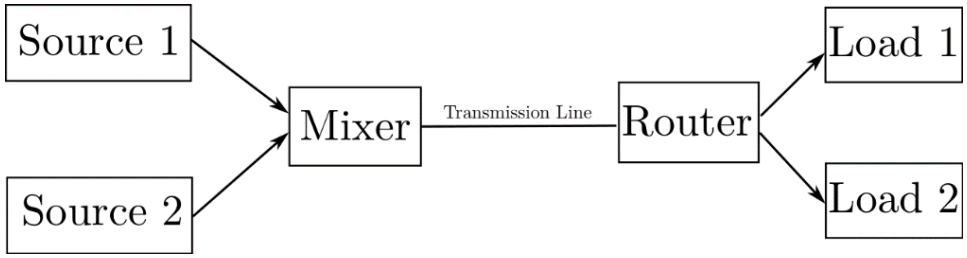


Figure 13. Schematic of the power packet dispatch system outlined in [40]**.**

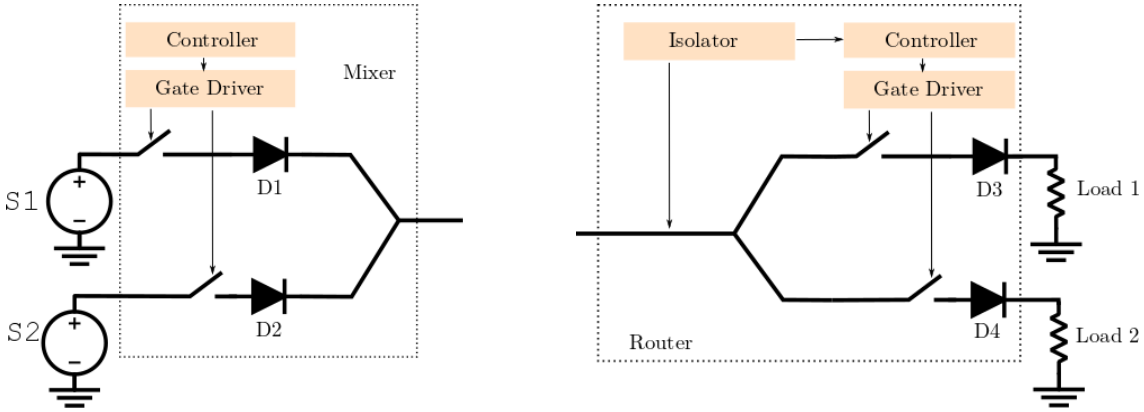


Figure 14. Schematic of power packet mixer and router units outlined in [40]

As can be observed from Figure 14 (a) and Figure 14 (b), designed mixer and router units had a diode in their forward path. It was used for avoiding the reverse flow of energy in the developed prototype. However, apart from inducing additional losses (which will be significant at high power levels), the diode also restricts the ability of the developed prototype in [40] to support the bi-directional transfer of the energy packets through the common TL connecting mixer and router. This limitation restricts the adoption of such mixer and router prototypes in HFDPS that require bi-directional power flow for applications encompassing energy storage systems, motor drives, etc. Moreover, the channel for power and data transfer is not decoupled, this results in HF data signals to be transmitted to the load. This can be observed in the experimental results provided in [40, Fig. 12]. Additionally, in experimental results provided in [41, Fig. 5] for a sub-1W system, large magnitude HF voltage spikes are visible at the load terminal during the time data is transmitted on the TL. This can lead to deterioration of closed-loop dynamics of the system as slower-

scale small-signal controllers are derived around quiescent points and do not incorporate such high-frequency dynamics of the system. Use of 47 μF capacitors has been proposed at the load in [41] to reduce the ripple on a 12 V system, which is not practically viable and significantly reduce power density and specific weight of a higher power PES prototype, where large EMI filters must be used to suppress the enormous common-mode and differential-mode noise of the system to meet the admissible levels. Additionally, the scheme outlined in [40], [41] is mainly proposed for applications involving dc loads, where a constant dc source is switched for creating the energy packets. Although, not much information is provided about the data tag generation circuit, from [40, Fig. 11], it can be deduced that the voltage level of all the bits in the data tag are equal to the voltage level of the energy packet and the dc source. Thus, the data tags are constructed using HF switching in the mixer unit, where for creating a "0" binary bit source was disconnected from the common TL and for creating a "1" binary bit source was connected to the common TL. This scheme for data generation is not practically viable in high-power applications and would result in high switching losses in the mixer unit and restrict the maximum data speed. In [40] a maximum data speed of 400kHz is reported, it is also the maximum switching frequency used in the design. Additionally, using such a mechanism for data bit generation, only unidirectional communication from the mixer to the router is possible. This restricts the possibility of bi-directional communication which is required for transferring the requirement of the load to the source. In successive improvement to the scheme proposed in [40], in [42] Reza et. al. proposed a request generation circuit that can be added to the router unit for realizing bi-directional communication. However, the rest of the limitations remained the same.

D. Motivation and Objective of Doctoral Research

HFDPS for suitable applications has demonstrated a compact solution for the overall power system while ensuring enhanced system efficiency and reliability. Moreover, adding a communication link for information exchange with limited overhead cost has always been of perpetual interest. However, designing a PLC network for simultaneous HF power and data transfer for an HFDPS poses various challenges. Firstly, a complex high-order analog filtering circuit is required for coupling/decoupling the power and data signals. Secondly, the PLC technique results in a spectral overlap between the HF power and data signals, which following Shannon's theorem [47], reduces the channel capacity for data transmission.

The predicaments of the abovementioned simultaneous HF power and data transfer can be overcome via sequentially transmitting HF power and data signals. The sequential transmission schemes outlined in [40]–[42] were successful in demonstrating the concept of packetized power routing using the attached information tag in a low-voltage low-power controlled environment. Notwithstanding, there are various challenges in the outlined schemes that restrict their scalability to high-power, high-voltage applications. Firstly, HF switching of the dc power source in the mixer unit for generating the data tags result in high-switching losses and makes the outlined scheme for data tag generation inefficient. Secondly, the EMI-noise emissions resulting due to the high dv/dt and di/dt stresses due to HF switching in the network will significantly limit the applications of the proposed schemes in [40]–[42], in next-generation power electronics systems. Moreover, all the previously outlined schemes dealt with packetized energy transfer to dc loads and challenges for ac synthesis have not been outlined.

In lieu of the above discussion, in this dissertation, a new scheme enabling discrete HF power and data transfer over an HF channel in an HFDPS is outlined and is termed as "Sequential co-transfer scheme". The sequential co-transfer scheme employs a circuit switching technique for HF power and data transfer in which a common HF channel alternates between HF power channel and data channel. The proposed scheme addresses the limitations of simultaneous wire-based communication schemes by transferring HF power and data sequentially. Additionally, the use of circuit switching technique in the sequential co-transfer scheme decouples the HF power and data circuits and provides advancements over the current state-of-the-art methods for packetized energy transfer in terms of enabling high-power applications and bidirectional data and power flow. These new added capabilities can help realize need based power delivery for dc or ac loads. Moreover, since in a sequential co-transfer scheme HF power and data signals are temporally distributed, this allows for the application of simple data coupling/decoupling mechanisms which are devoid of any higher-order analog filtering circuit.

The dissertation is divided into five chapters. In Chapter 2, an overview of the proposed sequential co-transfer scheme for HF power and data transfer will be presented. Next, a general discussion about the advantages of the proposed scheme in an HFDPS will be delineated. Further, to test the feasibility of the proposed scheme, two case illustrations (a) single-input-single-output (SISO), and (b) single-input-multi-output (SIMO) HFDPS will be considered. For the former, a scheme for need-based power delivery to a dc load using the sequential co-transfer

scheme will be discussed, and for the latter, along with need-based power delivery, use of the proposed scheme for routing of HF power and data packets for feeding dc and ac loads will be addressed.

To realize the case illustrations provided in Chapter 2, in Chapter 3, first, the design of the required power transmitter and receiver nodes will be discussed. Also, requirements from the data network in a sequential co-transfer scheme will be provided, and design of a modified serial communication interface (SCI) protocol for ensuring robust data transfer in the presence of HF impulsive channel noise will be given. Using the designed power and data nodes, circuit realization for the two cases illustrations will be provided, and various modes of operation during which HF channel is used for power and data transfer will be presented. Also, schemes for implementing need-based power delivery and packetized power routing using the data nodes for information exchange will be discussed. Furthermore, in Chapter 3, various practical design related issues with a GaN-FET based PES will be addressed and appropriate design solutions for each will be provided.

In Chapter 4 experimental validation for the proposed scheme will be presented and its advantages over simultaneous HF power and data co-transfer scheme will be established. At first, experimental results will be presented on a SISO HFDPS feeding dc load, and later experimental results for a SIMO HFDPS feeding dc and ac loads will be provided. Further, design modifications required in the data nodes for enabling high-power application of the proposed scheme will also be provided.

Finally, the dissertation will be concluded in Chapter 5, and some suggestions for the future work will be provided.

Chapter 2

Sequential Co-Transfer of HF Power and Data

Parts of this chapter, including figures and text, are based on my following papers:

- A. Gupta and S. K. Mazumder, "Sequential Co-transmission of High-Frequency Power and Data Signals," in *IEEE Transactions on Industrial Informatics*, vol. 14, no. 10, pp. 4440–4445, 2018.

A. Introduction

In lieu of the limitations of state-of-the-art simultaneous and sequential co-transmission schemes outlined in Chapter 1, in this chapter, a new approach for the co-transfer of HF power and data signals over a common HF channel is described. In the proposed approach, power and data networks are linked over a common HF channel mutually exclusively, thereby ideally eliminating any spectral overlap between the two. First, the mechanism required for realizing the co-transfer of HF power and data signals is outlined. Later, the design of an HFDPS following sequential co-transfer scheme is envisioned. Finally, to explore the feasibility of the sequential co-transfer scheme in an HFDPS two case illustrations are chosen and are discussed in detail.

B. Proposed Approach for Sequential Co-Transfer of HF Power and Data Signals

In this section, a new approach for the sequential co-transfer of HF power and data signals between n power and data transmitter nodes and n power and data receiver nodes is discussed. The new approach is termed as the "sequential co-transfer scheme". The sequential co-transfer scheme is based on circuit switching technique, in which network switches encompassing transfer and data switches are used for connecting/disconnecting power and data nodes from a common channel, respectively. This enables the transfer of HF power and data signals mutually exclusively over a common HF channel. In Figure 15, PN_{nS} (PN_{nL}) and DN_{nS} (DN_{nL}) refer to the n^{th} power and data transmitter (receiver) nodes while S_{nPS} (S_{nDS}) and S_{nPL} (S_{nDL}) are network switches that connect/disconnect the n^{th} power (data) node from the common HF channel. The network switches in Figure 15 follow the Boolean logic given in 2.1:

$$\overline{\mathrm{S_{nPS}}} \,\overline{\oplus}\, \overline{\mathrm{S_{nPL}}} = 1,$$

$$\overline{\mathrm{S_{nDS}}} \,\overline{\oplus}\, \overline{\mathrm{S_{nDL}}} = 1, \tag{2.1}$$

$$\mathrm{S_{nPS}} \oplus \mathrm{S_{nDS}} = 1,$$

$$\mathrm{S_{nPL}} \oplus \mathrm{S_{nDL}} = 1,$$

where $\overline{\oplus}$ and $\oplus$ represent the XNOR and XOR logic operators, respectively. Following these Boolean logic ensures that the n^{th} transmitting and receiving power and data switches are synchronized while the corresponding switches that support power- and data-transfers operate complementarily. When both S_{nPS} and S_{nPL} are turned ON, power transmission network nodes PN_{nS} and PN_{nL} are connected and power is transmitted over the HF channel. Similarly, when S_{nDS} and S_{nDL} are turned ON, data transmission network nodes DN_{nS} and DN_{nL} are connected and data is transmitted over the HF channel.

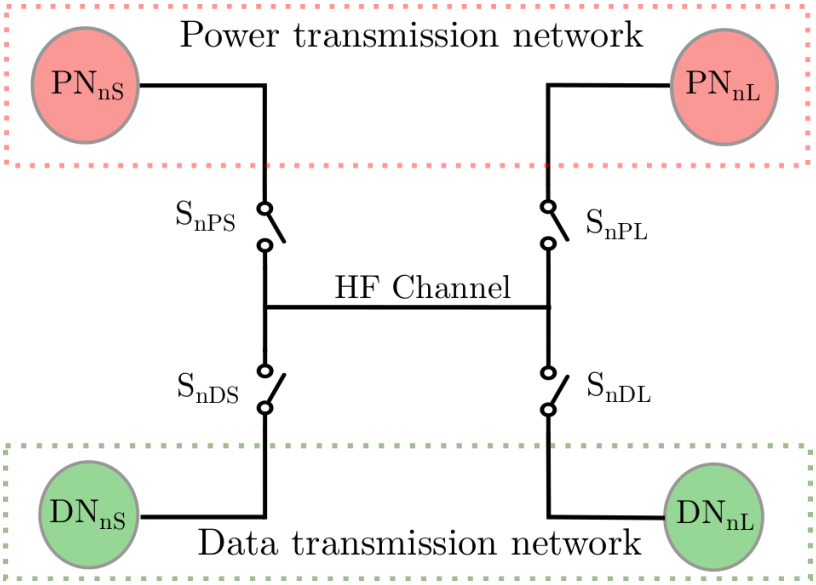


Figure 15. Overview of the network supporting sequential co-transfer of HF power and data over the common HF channel. PN_{nS} and PN_{nL} serve as the power transmitter and receiver nodes, while DN_{nS} and DN_{nL} represents data nodes corresponding to power nodes PN_{nS} and PN_{nL}, respectively.

The power transmission network outlined in Figure 15, transmits electrical power signals over a common HF channel in a fast and reliable manner between the power transmitting node PN_{nS} and the power receiving node PN_{nL}. Depending on the choice of power transmitting and receiving nodes, it can be configured to transmit discrete, continuous AC, and/or time-invariant DC power of arbitrary wave shape and/or arbitrary sequence. This can yield to time and/or event guided packetization of power transfer. Additionally, using the power transmission network HF power packets can be dynamically routed between a plurality of energy sources and energy loads. For example, the power transmission network can be used for realizing peer-to-peer power delivery between one or more energy sources

and one or more energy loads. In Figure 15, PN_{nS} is coupled to a power generating source and is configured to transmit HF power packets over the common HF channel, while PN_{nL} is coupled to a load and is configured to receive HF power packets over the common HF channel.

The data transmission network outlined in Figure 15 is used to exchange low-voltage data signals in a fast and reliable manner between data nodes DN_{nS} and DN_{nL}. DN_{nS} and DN_{nL}, serves as the corresponding data nodes to power nodes PN_{nS} and PN_{nL}, respectively and can be configured as a data transmitter or receiver. Various data transmission protocols can be incorporated in the data transmission network for transmitting digital or analog data signals through the HF channel. It can also be used for implementing advanced network control algorithms by exchanging status information, control commands, and/or sensor feedback between the components of the power transmission network and the network switches. This can lead to an intelligent management of the available energy resources in catering to the dynamic load-requirements.

An illustration of the HF power and data signals that can be exchanged using the sequential co-transfer scheme is provided in Figure 16. As can be observed in Figure 16, HF power and data signals are temporally distributed on the HF channel. Additionally, circuit switching technique enables the coupling of low-voltage data and high-voltage power signals on a common HF channel mutually exclusively thereby eliminating the need for switching the network switches at data frequency as was done in previously proposed sequential power and data schemes [40]. This results in increased system efficiency, reliability, and higher data rate.

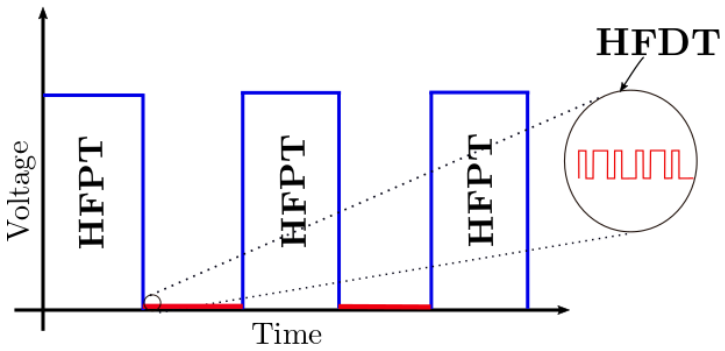
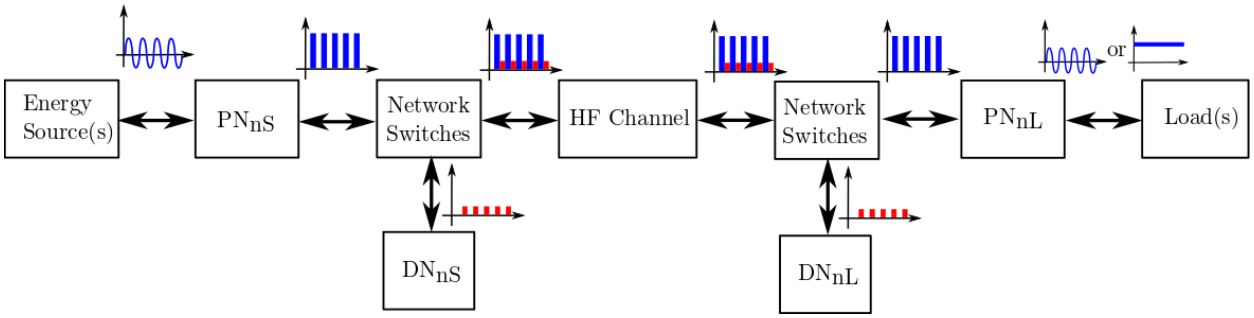


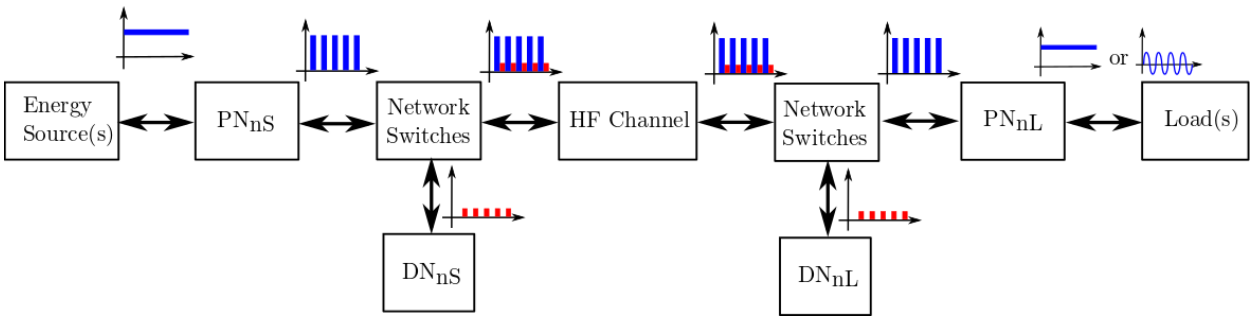
Figure 16. Illustration of the sequential co-transfer scheme for HF power and data (HFPT, HFDT) transmission [30], **©2018 IEEE.**

C. HFDPS Following Sequential Co-Transfer Scheme

The sequential co-transfer scheme as outlined in Section B can provide a mechanism for HF power and data transfer between a variety of sources and loads. It provides an alternative power distribution framework by transferring power in discretized energy packets, thereby asynchronously dispatching power based on demand. Additionally, the HF channel can serve a dual purpose, on the one hand, it can be used for transferring HF power packets from the DER to the load centers, while on the other it can be used for exchanging critical information regarding system performance and control. Further, enabling a DPS with HF power transfer increases system power density and dynamic response by decreasing the size of the system's magnetic and capacitive components.



(a)



(b)

Figure 17. An HFDPS following the sequential co-transfer scheme for transferring power from (a) an ac source to an ac/dc load, and (b) a dc source to a dc/ac load. PN_{nS} and PN_{nL} represents n^{th} power transmitter and receiver nodes, respectively. DN_{nS} and DN_{nL} represents data nodes corresponding to PN_{nS} and PN_{nL}, respectively.

Unlike conventional DPS, an HFDPS following sequential co-transfer scheme can transmit power and data in a discrete packet that can be routed to different power and data nodes using various packet routing techniques. Figure 17 (a) outlines an HFDPS following sequential co-transfer scheme connecting a dc source to a dc/ac load, and Figure 17 (b) outlines another HFDPS following sequential co-transfer scheme connecting a dc source to a dc/ac load. In both ac and dc HFDPS, a power transmitter node (PN_{nS}) transmits HF power packets over the HF channel to a power receiver node (PN_{nL}), and data nodes (DN_{nS} and DN_{nL}) are used for exchanging the control/status commands in a sequential manner. In operation of the HFDPS supporting ac source outlined in Figure 17 (a), the energy source supplies an ac power signal to the PN_{nS}. PN_{nS} transforms the continuous, ac power signal into discrete, HF power packets. Data packets are generated/received by the data node (DN_{nS}) corresponding to PN_{nS}. Network switches, that encompass the transfer and data switches, temporally distribute the discrete HF power and data packets over the common HF channel. At the load end, network switches decouple the temporally distributed discrete HF power and data packets. While PN_{nL} receive the discrete HF power packets and transform them back into an ac/dc power signal required by the load, data packets are received/generated by DN_{nL}. HFDPS supporting dc source outlined in Figure 17 (b) operates in a similar manner, with the difference being the input and output voltage characteristics on PN_{nS} and PN_{nL}, respectively.

In contrast to the conventional DPS which have a fixed power transmission characteristic, an HFDPS following the sequential co-transfer scheme, such as those outlined in Figure 17 (a) and Figure 17 (b), can be configured to transform the wave shape and/or form of the power signal transmitted over the HF channel by choosing an appropriate combination of PN_{nS} and PN_{nL}. For example, the wave shape of a continuous, sinusoidal bipolar ac signal may be transformed and transmitted as a different shape and/or type of signal, such as a discontinuous, unipolar packetized signal. Transforming the wave shape can improve transmission integrity of the HF power packet by choosing the frequency of HF power transfer signal based on transmission length and avoiding the occurrence of TL effects in long range transmissions [48]. Further improvement in system efficiency can be achieved by coding the discrete HF power packets to reduce the effort required in PN_{nL} for converting the HF power packets back to a continuous signal [49].

Further, the sequential co-transfer scheme enables routing of the HF power packets from one or more energy sources to one or more loads using network switches. Data nodes can be used for implementing network protocols

that can dynamically determine existing source availability and load demand. Since in the sequential co-transfer scheme, HF power is transferred using discrete HF power packets, it can connect a variety of sources with different voltage characteristics to a variety of loads using a common HF channel. Additionally, transfer of power in the form of discrete HF power packets can result in the elimination of standby power consumption which is prominent in a conventional DPS. As by using the sequential co-transfer scheme need-based power delivery can be realized, HF power packets can be routed to the load only upon reception of a request.

Based on the above discussion, in this dissertation, the feasibility of the proposed sequential co-transfer scheme for HF power and data signals is explored on a single-input-single-output (SISO) and single-input-multi-output (SIMO) HFDPS, details about which are provided next:

1. Case I: SISO HFDPS Following Sequential Co-Transfer Scheme

A SISO HFDPS is outlined in Figure 18. It comprises of a single power transmitter node (PN_{1S}) and a single power receiver node (PN_{1L}). Data nodes DN_{1S} and DN_{1L} serve as the corresponding data nodes to PN_{1S} and PN_{1L}, respectively. Network switches comprise of the transfer and data switches, are used for connecting and disconnecting power and data nodes from the HF channel, respectively, in a mutually exclusive manner.

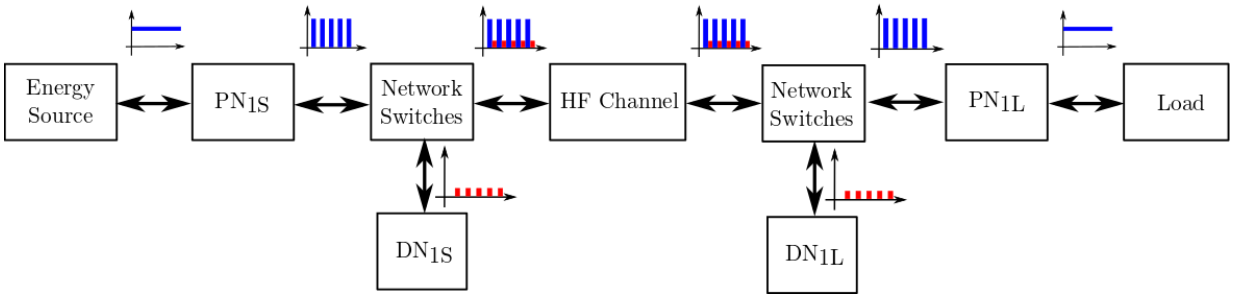


Figure 18. A SISO HFDPS following sequential co-transfer scheme.

SISO HFDPS can be used for realizing need-based power delivery using the sequential co-transfer scheme. During operation, the power demand of the load can be transferred from DN_{1L} to DN_{1S} through the HF channel. Based on the received request, PN_{1S} which is connected to a dc energy source can generate HF power packet and transfer it to PN_{1L}

through the HF channel which further converters it to a continuous dc output. Sequentially transmitted data can further be used to update the request after the reception of each HF power packet at PN_{1L}.

2. Case II: SIMO HFDPS Following Sequential Co-Transfer Scheme

Figure 19 outlines an HFDPS following sequential co-transfer scheme for a single-source multiload system. This illustration, which corresponds to a SIMO HFDPS, includes one energy sources feeding HF power packets to two loads through a common HF channel. Network switches that comprise of transfer and data switches are used for connecting and disconnecting power nodes (PN_{1S}, PN_{1L}, and PN_{2L}) and data nodes (DN_{1S}, DN_{1L}, and DN_{2L}) from the HF channel. In operation, SIMO HFDPS can transform and route HF power (data) packets from PN_{1S} (DN_{1S}) to PN_{1L} (DN_{1L}) and/or PN_{2L} (DN_{2L}) based on various HF channel access protocols through the HF channel.

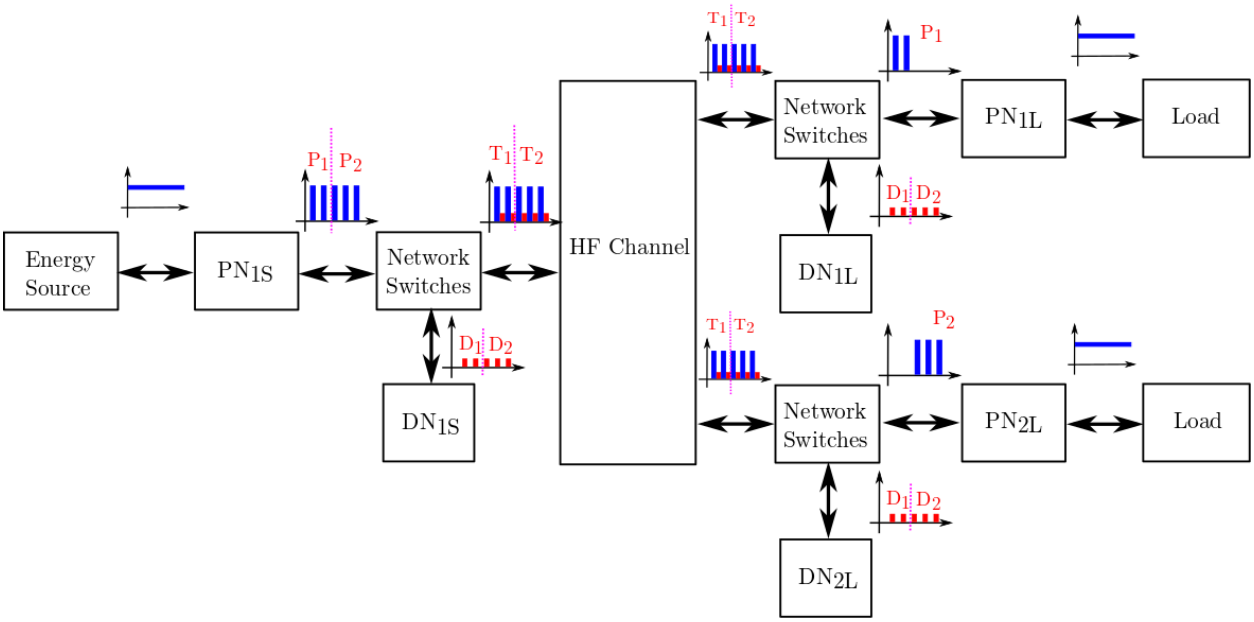


Figure 19. A SIMO HFDPS following the sequential co-transfer scheme. HF Power and data packets can be routed to different power nodes and data nodes using the network switches.

In the SIMO HFDPS outlined in Figure 19, PN_{1S} serves as the power transmitter node and transforms a continuous dc power signal into discrete HF power packets represented by P_1 and P_2. Network switches, that encompass the transfer and data switches, are used to temporally distribute the discrete HF power and data packets (D_1 and D_2,

transmitted by DN_{1S}) over the common HF channel. These, temporally distributed discrete HF power and data packets are represented by T_1 and T_2 in Figure 19. Next, T_1 and T_2 are transmits toward the power receiver nodes (PN_{1L}, PN_{2L}) and their corresponding data node (DN_{1L}, DN_{2L}) through the HF channel. In the illustration provided in Figure 19, network switches at the load-end route the HF power packets marked as P_1 (P_2) to PN_{1L} (PN_{2L}). Similarly, the data packets marked as D_1 (D_2) are routed to the data node DN_{1L} (DN_{2L}) by the network switches. Once P_1 (P_2) is received at PN_{1L} (PN_{2L}), it is transformed back to a continuous dc power signal and fed to the load. It is noted that the SIMO HFDPS outlined in Figure 19, can transfer different HF power and data packets to different loads using network switches. For instance, spatially distributed discrete HF power and data packets marked as T_1 can be transferred to PN_{2L} and DN_{2L}, and T_2 can be transferred to PN_{1L} and DN_{1L}. Using some other combination of network switches in a SIMO HFDPS it is also possible to transfer P_1 (P_2) to PN_{1L} ($PN_{2,L}$) and D_1 (D_2) to DN_{2L} (DN_{1L}). Furthermore, the size of the discrete HF power packets routed to the loads can be tailored as per the load demand.

D. Summary

In this chapter, a new approach for the co-transfer of HF power and data signals through a common HF channel is outlined. In the proposed approach power and data signals are transferred sequentially in a mutually exclusive manner. The proposed sequential co-transfer scheme can serve as a solution to the problem of data corruption caused by the HF sidebands of the power signals, being transmitted simultaneously in an HF PLC network. Additionally, it can also help in simplifying the data transmitter/receiver design. This is because, due to the elimination of spectral overlap between the HF power and data signals in a sequential co-transfer scheme, the need for large reactive couplers, line traps, and high-order analog-filtering circuitry, conventionally required in a PLC scheme are precluded. Furthermore, the proposed approach utilizes a circuit switching technique that enables the use of separate power and data transmitter and receiver circuitry. Using the proposed sequential co-transfer scheme, design of an HFDPS is discussed. Further, two case illustrations (a) SISO HFDPS, and (b) SIMO HFDPS are selected for exploring the feasibility of sequential co-transfer scheme in realizing need-based power delivery and routing of discrete HF power and data packets.

Chapter 3

Implementation of Sequential Co-Transfer Scheme

Parts of this chapter, including figures and text, are based on my following papers:

- A. Gupta and S. K. Mazumder, "Sequential Co-transmission of High-Frequency Power and Data Signals," in *IEEE Transactions on Industrial Informatics*, vol. 14, no. 10, pp. 4440–4445, 2018.
- A. Kulkarni, A. Gupta, and S. K. Mazumder, "Resolving practical design issues in a single-phase grid-connected GaN-FET-based differential-mode inverter," in *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3734–3751, May 2018.
- A. Gupta and S. K. Mazumder, "GaN-FET based grid-connected solar microinverter: Some design insights," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 233–237.

A. Introduction

In this chapter, an approach for implementing sequential co-transfer of HF power and data packets over a common HF channel is explored for a SISO HFDPS feeding dc loads, and a SIMO HFDPS feeding dc and ac loads, through a dc energy source. First, the design and power electronics system (PES) required for implementing the power transmitter and receiver nodes are discussed and later the design for the data nodes and data transfer protocol are provided. Further, system design for realizing the sequential co-transfer scheme in a SISO and SIMO configuration of an HFDPS are presented using the designed power transmitter and receiver nodes. Finally, a detailed discussion about the hardware challenges encountered while implementing a GaN-FET based PES are given and some practical solutions for the same are proposed.

B. Design of the SPES and LPES

As specified in Chapter 2, the sequential co-transfer scheme provides a mechanism for high-speed power and data transfer between a variety of DERs and loads. Generally, the output of DER is in the form of an unregulated dc or ac voltage. Interfacing such DER with an HF channel requires an active front-end power electronics interface that can generate discrete HF power packets. In this dissertation, this active-front-end power electronics interface and source combination is referred to as the source-end power electronics system (SPES) and serves as a power transmitter node. SPES create discrete HF power packets and serves as an interface between a DER and an HF channel. Each DER is interfaced to an HF channel using a separate SPES. Once generated by the SPES, HF power packets are transmitted sequentially over the HF channel, where they are received by the load-end power electronics system (LPES). LPES serves as an interface between the load and the HF channel. LPES comprise of an active-front-end power electronics interface that converts the received HF power packets in a form required by the load (either dc/ac or pulsating).

In this dissertation for realizing the case illustrations of SISO and SIMO HFDPS, provided in the previous chapter, an isolated Ćuk converter as shown in Figure 20, is selected as the PES. Conventional isolated Ćuk converter topology as shown in Figure 20 uses two low-side switches working in a complementary fashion to generate a step-up or step-down output voltage depending on the duty cycle provided to switches S_1 and S_2. In its first mode of operation (mode-1) when switch S_1 is turned ON input inductor L_1 current start building as the input supply V_{in} comes in parallel to it.

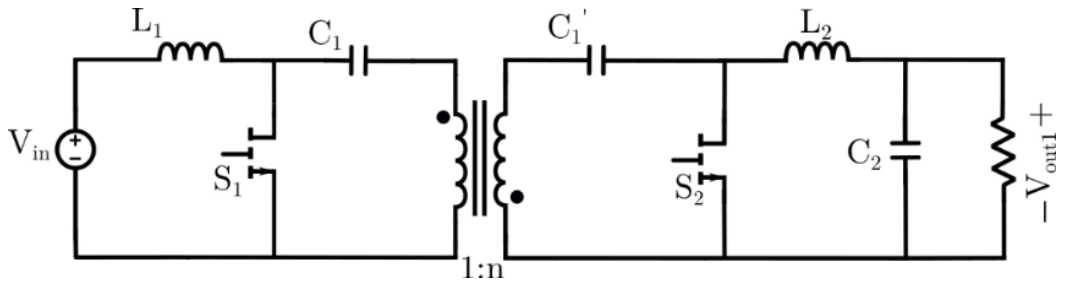


Figure 20. Schematic diagram of an isolated Ćuk converter.

Blocking capacitor $C_1$and C_1' supports the load current and the output inductor L_2 current rises. During its second mode of operation (mode-2) switch S_1 is turned OFF and S_2 is turned ON, the energy stored in L_1 is used to charge the blocking capacitors $C_1$and C_1' and the load is fed from the energy stored in the output inductor L_2 from mode-1.

As is shown in Figure 21, for inserting the HF channel to the conventional isolated Ćuk based topology, an additional diode (D_1) needs to be added in parallel to the secondary side switch S_2. Placing D_1 in the specified position provides a HF channel in which no power flows during mode-2. While at the same time, D_1 ensures that the distributed converter follows the exact same modes of operation as a conventional isolated Ćuk converter, by providing a freewheeling path to the charging current of C_1' in mode-2.

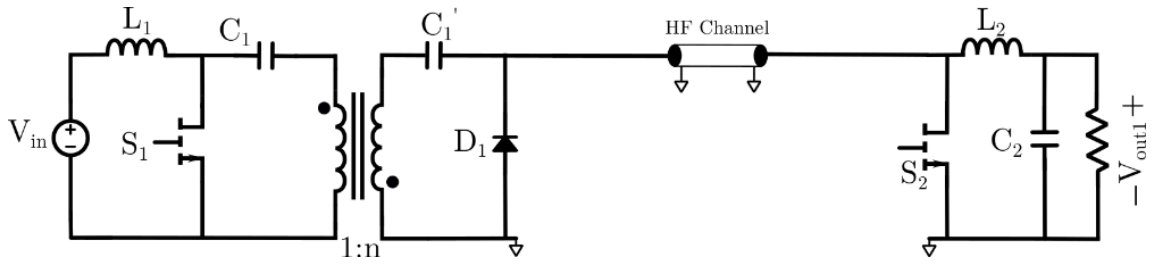


Figure 21. Schematic representation of a distributed converter with an integrated HF channel.

Since no power flows through the HF channel shown in Figure 21 during mode-2, it can be disconnected from the circuit with the help of HF switches (S_{1PS} and S_{1PL}) which are connected at either ends of the HF channel. Figure 22 shows the position of S_{1PS} and S_{1PL} with respect to the HF channel. Source-end of the distributed converter can now work as the required SPES and the load-end of the converter can work as the required LPES. In this dissertation switches that connect and disconnect the SPES and LPES from the HF channel are termed as transfer switches.

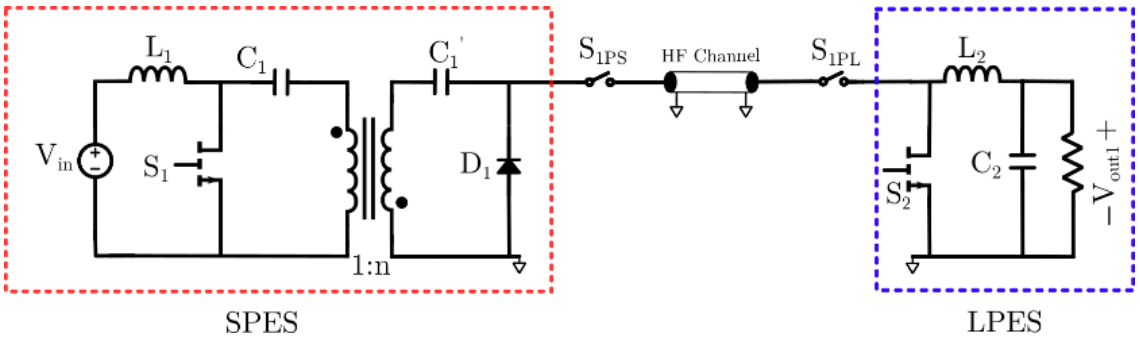


Figure 22. Schematic representation of a distributed converter with an integrated HF channel and transfer switches S_{1PS} and S_{1PL}.

C. Design of the Data Nodes

In contrast to the simultaneous co-transmission scheme, in the proposed sequential co-transfer scheme, since the power and data signals are transferred mutually exclusively, for a fixed frequency of power transfer, the time duration available for data transfer is limited by the size of power packet requested by the load. Consequently, conventional data transmission protocols used for simultaneous power and data transmission like HomePlug 1.0, HomePlug AV, Powerline AV, etc. [27], [28] that require significant data overheads in the range of 100-200 μs cannot be directly incorporated on a HFDPS following sequential co-transfer scheme.

Hence, in the following section some of the performance requirements from the data transmission protocol that is to be implemented in a sequential co-transfer scheme for HF power and data transfer are outlined:

- *Data Packet Size:*

In an HFDPS implementing a sequential co-transfer scheme for HF power and data transfer, information exchange between the data nodes is mainly limited to system state variables, status messages or load or source requirement. Most of the times this information is in the order of few bits and is relatively smaller as compared to the data size available in conventional data protocols used for simultaneous data transfer. Hence, a data protocol with a small number of data bits and low data overhead requirements can be a good fit for such a scheme.

- *Disturbance Rejection:*

The occurrence of HF power switching in the SPES and LPES and the non-ideal nature of the switching devices that are used as the transfer switches make the HF channel susceptible to noise even when HF power is not being transferred through it. This transition noise can corrupt the low-voltage data signals that are exchanged between the data nodes through the HF channel. Thus, the data protocol designed for the sequential co-transfer should have additional information in the form of data bits that can be used for ensuring data correctness upon reception.

1. Data-Transfer Protocol

As stated above, one of the foremost requirements for the data transfer protocol for sequential co-transfer is to have low frame size and a mechanism to identify corrupted data frames. Asynchronous SCI protocol with the data frame shown in Figure 23 emerges as a possible candidate for this application. SCI operates in a non-return-to-zero (NRZ) format and has a total of 11 bits in a single data frame. SCI data frame shown in Figure 23 contains one start bit, one to eight data bits (payload), an even/odd parity bit and a stop bit. SCI follows the asynchronous communication scheme, i.e. the clock for transmitter and receiver are generated locally. The SCI data receiver oversamples the received data using its local clock and the value of the data bit is decided based on the majority value of the sampled data bits in each sampling period [50]. Odd/even parity bit attached towards the end of the data frame is used to check the accuracy of the received data. However, due to the presence of impulsive HF channel noise more than one data bit can get corrupted during transmission. The parity check bit, which relies on the total sum of data bits value, might not solely be able to detect the data corruption. Hence an additional protection measure needs to be added to the existing SCI data frame.

Figure 23. Asynchronous SCI data frame format [30]**, ©2018 IEEE.**

To achieve more robust and reliable data transfer via the HF channel, two precursor signature bits along with the already available parity check bits are added to the SCI data frame. A total of 11 bits of data as shown in Figure 24,

comprising of one start, two signatures, six payload, one parity, and one stop bit are transmitted in every data packet. Upon reception, the received data is only considered valid when the signature bits match the pre-stored signature bits in the receiver unit.

Figure 24. Modified asynchronous SCI data frame format [30]**, ©2018 IEEE.**

2. Implementation of Data-Transmitter and Data-Receiver Circuit

To implement the modified SCI protocol, a simple data-transmitter circuit (Tx), as shown in Figure 25 is designed. An inverting gate-driver IC instead of a class B power amplifier as was used in [35] is employed to transmit the low voltage HF data signals on the HF channel. Inverting gate driver IC is chosen to make the idle state voltage of the SCI Tx channel output zero, which is high in normal condition. The gate driver IC receives data from the SCI module of the DSP through a digital-isolator interface and eliminates the need for any data-amplifier circuitry. An inverting gate-driver IC (IXDI609SIA), with a maximum propagation delay of 60 ns, is chosen and its output voltage peak is fixed at 5 V. A 5 V (0 V) on the gate-driver output corresponds to 0 (1) bit value of digital data bit being transmitted by the SCI module of the DSP.

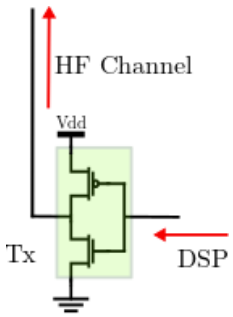


Figure 25. Inverting gate-driver IC is used as the data transmitter. Low voltage binary data is received from the DSP and amplified to a higher-voltage high-current signal for being transmitted through the HF channel.

A simple resistive data-receiver circuit (Rx) as shown in Figure 26 is designed to recover the transmitted data signals on the HF channel. The output of Rx is first fed to a logic inverter to recover the transmitted data, which is then fed to the SCI module of the DSP through a digital-isolator interface. Values of R_1 and R_2 in the Rx circuit can be chosen based on the signal strength of data signals being transmitted over the HF channel.

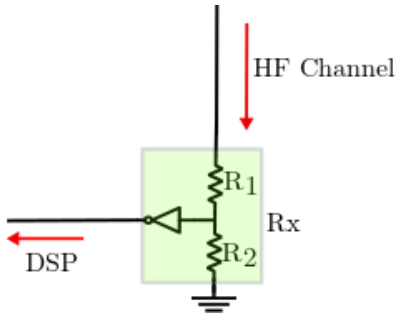


Figure 26. Design of a simple resistive data-receiver circuit being implemented to sense the data frame transferred over the HF channel. Sensed data is transmitted to the *DSP* SCI RX channel for further processing.

Additionally, a CMOS based SPDT switch is used for switching between the Tx and Rx functionality. A combination of SPDT switch, Tx and Rx circuits constitutes a data node. Depending on the required data node configuration, SPDT switch receives an input from a DSP and connects the Rx or Tx circuit to the HF channel through the data switch, as will be illustrated in Figure 28.

D. Case I: Implementation of a SISO HFDPS

Block diagram representation of a SISO HFDPS following the proposed sequential co-transfer scheme is provided in Figure 27. In the SISO HFDPS shown, a single SPES is connected to a single LPES over the HF channel which doubles as a data-link for data exchange when not in use for the HF power packet transmission. In Figure 27, S_{1PS} (S_{1PL}) and S_{1DS} (S_{1DL}) serve as the network switches at the source- (load-) end. Power nodes PN_{1S} (PN_{1L}) and its corresponding data node DN_{1S} (DN_{1L}) are connected to the HF channel using the transfer switch S_{1PS} (S_{1PL}) and the data switch S_{1DS} (S_{1DL}). Transfer and data switches are modulated in a mutually exclusive manner, such that at any given time either the power nodes (PN_{1S} and PN_{1L}) or the data nodes (DN_{1S} and DN_{1L}) have access to the HF channel. In Figure 27, power node PN_{1S} serves as the SPES and transmits HF power packets on the HF channel when the

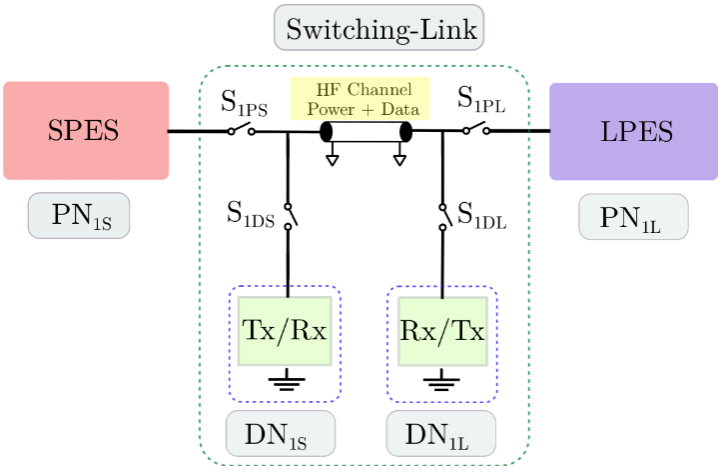


Figure 27. Block diagram of a single transmitting and receiving node forming a SISO HFDPS. Here, SPES and LPES represents a power transmitter (PN_{1S}) and receiver (PN_{1L}), respectively. Data transmission nodes corresponding to SPES and LPES are marked as DN_{1S} and DN_{1L}, respectively.

transfer switch S_{1PS} is turned ON. Data node DN_{1S} works as the corresponding data node to PN_{1S} and transmits/ receives data through the HF channel when S_{1DS} is turned ON. Power nodes PN_{1L} serves as the LPES and receive HF power packets transmitted by PN_{1S} on the HF channel when its corresponding transfer switch S_{1PL} is turned ON.

1. Circuit Realization of a SISO HFDPS Feeding dc Load

Using the designed SPES and LPES, a schematic representation of the SISO HFDPS following the proposed sequential co-transfer scheme is provided in Figure 28. As can be gathered from Figure 28, power nodes PN_{1S} and PN_{1L} and data nodes DN_{1S} and DN_{1L} are connected to the HF channel using transfer switches (S_{1PS} and S_{1PL}), and data switches (S_{1DS} and S_{1DL}), respectively. Both the transmitter and receiver side power and data nodes have separate digital controllers DSP_1 and DSP_2, respectively. When working together coded data is sent to DN_{1L}, by DSP_2, which is synchronized to DSP_1 using a centralized clock and provides the gating signals for S_{1PL}, S_{1DL}, and S_2. DSP_1 decodes the received data on DN_{1S} and provides the gating signals for S_1, S_{1DS}, and S_{1PS}.

Timing diagram and modes of operation of the SISO HFDPS following sequential co-transfer scheme are provided in Figure 29 - Figure 31. As shown in Figure 30, during mode-1 when switch S_1 is turned ON, current in the input inductor of SPES "L_1" starts building as it is directly connected across the input supply voltage "V_{in}". Transfer

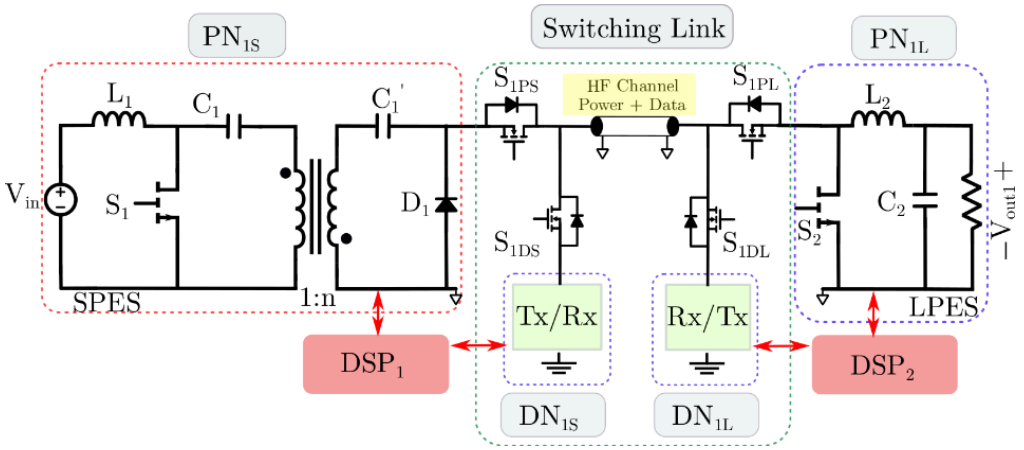


Figure 28. A schematic representation of the SISO HFDPS, showing PN_{1S}, PN_{1L}, DN_{1S}, DN_{1L}, and the HF channel. DSP_1 (DSP_2) coordinates locally with PN_{1S} (PN_{1L}) for gating and feedback signals, DN_{1S} (DN_{1L}) regarding data communication and switching link regarding sequential power and data co-transmission.

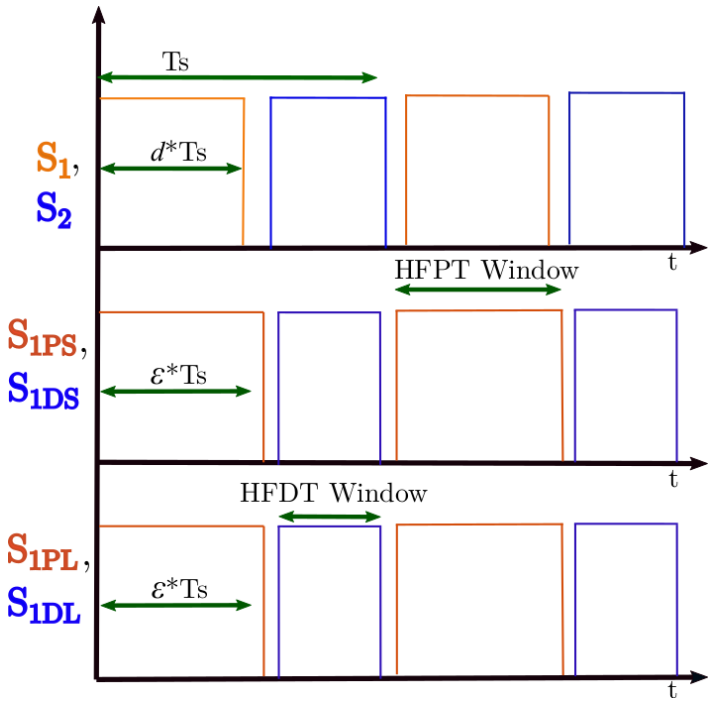


Figure 29. A timing diagram for the SPES and LPES. It is noted that all the switches in SPES and LPES are synchronized to a common clock.

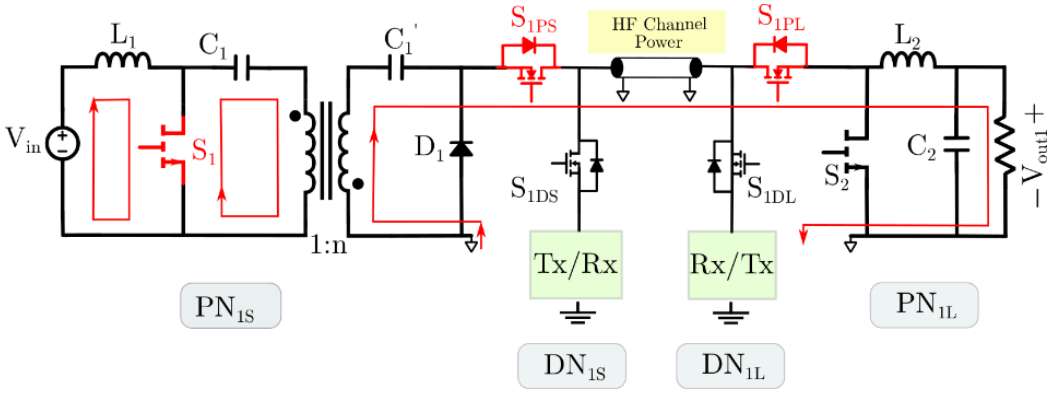


Figure 30. Mode-1, during this mode of operation HF channel is used for HF power packet transmission.

switches S_{1PS} and S_{1PL} are synchronized with the power switch S_1 of PN_{1S} and are turned ON during mode-1. This connects the power nodes PN_{1S} and PN_{1L} to the HF channel and allows the transfer of a HF power packet in the form of load current supported by the blocking capacitors C_1 and C_1'. During mode-1, data switches S_{1DS} and S_{1DL} in switching-link are turned OFF for isolating the data nodes from the HF channel. If we consider d to be the duty cycle of the SPES and d' (d' = 1- d) of the LPES and T_S be the total time for a single switching cycle, then, $d * T_S$ is the total conduction time for the switch S_1 and it governs the size of the HF power packet generated by SPES. In the timing diagram provided in Figure 29, the switching signals during mode-1 are marked as the HF power transfer (HFPT) window.

It is noted that during mode-1, although the transfer switches are synchronized to S_1 an additional duty cycle δ is added to the transfer switches to provide a conducting path for the transformer leakage current that flows through S_{1PS} and S_{1PL} to the load, when S_1 is turned OFF. The value of δ depends on the stored leakage energy in the HF transformer which is in turn related to the power requirement of the load. In the timing diagram provided in Figure 29, the duration for which transfer switches are turned ON is marked as $\varepsilon * T_S$, where $\varepsilon = d + \delta$.

Next mode of operation starts when the switch S_1 in PN_{1S} is turned-off. During this mode of operation (shown in Figure 31), the energy stored in the input inductor L_1 of SPES is used to charge the blocking capacitors C_1 and C_1' and the load is fed from the energy stored in the output inductor L_2 located in PN_{1L}. Transfer switches S_{1PS} and S_{1PL} are turned OFF, disconnecting the power nodes from the HF channel. Further, it is during mode-2 that the data nodes

DN_{1S} and DN_{1L} are connected through the HF channel using data switches S_{1DS} and S_{1DL}. This creates a dedicated channel for data exchange between the data nodes as is shown in Figure 31. In the timing diagram provided in Figure 29, the switching signals during this mode of operation are marked as the HF data transfer (HFDT) window. A consolidated view of the switch states of various switches and HF channel utilization during mode-1 and mode-2 of the designed SISO HFDPS are captured in Table I.

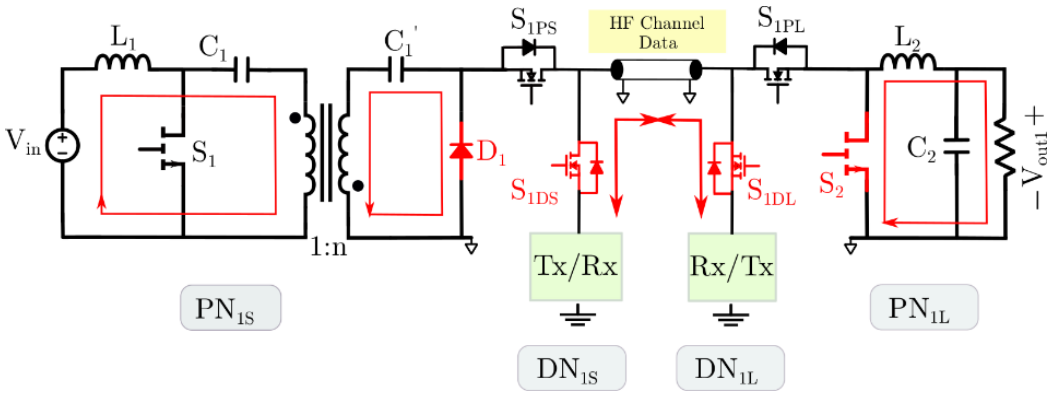


Figure 31. Mode-2, during this mode of operation HF channel is used for data transmission

Table I. Switch states of various switches in a SISO HFDPS following sequential co-transfer scheme.

HF Channel	***Mode***	***S_1, S_{1PS}***	***S_{1DS}, S_{1DL}***	***S_{1PL}***	***S_2***
Power-PN_{1L}	Mode-1	1	0	1	0
Data	Mode-2	0	1	0	1

Finally, it can be concluded that when transfer switches S_{1PS} and S_{1PL} are active, HF power packet is transferred from the SPES to the LPES. For the remaining switching-cycle time (T_S), the HF channel is available for data transmission, which is enabled by turning ON the data transfer switches S_{1DS} and S_{1DL} as illustrated in Figure 29. The durations for power and data transmissions depend on the value of d. If a low (high) output voltage is required by the

load, a low (high) d is needed and hence, the time duration available for the data transmission in T_S is increased (decreased). However, when d is high (high output voltage required by the load), for a given channel capacity, communication speed can be increased to enhance data baud rate. Moreover, duty cycle information can be used to realize need-based power delivery in a SISO HFDPS following sequential co-transfer scheme. A closed-loop system can be designed to generate the required duty cycle in DSP_2 as per load demand. Then using the data nodes, this demand can be transferred to DSP_1 which can further control the size of the HF power packet as per the requested duty cycle by the load.

E. Case II: Implementation of a SIMO HFDPS

In a SIMO HFDPS following the proposed sequential co-transfer scheme, a single SPES is connected to multiple LPESs over a common HF channel. This requires routing of HF power packets to various LPESs in addition to the ability to adjust HF power packet size as per load demand. In Figure 32, block diagram representation of one such SIMO HFDPS with a single SPES and m $(m \in I)$ LPESs connected on a common HF channel is outlined. Power nodes PN_{1S}, PN_{1L}, PN_{2L}, … PN_{mL} and data nodes DN_{1S}, DN_{1L}, DN_{2L}, … DN_{mL} are connected to the HF channel using transfer switches S_{1PS}, S_{1PL}, S_{2PL}, … S_{mPL} and data switches S_{1DS}, S_{1DL}, S_{2DL}, … S_{mDL}, respectively. As was the case in a SISO HFDPS, in a SIMO HFDPS transfer switches and data switches are modulated in a mutually exclusive manner, such that at any given time either the power nodes or the data nodes have access to the HF channel. In Figure 32, power node PN_{1S} serves as the SPES and transmits HF power packets on the HF channel when the transfer switch S_{1PS} is turned ON. Data node DN_{1S} works as the data node for PN_{1S} and transmits/receives data through the HF channel when S_{1DS} is turned ON. Power nodes PN_{1L}- PN_{mL} serves as the LPESs and receive HF power packets transmitted by PN_{1S} on the HF channel when their corresponding transfer switch S_{1PL}- S_{mPL} are turned ON. Data nodes DN_{1L}- DN_{mL} works as the data node for PN_{1L}- PN_{mL} and transmits or receives data through the HF channel when data switch S_{1DL}- S_{mDL} are turned ON. Each power node (either transmitter or receiver), its data node, and their corresponding transfer and data switches are controlled using a single digital controller. Same digital controller also interacts with the data node for transmitting and receiving modified SCI data frames.

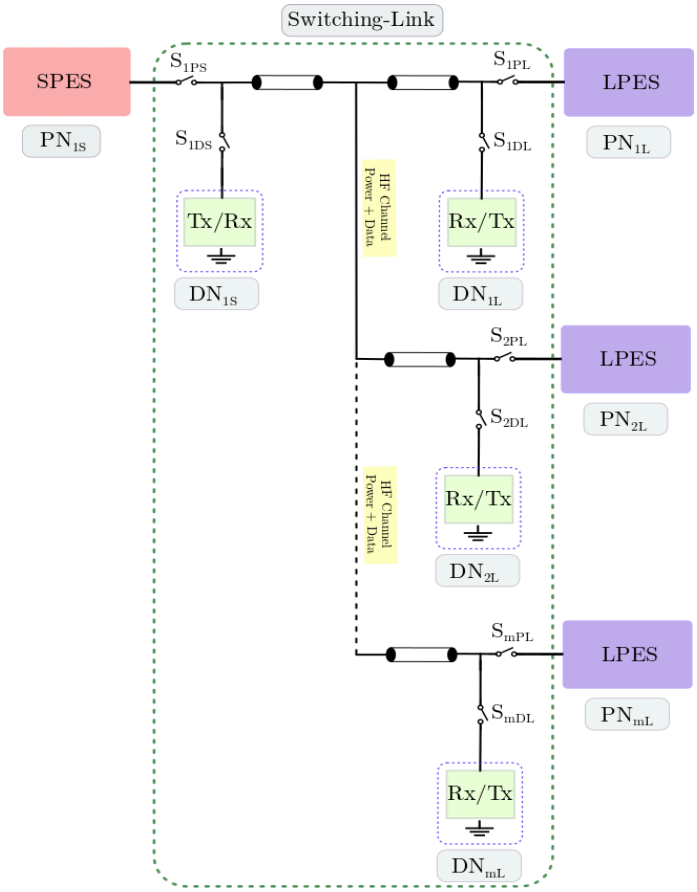


Figure 32. Block diagram representation of a single power transmitter and multiple power receiver nodes forming a SIMO HFDPS. SPES and LPES represents a power transmitter (PN_{1S}) and receiver nodes ($PN_{1L}, PN_{2L} \dots PN_{mL}$), respectively. Source side and load side data nodes are marked as DN_{1S} and $DN_{1L}..DN_{mL}$.

1. HF Channel Access Protocol

In a SISO HFDPS, HF power (data) packets generated at the power (data) transmitter node were directly transferred to the power (data) receiver node through the HF channel. However, in case of a SIMO HFDPS, a single power (data) transmitter node may need to generate HF power (data) packets for multiple receiver nodes connected on the HF channel. Depending on the required functionality and HFDPS conditions, these power and data nodes can access the HF channel based on various media access control (MAC) protocols designed for the modern communication system [51]. An optimal packetized power dispatching protocol for a local area packetized power network has been designed in [52], [53]. In [41], [54], authors have used time division multiplexing (TDM) for

demonstrating the feasibility of power packet dispatching in an in-home dc distribution network. Additionally, advanced protocols for power packet dispatch based on load demand optimization have been outlined in [14], [42].

In this dissertation for demonstrating the feasibility of the sequential co-transfer scheme in a SIMO HFDPS, TDM with equal time slots is utilized. Use of TDM enables the realization of a SIMO HFDPS as multiple SISO HFDPS with a single transmitter feeding multiple receivers in a sequential manner. Using TDM, HF power packets can be routed to several power receiver nodes from a single power transmitter node by allocating fixed time slots during which a power receiver and transmitter node can access the HF channel. All the data nodes can be configured to access the HF channel for exchanging control/status information when it is not being used for HF power transfer.

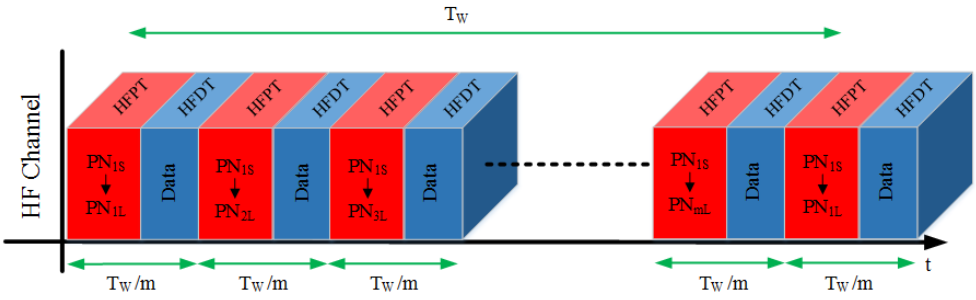


Figure 33. The TDM frame structure for the sequential co-transfer of power and data signal over a common HF channel in a SIMO HFDPS. For transferring power packets to m power receiver nodes, TDM frame is divided into m equal sub-intervals which are further divide in HFPT and HFDT windows.

An illustration of the TDM protocol that can be used for the designed SIMO HFDPS following sequential co-transfer scheme is outlined in Figure 33. PN_{1S} serves as the power transmitting node and transfers power packets to PN_{1L}, PN_{2L}, … PN_{mL} in a sequential manner. T_W represents the time duration of one complete TDM frame. For transferring HF power packets to m receiver nodes, T_W is sub-divided in m equal time slots each with a time duration of T_W/m. Each time slot is further sub-divided in HFPT and HFDT windows. HF power packets are only transferred on the HF channel during the HFPT window and data packets are only transferred during the HFDT window. Same as a SISO HFDPS, in a SIMO HFDPS, HFPT and HFDT windows do not overlap each other.

While the minimum time that can be allocated for the HFPT window depends on the size of the HF power packet

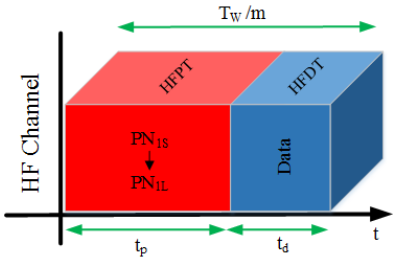


Figure 34. A single time slot of the TDM frame designed for feeding m power receiver nodes in a SIMO HFDPS. Each time-slot is further sub-divided in HFPT and HFDT windows having time durations t_p and t_d, respectively.

requested by the load, the time allocated for the HFDT window can be fixed or variable. In Figure 34, a single time slot of the TDM frame outlined in Figure 33 is shown. During this time slot, the HF power packet is routed from PN_{1S} to PN_{1L} and depending on the communication scheme used data packet can be exchanged between the data nodes. In Figure 34, t_p and t_d represents the time allocated for HFPT and HFDT windows, respectively. Minimum duration of t_d depends on the minimum time required for transmitting a complete modified SCI data frame on the HF channel and this duration is independent of the duration of t_p. However, the duration of t_d limits the maximum time available for HFPT window in a single time slot.

In Figure 33, during the HFPT window of the first time slot, transfer switches S_{1PS} and S_{1PL} (shown in Figure 32) are turned ON and the HF channel is accessed by the power transmitter node PN_{1S} and the power receiver node PN_{1L}. All other transfer and data switches in the switching link are in their OFF state. It is during this interval HF power packet generated by PN_{1S} are routed to PN_{1L} depending on its requirements/status that can be provided to the digital controller of PN_{1S} during the previous HFDT window. Next, during the HFDT window of the first time slot, all the power switches in the switching link are turned OFF and data switches are turned ON. During this interval requirements/status of the next in line power node (PN_{2L}) can be provided to the controller of PN_{1S}. This process is repeated for all the power nodes connected in the SIMO HFDPS based on their position in the TDM frame.

2. Circuit Realization of a SIMO HFDPS Feeding Multiple dc Loads

Using the designed SPES and LPES, a case illustration for a SIMO HFDPS with a single SPES and two LPESs is shown in Figure 35. In Figure 35, PN_{1S} serves as the SPES and PN_{1L} and PN_{2L} serve as the two LPESs. Power nodes

PN_{1S}, PN_{1L}, and PN_{2L} and data nodes DN_{1S}, DN_{1L} and DN_{2L} are connected to the HF channel using transfer switches S_{1PS}, S_{1PL}, and S_{2PL} and data switches S_{1DS}, S_{1DL}, and S_{2DL}, respectively. Consistent with a SISO HFDPS, in a SIMO HFDPS following sequential co-transfer scheme, transfer and data switches are operated in a mutually exclusive manner. Each combination of a power node and its corresponding data node is managed using a separate digital controller. In Figure 35, DSP_1 coordinates locally with PN_{1S} for gating signals and feedback signals, DN_{1S} regarding data communication and mode selection and switching-link regarding sequential power and data co-transmission. Similar roles are performed by DSP_2 and DSP_3 for power node PN_{1L} and PN_{2L}, data node DN_{1L} and DN_{2L}, and the switching-link. When working together, coded data is exchanged between the data nodes, and power packets generated by PN_{1S} are routed to PN_{1L} and PN_{2L} following TDM as was outlined in the previous section.

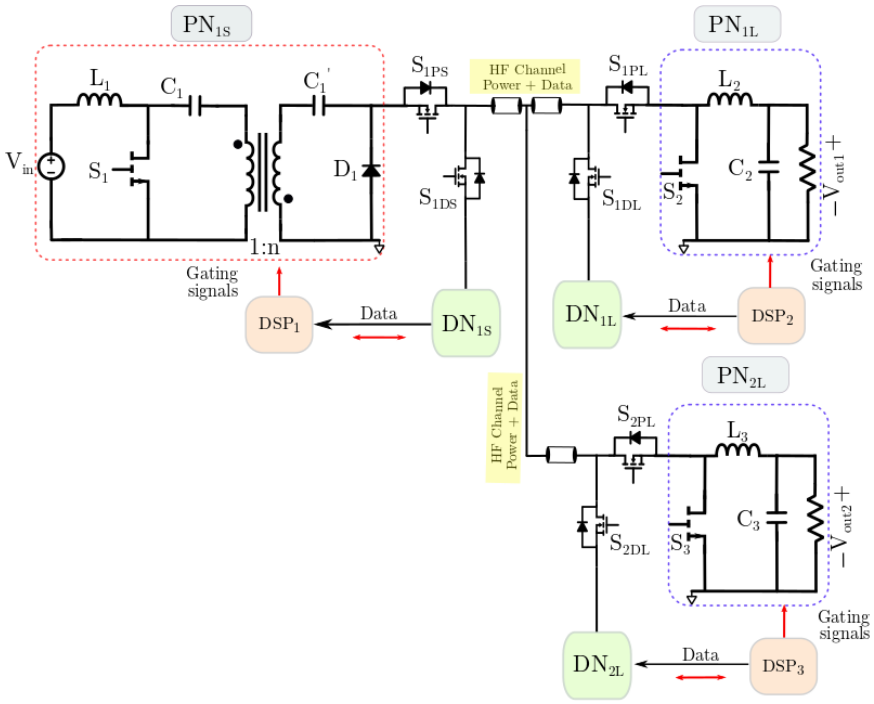


Figure 35. Schematic representation of a SIMO HFDPS, with power nodes PN_{1S}, PN_{1L}, and PN_{2L}, data nodes DN_{1S}, DN_{1L}, and DN_{2L}, and the HF channel.

Timing diagram and modes of operation of the SIMO HFDPS shown in Figure 35 following TDM, are provided in Figure 36 - Figure 39. In Figure 36, T_w represents the time duration of a TDM frame required for routing HF power and data packets in the designed SIMO HFDPS. Since in the designed SIMO HFDPS, HF power packet needs to be

routed to the two LPES, the TDM frame is sub-divided in two equal time slots each with a duration of $T_w/2$ as is shown in Figure 36. During the time interval t_0 - t_1 in Figure 36, the HF power packet is routed from PN_{1S} to PN_{1L} and during the time interval t_2 - t_3, HF power packet is routed from PN_{1S} to PN_{2L}, these durations are marked as HFPT PN_{1L} and HFPT PN_{2L}, respectively . The HF channel is available for data transferred during the time intervals t_1 - t_2 and t_3 - t_4, these durations are marked as HFDT. Additionally, in Figure 36, α_1 and α_2 are the time allocation values requested by the load and determine the size of the HF power packet generated by the power transmitter node. Since, T_W is the total time required for completing a full HF power and data transfer cycle for the designed SIMO HFDPS, it also represents the switching cycle time for all the power nodes in which they need to achieve their inductor charge balance and capacitor voltage balance for ensuring a stable steady state operation.

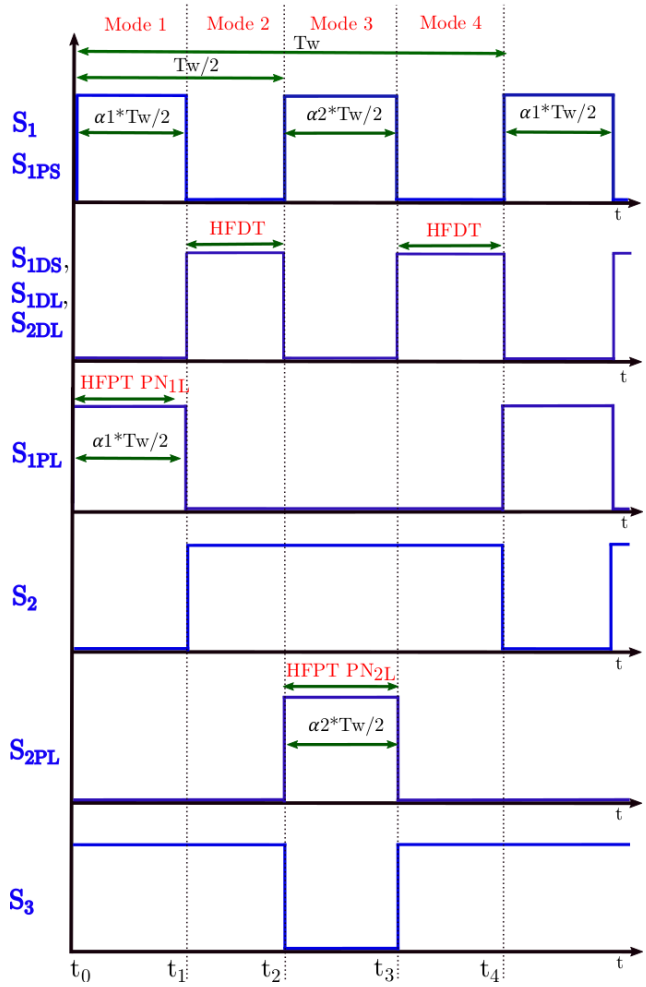


Figure 36. A timing diagram for the SIMO HFDPS shown in Figure 35.

The modes of operation of the SIMO HFDPS following sequential co-transfer scheme are shown in Figure 37-Figure 39. As can be deduced, during each time slot of the TDM frame, SIMO HFDPS follow the same modes of operation as a SISO HFDPS. However, HF power packets are routed to different LPESs in different time slots. Size of the HF power packet depends on the load requirement that is communicated using the data nodes. More details about the modes of operation, state equations, and dependence of output voltage on the time allocation value (size of HF power packet) are provided in Appendix B.

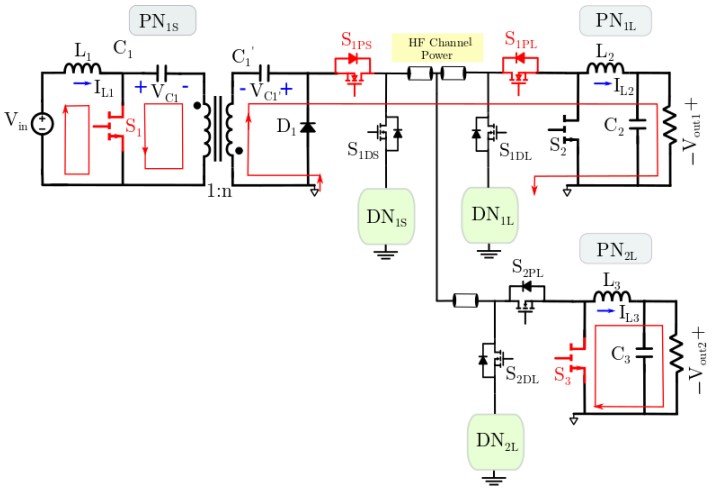


Figure 37. Mode-1 (t_0 - t_1), during this mode HF power packets are routed from PN_{1S} to PN_{1L} through the HF channel.

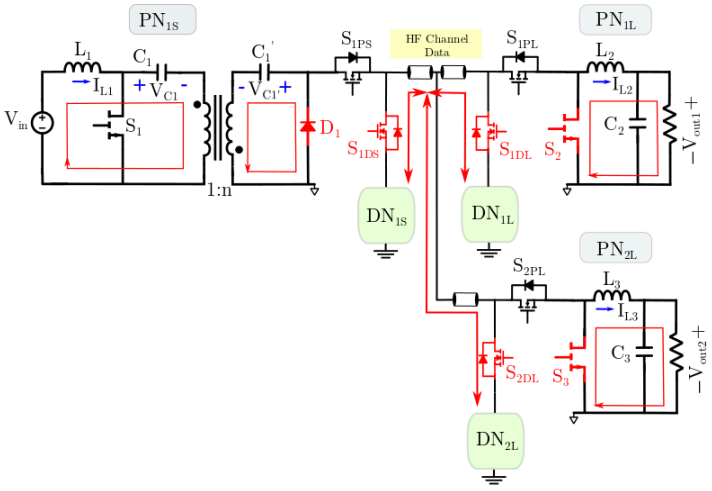


Figure 38. Mode-2 (t_1 - t_2) and mode-4 (t_3 - t_4), during these modes of operation, HF channel is used for the exchange of data between the data nodes.

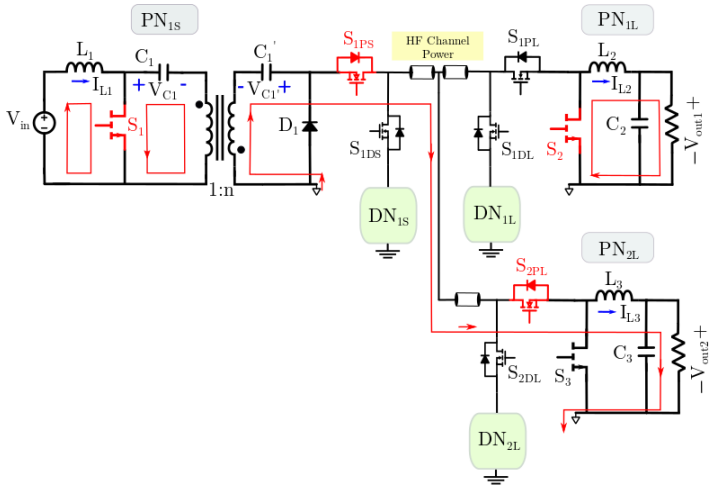


Figure 39. Mode-3 (t_2 - t_3), during this mode HF power packets are routed from PN_{1S} to PN_{2L} through the HF channel.

Table II provides a consolidated view at the switch states of various switches and the HF channel utilization in the four modes of operation of the designed SIMO HFDPS following TDM. In Table II, ON state of a switch is referred to as "1" and the OFF state is referred to as "0". During mode-1 and mode-3 HF channel is used for the transfer of HF power packet and in mode-2 and mode-4 the HF channel is made available for data transfer.

Table II. Switch states of various switches in the SIMO HFDPS following sequential co-transfer scheme.

HF Channel	***Mode***	***S_1, S_{1PS}***	***S_{1DS}, S_{1DL}, S_{2DL}***	***S_{1PL}***	***S_2***	***S_{2PL}***	***S_3***
Power-PN_{1L}	Mode-1	1	0	1	0	0	1
Data	Mode-2	0	1	0	1	0	1
Power-PN_{2L}	Mode-3	1	0	0	1	1	0
Data	Mode-4	0	1	0	1	0	1

3. Circuit Realization of a SIMO HFDPS Feeding ac Load

The proposed sequential co-transfer scheme provides a mechanism for transferring HF power and data packets over a common HF channel in a mutually exclusive manner. A SISO and a SIMO HFDPS following the sequential

co-transfer scheme have been illustrated, in Figure 28 and Figure 35, respectively, that generates dc voltage at the load terminal. If the two power receiver nodes of the designed SIMO HFDPS are in close vicinity, it can be used for realizing a dc/ac operation by suitably routing and adjusting the size of the HF power packets as per load demand. Figure 40 illustrates the use of a SIMO HFDPS with a single power transmitter and two power receiver nodes for realizing a dc/ac operation.

In Figure 40, dc input supply (V_{in}) is connected to PN_{1S} and the load is connected differentially across the power nodes PN_{1L} and PN_{2L}. Power nodes PN_{1S}, PN_{1L} and PN_{2L} are physically separated and are connected through the switching-link that houses the HF channel, data nodes (DN_{1S}, DN_{1L}, and DN_{2L}), transfer switches (S_{1PS}, S_{1PL}, and S_{2PL}), and data switches (S_{1DS}, S_{1DL}, and S_{2DL}). Data switches S_{1DS}, S_{1DL}, and S_{2DL}, switch in a complementary manner to S_1, while the operation of S_{1PS} is synchronized to S_1. Receiver-end transfer switches S_{1PL} and S_{2PL}, are operated complimentary to their respective power switches S_2 and S_3 of power nodes PN_{1L} and PN_{2L}, respectively. HF power packet are transferred on the HF channel during the HFPT window, during this window all the data switches are in their OFF state. Similarly, data packets are transferred on the HF channel during the HFDT window when all the transfer switches are in their OFF state.

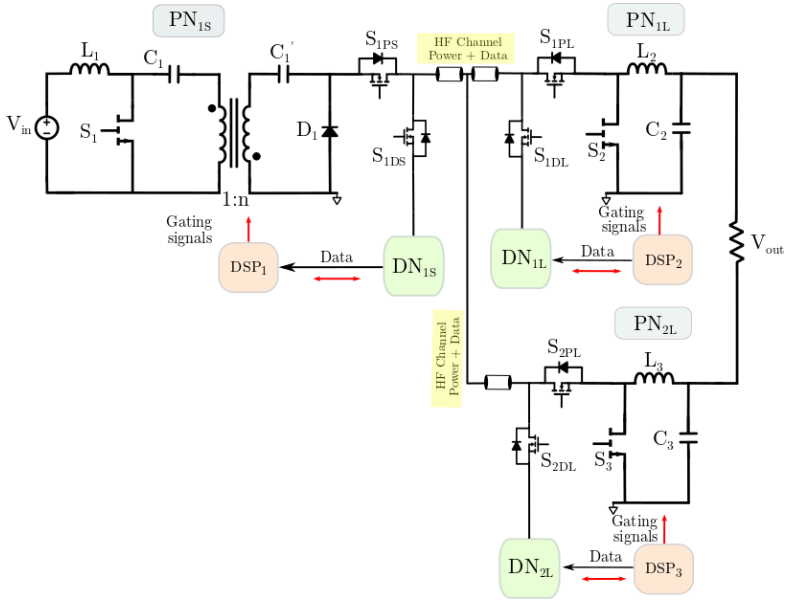


Figure 40. Illustration of the SIMO HFDPS in a dc/ac mode of operation. The designed SIMO HFDPS consists of one power transmitter (PN_{1S}) and two power receiver nodes (PN_{1L} and PN_{2L}) connected over a HF channel.

To enable the dc/ac operation, topological switching is considered for the designed SIMO HFDPS in Figure 40. In topological switching, each power receiver node is active for one-half of the fundamental line cycle [55]. The modulation scheme used for the power receiver nodes in SIMO HFDPS follows discontinuous modulation scheme (DMS) proposed for differential mode Ćuk Inverter (DMCI) in [55]. With reference to Figure 40, DMS for the designed SIMO HFDPS can be quantified as follows. For the positive-half of the sinusoidal output voltage, HF power packets are routed from PN_{1S} to PN_{1L} through the HF channel during the HFPT window. The required time allocation value for each HF power packet during this duration is generated by DSP_2 and is exchanged between DN_{1S}, DN_{1L} and DN_{2L} during HFDT window, such that half-sinusoidal unipolar voltage is generated at the output of PN_{1L}. Based on

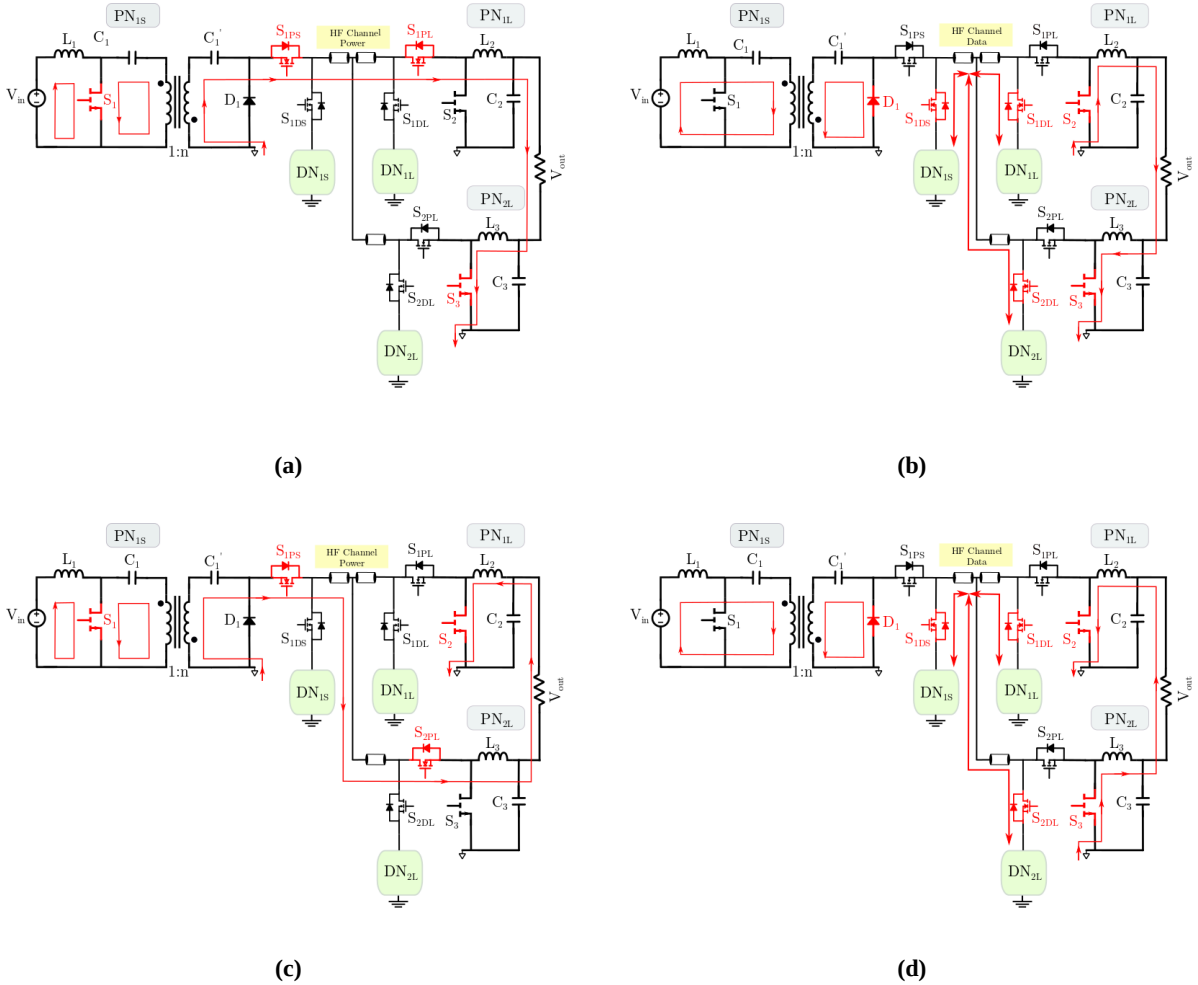


Figure 41. Modes of operation of the SIMO HFDPS in a dc/ac operation. During positive-half of the line cycle SIMO HFDPS follows (a) mode-1 (b) mode-2, and during negative-half of the line cycle, it follows (c) mode-3 and (d) mode-4.

the received data at DN_{2L}, during this duration, the power switch S_3 in PN_{2L} is in its ON state and results in the production of zero voltage at its output of PN_{2L}. Similarly, during the negative-half cycle, HF power packets are routed from PN_{1S} to PN_{2L} through the HF channel to realize the necessary output voltage. During this period, PN_{1L} is operated with S_2 permanently in its ON state, to produce zero output voltage in PN_{1L}. Modes of operation of the designed SIMO HFDS in a dc/ac operation are provided in Figure 41, SIMO HFDS follows mode-1 and mode-2 during the positive-half of the line cycle and mode-3 and mode-4 during the negative half of the line cycle. As can be observed, the modes of operation of the designed SIMO HFDPS in Figure 41 matches the modes of operation of DMCI operated using a DMS [55]. However, in the designed SIMO HFDPS, because of the use of transfer switches for routing the HF power packets generated at PN_{1S} to PN_{1L} and PN_{2L}, need for an additional power transmitter node is avoided. This results in an increased utilization factor of the circuit components in the power transmitter node while achieving the same advantages as the conventional DMCI topology. Details about the modes of operation and reference modulation signals for PN_{1L} and PN_{2L} are provided in Appendix C.

F. Resolving Practical Design Issues in SPES and LPES

As discussed, in the proposed sequential co-transmission scheme, power and data paths through the HF channel are decoupled. This eliminated the impact of one on the other in an ideal scenario. However, efficient and reliable transfer of HF power packet across the HF channel necessitates proper design of the SPES and LPES where these HF power packets are generated and received, respectively. The SPES and LPES seldom consist of high-frequency wide bandgap (WBG) devices having rapid switching transitions and operated at extremely high-frequencies which aggravates reliable PES communication and hence, global operation. The ever-evolving fast switching transitions of the semiconductor devices that can result in increased PES efficiency and power density necessitates strict PES design principles in terms of power and gate circuit designs. Poor PES design guidelines may lead to sustained HF oscillations in both the source-end and load-end PES, resulting in their reflection on the HF channel bridging the LPES and SPES, deteriorating overall performance of the HFDPS.

In the current design revolving the present scenario, GaN-FETs governed by ultra-fast transitions and HF switching have been used to positively affect the efficiency, power density and specific weight of the LPES and SPES, which

will make even higher power translation of the described HFDPS feasible. However, the high slew rate of the GaN FETs coupled with its low device capacitance can excite resonance in the power electronics circuitry, causing large voltage spikes and electromagnetic interference (EMI) noise [56]–[60]. Additionally, having a low threshold voltage of around 1.4 V makes GaN-FETs more susceptible to false-triggering in case of oscillations in the gate driver circuit. Furthermore, the allowable gate-driving voltage range for GaN-FETs is small. For instance, the minimum gate drive voltage for complete channel formation in GaN Systems (GS66508P) is specified at 7 V, and the gate breakdown voltage is specified as 10 V, resulting in a very small allowable operating voltage range. Meeting such tight performance parameters requires special care while designing the PCB layouts for SPES and LPES and selecting power components that can work together and leverage on the advantages provided by the GaN-FETs.

In research, the presence of PCB parasitic track inductance has been identified as one of the prime cause for the generation of the HF noise in the GaN-based circuits [56], [58]. Thus, past work mainly focuses on PCB level optimization for achieving a reduced loop inductance and/or an improved gate-drive design [58]. However, it was observed that very limited work had been done to study the effects of the high slew rate of GaN-FETs on other circuit components. In the design process of GaN-FETs based SPES and LPES it was observed that the non-ideal behavior of the passive components and PCB parasitic affected the overall HF noise in the circuit. In lieu of that, in this section the HF noise issues related with the design of SPES and LPES utilizing GaN-FETs will be discussed and adequately tackled with efficient designs for the gate and power loops, so as not to perturb the HF channel negatively.

1. The Occurrence of HF Noise Due to PCB Layout

In a single transmitter and receiver node of an HFDPS, as shown in Figure 42, there are four main current loops comprising of parasitic inductances that may have a significant impact on the performance of the SPES and the LPES. The HF power loops in SPES are captured by $Loop_{P1}$ and $Loop_{P1}{}'$ and mainly comprise of the parasitic inductance between the blocking capacitor (C_1), GaN-FET (S_1), and HF transformer on primary and blocking capacitor (C_1'), diode, and HF transformer on the secondary. The gate driver loops are identified by $Loop_{G1}$ and $Loop_{G2}$ for the SPES and the LPES, respectively. These mostly include the parasitic inductance between the gate terminal of the device and the source terminal.

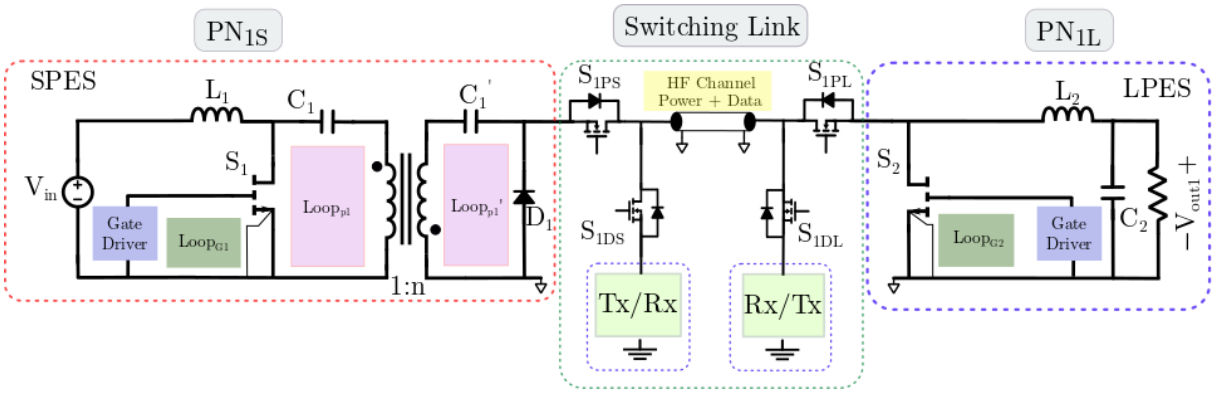


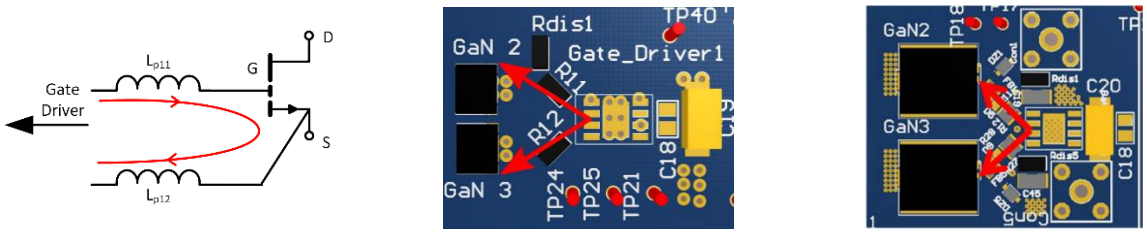
Figure 42. A single transmitter and receiver node of an HFDPS forming a SISO HFDPS, with marked gate loops $Loop_{G1}$ and $Loop_{G2}$ and HF power loops $Loop_{P1}$ and $Loop_{P1}{}'$.

In the past, the effect of parasitic inductance in the HF power loops $Loop_{P1}$ and $Loop_{P1}{}'$ have been extensively studied and given prime importance as it directly affects the switching transition voltage of the devices and limit their switching frequencies [61]–[63]. However, with the recent introduction of GaN-FETs, limiting the parasitic inductance in $Loop_{G1}$ and $Loop_{G2}$ has surfaced as a major concern [58]. This is primarily because of the low threshold and maximum allowable gate voltage for GaN-FETs. As compared to a conventional Si MOSFET, a typical GaN-FET has approximately 10 times lower difference between the optimal and maximum allowable gate voltage and about 4 times lower threshold voltage. This leaves a very limited margin for voltage oscillations in the gate-driver loop. So, if these gate oscillations are not controlled, they may lead to false turn ON of the GaN-FETs or can permanently damage them. Hence, one of the key objectives while designing a GaN-FET based SPES and LPES is to keep the parasitic inductance in the gate-driver loop minimum.

One way to limit this parasitic inductance in an HF circuit is to design a well laid out printed circuit board (PCB). Figure 43(a) shows the HF parasitic model of the gate-driver circuit with parasitic inductance in $Loop_{G1}$ marked as L_{p11} and L_{p12}. To capture the effect of gate-loop parasitic on the SPES and LPES, two different gate-driver PCB layouts were designed for the SPES and LPES employing GaN Systems GS66506T and GS66508P FETs as shown in Figure 43 (b) and Figure 43 (c), respectively. To achieve a better HF performance, in Figure 43(c) component placement is optimized such that, the distance between the gate driver output terminal and the gate terminal of the GaN-FET is minimized. This, along with the presence of Kelvin source in GS66508P, may help reduce parasitic

inductance in the driver loop considerably.

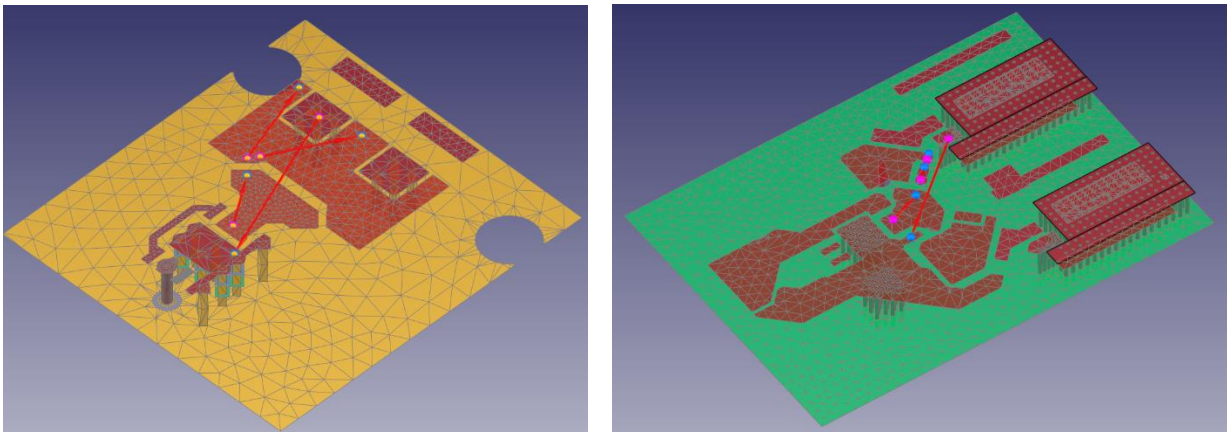
To get a measure on the circuit parasitic elements in the two designs, finite-element analysis-based design software EMCoS PCB VLab v.3.2 was employed. ODB++ PCB files generated using Altium Designer were directly loaded in the PCB VLab v3.2. Next, tracks between which parasitic elements were to be measured were defined in the software. Screen capture of the uploaded gate-driver PCB design files in PCB VLab v3.2 with the defined tracks is shown in Figure 44. Later, Rapid RLC solver included in the EMCoS PCB VLab package was used for calculating resistance, inductance and capacitance matrices from complex three-dimensional geometries. The lumped equivalent circuit files generated by the solver were then stored in SPICE format for further analysis.



(a) **(b)** **(c)**

Figure 43. Schematic drawing showing the location of HF parasitic inductance L_{p11} and L_{p12} in the gate driver loops $Loop_{G1}$ and $Loop_{G2}$ of the SPES and LPES, respectively. (b) Primary side gate driver PCB design for the SPES implemented using GaN Systems GS66506T and (c) GS66508P as the switching device. The direction of gate-driver current is marked in red during the event of turn on [56]**, ©2018 IEEE.**

Table III provides a measure of the PCB parasitic inductance in the two circuit layouts for the gate-driver as is shown in Figure 43 (b) and Figure 43 (c) at a switching frequency of 100 kHz. Further, Figure 45 provides its variation as a function of frequency signal varying between 100 kHz to 200 MHz. From Figure 45 it can be observed that, the minimum gate-loop parasitic inductance for SPES using GS66506T GaN-FET is about 9.65 nH at 200 MHz which is higher than the maximum parasitic inductance of the $Loop_{G1}$ using GaN Systems GS66508P FET. To further attenuate the high-frequency oscillations in the gate-driver loop for the SPES employing GS66508P GaN-FET, surface mounted ferrite beads were added before the gate terminal of the device.



(a) **(b)**

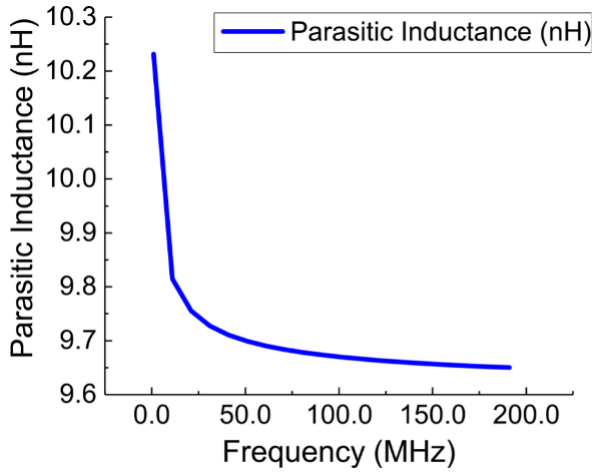
Figure 44. Imported PCB gate-driver layout in EMCoS PCB VLab v.3.2 with trace definition between which parasitic elements need to be measured for designs using (a) GS66506T and (b) GS66508P as the switching device [57]**, ©2017 IEEE.**

Further, the parallel operation of the GaN-FETs requires a carefully-designed PCB layout. As GaN-FETs can operate with a small rise and fall times of 3.7 ns and 5.2 ns, respectively, inter-trace signal delays can cause an imbalance in dynamic current sharing between the FETs connected in parallel [64]. To avoid this problem, driver-loop length to all the parallel FETs should be identical. Figure 43(b) and Figure 43 (c) outline the PCB layout designed for connecting 2 GaN-FETs in parallel.

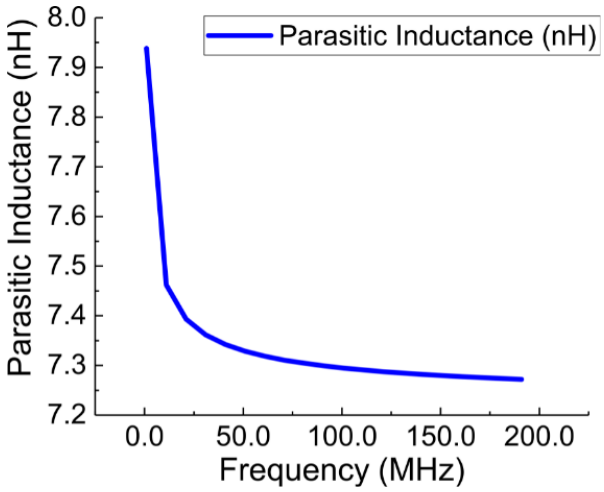
Since the switching-link design was not altered, the experimental result for demonstrating the effect of PCB layout was obtained on a non-distributed converter as is shown in Figure 20. Gate-to-source switching waveforms and corresponding drain-to-source voltage (V_{DS}) waveforms for the SPES employing GaN Systems GS66506T and

Table III. Parasitic inductance of the gate-driver circuit at the nominal switching frequency of 100 kHz.

Device	L_{p11}	L_{p12}
GS66506T	3.64 nH	6.58 nH
GS66508P	2.2 nH	5.92 nH



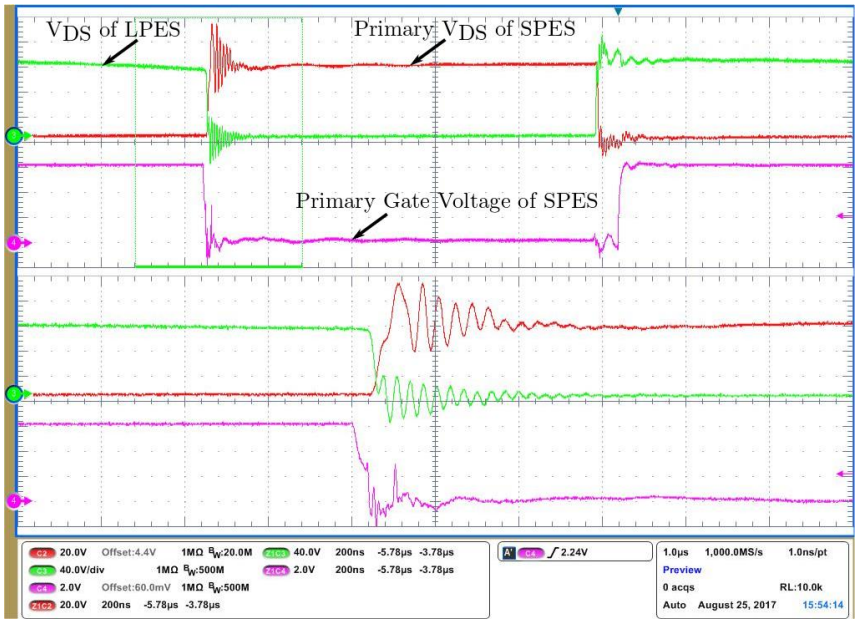
(a)



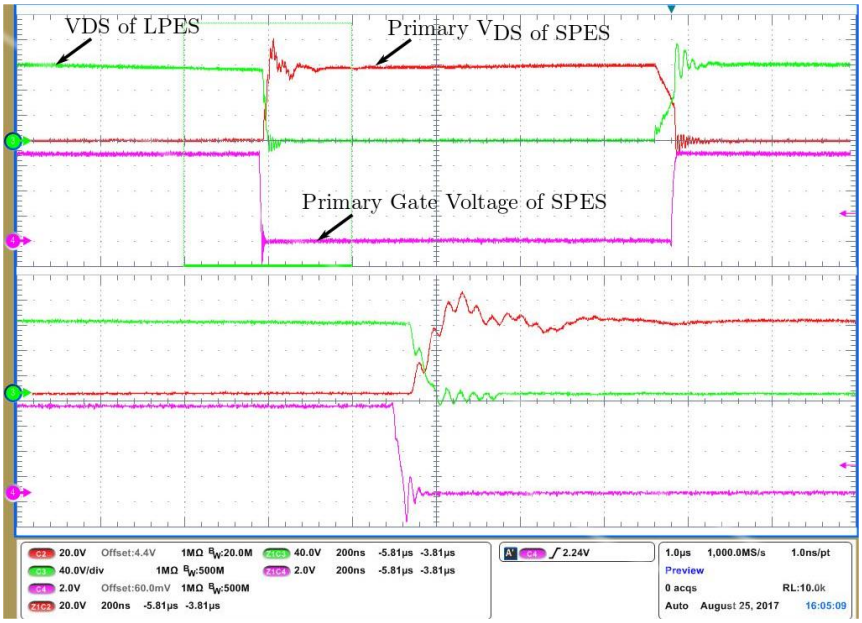
(b)

Figure 45. Simulation results showing the variation of PCB parasitic track inductance in SPES as a function of signal frequency in the $Loop_{G1}$ for a design using (a) GS66506T and (b) GS66508P as the GaN-FET [56]**, ©2018 IEEE.**

GS66508P GaN-FETs are provided in Figure 46 (a) and Figure 46 (b), respectively. The drain-to-source voltage waveform across S_2 in LPES has also been included in Figure 46. It can be seen from the experimental results that the oscillations in the gate-driver circuit are completely eliminated and the oscillations in V_{DS} waveforms are also minimized. It is noted that, along with the reduction in PCB parasitic inductance, use of Kelvin source on GaN Systems GS66508P and SMD ferrite beads helped in obtaining better results.



(a)



(b)

Figure 46. Primary side SPES switching waveform on Ch. 4 and SPES and LPES V_{DS} on Ch. 2 and Ch. 3, respectively, with a zoomed view, for the SPES and LPES PCB designs employing (a) GaN Systems GS66506T with gate loop parasitic inductance of 10.22 nH and (b) GaN Systems GS66508P with gate loop parasitic inductance of 8.12 nH.

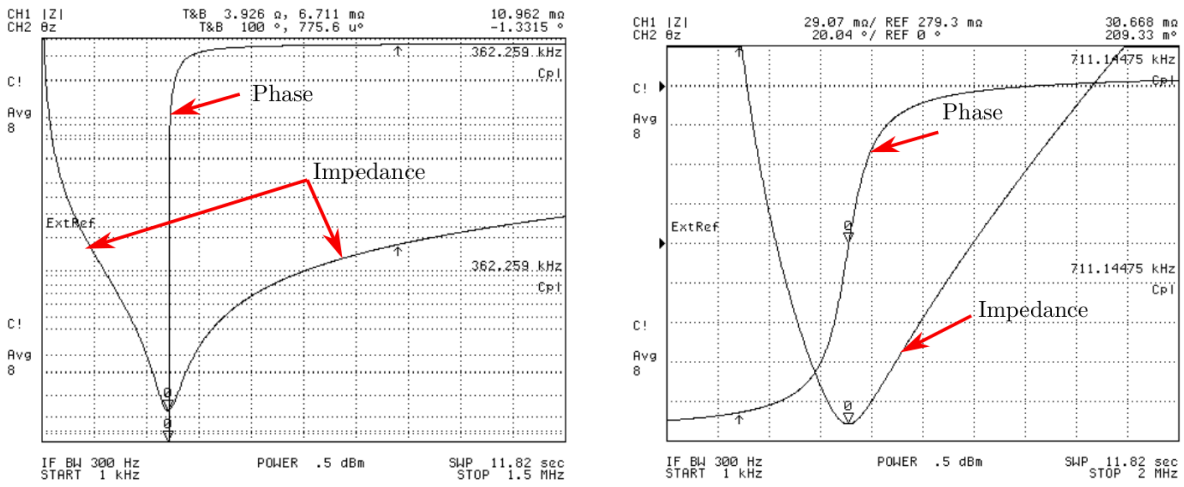
2. The Occurrence of HF Noise Due to High Slew Rate

The low output capacitance of the GaN-FET may undergo resonating interaction with the parasitic inductance present in the power loop $Loop_{P1}$ and $Loop_{P1}{}'$ of the SPES. This may lead to the generation of HF noise in the form of voltage oscillations across the FET drain and source terminals.

As stated earlier, parasitic inductance in the power loops $Loop_{P1}$ and $Loop_{P1}{}'$ of the SPES comprise primarily of the transformer leakage inductance, device package inductance, and parasitic inductance of the PCB traces. In addition to these, the non-ideal behavior of the primary (C_1) and secondary (C_1') blocking capacitors in the SPES also adds to the parasitic inductance present in the power loops. When a power semiconductor device in a PES undergoes HF switching, HF harmonics are generated, whose frequency depends on the slew-rate of the device. Even though most of its signal strength is concentrated near the device switching frequency, higher order sidebands constitute a considerable amount. When such a waveform with a high slew-rate is applied to a circuit constituting of the non-ideal passive circuit element, increased conductive EMI noise, and voltage oscillations may be observed.

As can be observed from Figure 42, HF power signals are present in the power loops $Loop_{P1}$ and $Loop_{P1}{}'$, which comprise of the blocking capacitors C_1 and $C_1{}'$, respectively. Owing to the fast energy capture and release capabilities required by the blocking capacitors, film capacitors with its self-healing ability is found to be a reasonable choice. Capacitor C_1 is chosen to be 6.8 μF (ECWF2685JA) while $C_1{}'$ is chosen to be 1.5 μF (B32674D4155K). Impedance response captured using Keysight 4395A impedance analyzer and 87512A transmission/reflection test set, for blocking capacitors C_1 and $C_1{}'$, are provided in Figure 47 (a) and Figure 47 (b), respectively.

Figure 47(a) and Figure 47 (b) shows that, the self-resonance frequency for C_1 and $C_1{}'$ are 362.25 kHz and 711.14 kHz, respectively. As these frequencies are close to the chosen switching frequency of 100 kHz, HF noise components of the switching voltage will encounter different circuit impedances than experienced by the switching frequency component. At the self-resonance frequency, C_1 and $C_1{}'$ behave as an ideal resistance, however, with the increased frequency they start showing inductive nature. This adds to the already present parasitic inductance in the power loops $Loop_{P1}$ and $Loop_{P1}{}'$ and leads to increased voltage oscillations and conductive EMI noise in the SPES. Voltage spectrum for a frequency range of 10 kHz to 10 MHz across C_1 is provided in Figure 48 (a). It can be observed



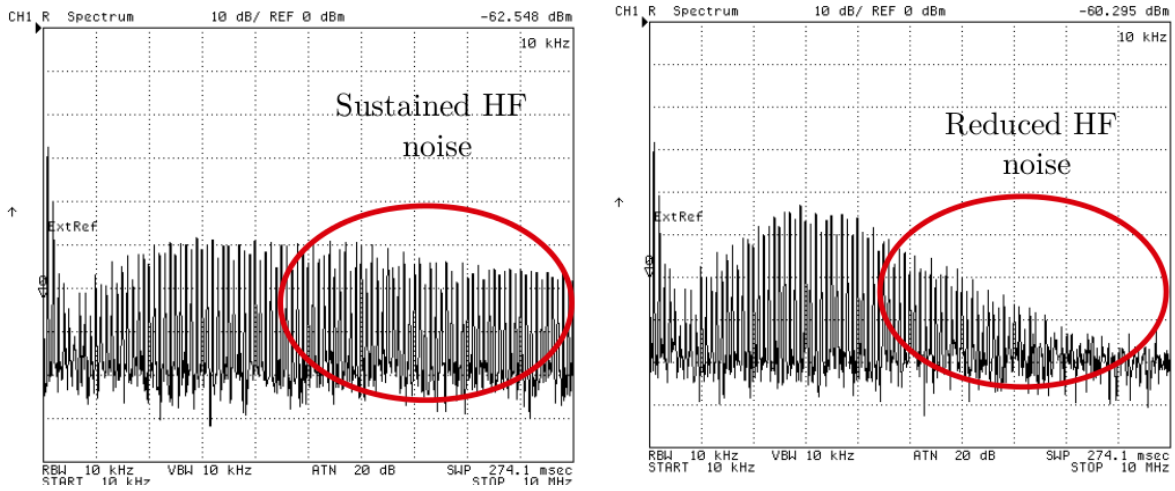
(a) **(b)**

Figure 47. Impedance magnitude and phase plot for (a) C_1 and (b) $C_1{}'$ [56], ©2018 IEEE.

that; the voltage spectrum comprises of a wide spectrum of HF noise and has its fundamental component (100 kHz) with the maximum amplitude.

A practical solution to this problem is to add an HF ceramic capacitor across the blocking capacitors in the SPES. This HF ceramic capacitor can ensure that a low impedance capacitive path is available to the HF noise components and can in-turn limit the parasitic inductance in the power loops. Adding a 0.2 μF HF ceramic capacitors in parallel to the blocking capacitors C_1 and $C_1{}'$ was found to be optimum in the experimental SPES circuit. Figure 48 (b) provides the spectrum of the voltage across the primary-side blocking capacitor, which now comprises a parallel combination of a film and ceramic capacitor. As is apparent in Figure 48 (b), the spectrum of the voltage across the blocking capacitor has a much lower amplitude for the HF noise as compared to Figure 48 (a). It is noted that, due to an increase in the effective inductive behavior of the combined capacitor for the mid-frequency range, a slight increase in the noise amplitude is observed. However, an overall reduction in the parasitic impedance in $Loop_{P1}$ and $Loop_{P1}{}'$ and conductive EMI noise is observed using this method.

In addition to the careful design practices required while using GaN FETs, the thermal design of a GaN-FET based PES needs special attention. GaN systems GaN_{PX} package offers thermal pads on the bottom side of the switching device, for such a package, thermal design of the PCB plays an essential role in the overall thermal management of



(a) **(b)**

Figure 48. Experimental spectrum analyzer results for the voltage across the primary side blocking capacitor in SPES (a) without a ceramic capacitor in parallel, (b) with a ceramic capacitor in parallel [56]**, ©2018 IEEE.**

the PES. Specifically, the design of PCB tracks, heat spreading thermal pads and the use of thermal vias for heat transfer from the device package to the heat sink. Details about the thermal design are provided in Appendix D.

G. Summary

In this chapter, first, the designs of SPES, LPES, data transmitter (Tx) and receiver (Rx) circuits are provided. For ensuring fast and reliable data transfer in the proposed sequential co-transfer scheme, an SCI protocol with additional signature bits has been selected. Next, Using the designed SPES, LPES and data nodes, in this chapter circuit realization and modes of operation for the two case illustrations provided in Chapter 2: (a) SISO HFDPS and (b) SIMO HFDPS, are provided. For the former, transfer and data switches have been primarily used for decoupling the power and data circuit. Further, data exchanged between the data nodes have been utilized for varying the size of the HF power packet as per load demand. For the latter, transfer and data switches along with decoupling the power and data circuit, have been used for routing the HF power and data packets based on TDM. Additionally, for SIMO HFDPS a data transfer scheme is outlined, in which load demands are transferred to source in each TDM time slot.

Finally, in this chapter, issues related to HF noise in the designed PES using GaN FETs as switching components are outlined. The circuit PCB track inductance and non-ideal behavior of the circuit passive elements are identified as the significant factors contributing to the HF noise in the SPES and LPES. An optimized PCB layout is designed to limit the PCB track inductance. Further, the addition of suitable passive components based on their HF impedance response is used to reduce the HF noise in the SPES. The effect of these modifications in reducing the HF noise in the SPES and LPES have been validated experimentally.

Chapter 4

Results and Discussion

Parts of this chapter, including figures and text, are based on my following papers:

- A. Gupta and S. K. Mazumder, "Sequential Co-transmission of High-Frequency Power and Data Signals," in *IEEE Transactions on Industrial Informatics*, vol. 14, no. 10, pp. 4440–4445, 2018.
- A. Gupta and S. K. Mazumder, "Smart LED Lighting using GaN-based 'Discrete' Power and Data Sequential Co-Transfer Network," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, 2018, pp. 68–72.

A. Introduction

Experimental and simulation results validating the proposed sequential co-transfer scheme for HF power and data transfer have been presented in this chapter. The chapter has been divided into five sections. In Section B, experimental results demonstrating the operational feasibility of a SISO HFDPS following sequential co-transfer scheme are provided. Additionally, details about the control scheme implemented for realizing need-based power delivery in the designed SISO HFDPS is outlined. In Section C, practical challenges faced with the functioning of the data nodes at high power levels are discussed, and suitable solutions for the same are outlined and supporting experimental results are provided. In Section D, experimental results validating the HF power packet routing in a SIMO HFDPS following sequential co-transmission scheme are provided for dc and ac loads. Finally, a summary of the chapter is provided in Section E.

B. Experimental Validation of Sequential Co-Transfer Scheme in a SISO HFDPS

1. Experimental Setup

Based on the design considerations using GaN FETs provided in Chapter 3 for SPES and LPES, an experimental prototype, as shown in Figure 49, is developed and used for the experimental demonstration of the sequential co-transfer scheme in a SISO HFDPS. TI's TMS320F28335 DSP is selected for generating the gating signals for all the switches and for implementing the modified SCI protocol for data transmission. DSP is programmed in C language using TI's Code Composer Studio V 3.3. With reference to Figure 50, variation in the data packets and the duration of HF power packet transfer signal for PN_{1S} and DN_{1S} are handled by DSP_1, whereas for PN_{1L} and DN_{1L} are handled by DSP_2. Further, PCB traces on the switch board connecting SPES and LPES are used as the HF channel for sequential co-transfer of HF power and data signals. Si MOSFETs (STW18N60M2) from ST Microelectronics are used for realizing the network switches in the switch board. A centralized clock generated using the EPWMxSYNCI bit available in the time-based clock (TBCLK) register of the ePWM submodule of DSP_1 is used for synchronizing the ePWM submodules of DSP_2 through an external connection. Additional power-stage parameters for SPES and LPES are derived using [56] and are captured in Table IV.

Table IV. Specifications of the SPES and LPES.

Transformer turns ratio	*Switching frequency*	L_1	L_2	C_1	C_1'
2	80-120 kHz	50 μH	100 μH	6.8 μF	1.5 μF

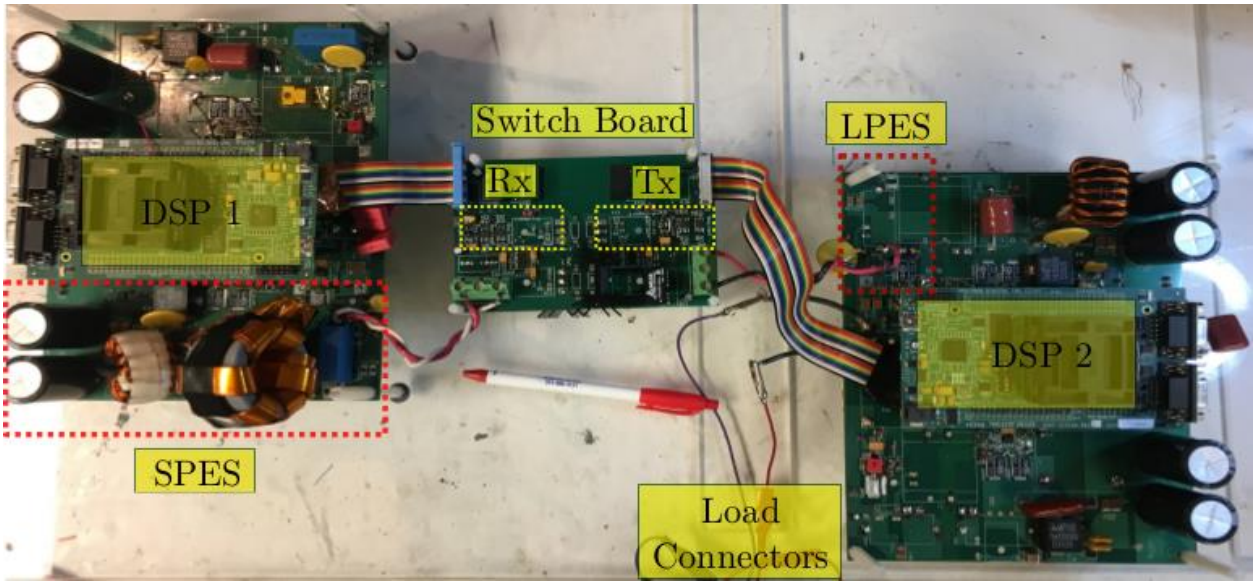


Figure 49. The developed experimental prototype for the SISO HFDPS following sequential co-transfer scheme. HF channel, transfer and data switches are realized on the switch board. It is noted that only a small section marked as SPES and LPES is used on each power board which contains two modules of isolated Ćuk converter [30]**, ©2018 IEEE.**

2. Control Approach for Sequential Co-Transfer of Power and Data

The designed prototype can be used for realizing the transfer of fixed duration HF power packets (open-loop) or variable duration HF power packets (closed-loop) which are based on dynamically varying load demand. Dynamic load demand is captured through variation in the duty cycle of the prototype, information about which can be exchanged between the LPES and SPES through the HF channel using the data nodes. Schematic diagram of a single pair of SPES and LPES with the control approach used for meeting the dynamic load demand implemented in DSP_1 and DSP_2 is shown in Figure 50. A simple PI-based closed-loop controller with output voltage feedback is implemented in DSP_2 and load demand is computed in terms of duty cycle. This duty cycle information generated in

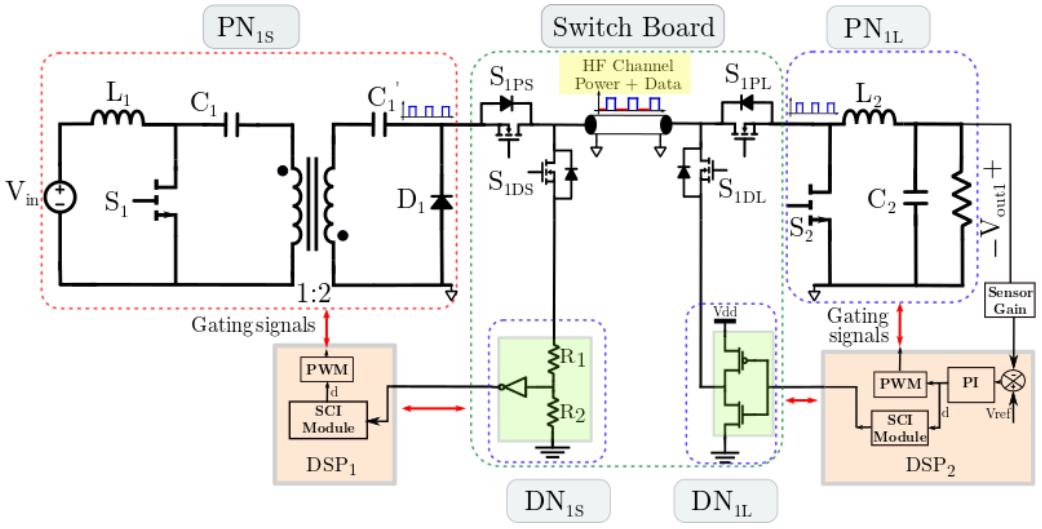
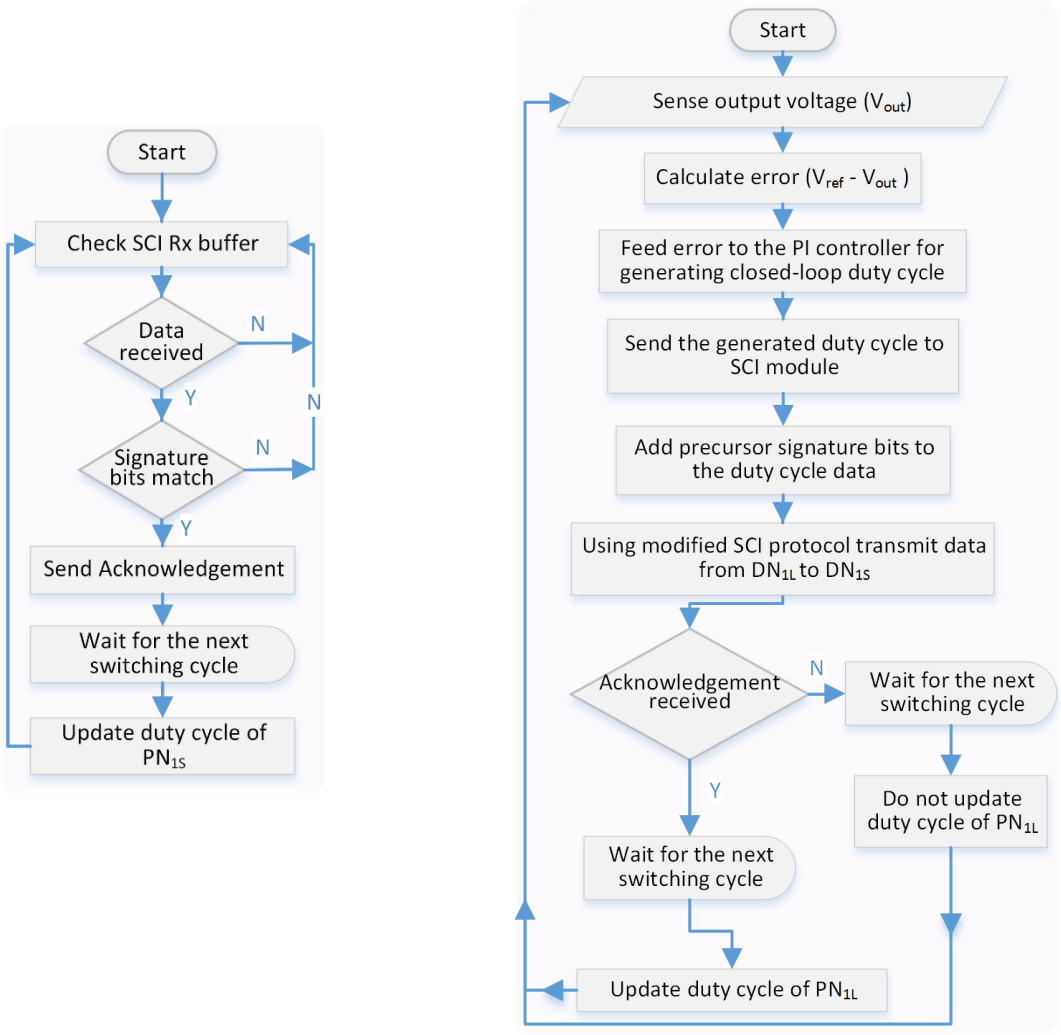


Figure 50. Schematic diagram outlining a single pair of SPES and LPES connected over the HF channel. Control approach implemented in DSP_1 and DSP_2 are also illustrated, with V_{ref} representing the reference for regulating the output voltage.

DSP_2 is transferred to DSP_1 through the data nodes using the modified SCI protocol. Further, flowcharts explaining the control approach implemented in DSP_1 and DSP_2 for regulating the output voltage of the LPES are provided in Figure 51 (a) and Figure 51 (b), respectively.

As shown in Figure 51 (b), at the onset of each switching cycle, the output voltage of the LPES is sensed and fed to a PI compensator in DSP_2. Using this sensed voltage, an error is generated by comparing it with the pre-defined reference value (V_{ref}). This error is then fed to a PI compensator and a closed-loop duty cycle emulating the dynamic load demand is generated. The generated duty cycle is then converted to an 8-bit data format comprising of 2 precursor signatures bits (detailed in Chapter 3). Next, during the HFDT window, as depicted in Figure 29, the generated duty cycle data is transmitted from DN_{1L} to DN_{1S} via the HF channel.

As shown in Figure 51 (a), once this data packet reaches the Rx buffer in DSP_1, its precursor signature bits are matched with the stored signature. If the match is good, an acknowledgement is sent to DSP_2 and the duty cycle of SPES and LPES are updated in the next switching cycle. Using the updated duty cycle, gating pulses for S_1, S_{1PS} and S_{1DS} are generated by DSP_1 and the duration of HF power packet is adjusted as per load demand.



(a) **(b)**

Figure 51. Flowcharts outlining the control approach implemented in the controller of (a) data receiver module (DN_{1S}) (b) data transmitter module (DN_{1L}).

If the data received by DSP_1 is corrupted and the matching fails, then, no acknowledgement is sent to DSP_2. In such a scenario, the duty cycle for each power node remain unchanged and equal to the last successfully transmitted duty cycle. During this period, the SISO HFDPS continues to operate in the quasi-closed loop and achieves a quasi-steady state with the delayed duty cycle, until satisfactory communication between the data transmitter and the receiver is re-established.

3. Experimental Results for SISO HFDPS Feeding dc Load

In this section, experimental results obtained using the designed prototype are presented. Experimental results in Figure 52 -Figure 55 are obtained for an input voltage of 20 V at SPES and a fixed HF power packet duration of 5.7 μs and data packet duration of 4 μs. HF power signals (HF power packets) are transferred at a frequency of 100 kHz from the SPES to LPES.

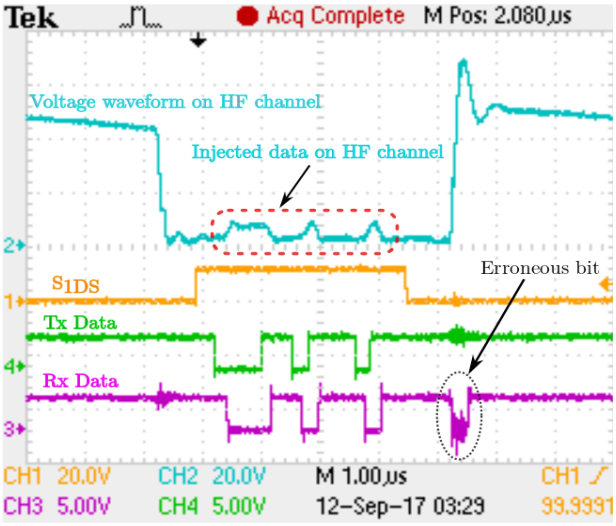


Figure 52. Experimental waveform (Ch. 2) shows the sequential co-transfer of HF power and data over the HF channel. Embedded data signals (Ch. 3 and 4), which are transmitted from DSP_2, when S_{1DS} (Ch. 1) is high, to DSP_1 are shown on Ch. 4 and 3, respectively.

The experimental result provided in Figure 52, demonstrates the sequential co-transmission of the HF high-voltage power and low-voltage data signals on Ch. 2. The embedded data signals containing load demand in the above trace, are transmitted from DSP_2, when S_{1DL} is ON, to DSP_1 and are shown on Ch. 4 and Ch.3, respectively at the DSP SCI channels. Gating signal for the data switch S_{1DS} is plotted on Ch. 1. A total delay of 340 ns is observed between the transmitted and the received data signals due to the propagation delay incurred in the digital components and the HF channel. Further, the occurrence of an erroneous bit at the onset of the power signal is observed in the received data; this is due to the voltage drop across R_1 and R_2 (shown in Figure 42) in DN_{1S} caused by the current that is required to charge the C_{oss} of S_{1DS} for developing its blocking potential. This erroneous data bit generated by the charging current is rejected in DSP_1 using the modified SCI protocol which is outlined in Chapter 3.

With reference to the co-transfer signal shown on Ch. 3 in Figure 52, Figure 53 validates the transfer of HF power packet to PN_{1L} when S_{1PS} is turned ON. During this time, power is transferred from the dc source in SPES to the load attached at the output of LPES over the HF channel. This is validated by the increase in the magnitudes of the input and output inductor currents during this interval. Similarly, when S_{1PS} is turned OFF, one can observe that, magnitudes of the input and output inductor current decreases, showing that no power is being transferred through the HF channel and the stored energy in the inductors is being used to supply the load.

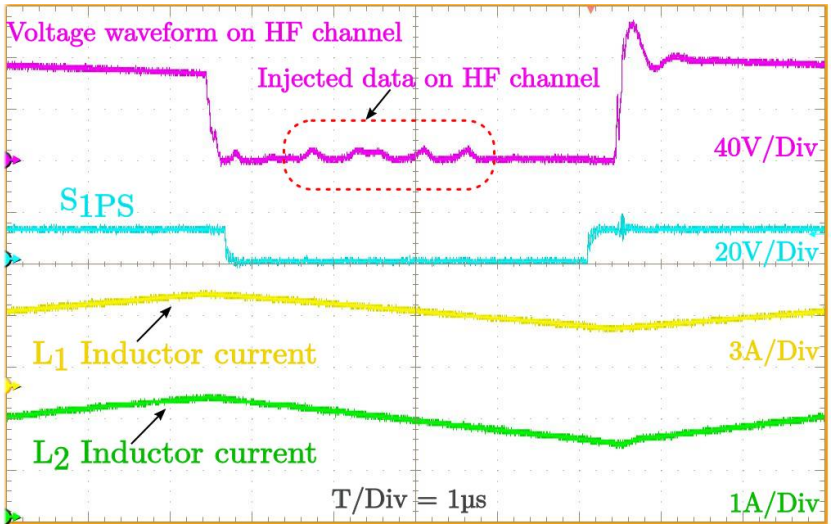


Figure 53. Experimental waveform (Ch. 3) shows the sequential co-transfer of HF power and data over the HF channel. Only when S_{1PS} (Ch. 2) is turned ON, the magnitudes of the input and output inductor currents (Ch. 1 and 4) increase indicating power transfer between SPES and LPES over the HF channel.

Next, with reference to the same co-transfer signal, shown in Figure 52, the status of the local switches S_1 and S_2 in SPES and LPES, respectively, with reference to S_{1PS} and S_{1DS}, are shown in Figure 54. They comply with the timing diagram provided in Figure 29. The corresponding drain to source voltages (V_{ds}) across S_1 and S_2 for the same operating conditions are shown in Figure 55. As can be observed from Figure 55, V_{ds} across S_2 develops when the HF power packet is transferred from SPES to the LPES. V_{ds} across S_1 develops during the time HF channel is used for the transfer of data packets. Further, as can be observed from the gating signals provided in Figure 54, the transfer switches S_{1PS} and S_{1PL} (not shown in Figure 54, but is synchronized to S_{1PS}) are ON during the time HF power packets are transferred on the HF channel and only block the data packets from entering the power nodes in a SISO HFDPS.

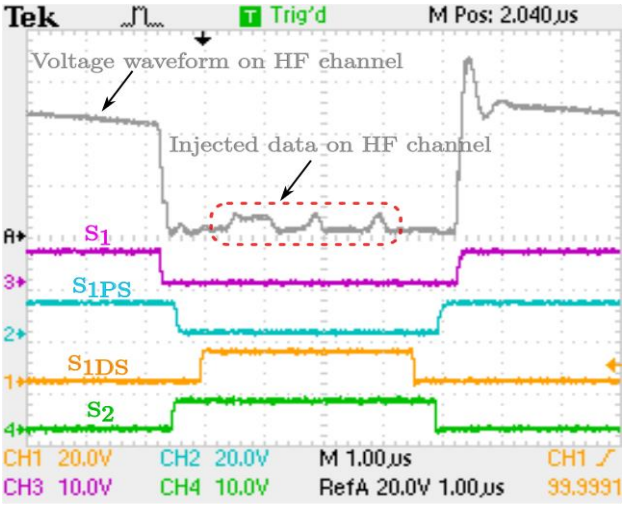


Figure 54. Experimental waveform (Ref A) shows the sequential co-transfer of HF power and data over the HF channel, along with the gating signals for S_1, S_{1PS}, S_{1DS} and S_2.

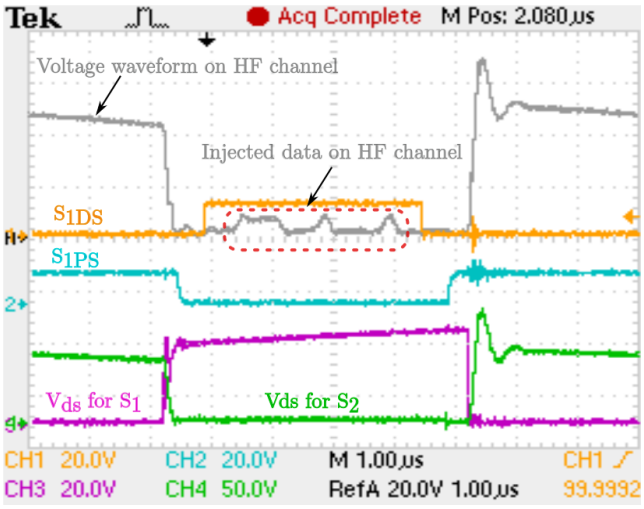


Figure 55. Experimental waveform (Ref A) shows the sequential co-transfer of HF power and data over the HF channel, along with the V_{ds} waveforms across switches S_1 and S_2.

Thus, only low-voltage data packets will be observed while measuring their V_{ds} waveforms. However, data switches S_{1DS} and S_{1DL} are OFF during the time HF power packets are transferred on the HF channel, and hence V_{ds} waveforms across the data switches will replicate the waveshapes of the HF power packets which are transferred on the HF channel. It is noted that, transfer and data switches are operated under a zero-voltage condition on the HF channel, which results in the elimination of their switching losses.

Table V. Effect of the frequency of power transfer on the data rate

Frequency of power transfer (kHz)	80	90	100	110	120
Data rate (Mbps)	4.68	4.68	4.68	4.68	4.68

Further, to test the dependence of the data rate on the frequency of HF power packet transfer in the proposed sequential co-transfer scheme, the experimental prototype is examined by varying the frequency of HF power packet transfer between 80–120 kHz. Experimental measurements from the test are listed in Table V. A maximum data rate of 4.68 Mbps is maintained irrespective of the change in transfer frequency of the HF power packets.

Experimental result demonstrating the effect of HF power packet size variation is provided in Figure 56. Load demand is varied sinusoidally at a rate of 1kHz, corresponding to which an open-loop duty cycle between 54 % and 23 % is computed by DSP_2 for a fixed input voltage of 20 V at SPES. Further, this load demand in terms of the requested duty cycle is transfer to DSP_1 in every switching cycle using the data nodes. Depending on the received duty cycle, DSP_1 generates gating pulses for S_1, S_{1PS} and S_{1DS} and thus adjust the size of the HF power packet as per load requirement.

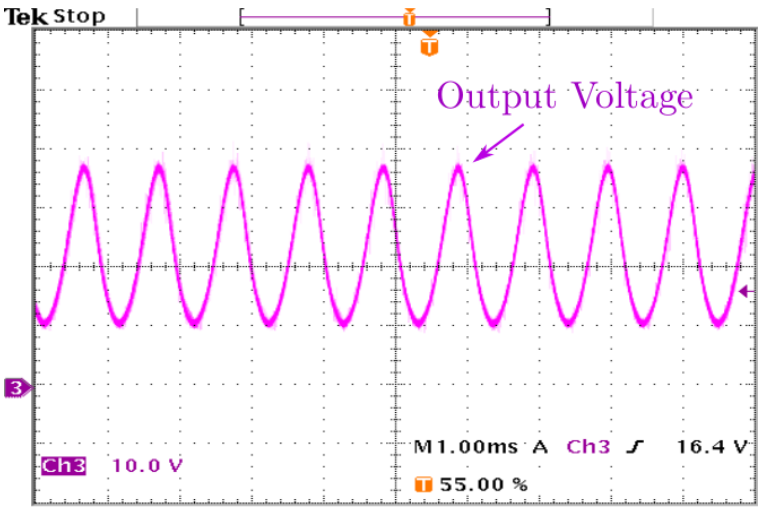


Figure 56. Variable output voltage waveform obtained at the load connected to the output terminal of LPES. The applied duty cycle has sinusoidal modulation with a frequency of 1 kHz along with a dc offset. Constantly changing load demand is transferred to the data node of SPES over the HF channel in every switching cycle.

Next, the experimental prototype is subjected to a cyclic load transient from 36 W to 48 W with a frequency of 20 Hz using Agilent 6060B dc electronic load. Cyclic load variation, changes the power requirement of the load from 36 W to 48 W in every 25 ms. A PI compensator based closed-loop voltage-control approach illustrated in Figure 50 is implemented in DSP_2 to track a 30 V dc at the output with a fixed input dc voltage of 20 V. The PI compensator is tuned to achieve an acceptable tradeoff between output-voltage regulation and dynamic response. Duty cycle computed in DSP_2 is later transferred to DSP_1 over the HF channel for generating gating pulses for S_1, S_{1PS} and S_{1DS}. In Figure 57, output-voltage (V_{out}) is plotted along with the output current of the load connected to the LPES. It is observed that, the closed-loop converter tracks the output voltage with a continually changing load current by constantly varying the size of the HF power packet which is computed using the duty cycle information being transmitted in every switching cycle. Application of the outlined control has also been experimentally demonstrated for a smart LED lighting system using sequential co-transmission scheme in [65].

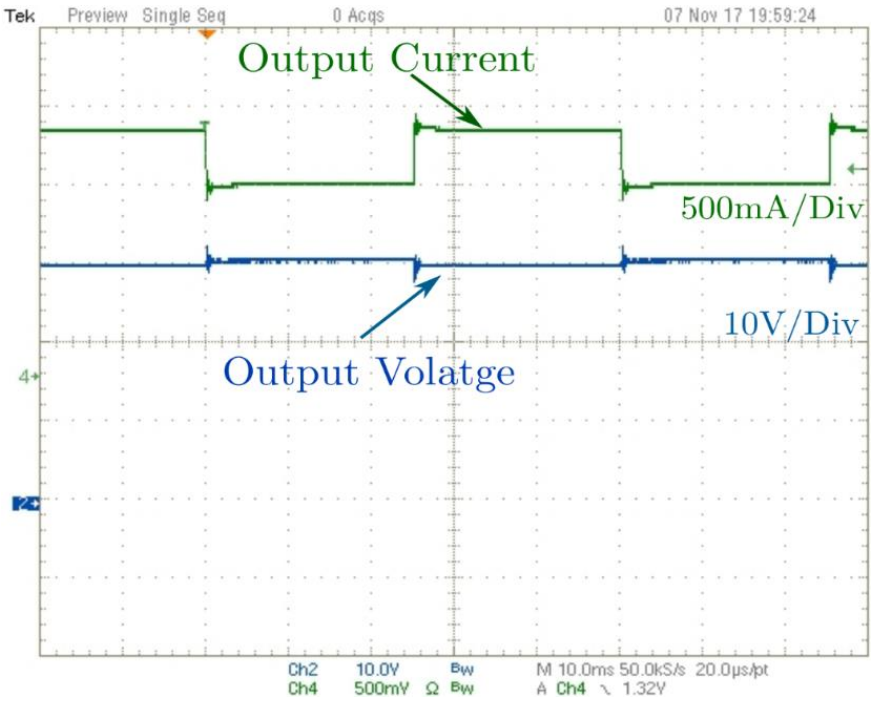
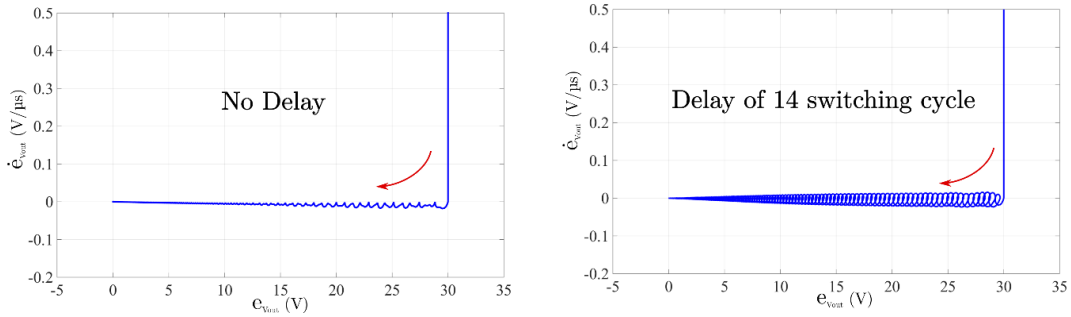
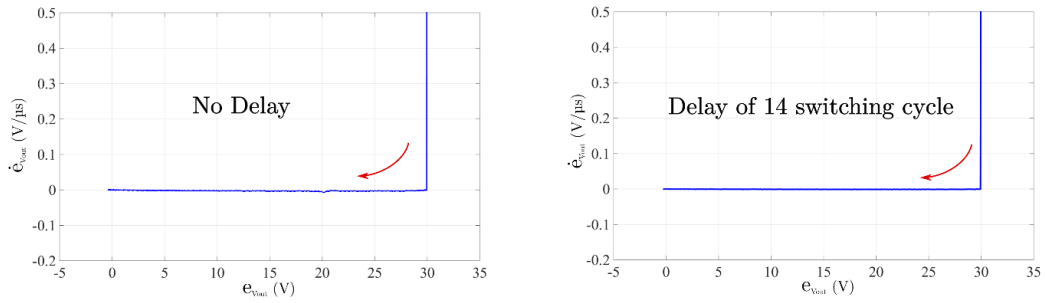


Figure 57. Output-voltage and output-current waveforms of the load connected to the LPES during a cyclic 20 Hz load variation between 48 W and 36 W. A PI compensator is designed to track the output voltage of 30 V given an input voltage of 20 V. Load demand in terms of duty cycle variation is transferred from DSP_2 to DSP_1 in every switching cycle using the data nodes [30]**, ©2018 IEEE.**

Further, to emulate the effect of communication failure, the experimental prototype was subjected to a delay of n switching cycle, i.e., the closed loop duty cycle was updated once in n switching cycles. As explained in the flowchart provided in Figure 51, during this delayed period the converter runs with the last successfully transmitted duty cycle value. For a V_{in} of 20 V, V_{ref} of 30 V and $n = 14$, simulation along with experimental results for the state error trajectories of the output voltage ($e_{Vout} = V_{ref} - V_{out1}$) are provided in Figure 58 (a) and Figure 58 (b), respectively. It can be observed that the state error trajectory of the output voltage converges for both the delayed and non-delayed system showing its reachability.



(a)



(b)

Figure 58. (a) Simulated and (b) experimental results for the state error trajectories of the output voltage at LPES with no delay and a delay of 14 switching cycle. Converges of state error trajectory guarantees the reachability of the delayed and non-delayed system [30]**, ©2018 IEEE.**

C. Design Modifications in Data Circuit

When HF power packets are placed on the HF channel by SPES, all the data switches (S_{1DS}, S_{1DL}) need to block them from entering their corresponding data nodes (DN_{1S} and DN_{1L}, respectively). This is achieved by turning OFF the data switches when HF power packets are transferred. However, because of the non-ideal nature of the data switches which are used for decoupling the data nodes from the power nodes, an unwanted transitional coupling occurs between the two. More specifically, during transition period a charging current pass through the output capacitance (C_{oss}) of the data switches into the low-voltage data circuitry. This charging current builds-up the drain to source voltage (V_{ds}) across the data switches while they are OFF. Value of this charging current depends on the C_{oss} of the data switches and dv/dt of the HF power packet. In experimentation, as the power level of the SISO HFDPS was increased beyond 50 W, by increasing the input voltage, data nodes failed. This was because of the increased value of charging current which was now beyond the current handling capability of the low-voltage data circuit. Thus, for ensuring the nominal operation of the data switches at higher power levels of the HFDPS, a protection mechanism is required. Additionally, as discussed before, the charging current also introduces an erroneous data bit to the data packet which is rejected using the modified SCI protocol. Although effective, this solution results in reducing the payload capacity of the SCI data frame from 8-bits to 6-bits. Thus, causing a reduction in the overall quantity of information that can be exchanged between the data nodes during each HFDT window.

To tackle the challenges mentioned above, in this section a two-stage protection design for the data nodes and a hardware solution for removing the erroneous data bit are proposed. Experimental results validating the effectiveness of the modified data node design are also provided.

1. Protection Design for the Data Nodes

One of the most commonly used devices for protection against transients in a low-voltage circuit is a transient voltage suppressor (TVS) diode [66]. Ideally, TVS diode is presumed to have a brick wall characteristic and goes into avalanche breakdown as soon as its breakdown voltage is reached. However, in practice TVS diode characteristics are softer and have gentle slope compared to the abrupt vertical characteristics of an ideal TVS diode as is shown in Figure 59. As a result, in case of a surge event TVS diode will only be able to steer a portion of the energy away from the

circuit that is to be protected leaving it exposed to high voltages and currents. Hence for achieving complete protection from transient currents and voltages in the data nodes, the use of transient current suppressors (TCS) in conjunction with the TVS diode is proposed.

TCS is a series connected device. During normal operation, TCS exhibits the behavior of a low-value resistor. However, during the surge condition, when the current flowing through the TCS raises above its trigger value there is a steep increase in the device impedance, and it transitions into a current limiting state [67]. I-V characteristics of a 250 mA DL-series TCS device from Bourns is shown in Figure 60 [68].

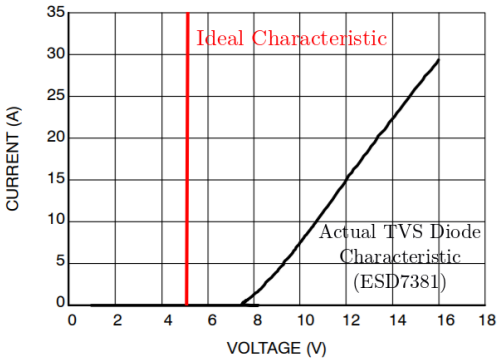


Figure 59. Comparison between an ideal 5V TVS diode characteristic (Red) and actual TVS diode characteristic of ON Semiconductor 5V TVS diode, ESD7381 (Black).

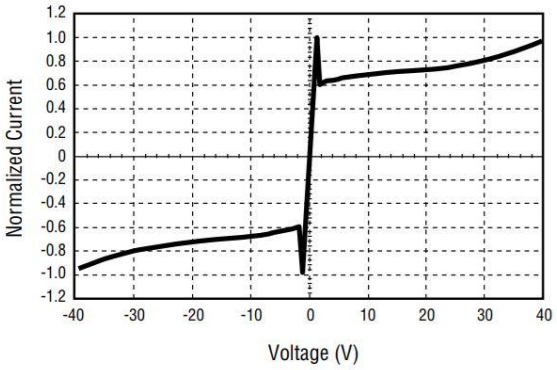


Figure 60. Normalized V-I characteristics of a Bourns DL-series high-speed TCS under surge condition [68].

Circuit placement of the TCS device is shown in Figure 61. TCS device is connected in series to the data node along with a TVS diode which is connected in parallel to this arrangement. During the surge condition, the voltage at the TVS junction increases which causes a current to flow through the TCS device and into the data circuit. As the current trigger limit of the TCS device is reached it prevents any further increase in its current by abruptly increasing its internal resistance. As a result, the transient current entering the data node during the surge event is minimized and kept within a safe limit. The TCS device voltage-drop continues to rise until the TVS diode reaches its breakdown voltage. Bourns DL-series TCS device can block voltages up to a voltage of 40 V across its input and output terminal [68]. This two-stage protection limits the maximum voltage at the junction of TVS and TCS to the breakdown voltage of the TVS diode, while also limiting the maximum current that can flow through the TCS device into the data node.

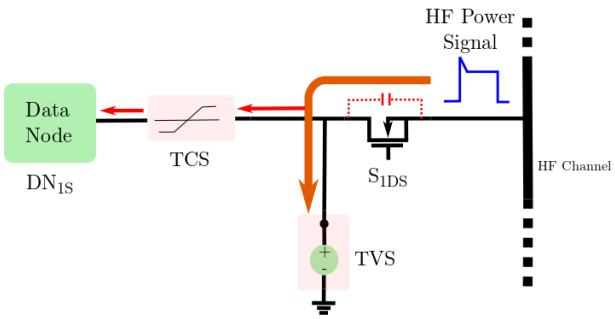


Figure 61. Implementation of a two-stage protection scheme with a TCS device in conjunction with a suitable over voltage limiting device (TVS diode) for providing comprehensive current and voltage limiting protection to the data node in surge conditions.

In the hardware design of the data node, an SPDT switch (as shown in Figure 62) is used to transition between Tx and Rx functionalities of the data node. When SPDT switch is in position "1" and "2", the data node is configured as Tx and Rx, respectively. In the data node, the SPDT switch is the most vulnerable element in terms of the maximum allowable current limit during the Tx operation. This is mainly because, during Tx mode of operation, source terminal of the data switch (S_{1DS}) has a low impedance path to ground through the SPDT switch and Tx circuit, as shown in Figure 62. This results in a transient current to flow through the SPDT switch during the event of transitional coupling. This transient current can be suppressed by adding TCS and TVS devices in the data node, at the locations shown in Figure 62. However, the presence of the series resistors R_1 and R_2 in the Rx circuitry, precludes the need for TCS device during Rx mode of operation.

In the experimental setup, for implementing the two-stage protection scheme, Bourns TCS device (TCS-DL004-250-WH) with maximum trigger current rating of 500 mA and transition time of 50 ns between normal operating state and current limiting state is chosen in conjunction with a 10 V TVS diode from Littlefuse (SMAJ10A) having a maximum clamping voltage of 17 V [67], [69]. Additionally, a 5 V Zener diode is added at the output of the Rx circuit for limiting the maximum voltage that can be applied to the signal conditioning circuit.

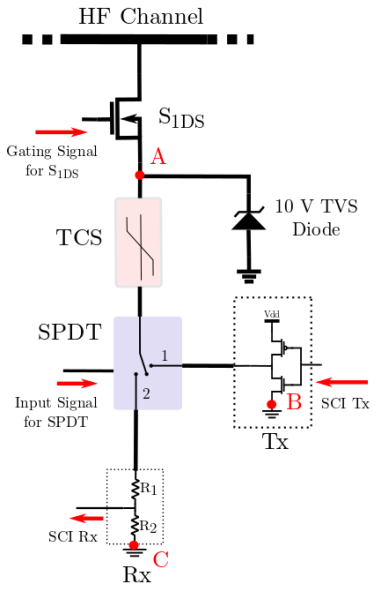


Figure 62. Schematic representation of the data node with enhanced two-stage protection with DN_{1S} as case illustration. During transitional coupling in Tx mode of operation, TCS device suppress transient current flow in path $A \rightarrow B$. However, the enhanced protection features of the TCS device are precluded by the inherent higher impedance of the path $A \rightarrow C$ provided by resistors R_1 and R_2 in the Rx mode of operation.

The experimental result obtained on a SISO HFDPS prototype demonstrating the operation of the designed two-stage protection scheme for the data nodes is presented in Figure 63. DN_{1L} and DN_{1S} are configured as Tx and Rx, respectively. It can be observed that, transitional coupling occurs at the onset of HF power packet on the HF channel and results in a voltage spike of 17 V to appear across the TCS in DN_{1L}. No appreciable voltage drop is observed across the TCS connected in DN_{1S} as the terminal voltage at the junction of the TVS is generated by the resistors used in the Rx circuit. Voltage spikes are also observed across the TCS in DN_{1L} when data is transmitted on the HF channel. These are caused by the TCS device which is acting as a series resistor to the inverting gate driver IC transferring data

bits on the HF channel. The resistance induced by the TCS device will increase as the number of transfer switches in the HFDPS are increased, this is because with the addition of each transfer switch to the HFDPS, an additional path will be available to the HF data bits through their C_{oss}. This will result in the increased current output of the gate driver IC, that can be higher than the trigger current of the TCS device and further result in a reduction in the magnitude of the data bits. To avoid such issue, devices with low C_{oss} can be used as the transfer switches. In the present experimental setup, to counter this issue, a comparator circuit is added at the output of the Rx, for providing it more flexibility while measuring the low voltage data signals.

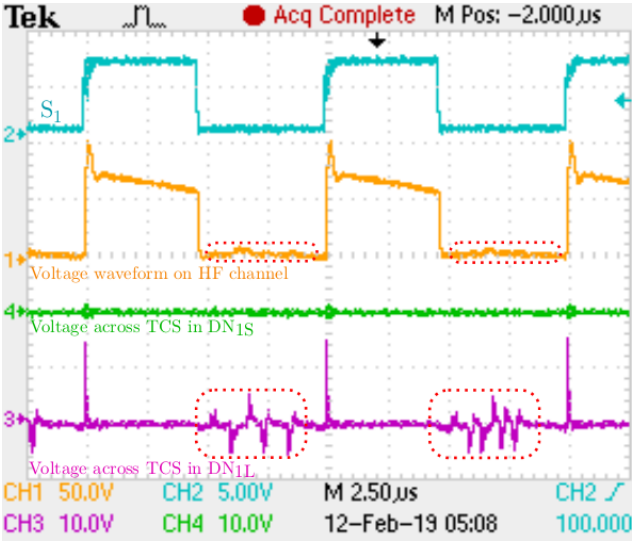


Figure 63. Experimental waveforms demonstrating the operation of protection designed for the data nodes. Transitional coupling between the power and the data nodes occur when S_1 is turned ON (Ch. 2). Voltage spikes equal to the clamping voltage of TVS diode appear across the TCS in DN_{1L} (Ch. 3) validating its operation during transitional coupling. No significant voltage drop appears across TCS in DN_{1S} (Ch. 4).

2. Hardware Solution for Eliminating Erroneous Data Bit

In the data node that is configured as an Rx, charging current during the transition period, can results in a voltage drop to appear across its data sensing circuitry. This unwanted voltage drop is presumed as a data bit by the *DSP* SCI receiver and can result in distortion of the complete data frame. In initial experiments, this erroneous data bit was rejected using the modified SCI protocol. However, using the modified SCI protocol, the payload size of the SCI data

frame was reduced. Hence, in this section, a hardware modification is proposed for the Rx circuit that can eliminate the erroneous data bit from the SCI data frame that is transferred to the SCI receiver of the DSP.

In Figure 64, a data correction circuit is added to the Rx circuit of the data node for removing the erroneous bit from the SCI data frame that is transferred to the DSP. In the data correction circuit, a two input AND gate with inputs as the output of the comparator stage and gating signal for the data switch have been added. Since, a small portion of the surge current will flow through the data node at the onset of HF power packet while the data switch is OFF, adding an AND gate in the Rx path will remove the generated erroneous bit from the received SCI data frame. Figure 64, shown the complete arrangement of the modified data node with a data correction circuit and integrated two-stage protection on DN_{1S} as case illustration. Pictorial representation of data signals in the Rx circuit at positions marked in Figure 64, are shown in Figure 65. It is noted that, the data correction circuit does not eliminate the occurrence of the erroneous bit, but by using an AND gate with inputs as the gating signal of S_{1DS} and the comparator output this erroneous bit is removed from the SCI data frame that is transferred to DSP_1.

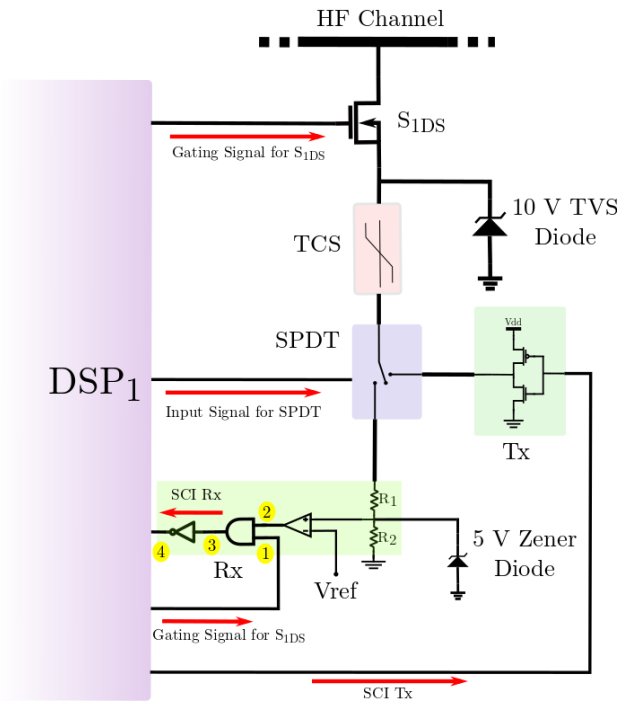


Figure 64. Schematic representation of the modified data node with integrated transient current protection and data correction circuit with DN_{1S} as case illustration.

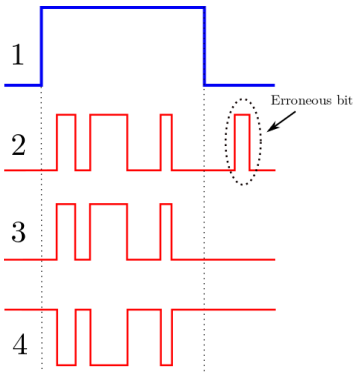


Figure 65. Various signals in the Rx circuit with the positions as marked in Figure 64. The erroneous bit seen in the comparator output is removed from the SCI Rx signal by using a two-input AND gate.

In Figure 66, for the same operating conditions as Figure 52, the experimental result with the use of two-stage protection and data correction circuits in the data nodes is provided. The decrease in signal strength of the low-voltage data signals being transmitted sequentially on the HF channel can be observed on Ch. 2 in Figure 66. This is because of the use of TCS device in DN_{1L}, which acts as a series resistor to the Tx circuit. SCI data frame devoid of any erroneous data bit is recreated in DN_{1S} (Ch. 3) by adjusting the reference voltage of the comparator and using the data correction circuit.

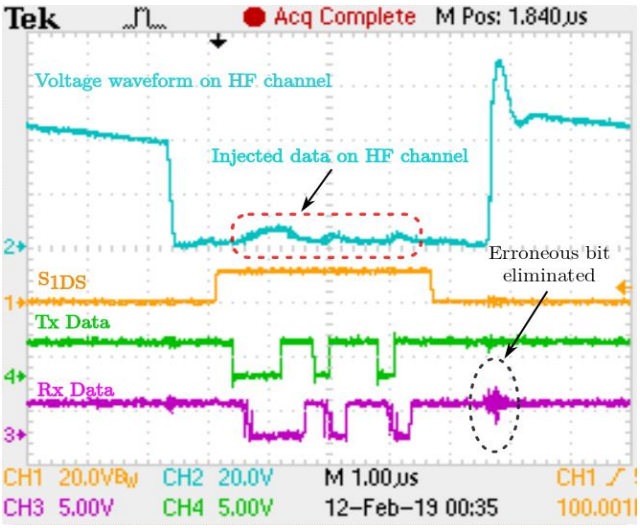


Figure 66. Experimental waveform (Ch. 2) shows the sequential co-transfer of HF power and data over the HF channel with modified data node design. Embedded data signals, which are transmitted from DSP_2, when S_{1DS} (Ch. 1) is high, to DSP_1 are shown on Ch. 4 and Ch. 3, respectively.

D. Experimental Validation of Sequential Co-Transfer Scheme in a SIMO HFDPS

1. Experimental Setup

Using the same circuit configuration for the GaN-based SPES and the LPES used in the experimental prototype design of a SISO HFDPS in Section C, Figure 67 shows the experimental prototype developed for realizing a SIMO HFDPS following sequential co-transfer scheme. In Figure 67, PN_{1S} serves as the SPES, and $PN_{1L}$and PN_{2L} serve as the two LPESs. A TI's TMS320F28335 DSP is selected for generating the gating signals for all the switches based on the TDM and for implementing the modified SCI protocol for data transmission. DSP is programmed in C language using TI's Code Composer Studio V 3.3. With reference to Figure 35, variation in the data packets and the size of the HF power packet for PN_{1S} and DN_{1S} are handled by DSP_1. Similar role is performed by DSP_2 for PN_{1L} and DN_{1L}, and by DSP_3 for PN_{2L} and DN_{2L}. A TDM frame time of 20 μs is selected, which results in two equal time slots, each with a duration of 10 μs. During each time slot, HF power packets are routed to PN_{1L} and PN_{2L} by PN_{1S} and data packets are exchanged between DN_{1S}, DN_{1L}, and DN_{2L}. Further, PCB traces on the switch board are used as the HF channel for sequential co-transfer of HF power and data packets. Power stage parameters for the SPES and LPESs are derived using [56] and are captured in Table VI.

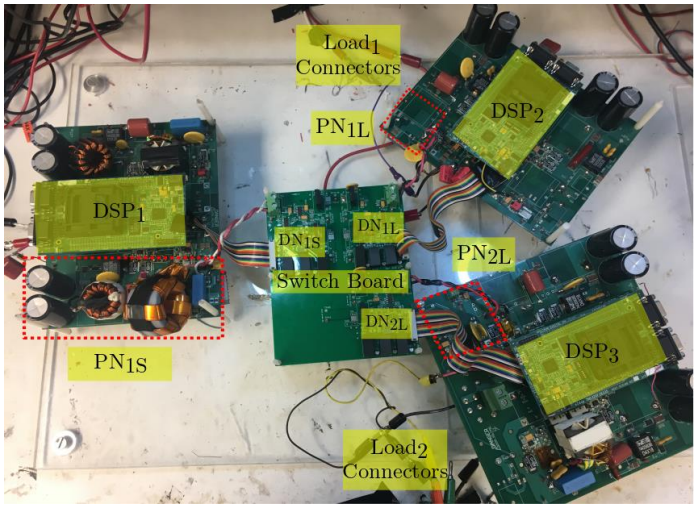


Figure 67. The experimental prototype for the SIMO HFDPS comprising of one SPES (PN_{1S}) and two LPESs (PN_{1L} and PN_{2L}). HF channel, transfer switches (S_{1PS}, S_{1PL}, and S_{2PL}) and data switches (S_{1DS}, S_{1DL}, and S_{2DL}) along with the data nodes (DN_{1S}, DN_{1L}, and DN_{2L}) are realized on the switch board.

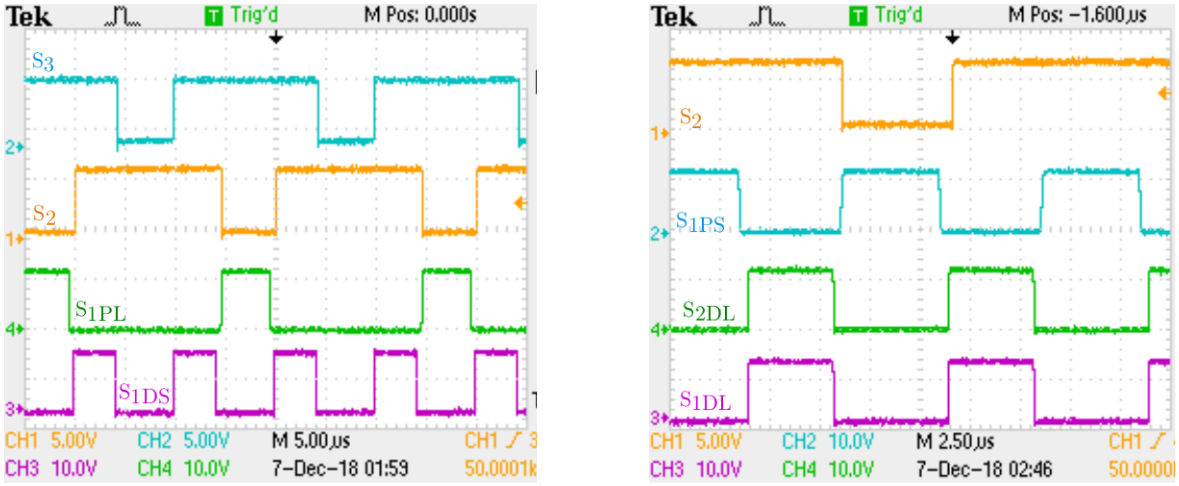
Table VI. A table listing the power and data nodes parameters of the experimental setup.

Power and Data nodes parameters	***Value***
TDM frame time (T_W)	20 μs
HF transformer turns ratio (1: n)	1 : 2
Inductor in PN_{1S} (L_1)	50 μH
Inductor in PN_{1L} and PN_{2L} (L_2, L_3)	100 μH
Blocking capacitors in PN_{1S} (C_1, C_1')	6.8 μF, 1.5 μF
Data rate	4.68 Mbps

2. Experimental Results for SIMO HFDPS Feeding Multiple dc Loads

The designed experimental prototype of the SIMO HFDPS in Figure 67 can be operated either as an open-loop system with the fixed size of HF power packet or as a closed-loop system for realizing need-based HF power packet transfer. Experimental results provided in this section are based on a closed-loop system, where load needs are transferred to the source using the data nodes. Modified SCI Data bits are transferred at a rate of 4.68 Mbps, with the synchronization bits now being used as the address bits. DN_{1S} is given a binary address of "11", DN_{1L} is given a binary address of "01" and DN_{2L} is given a binary address of "10". For experimental results provided in this section, DN_{1S} works as a Rx and receives data packets from DN_{1L} and DN_{2L} containing load-demand (time allocation value requested) during the HFDT window of the first and the second time slot of the TDM frame, respectively. Address bits are used primarily to specify the source of the data packet. Based on experimental calibrations, 4μs has been deduced as the minimum time required for the transmission of a complete modified SCI data frame over the HF channel. Thus, the maximum duration of the HFPT window available in each time slot of 10 μs is 6 μs, i.e. $\alpha_1, \alpha_2 \in [0,0.6]$. Location and duration (4μs) of HFDT window is kept fixed during the experiments.

Gating signals for various switches in the designed SIMO HFDPS are provided in Figure 68 and follow the timing diagram presented in Figure 36. HF channel is used for the transfer of HF power packets when the transfer switch S_{1PS} is turned ON and provides HF channel access to PN_{1S}. During the first (second) time slot of TDM frame, HF power packet is routed to PN_{1L} (PN_{2L}) when its corresponding transfer switch S_{1PL} (S_{2PL}) is turned ON. Further, as can be observed from Figure 68, in a single TDM frame of 20 μs, transfer switch S_{1PS} is operated twice and S_{1PL} and



(a) (b)

Figure 68. Gating signals for various switches in the designed SIMO HFDPS.

S_{2PL} are operated once, signifying that during each TDM frame two HF power packets are generated. HF power packet generated during the first time slot of the TDM frame is routed to PN_{1L} and the one generated during the second time-slot is routed to PN_{2L}. Size of HF power packet routed to PN_{1L} and PN_{2L} is based on the need received by DN_{1S} from DN_{1L} and DN_{2L}, respectively, during the HFDT window.

Figure 69 shows embedded data signals on the HF channel that are transferred from DN_{1L} and DN_{2L} to DN_{1S} during the HFDT window of the first and second time slot of TDM frame, respectively. Results in Figure 69 are taken keeping V_{in} at 0 V so as to capture the waveshape of the embedded low-voltage data packet on the HF channel. As can be observed, data bits transmitted on the HF channel have a softer slope than the data bits observed in SISO HFDPS and have reduced magnitude. This is mainly because of the increased leakage data current associated with each data bit caused by the addition of an extra power and data node for realizing SIMO HFDPS. Data bits are recreated in DN_{1S} Rx circuit by adjusting the comparator reference voltage.

As explained in the previous chapter, in the designed SIMO HFDPS, transfer switch S_{1PL} (S_{2PL}) needs to block the HF power packet that is being routed from PN_{1S} to PN_{2L}(PN_{1L}) during the second (first) time slot of the TDM frame. This results in HF oscillations to appear across S_{1PL} (S_{2PL}), with resonace frequency determined by the C_{oss} of

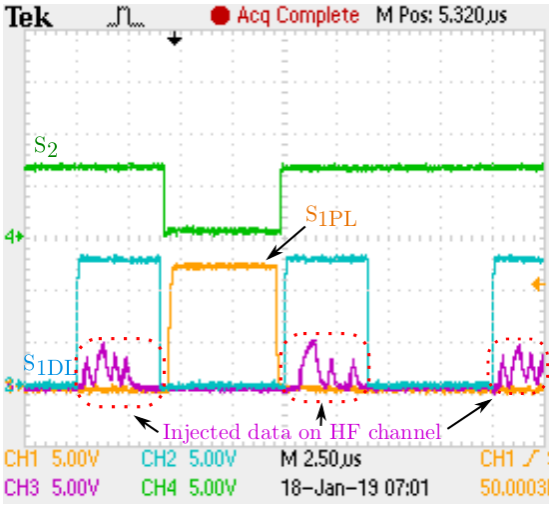


Figure 69. Experimental waveforms showing the transfer of HF data signals over the HF channel, along with the gating signals for S_{1DL}, S_{1PL}, and S_2 with $V_{in} = 0$ at PN_{1S}.

S_{1PL} (S_{2PL}) and parasitic inductance of the HF channel. To supress these HF oscillations in the experimental setup, an RC snubber with a capacitance value of $2n$F and a resistance of 50 Ω is connected across S_{1PL} and S_{2PL}. This RC snubber acts as a rate of rise control snubber and controls the rate at which the C_{oss} of S_{1PL} (S_{2PL}) is charged when HF power packets are routed to PN_{2L} (PN_{1L}). RC snubbers are not required across the data switches S_{1DS}, S_{1DL}, and S_{2DL} as the rate of rise of voltage across the C_{oss} of the data switches are controlled by the TCS devices.

The transfer of HF power and data packets on the HF channel is displayed on Ch. 3 of the experimental result provided in Figure 70. The experimental result in Figure 70 is obtained with $\alpha_1 = \alpha_2 = 0.4$ and V_{in} = 20 V. HF power packet is routed from PN_{1S} to PN_{1L} when S_1 is turned ON and S_2 is turned OFF in the first time slot of the TDM frame. Similarly, during the second time slot of the TDM frame, HF power packet is routed from PN_{1S} to PN_{2L} when S_1 is turned ON and S_3 is turned OFF. Required value of α_1 and α_2 is transfred to DN_{1S} by DN_{1L} and DN_{2L} during the HFDT window of the first and the second time slot, respectively.

In Figure 71, experimental V_{ds} waveforms across S_{1PL} and S_{2PL} are shown on Ch. 3 and Ch.1, respectively. As can be observed from Figure 71, the transfer switch S_{1PL} (S_{2PL}) in addition to blocking the HF data packets during HFDT window, blocks the HF power packet which are routed to PN_{2L} (PN_{1L}) by PN_{1S} during the HFPT window of the second (first) time slot of the TDM frame. S_{1PL} (S_{2PL}) remains ON when HF power packets are routed to PN_{1L} (PN_{2L}).

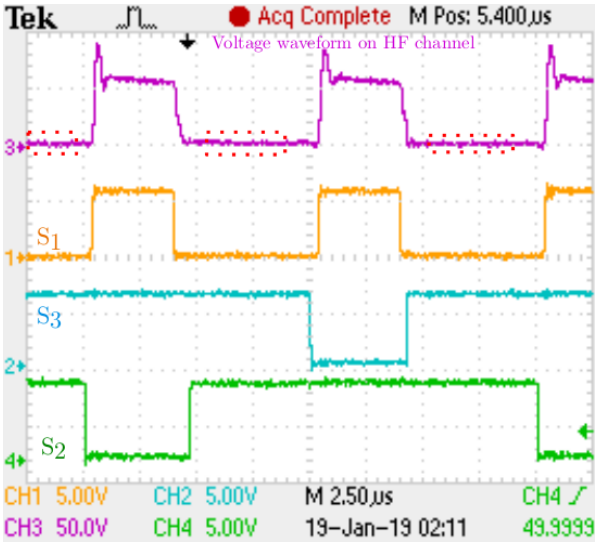


Figure 70. Experimental waveform showing sequential co-transfer of HF power and data over the HF channel in a SIMO HFDPS (Ch. 3), along with the gating signals for S_1(Ch. 1), S_3 (Ch. 2), and S_2 (Ch. 4).

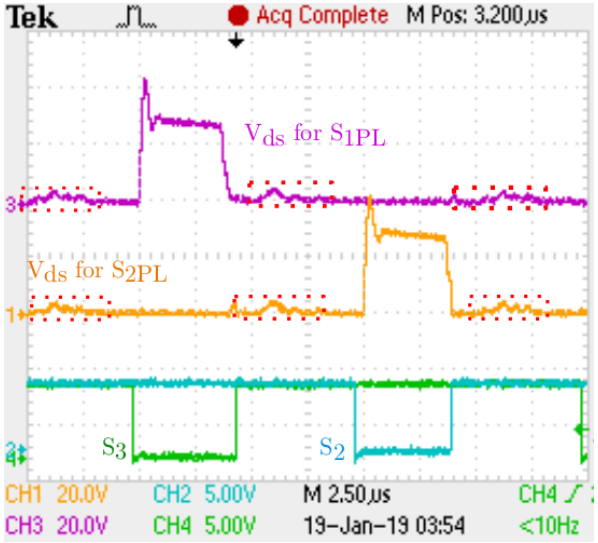


Figure 71. V_{ds} voltage waveforms across the transfer switches S_{2PL} (Ch. 1), and S_{1PL} (Ch. 3) and gating signals for S_2 (Ch. 2) and S_3 (Ch. 4).

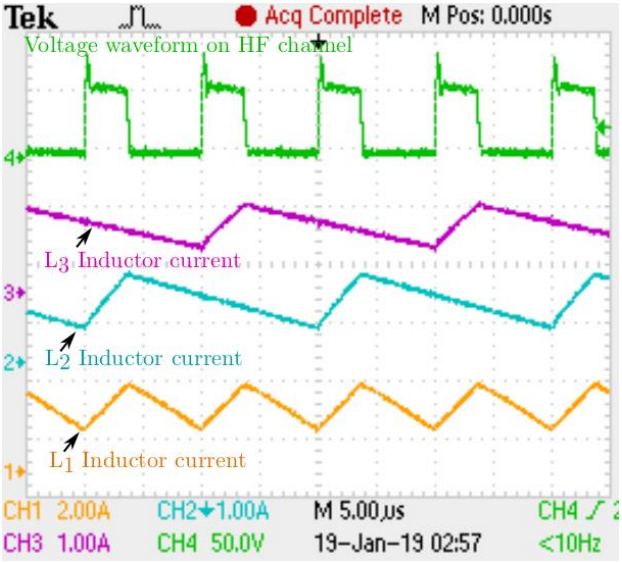


Figure 72. Experimental waveforms showing sequential co-transfer of HF power and data over the HF channel (Ch. 4). Inductor currents for L_1, L_2, and L_3 are shown on Ch. 1, Ch. 2, and Ch. 3, respectively.

The experimental result provided in Figure 72 validate the routing of HF power packets from PN_{1S} to PN_{1L} and PN_{2L}. During the first time-slot of the TDM frame, based on the previously communicated need of the load connected to PN_{1L}, the HF power packet is routed from PN_{1S} to PN_{1L} through the HF channel. This is marked by an increase in the magnitude of inductor currents of L_1 and L_2, and a decrease in the inductor current of L_3 which discharges in the load connected to PN_{2L}. Further, during the HFDT window since no HF power packet is transferred, the magnitude of all the inductor currents deceases and the updated need of load connected to PN_{1L} is routed from DN_{1L} to DN_{1S}. Similar, during the second time slot of the TDM frame, HF power packet is routed from PN_{1S} to PN_{2L} through the HF channel. As can be observed from the experimental result provided in Figure 72, during this interval inductor current magnitude of L_1 and L_3 increases, and the inductor current of L_2 decreases.

Finally, experimental results provided in Figure 73 and Figure 74 verify that, depending on the load demand received by DN_{1S} from DN_{1L} and DN_{2L}, size of the HF power packet delivered to PN_{1L} and PN_{2L} can be adjusted to control the output voltages (V_{out1} and V_{out2}) of the SIMO HFDPS independently. In the experimental results provided in Figure 73, the output voltage of 20 V is generated at the load terminals of PN_{1L} and PN_{2L} by routing equal sized HF power packet to each LPES. Result provided in Figure 73 is obtained at an input voltage of 40 V and $\alpha_1 = \alpha_2 = 0.4$,

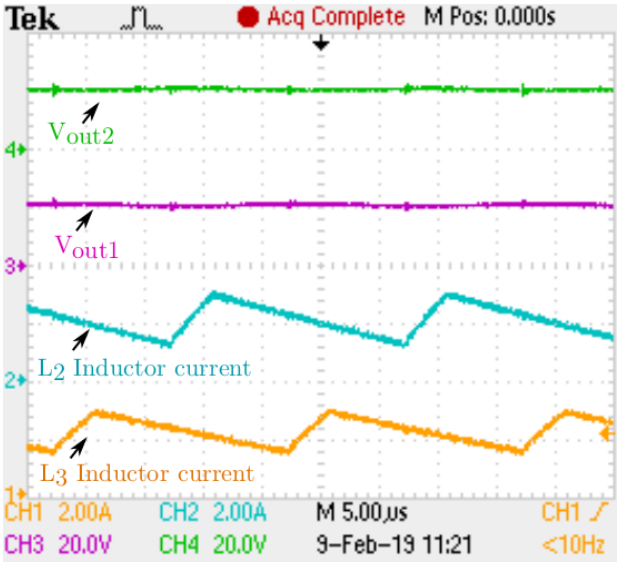


Figure 73. The experimental result when HF power packets of equal size are routed to PN_{1L} and PN_{2L} from PN_{1S}. Equal output voltage of 20 V is generated at V_{out1} and V_{out2} with V_{in} of 40 V.

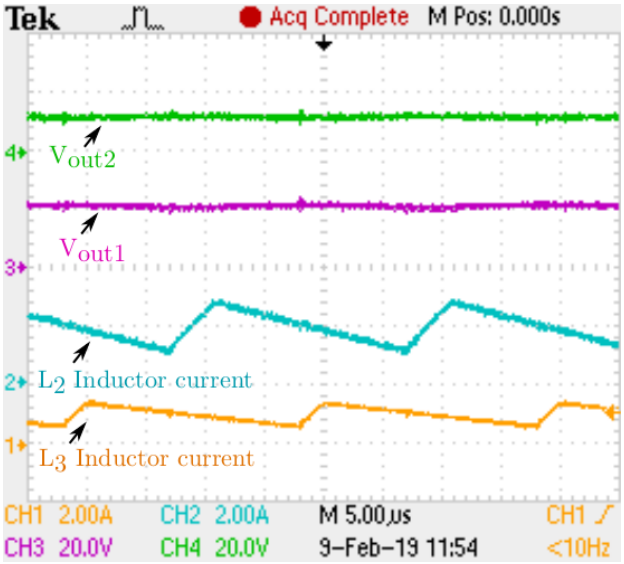


Figure 74. The experimental result when HF power packets with different size are routed to PN_{1L} and PN_{2L} from PN_{1S}. Output voltage of 20 V is generated at V_{out1} and 10 V is generated at V_{out2} with V_{in} of 40 V.

with a resistive load of 10 Ω connected at the output of each LPES. Values of α_1 and α_2 are transferred to DN_{1S} by DN_{1L} and DN_{2L}, respectively. For the same resistive loads and input voltage, the experimental result provided in Figure 74 demonstrate output voltages of 20 V and 10 V being obtained at the output terminals of PN_{1L} and PN_{2L}, respectively. This is achieved by creating HF power packets based on α_1= 0.42 and α_2 = 0.22 and routing them to the respective LPES which generated the request. In both Figure 73 and Figure 74, the arrival of a HF power packet at a LPES is associated with an increase in its inductor current. Maximum value of the inductor current depends on the size of the HF power packet that is received by the LPES.

3. Network Capacity for a SIMO HFDPS Feeding Multiple dc Loads

Next, a simulation study is provided for discussing the network capacity of the designed SIMO HFDPS. Network capacity for a SIMO HFDPS following sequential co-transmission scheme can be defined as the maximum number of power and data nodes that the HFDPS can support at any given time while successfully matching their performance parameters. These performance parameters can be in the form of load regulation, maximum output voltage, output voltage ripple, efficiency, etc. In this section, a case study is conducted to get a measure on the network capacity of the designed SIMO HFDPS that follows TDM for sequential power and data co-transfer.

For the case study, output voltage ripple has been considered as the performance parameter that is to be kept within 5% of the desired output voltage. A SIMO HFDPS is considered having one SPES and m LPES. HF Power and data packets are routed from the SPES to the LPESs sequentially following TDM. A complete TDM frame is considered to have a time duration of T_W which is subdivided in m equal time-slots to support m LPESs. All the LPESs are designed to have the same configuration with an output inductor of 100 μH and an output capacitor of 5μF. Input voltage to the SPES is fixed at 40 V and each LPES is required to produce 10 V at the output with a maximum output voltage ripple of 5%, i.e., the ripple magnitude needs to be less than 0.5 V for a 10 V output. If 4 μs is considered as the minimum time required for the HFDT window in the designed SIMO HFDPS. Then, the maximum allowable time allocation (α_{max}) in each time slot can be determined as

$$\alpha_{max} = \left[1 - \frac{4\mu * m}{T_W}\right], \tag{4.1}$$

where a positive value of α_{max} is a feasible outcome and determines the maximum size of the HF power packet that can be generated by the SPES in a TDM time slot of duration T_W/m. However, it is noted that, α_{max} can only determine if the TDM mode is feasible (HFDT window duration is sufficiently), whether the m^{th} LPES be able to attain the required output voltage using the routed HF power packet is governed by equation B.34 in Appendix B.

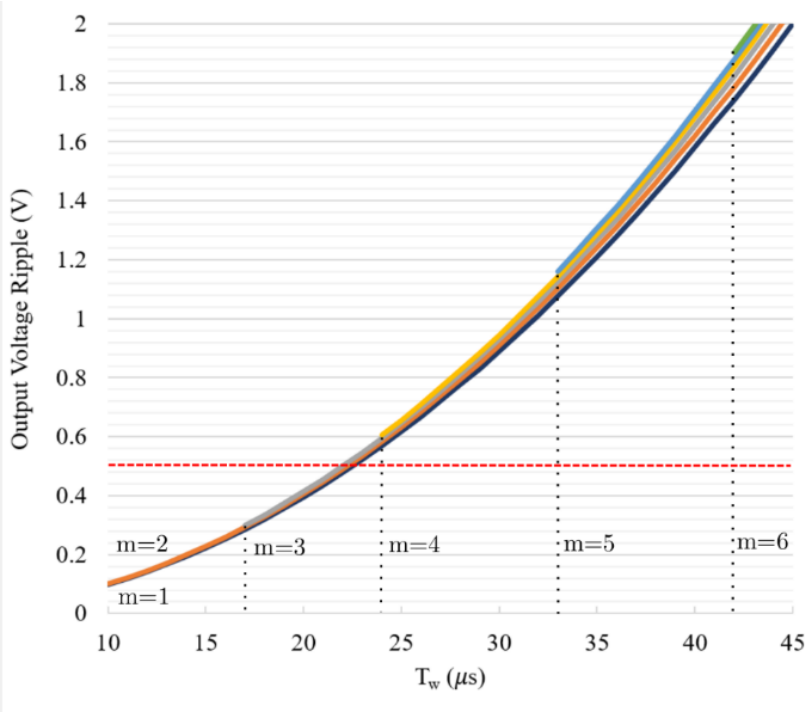


Figure 75. Variation in the output voltage ripple at each LPES generating 10 V output with 40 V input at the SPES. HF power and data packets are transferred over the HF channel using TDM with a frame time of T_W. m represents the number of LPES nodes connected on the SIMO HFDPS.

Using B.33 - B.36 (in Appendix B), Figure 75 shows the variation in the output voltage ripple with variable TDM frame time for $m \in [1,6]$. As can be observed from Figure 75, for achieving an output voltage of 10 V with 40 V input for a HFDPS with three LPESs, the minimum duration of T_W required is 17 μs. Required duration of T_W increases as the number of LPESs connected in the HFDPS are increased. For instance, to support a HFDPS with six LPESs generating an output voltage of 10 V each with 40 V input, the minimum duration of T_W required is 42 μs. This is because as the number of LPESs increase, the TDM frame is subdivided in multiple intervals of equal duration and the size of HF power packet that are routed to each LPES decreases (α_{max} decreses).

Moreover, as the duration of T_W is increased for a fixed number of nodes, the magnitude of output voltage ripple increases. For instance, if two LPESs are connected in the HFDPS, with T_W of 10 μs, only 0.1 V output voltage ripple is observed. However, for the same number of nodes if the duration of T_W is increased to 30 μs, an output voltage ripple of 0.9 V is observed. This is because, with an increased duration of T_W, the duration in which HF power packets are routed to each LPES increases and results in higher output ripple. As can be observed from Figure 75, the designed SIMO HFDPS can only support up to three LPESs while maintaining the performance parameter of 5% output voltage ripple. This limits the network capacity of the designed SIMO HFDPS to three LPESs.

One possible solution for increasing the network capacity is to increase the value of the output capacitors in each LPES. This increased output capacitor will act as a local energy storage buffer and maintain output voltage ripple within the permissible limit. However, this will result in the reduced dynamic performance of the HFDPS. Another solution is to increase the energy content of each HF power packet generated at SPES; this can be achieved either by increasing the input voltage or reducing the time required by the HFDT window.

4. Experimental Results for SIMO HFDPS Feeding ac Load

In this section, experimental results validating the operation of the designed SIMO HFDPS during dc/ac operation are provided. Experimental results are obtained on the experimental setup shown in Figure 67, with a 50 Ω resistive load connected differentially across PN_{1L} and PN_{2L}. Each time slot of the TDM frame has a duration of 10 μs and an SCI data rate of 4.68 Mbps is used.

Dc/ac operation is realized using an open-loop duty cycle. Lookup tables with reference modulation signals (as shown in Figure 86, Appendix C) are stored in DSP_2, and DSP_3, respectively. DN_{1S} is configured as Rx and DN_{1L} and DN_{2L} switch between Tx and Rx operation in each half-line cycle. Data packets exchanged during the HFDT window contain the address of the sender and information about the size of the HF power packet requested by the LPES. Once a data packet is received by DN_{1S}, during the next HFPT window, requested size of the HF power packet is routed towards the node where the request originated. During the positive- (negative-) half of the line cycle, requests are generated by DN_{1L} (DN_{2L}) and hence HF power packets are routed to PN_{1L} (PN_{2L}). It is assumed that, PN_{1S} is always

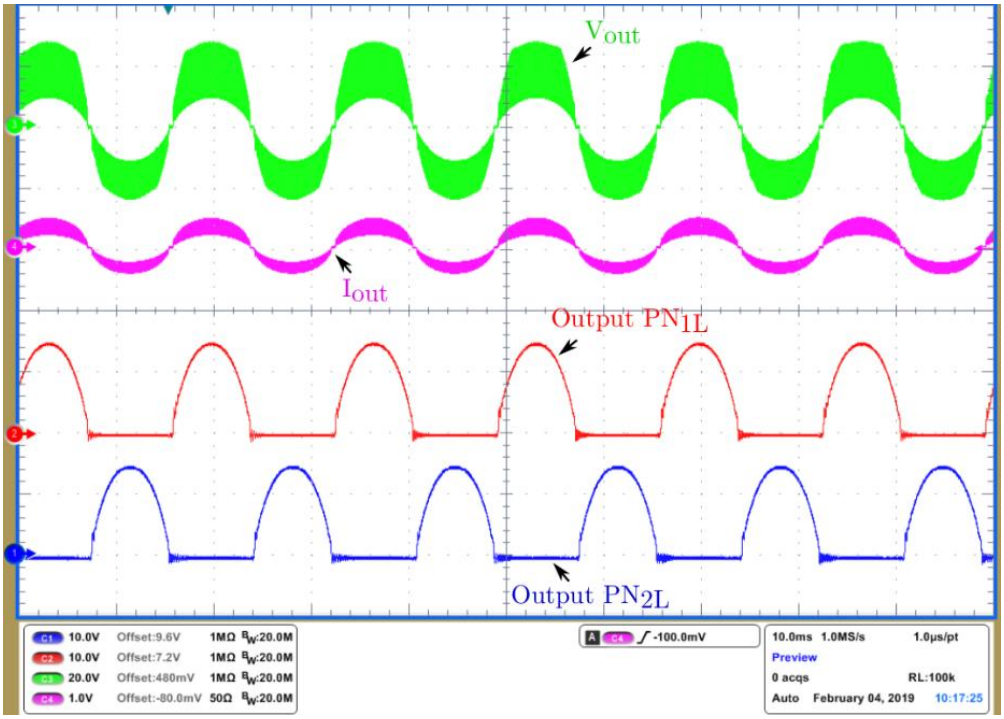


Figure 76. Experimental result of the SIMO HFDPS feeding an ac load. HF oscillations can be observed in V_{out} and I_{out} waveforms.

able to meet the request generated by PN_{1L} and PN_{2L}. Additionally, it is assumed that the physical placement of PN_{1L} and PN_{2L} are in close proximity.

Experimental result for the dc/ac mode of operation of the SIMO HFDPS is provided in Figure 76. Although, output voltage waveforms of PN_{1L} and PN_{2L} verify the routing of HF power packet to PN_{1L} during positive-half and PN_{2L} during the negative-half of the line cycle, HF oscillations can be observed in the differential output voltage and current that can lead to output voltage THD much higher than the permissible limit of 5%. These HF oscillations are caused by a combined effect of the parasitic inductance of the HF channel and LF differential load current (I_{out}) that is flowing between the two LPESs. Details about the cause of these HF oscillations are discussed next.

- *Effect of Parasitic Inductance*

A detailed analysis of the impact of parasitic inductance in HF power loops and gate driver loops of SPES and LPES has been provided in Chapter 3. The analysis provided in Chapter 3 is limited to PCB level parasitic inductance

and does not deal with the parasitic inductance present in the interconnections used between the SPES, LPES and the switch board in the experimental setup.

As the distance between various SPESs and LPESs is increased in an HFDPS, parasitic inductance induced by the interconnections becomes significant. For the SISO HFDPS supporting dc load, the solution to the increased parasitic inductance came in the form of increased snubber value across the power switch in LPES. Similarly, in the designed SIMO HFDPS, the same solution proved useful while supporting dc loads. This was because the designed SIMO HFDPS was operating as a SISO HFDPS during each time slot of the TDM frame and there were no interactions between the various LPESs. However, when the designed SIMO HFDPS is operated in a dc/ac mode, the line-frequency differential current (I_{out}) flows between PN_{1L} and PN_{2L}. This results in a low-frequency interaction between PN_{1L} and PN_{2L} and require analysis on the effect of parasitic inductance in its path.

A simplified circuit representation of the experimental SIMO prototype shown in Figure 67, is provided in Figure 77, in a dc/ac mode of operation. In the experimental setup, power nodes PN_{1S}, PN_{1L}, and PN_{2L} and the switch board are realized on separate PCB's and are connected using 10 cm long, 16 AWG twisted-wires. In Figure 77, these interconnections are represented using TW_1, TW_2, and TW_3. For better understanding, the location of the parasitic inductance in the current flow path, data nodes present on the switch board have been eliminated from Figure 77.

Block diagram representations of mode-1 and mode-2 of the SIMO HFDPS in dc/ac mode of operation (shown in Figure 41 (a) and Figure 41 (b)) are captured in Figure 78 and Figure 79, respectively. In Figure 78 and Figure 79, L_{AB} represents the lumped parasitic inductance between points A and B shown in Figure 77, and encompasses the parasitic inductance in the forward path of TW_1, the switch board PCB parasitic inductance and device parasitic inductance of S_{1PS}. Similarly, L_{BC} represents the lumped parasitic inductance between points B and C in Figure 77, and encompasses the parasitic inductance in the forward path of TW_2, the switch board PCB parasitic inductance and device parasitic inductance of S_{1PL}. L_{HG}, L_{GD}, and L_{GF}, represents, respectively the lumped parasitic inductance between points H- G, G- D, and G- F. In Figure 78 and Figure 79, lumped parasitic inductances have only been shown in the links that are active during mode-1 and mode-2 of the designed SIMO HFDPS during dc/ac mode of operation, respectively.

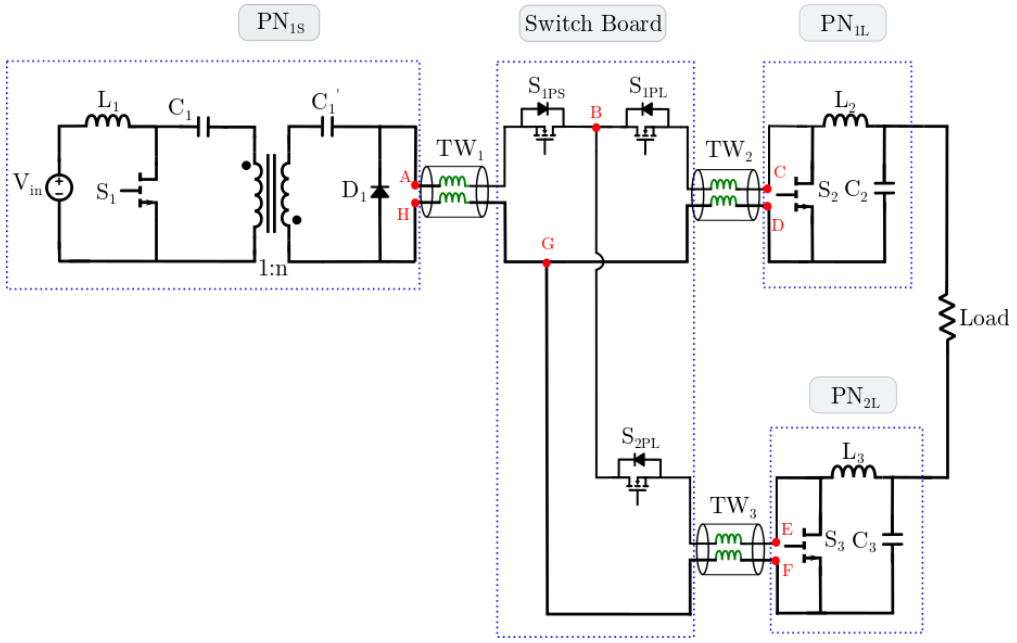


Figure 77. Simplified circuit representation of the experimental prototype shown in Figure 67, in a dc/ac mode of operation. TW_1, TW_2, and TW_3 represents the twisted-wires used for interconnecting PN_{1S}, PN_{1L}, and PN_{2L} to the switch board.

The HF (Red) and line-frequency (Blue) current flow directions when the HF power packet is routed from PN_{1S} to PN_{1L} during mode-1, are shown in Figure 78. During this mode of operation, the low-frequency current flows between all three power nodes PN_{1S}, PN_{1L}, and PN_{2L} through the load, L_{GF}, L_{HG}, L_{AB}, and L_{BC}. HF current flows between PN_{1S} and PN_{1L} through L_{AB}, L_{BC}, L_{GD}, and L_{HG}.

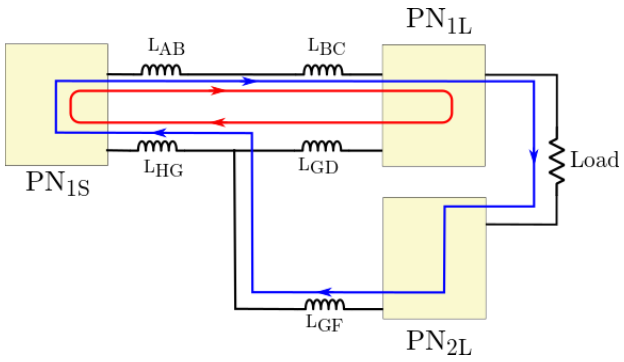


Figure 78. HF (Red) and line-frequency (Blue) current flow paths through the switch board in a block diagram representation during mode-1 of the SIMO HFDPS in a dc/ac operation.

During mode-2, transfer switches S_{1PS} and S_{1PL} are turned OFF and S_2 is turned ON. This limits the HF current to PN_{1L} as is shown in Figure 79. The low-frequency current during this mode flows between PN_{1L} and PN_{2L} through the load, L_{GF}, and L_{GD}. This results in the change in direction of the current flowing through L_{GD}, which was supporting HF current in reverse direction during mode-1. The sudden change in the direction of the current flowing through L_{GD} results in an induced voltage spike across it, which is ultimately reflected across the load. Similar effect will be observed with L_{GF} during the transition between mode-3 and mode-4 of the dc/ac operation.

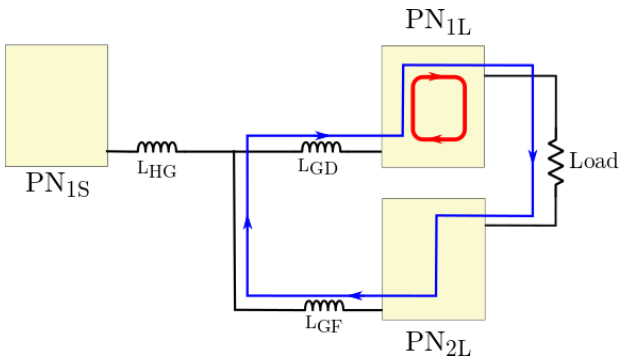


Figure 79. HF (Red) and line-frequency (Blue) current flow paths through the switch board in a block diagram representation during mode 2 of the SIMO network operating in the microinverter mode of operation.

The magnitude of these voltage spikes will depend on the value of L_{GD} and L_{GF}, load current and the transition time of current across the parasitic inductance. Solution to this problem can be the use of interconnections with low parasitic inductance. Additionally, the transition time of the current across the parasitic inductance can be increased, by slowing down S_2 and S_3. However, this will result in increased switching losses and in turn decrease system efficiency. Another solution is to add a capacitor across the load terminals that can provide a low impedance path to these HF oscillations and bypass them from entering the load.

Simulations results verifying the effect of adding parasitic inductance L_{GD} and L_{GF} in the ground return path of the SIMO HFDPS are provided in Figure 80. Simulation results are captured at an input voltage of 40 V with 50 Ω load connected differentially across PN_{1L} and PN_{2L}. To replicate the parasitic inductance, present in the hardware setup,

the parasitic inductance value of 200 nH is chosen. First, for validate the given hypothesis, the effect of ground inductance in a single ground return path is studied. Simulation result for the output voltage across the load provided in Figure 80 (a), shows HF oscillations during positive-half of the line cycle. This result is generated by selecting, L_{GD} = 200 nH and L_{GF} = 1pH. Simulation result provided in Figure 80 (a) validate that L_{GD} only come into play during mode-1 and mode-2 of the microinverter operation and has no impact on the output voltage waveform during mode-3 and mode-4. Similarly, the simulation result provided in Figure 80 (b) are generated using L_{GD} = 1pH and L_{GF}= 200 nH and validate that L_{GF} impacts the network during negative-half of the line cycle. Figure 80(c) shows the combined effect of the ground return path parasitic inductance. Result in Figure 80 (c) are generated using L_{GD} = 200 nH and L_{GF} = 200 nH. Figure 80 (d) shows the V_{out} waveform with considerably small HF oscillations when a 10 μF capacitor is connected across the load while keeping L_{GD} = 200 nH and L_{GF} = 200 nH.

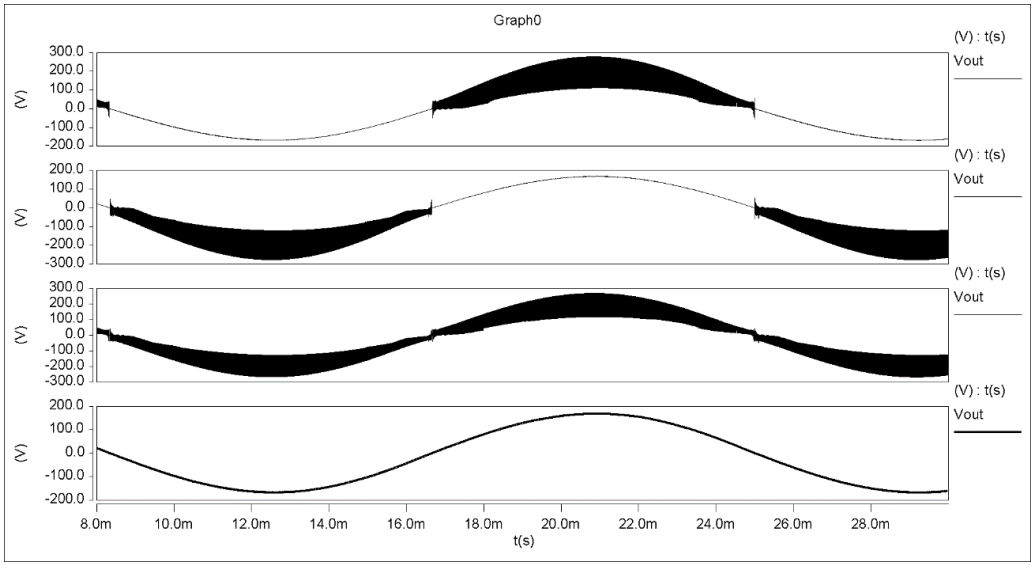


Figure 80. Simulation result for V_{out} with the parasitic inductance values of (a) L_{GD} = 200 nH and L_{GF} = 1pH, (b) L_{GD} = 1pH and L_{GF} = 200 nH, (c) L_{GD} = 200 nH and L_{GF} = 200 nH, and (d) L_{GD} = 200 nH, and L_{GF} = 200 nH and a 10 μF capacitor connected across the load terminals.

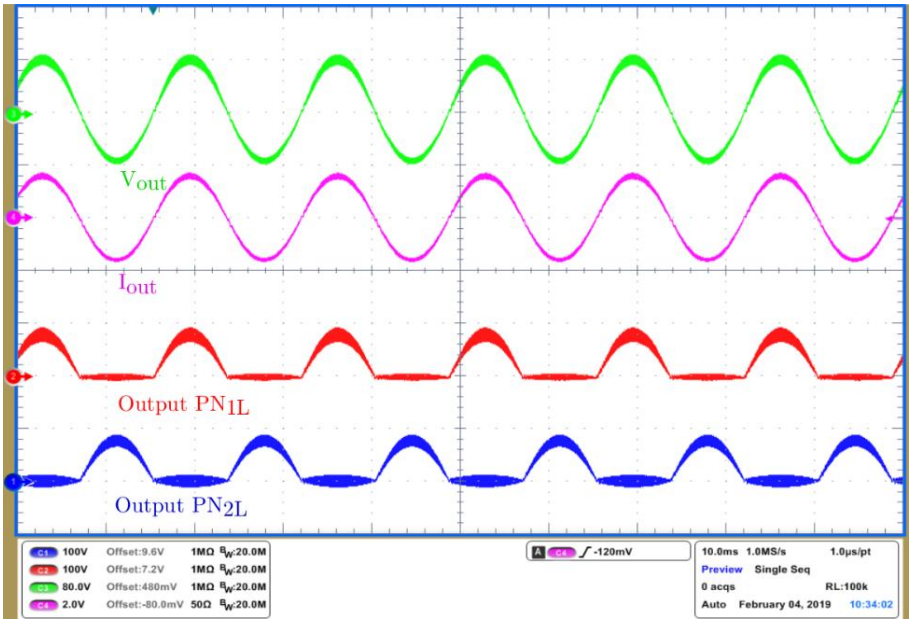


Figure 81. Experimental result of SIMO HFDPS feeding an ac load with a 10μF capacitor connected across it. HF oscillations in V_{out} and I_{out} waveforms are reduced.

Experimental results captured after connecting a 10 μF capacitor in parallel to the load resistor are provided in Figure 81. Adding a capacitor provided a low impedance path to the HF current component that were previously flowing through the load. This resulted in a reduction of the HF oscillations that were previously observed in V_{out}. However, the HF oscillations are now visible in the output voltage of PN_{1L} and PN_{2L} as can be observed in Figure 81.

The experimental result provided in Figure 82, display the HF power packets received by PN_{1L}, and PN_{2L} in the form of V_{ds} across S_2 and S_3 on Ch. 4 and Ch. 3, respectively. It can be verified that the HF power packets are routed to PN_{1L} (PN_{2L}) during the positive (negative)-half of the line cycle and the size of the HF power packets are based on the load requirement transferred to DN_{1S} by DN_{1L} (DN_{2L}) in the HFDT window. Next, in Figure 83, for the same operating conditions, voltage waveform on the HF channel is shown on Ch. 2. HF power packets that are routed to PN_{2L} are shown on Ch. 3 in the form of V_{ds} waveform across S_3. S_{1PL} blocks the HF power packets that are being routed from PN_{1S} to PN_{2L} during the negative-half of the line cycle from entering PN_{1L}, thus on Ch. 4 of Figure 83 V_{ds} waveform matching the HF power packet envelop is observed across S_{1PL}.

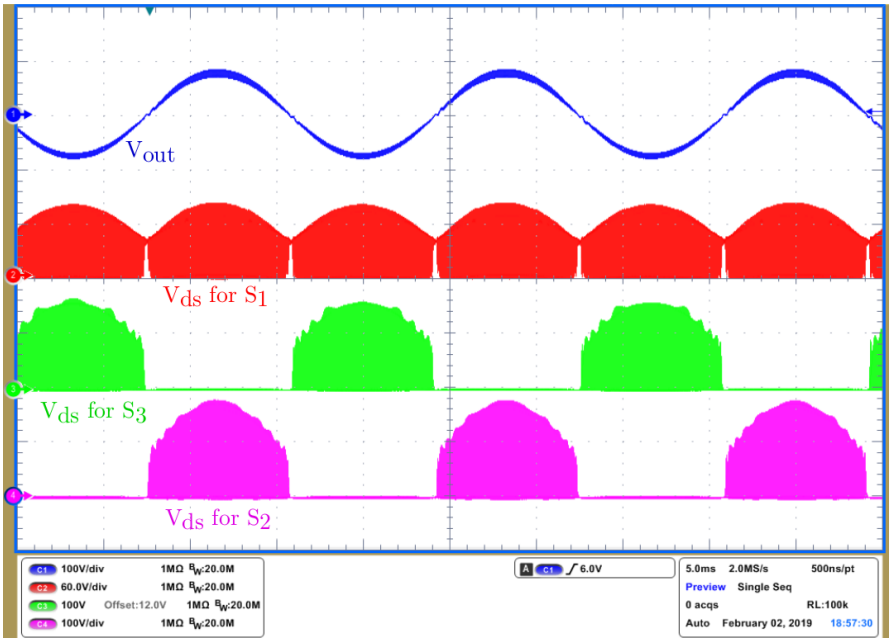


Figure 82. V_{out} along with V_{ds} waveforms across the power switches in the power nodes PN_{1S}, PN_{1L}, and PN_{2L}. Result is captured with V_{in}= 40 V and α_{max}= 0.51.

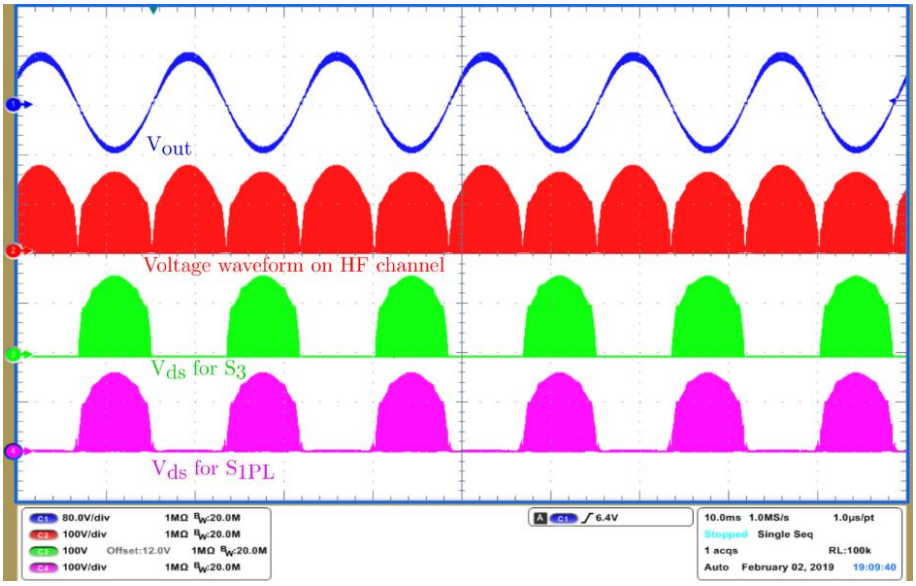


Figure 83. Experimental voltage waveform on Ch. 2 captures the HF power and data packets that are being routed through the HF channel using sequential co-transfer scheme. HF power packets routed to PN_{2L} are shown on Ch. 3. The same HF power packets are blocked from entering PN_{1L} by S_{1PL} and are shown Ch. 4.

E. Summary

In this Chapter, experimental results validating the feasibility of the sequential co-transmission scheme in a SISO and SIMO HFDPS are provided. First, using a SISO HFDPS, it was demonstrated that the size of the HF power packet generated by the SPES could be adjusted as per dynamically varying load demand by using the data nodes for information exchange. Next, it was experimentally proven that in a sequential co-transfer scheme data rate is independent of the frequency of power transfer, and no complex analog-filtering circuitry is required for coupling and decoupling data signals on the HF channel, as is usually the case in conventional PLC. In the experimental prototype, a transitional coupling between the power and the data nodes was observed due to non-ideal behavior of the semiconductor devices. To eliminate the effect of data corruption caused by it, a modified SCI protocol was implemented. Further, it was observed that at higher power levels, transitional coupling resulted in the failure of the data nodes. To protect the data nodes against transient current induced by it, a two-stage protection circuit was designed and implemented in the data nodes. Moreover, a data correction circuit was added to Rx to preclude the need of signature bits and increase the payload capacity of the SCI data frame. A reduction in the voltage level of data bits was observed on the HF channel while using the modified data node design. The reference voltage of the comparator in Rx was readjusted to recreate the data bits.

Next, routing of the HF power packets using sequential co-transfer scheme was experimentally verified on a SIMO HFDPS. In the experimental setup, an additional snubber was added across the transfer switches in a SIMO HFDPS. Using a single SPES and two LPES, it was experimentally demonstrated that HF power packets could be flexibly managed and routed to different loads using TDM. Additionally, using a case study, it was established that for supporting a higher number of nodes in a SIMO HFDPS either data packet size needs to be reduced or higher TDM frame time is required. Further, increased ground parasitic inductance was determined as the cause of HF oscillations that were observed during the dc/ac operation of the SIMO HFDPS in Figure 76. Adding a capacitor across load resulted in a reduction of these HF oscillations.

Chapter 5

Conclusions and Future Works

A. Summary and Contributions

HFDPS has significant advantages over the conventional DPS in terms of energy-efficiency, reliability, power-density, and rapid-response. To realize these advantages and for enabling the optimal utilization of the available resources in an HFDPS, designing a suitable communication architecture is of paramount importance. However, the presently available simultaneous and sequential communication schemes have various limitations in terms of available communication bandwidth, complex system design yet lower data rates and applicability for high power designs.

In this dissertation, first, an approach for the co-transfer of HF power and data signals over a common channel is outlined. In the proposed approach, power and data signals are transferred mutually exclusive in a sequential manner, which guarantees the availability of complete channel bandwidth for either power or data signals. Secondly, in contrast to the available wire-based communication architectures, using the developed scheme, it is experimentally validated that the data transfer rate is independent of the frequency of power transfer. Third, it is shown that the proposed sequential co-transfer scheme provides a highly simplified hardware solution avoiding the use of complex analog-filtering circuitry for coupling and decoupling data signals on the HF channel. Further, the developed scheme seamlessly decouples the power and data networks which enable higher power applications resulting due to the drastic reduction in EMI emissions generated by the high-voltage switching transient in the data signals present in the state-of-the-art techniques for packetized power and data transfer.

Further, to prove the efficacy of the above-mentioned scheme, in this dissertation, two case illustrations (a) SISO HFDPS and (b) SIMO HFDPS have been chosen. For the SISO HFDPS, the load demand was dynamically varied, and it was verified whether the HFDPS was able to react to such fast-varying operating conditions without deteriorating overall system performance. The high rate of data transfer and dynamic HF power packet size adjustment

helped in attaining satisfactory steady-state and transient performance. Next, based on load demand, the feasibility of HF power packet routing was experimentally verified using a SIMO HFDPS. First, it was experimentally demonstrated on the designed SIMO HFDPS that the discrete HF power packets could be flexibly managed and routed to different dc loads using TDM. Further, it was experimentally verified that the output voltage of each dc load could be controlled independently depending on the size of the received HF power packet. Next, using the ability to manage the output voltage of each LPES independently, a reduced order DMCI topology was realized by connecting a load differentially to two LPESs. The reduced-order DMCI provided satisfactory steady-state performance.

For the experimental validation of the sequential co-transfer scheme, SPES and LPES have been designed using the next generation ultra-fast GaN-FETs to meet futuristic PES demands in terms of ever-increasing efficiency and power density requirements. Notwithstanding, the rapid switching transition of the GaN-FETs may create EMI issues in the SPES and LPES that have been properly addressed and resolved in this dissertation via strict HF gate and power loop designs. Moreover, in the experimental converter, a transitional coupling between the power- and the data-transmission nodes is observed due to the non-ideal behavior of the semiconductor devices. Initially, to eliminate data corruption caused by it, a modified SCI protocol was implemented. However, with increased system power ratings apart from data corruption, the transitional coupling resulted in the failure of data nodes. Hence, a modified data node design with a two-stage protection scheme and a data correction circuit was designed and implemented to mitigate the above-mentioned predicaments. Thus, resolving the practical design and protection issues in the power and data nodes woven fine with the efficacies of the sequential co-transfer scheme, previously delineated, helped sustained operation of the entire system at increased power ratings.

B. Future Work

The research work delineated in this dissertation can be extended to encompass the following future works:

- A multi-input-multi-output (MIMO) HFDPS design can be synthesized and the necessary HF power packet routing and data transfer protocols can be designed for both the source and load side management.
- Clock synchronization schemes can be explored for attaining full decentralization.

- Owing to the symmetrical nature of the designed HFDPS its bi-directional capability can be verified using it in a battery management system.
- Since, the main focus of this dissertation was to validate the proposed scheme for sequential co-transfer of HF power and data signals, full-scale optimization of the complete HFDPS has not been undertaken. It can lead to an interesting future work possibility where performance measures like transmission efficiency, power quality and power density can be investigated.

APPENDICES

APPENDIX A

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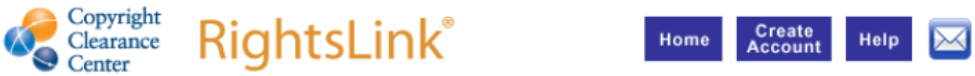
APPENDIX A (Continued)



Title: Generalized Input Impedance Modeling of TL-Network-Based HFDPS for Validating Frequency-Dependent Criteria for Power-Signal Integrity
Author: Ankit Gupta
Publication: Industrial Electronics, IEEE Transactions on
Publisher: IEEE
Date: May 2018

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APPENDIX A (Continued)

APPENDIX A (Continued)

APPENDIX A (Continued)

APPENDIX A (Continued)

APPENDIX B

B. Modes of operation of the Designed SIMO HFDPS Feeding dc Loads

The modes of operation of the SIMO HFDPS shown in Figure 35 with various switches following the switching sequence outlined in Figure 36 can be delineated as follows:

A) ***Mode-1:*** ($t_0 \leq t < t_1$)

During mode-1 (as shown in Figure 37), the HF channel is used for the transfer of HF power packet from PN_{1S} to PN_{1L}. Mode-1 starts at t_0 when switch S_1 is turned ON, current in the input inductor (I_{L1}) of PN_{1S} "L_1" starts building as it is directly connected across the input supply voltage V_{in}. Transfer switches S_{1PS} and S_{1PL} are synchronized with the power switch in PN_{1S} "S_1" and are turned ON to provide a path for the HF power packet to be transferred to PN_{1L} through the HF channel. The HF power packet, that is transferred over the HF channel in mode-1, supports the load current of PN_{1L} and is generated by the blocking capacitors C_1 and C_1' in PN_{1S}. During this mode of operation, data switches S_{1DS}, S_{1DL}, and S_{2DL} in the switching-link are turned OFF for isolating the data network from the HF channel. Additionally, the transfer switch S_{2PL} in the switching-link is also turned OFF for avoiding the HF power packet from entering the power node PN_{2L}. In mode-1, the load current of PN_{2L} is supported by the energy stored in the inductor "L_3".

If we consider α_1 to be the time allocation for various switch states in mode-1, then $\alpha_1 * T_w/2$ is the total conduction time for S_1 in mode-1 and determines the size of the HF power packet generated during this mode. Various state equations in mode-1 for the designed SIMO HFDPS can be written as follows:

$$L_1 \frac{dI_{L1}}{dt} = V_{in} \tag{B.1}$$

$$L_2 \frac{dI_{L2}}{dt} = nV_{C1} + \frac{C_1}{nC_1'} V_{C1} - V_{out1} \tag{B.2}$$

$$L_3 \frac{dI_{L3}}{dt} = -V_{out2} \tag{B.3}$$

APPENDIX B (Continued)

$$C_1 \frac{dV_{C1}}{dt} = -nI_{L2} \quad \text{(B.3)}$$

$$C_2 \frac{dV_{C2}}{dt} = I_{L2} - \frac{V_{out1}}{R_1} \quad \text{(B.4)}$$

$$C_3 \frac{dV_{C3}}{dt} = I_{L3} - \frac{V_{out2}}{R_2} \quad \text{(B.5)}$$

In (B.1) - (B.5), n represents the turns ratio of the transformer and the state variables I_{L1}, I_{L2}, I_{L3}, V_{C1}, V_{C2}, and V_{C3} are, respectively, the current flowing through inductor L_1, L_2 and L_3, and the voltage across capacitors C_1, C_2 and C_3. The secondary-side capacitor voltage in the power node PN_{1S} "C_1'" is proportional to the primary side capacitor voltage "C_1" and as such no additional states are needed to capture its dynamics. It is noted that, as in the case of a SISO HFDPS, in the SIMO HFDPS, additional time allocation may be required for the transfer switches to provide a conducting path for the transformer leakage current that flows to the load when S_1 is turned OFF.

B) ***Mode-2:*** ($t_1 \leq t < t_2$)

During mode-2 (as shown in Figure 38), the HF channel is used for the transfer of HF data packet between DN_{1S}, DN_{1L}, and DN_{2L}. Mode-2 starts when S_1 in PN_{1S} is turned OFF. During this mode of operation, the energy stored in the input inductor of PN_{1S} "L_1" is used to charge the blocking capacitors $C_1$and C_1'. Load connected to power nodes PN_{1L} and PN_{2L} are fed from the energy stored in inductors L_2 and L_3, respectively. Transfer switches S_{1PS}, S_{1PL}, and S_{2PL} are turned OFF during this mode of operation for isolating the power nodes PN_{1S}, PN_{1L}, and PN_{2L}, respectively from the HF channel. In one of its embodiments, mode-2 can be used for transferring the requirements/status of PN_{2L} to PN_{1S} by configuring DN_{2L} as Tx and DN_{1S}, and DN_{1L} as Rx, using the SPDT switch available in each data node.

If α_1 is considered as the time allocation of various switch states in mode-1, then time duration available for mode-2 can be given by $(1 - \alpha_1) * T_w/2$. For a successful data exchange, a complete frame of data

APPENDIX B (Continued)

following modified SCI protocol needs to be transmitted over the HF channel during mode-2. This puts a limit to the minimum time duration required for mode-2 and subsequently limits the maximum value of α_1 and puts a limit on the maximum size of the generated HF power packet. Various state equations in mode-2 for the SIMO HFDPS can be written as follows:

$$L_1 \frac{dI_{L1}}{dt} = V_{in} - V_{C1} - \frac{C_1}{n^2 C_1'} V_{C1} \tag{B.6}$$

$$L_2 \frac{dI_{L2}}{dt} = -V_{out1} \tag{B.7}$$

$$L_3 \frac{dI_{L3}}{dt} = -V_{out2} \tag{B.8}$$

$$C_1 \frac{dV_{C1}}{dt} = I_{L1} \tag{B.9}$$

$$C_2 \frac{dV_{C2}}{dt} = I_{L2} - \frac{V_{out1}}{R_1} \tag{B.10}$$

$$C_3 \frac{dV_{C3}}{dt} = I_{L3} - \frac{V_{out2}}{R_2} \tag{B.11}$$

C) ***Mode-3:*** $(t_2 \leq t < t_3)$

During mode-3 (as shown in Figure 39), the HF channel is used for the transfer of HF power packet from PN_{1S} to PN_{2L}. Mode-3 starts at t_2 when S_1 is again turned ON, this time during the second time slot of the TDM frame. Current in the input inductor (I_{L1}) of PN_{1S} "L_1" starts building as it is directly connected across the input supply voltage V_{in}. Contrary to the switching states of transfer switches in mode-1, during mode-3, transfer switches S_{1PS} and S_{2PL} are synchronized with the power switch in PN_{1S} "S_1" and are turned ON to route the HF power packet generated at PN_{1S} to PN_{2L} through the HF channel. The HF power packet that is routed through the HF channel in mode-3 supports the load current of PN_{2L} and is generated by the blocking capacitors C_1 and C_1' in PN_{1S}. During this mode of operation data switches S_{1DS}, S_{1DL}, and S_{2DL} in the switching-link are turned OFF for isolating the data nodes from the HF channel. Additionally, the transfer

APPENDIX B (Continued)

switch S_{1PL} in the switching-link is also turned OFF for avoiding the HF power packet from entering the power node PN_{1L}. In mode-3, the load current of PN_{1L} is supported by the energy stored in the inductor "L_2".

If we consider α_2 to be the time allocation for various switch states in mode 3, then $\alpha_2 * T_w/2$ is the total conduction time for the switch S_1 in mode-3 that governs the size of the generated HF power packet. Various state equations in mode-3 for the SIMO HFDPS can be written as follows:

$$L_1 \frac{dI_{L1}}{dt} = V_{in} \tag{B.12}$$

$$L_2 \frac{dI_{L2}}{dt} = -V_{out1} \tag{B.13}$$

$$L_3 \frac{dI_{L3}}{dt} = nV_{C1} + \frac{C_1}{nC_1'} V_{C1} - V_{out2} \tag{B.14}$$

$$C_1 \frac{dV_{C1}}{dt} = -nI_{L3} \tag{B.15}$$

$$C_2 \frac{dV_{C2}}{dt} = I_{L2} - \frac{V_{out1}}{R_1} \tag{B.16}$$

$$C_3 \frac{dV_{C3}}{dt} = I_{L3} - \frac{V_{out2}}{R_2} \tag{B.17}$$

D) *Mode 4:* ($t_3 \leq t < t_4$)

Mode-4 is analogous to mode-2 in terms of the state of various switches in the SIMO HFDPS. During mode-4 (as shown in Figure 38), the HF channel is used for the transfer of HF data packet between DN_{1S}, DN_{1L}, and DN_{2L}. Mode-4 starts when S_1 in PN_{1S} is turned OFF during the second time slot. During this mode of operation, the energy stored in the input inductor of PN_{1S} "L_1" is used to charge the blocking capacitors $C_1$and C_1'. The load connected to power nodes PN_{1L} and PN_{2L} are fed from the energy stored in inductors "L_2" and "L_3", respectively. Transfer switches S_{1PS}, S_{1PL}, and S_{2PL} are turned OFF during this mode of

APPENDIX B (Continued)

operation for isolating the power nodes PN_{1S}, PN_{1L}, and PN_{2L}, respectively from the HF channel. In one of its embodiments, mode-4 can be used for transferring the requirements/status of PN_{1L} to PN_{1S} by configuring DN_{1L} as Tx and DN_{1S}, and DN_{2L} as Rx, using the SPDT switch available in each data node.

If α_2 is considered the time allocation of various switch states in mode-3, time duration available for mode-4 can be given by $(1-\alpha_2) * T_w/2$. For a successful data exchange, a complete frame of data following modified SCI protocol needs to be transmitted over the HF channel during mode-4. This puts a limit to the minimum time duration required for mode 4 and subsequently limits the maximum value of α_2 which puts a limit on the maximum size of the generated HF power packet in mode-3. Various state equations in mode-4 for the SIMO HFDPS can be written as follows:

$$L_1 \frac{dI_{L1}}{dt} = V_{in} - V_{C1} - \frac{C_1}{n^2 C_1'} V_{C1} \tag{B.18}$$

$$L_2 \frac{dI_{L2}}{dt} = -V_{out1} \tag{B.19}$$

$$L_3 \frac{dI_{L3}}{dt} = -V_{out2} \tag{B.20}$$

$$C_1 \frac{dV_{C1}}{dt} = I_{L1} \tag{B.21}$$

$$C_2 \frac{dV_{C2}}{dt} = I_{L2} - \frac{V_{out1}}{R_1} \tag{B.22}$$

$$C_3 \frac{dV_{C3}}{dt} = I_{L3} - \frac{V_{out2}}{R_2} \tag{B.23}$$

When observed carefully, during each time slot of the TDM frame, the designed SIMO HFDPS follows the same modes of operation as the SISO HFDPS. In the time interval t_0 - t_2 shown in Figure 36, the designed SIMO HFDPS operates as a SISO HFDPS with PN_{1S} as the SPES and PN_{1L} operating as a LPES. During the first time slot of the TDM frame (t_0 - t_2), PN_{2L} operates independently. Similarly, during the time interval t_2 - t_4 shown in Figure 36, the

APPENDIX B (Continued)

designed SIMO HFDPS operates as a SISO HFDPS with PN_{1S} operating as the SPES and PN_{2L} operating as a LPES. Furthermore, PN_{1L} operates independently during this time duration. The transfer of HF power packets to the two power receiver nodes (PN_{1L} and PN_{2L}) in the designed SIMO HFDPS is achieved during one complete TDM frame. Hence, for maintaining a stable steady-state operation of the designed SIMO HFDPS, inductors L_1, L_2, and L_3 need to maintain their volt-second balance in one TDM frame of duration T_w.

Using B.1 - B.23 and applying inductor volt-second balance on the three inductors, L_1, L_2, and L_3 during the four modes of operation of the designed SIMO HFDPS, one obtains

for L_1,

$$\frac{V_{in}*\alpha_1\frac{T_w}{2}+\left[V_{in}-V_{C1}-\frac{C_1}{n^2C_1'}V_{C1}\right]*\alpha_1'\frac{T_w}{2}+V_{in}*\alpha_2\frac{T_w}{2}+\left[V_{in}-V_{C1}-\frac{C_1}{n^2C_1'}V_{C1}\right]*\alpha_2'\frac{T_w}{2}}{T_w}=0 \tag{B.24}$$

for L_2,

$$\frac{\left[nV_{C1}+\frac{C_1}{nC_1'}V_{C1}-V_{out1}\right]*\alpha_1\frac{T_w}{2}+[-V_{out1}]*\alpha_1'\frac{T_w}{2}+[-V_{out1}]*\alpha_2\frac{T_w}{2}+[-V_{out1}]*\uparrow\alpha_2'\frac{T_w}{2}}{T_w}=0 \tag{B.25}$$

for L_3,

$$\frac{[-V_{out2}]*\alpha_1\frac{T_w}{2}+[-V_{out2}]*\alpha_1'\frac{T_w}{2}+\left[nV_{C1}+\frac{C_1}{nC_1'}V_{C1}-V_{out2}\right]*\alpha_2\frac{T_w}{2}+[-V_{out2}]*\alpha_2'\frac{T_w}{2}}{T_w}=0 \tag{B.26}$$

Solution for α_1 and α_2 yields

$$\alpha_1=\frac{2V_{out1}}{nV_{in}+V_{out1}+V_{out2}} \tag{B.27}$$

$$\alpha_2=\frac{2V_{out2}}{nV_{in}+V_{out1}+V_{out2}} \tag{B.28}$$

and the solution for V_{out1} and V_{out2} yields

$$V_{out1}=\frac{nV_{in}\alpha_1}{2-\alpha_1-\alpha_2} \tag{B.29}$$

APPENDIX B (Continued)

$$V_{out2} = \frac{nV_{in}\alpha_2}{2-\alpha_1-\alpha_2}. \tag{B.30}$$

Furthermore, the expression for output voltage ripple ΔV_{out1} and ΔV_{out2} can be computed as

$$\Delta V_{out1} = \frac{V_{out1}}{16L_2C_2}\left(1 - \frac{V_{out1}}{nV_{in}+V_{out1}+V_{out2}}\right)^2 {T_w}^2 \tag{B.31}$$

$$\Delta V_{out2} = \frac{V_{out2}}{16L_3C_3}\left(1 - \frac{V_{out1}}{nV_{in}+V_{out1}+V_{out2}}\right)^2 {T_w}^2. \tag{B.32}$$

A generalized expression for the time allocation, output voltage and output voltage ripple in a SIMO HFDPS with one SPES and m LPES, and for $i \in [1, m]$ can be written as

$$\alpha_i = \frac{mV_{outi}}{nV_{in}+\left[\sum_{j=1}^{m} V_{outj}\right]} \tag{B.33}$$

$$V_{outi} = \frac{nV_{in}\alpha_i}{m-\left[\sum_{j=1}^{m} \alpha_j\right]} \tag{B.34}$$

$$\Delta V_{outi} = \frac{V_{outi}}{16L_{i+1}C_{i+1}}\left(1 - \frac{V_{outi}}{nV_{in}+\left[\sum_{j=1}^{m} V_{outj}\right]}\right)^2 {T_w}^2. \tag{B.35}$$

For a fixed TDM frame time T_w, if 0.6 is assumed as the maximum limit on α_1 and α_2 imposed by the minimum time required for HFDT window in mode-2 and mode-4. Then, Figure 84 and Figure 85 provides a 3-D representation of the achievable output voltages V_{out1} and V_{out2} at PN_{1L} and PN_{2L}, respectively, with different combinations of α_1 and $\alpha_2\ \epsilon[0, 0.6]$ at an input voltage (V_{in}) of 20 V, 40 V, and 60 V at PN_{1S}. As can be observed from B.29 and B.30, and Figure 84 and Figure 85, output voltages of both PN_{1L} and PN_{2L} depends on the value of time allocation α_1 and α_2. Hence, for attaining a fixed output voltage in a SIMO HFDPS following the sequential co-transfer scheme, time allocation values need to be adjusted for both the power nodes PN_{1L} and PN_{2L}.

APPENDIX B (Continued)

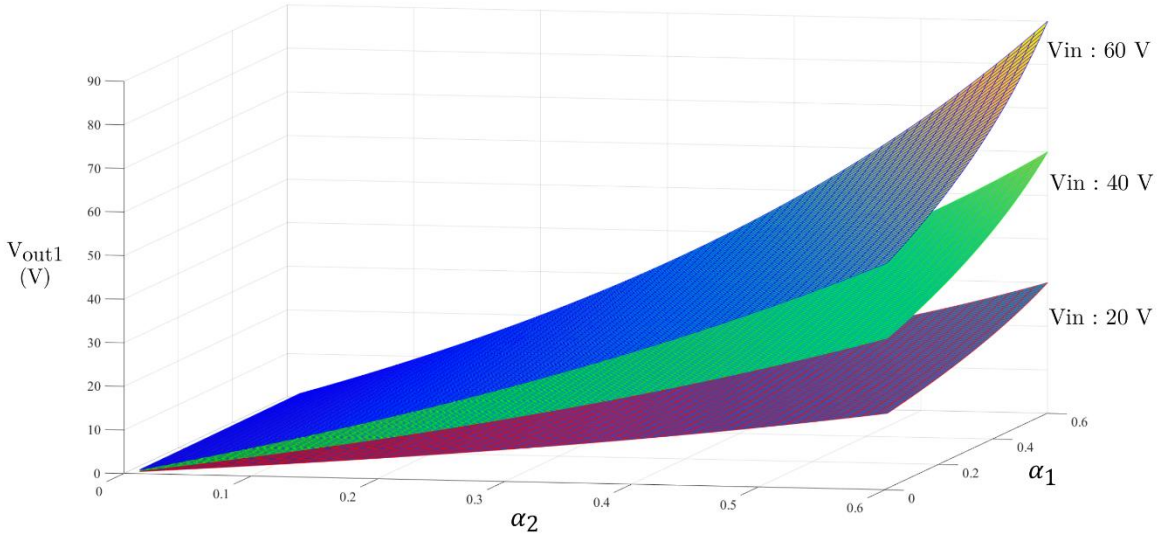


Figure 84. Variation in V_{out1} with the time alocation α_1 and α_2 $\epsilon[0, 0.6]$ for V_{in} of 20 V, 40 V and 60V.

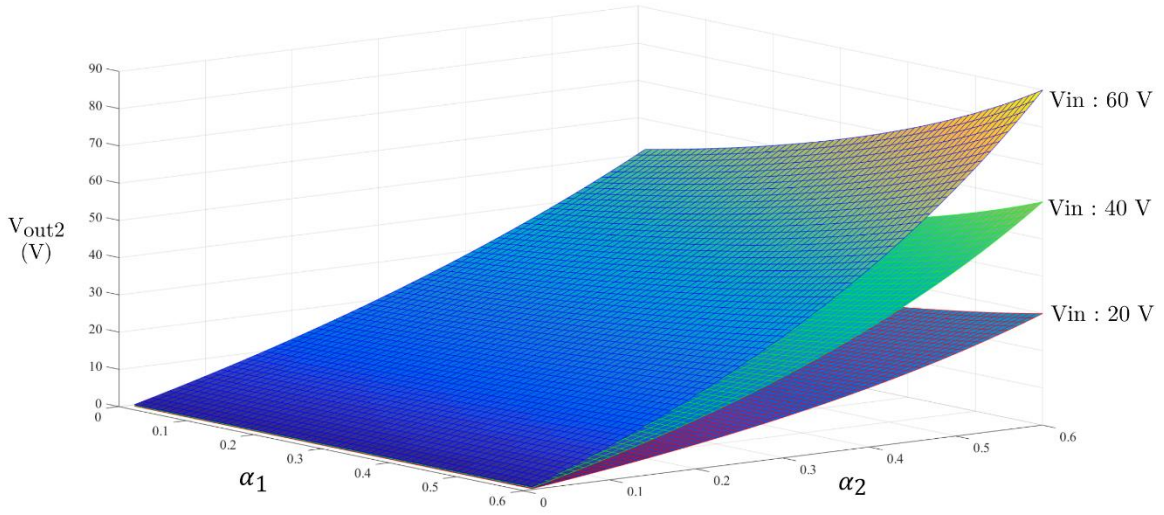


Figure 85. Variation in V_{out2} with the time alocation α_1 and α_2 $\epsilon[0, 0.6]$, for V_{in} of 20 V, 40 V and 60V.

APPENDIX C

C. Modes of operation of the Designed SIMO HFDPS Feeding ac Loads

During mode-1, as shown in Figure 41 (a), transfer switches S_{1PS} and S_{1PL}, and power switches S_1 and S_3 are turned ON, while data switches S_{1DS}, S_{1DL}, and S_{2DL}, transfer switch S_{2PL} and the power switch S_2 are turned OFF. Current flowing through the input inductor L_1 of power node PN_{1S} increases and the inductor stores energy. The blocking capacitor C_1 in PN_{1S} discharges through S_1 resulting in the transfer of energy from the primary-side of HF transformer to the secondary. The energy stored in the secondary-side blocking capacitor C_1' of PN_{1S} is routed to PN_{1L} through the HF channel. HF power packet routed from PN_{1S} to PN_{1L}, results in an increase in the current flowing through the inductor L_2 of power node PN_{1L} and supports the load current. This HF power packet is blocked from entering PN_{2L} by turning OFF the transfer switch S_{2PL}. Power switch S_3 in PN_{2L} remains ON during this mode of operation for providing a continuous path to the load current.

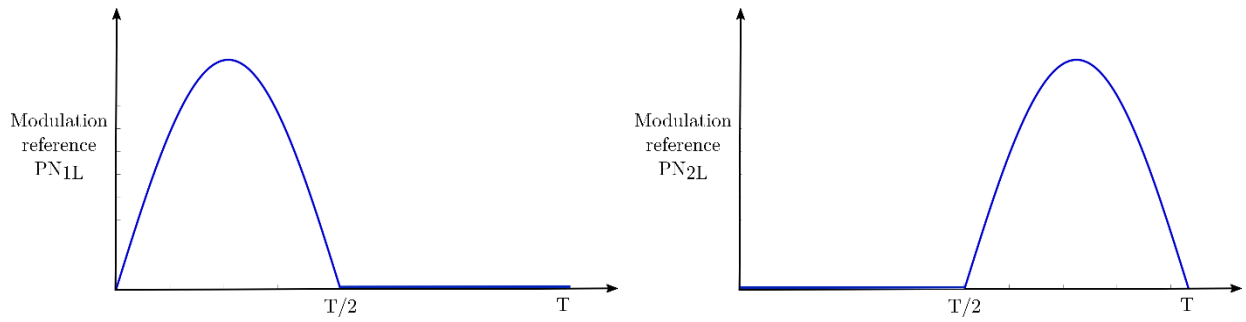
During mode-2, as shown in Figure 41 (b), the HF channel is used for the transfer of data packets between the data nodes DN_{1S}, DN_{1L}, and DN_{1S}. This is achieved by disconnecting the power nodes PN_{1S}, PN_{1L}, and PN_{2L} from the HF channel by turning OFF transfer switches S_{1PS}, S_{1PL}, and S_{2PL}, respectively and connecting data nodes DN_{1S}, DN_{1L}, and DN_{2L} to the HF channel by turning ON data switches S_{1DS}, S_{1DL}, and S_{2DL}, respectively. During this mode of operation, power switch S_1 in PN_{1S} is turned OFF and blocking capacitors C_1 and C_1' are charged using the energy which was stored in the inductor L_1 during mode-1. Diode D_1 in PN_{1S} freewheels to support the charging current for C_1'. Additionally, the power switch S_2 in PN_{1L} is turned ON and support the inductor current of L_2 which discharges in the load. During mode 2, switch S_3 in PN_{2L} remains ON and provides a continuous path to the load current.

In mode-3, as shown in Figure 41 (c), the HF power packet is routed from PN_{1S} to PN_{2L} through the HF channel. This is achieved by turning ON S_{1PS} and S_{2PL} and turning OFF S_{1DS}, S_{1DL}, S_{2DL}, and S_{1PL} in the switching link. Operation of PN_{1S} in mode-3 is similar to its operation in mode-1, with the exception that the HF power packet generated at PN_{1S} is now routed to PN_{2L}. During mode-3, the power switch S_2 in PN_{1L} remains ON and supports the load current, which now flows in the negative direction. Transfer switch S_{1PL} remains OFF during this mode of

APPENDIX C (Continued)

operation and blocks the HF power packet routed on the HF channel from entering PN_{1L}. Finally, mode-4, as is shown in Figure 41 (d) is similar in operation to mode-2, with the exception that the load current is negative and negative voltage is generated across the load terminals.

Modes of operation of the designed SIMO HFDPS feeding ac load, follow the modes of operation of DMCI under DMS closely. The main difference between the two arises because of the use of a single power transmitter node in the former. Reference modulation signal for the power switch S_2 and S_3 in PN_{1L} and PN_{2L} are given in Figure 86 (a) and Figure 86 (b), respectively. During the positive-half of the line cycle $(0 - T/2)$, load requests are transferred to DN_{1S} by DN_{1L} and the power switch S_2 in PN_{1L} operates in a complementary manner to S_1 to accept the HF power packet. Power switch S_3 in PN_{2L} remains ON during the complete duration of the first-half of the line cycle $(0 - T/2)$. During the second half of the line cycle $(T/2 - T)$, load requests are transferred to DN_{1S} by DN_{2L} and the power switch S_3 in PN_{2L} operates in a complementary manner to S_1, and S_2 in PN_{1L} remains ON. Since, during each half of the line cycle, SIMO HFDPS replicates DMCI modes of operation, the output-to-input relationship of the two is equivalent and a static-inverse-transformation as provided in [70] is used to compensate for the output-to-input nonlinearity.



(a) **(b)**

Figure 86.The modulation reference signal for the power node (a) PN_{1L} and (b) PN_{2L}, when SIMO HFDPS is feeding ac load using the sequential co-transfer scheme. T refers to the time-period of a full line cycle.

APPENDIX D

D. Thermal Design of a GaN-Based Power Converter

Plot outlining the temperature dependence of the turn-on resistance ($R_{DS(on)}$) of GaN Systems GS66508P GaN FET is provided in [64, Figure 11]. It can be observed that, the junction temperature and the $R_{DS(on)}$ have a non-linear relation. This signifies an increase in conduction loss at higher operating temperatures. Furthermore, the performance of a GaN-FET degrades at increasing temperatures. For instance, the continuous drain current rating of GaN systems GS66508P is specified at 30 A for an operating temperature of 25 ^{0}C which reduces to 25 A for an operating temperature of 100 ^{0}C. Hence, for a GaN-based design, it is critical to pay careful consideration while designing the thermal management of the PES.

For a GaN$_{PX}$ package, junction to case thermal resistance for the top side of the device ($R_{\emptyset J\,Top} = 7\ ℃/W$) is several times higher than the junction to case thermal resistance of the bottom side ($R_{\emptyset J\,C} = 0.5\ ℃/W$). Hence, for the thermal design of SPES and LPES, bottom side cooling of the GaN devices with an attached heat sink is selected as the most effective means for heat dissipation. Figure 87 outlines the implemented thermal design. Heat generated inside the die is directed towards the device thermal pad and is then transferred to the PCB. On the PCB, a combination of internal copper layers and thermal vias are used to internally dissipate and transfer the remaining heat to the heat sink, which is connected to the bottom layer of the PCB, using a thermal interfacing material. A minimum of 2 oz. copper thickness is recommended to be used for all the PCB layers. An optimum number of thermal vias as specified in [71] are used. These thermal vias are also used as the connection to the source terminal of the GaN-FET.

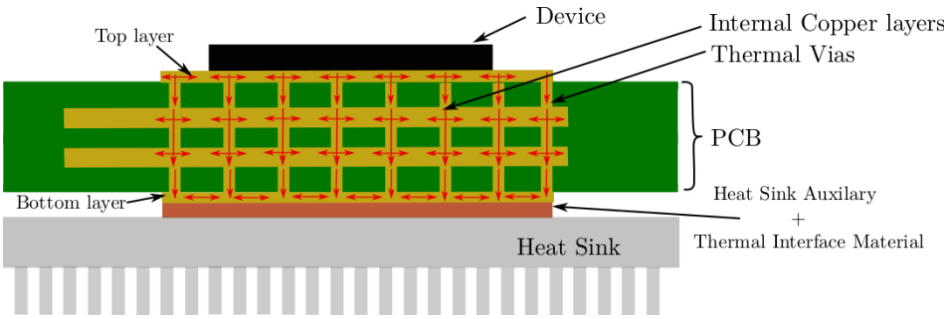


Figure 87. Thermal design for a GaN$_{PX}$ package.

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