Mitigation of Threshold Voltage Variability by Exploiting Interaction of Oxygen Vacancies and MGG

BY

MADHU PADMANABHA SUMANGALA
B.E., Visvesvaraya Technological University, India, 2011.

THESIS

Submitted as partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Chicago, 2020

Chicago, Illinois

Master's Committee:

Dr.Amit Ranjan Trivedi, Chair and Adviser
Dr.Michael Strocio
Dr.Pai-Yen Chen

To my parents and brother for their love and support.

ACKNOWLEDGMENTS

First of all, I would like to thank the department of Electrical and Computer Engineering, UIC for providing me the suitable platform and opportunity to pursue research.

I express my immense gratitude to my thesis advisor Prof.Amit Ranjan Trivedi for providing me this opportunity to pursue a thesis research under his guidance. He has always been a very approachable person and has provided valuable insights. I specially thank him for showing tremendous amount of patience during the course of the research and guiding me in the necessary direction.

I am very grateful to my parents Sumangala P Bhat, Dr.Padmanabha Bhat and my brother Manu P S for constantly supporting me.

I am also grateful to all my teachers who have shaped my thoughts throughout my student life.

I am thankful to fellow student researcher at AEON Lab, Ahish Shylendra for giving valuable suggestions whenever I approached him.

I would like to also extend my sincere thanks to everyone who have either directly or indirectly helped me complete my thesis.

MPS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF ABBREVIATIONS

V_{FB}	Flat Band Voltage
OV	Oxygen Vacancy
MGG	Metal Grain Granularity
p_{O2}	Oxygen Partial Pressure
$\sigma(V_{TH})$	Standard Deviation of Threshold Voltage
$\mu(V_{TH})$	Mean Value of Threshold Voltage

SUMMARY

The scaling of transistor beyond $65nm$ was backed by replacing SiO_2 by a high-κ dielectric material such as HfO_2. The use of HfO_2 on the silicon bulk introduced positively charged thermodynamic point defect oxygen vacancy. The surplus electrons transferred to the gate of the transistor by oxygen vacancy, creates a dipole and hence affects the local electrostatics. As formation of oxygen vacancy is random and statistical in nature, this will create its own variability.

The deposition of metal gate of the transistor in the form of grains of various size along different orientation is known to posses varying workfunctions. This alters the localized flat band voltage causing threshold voltage variability. The higher value of workfunction reduces the surface potential, whereas lower value of the workfunction increases the surface potential. Interestingly, the positively charged oxygen vacancies create voltage spikes. Hence, by carefully placing oxygen vacancies via altering processing conditions, the effect of metal grain granularity can be invalidated.

The law of mass action based oxygen vacancy generation model was used to simulate the theory in Synopsys's Sentaurus TCAD Tool. With the proposed method, the threshold voltage variability induced by metal grain granularity($\sigma(V_{TH})$) was reduced by 50% for $9nm$ average edge length.

CHAPTER 1

INTRODUCTION

After the invention of the fire and electricity, if there is one greatest invention which changed the life style of the humanity, it is the transistor. The invention of transistor especially MOSFET, changed the computing style, capacity and in turn facilitated simplest applications to super computers. This was aided immensely by the scaling of the devices from few μmeters to $5nm$ at the time of the writing[1]. As the transistors were scaled down, it became increasingly impossible to fabricate transistor with exact level of control. The transistors manufactured in a wafer became non uniform. The transistors were no longer operated deterministically due to non uniform variability. This deviation from ideal characteristics affected the reliability of the operation. Many probabilistic methods to model the variability became popular.

Along with the reliability, the power consumed by the circuit and speed with the circuit block was intended to operate deviated from the ideal value resulting variation in the parametric yield. Leakage currents started dominating the over all power dissipation. To support the scaling of transistors, oxide layers were too scaled down resulting in gate leakage current. The leakage currents affected sub-threshold slope of the transistor and in turn the threshold voltage. Threshold voltage variability became an important factor affecting the reliability of operation specially in low power and memory circuits.

To deal with the variability, some of the short channel effects and to make up the loss in parametric yield, many circuit level techniques were invented from power aware design to torrent aware design. The on-chip characterization circuits were used to determine the variation and give the feedback to the required block. The circuits were operated in slower clock and hence giving more time to complete the operation. The device engineers too used different techniques such as below the $65nm$ gate length, to prevent the gate leakage the SiO_2 was replaced by high-κ oxide[2], halo doping were used to minimize the DIBL etc. Over the time as transistors were shrunk further some of the techniques became unattractive. Benefits became marginal. For example beyond $32nm$, power saving from DVFS became marginal[3].

The variability are classified into 'process related', 'environmental related' and 'temporal related' variability. Each of these variability impact differently on the threshold voltage of the transistor

The process related variability occur due to insufficient control on the fabrication process such as mask errors or the structure of the transistor or due to the inherent property of the material and the way they interact with other materials. Due to these process related variability, a well designed and tested circuit during simulation may behave differently once it gets manufactured. In the worst case, due to threshold voltage variability, non critical path of the circuit might end being slowest path. Some of the process related variability are Lithographical Variations, Chemical Mechanical Polishing(CMP), Variation in the contact resistance, Random Dopant Fluctuations (RDF), Line Edge Roughness(LER) etc.

The environment related variability occur due to the environment in which the circuit operates. This could be the supply voltage of the particular block or the temperature around the circuit. If the supply voltage gets reduced,

the speed with which the circuits get operated reduces. A circuit which was supposed to operate in 1GHz might end up in operating 500MHz. The increase in the temperature affects the mobility, threshold voltage of the transistor and resistivity of wires.. The transistors will become leaky causing static power dissipation or data loss in the case of DRAM circuits.

The temporal related variability affects the device's ideal characteristics. The Time Dependent Dielectric Breakdown(TDDB), Hot Carrier Injection and Bias Temperature Instability are the general temporal related variability. This change in device's ideal characteristic aggravates the performance, power consumption resulting error in the operation or slower performance.

1.1 Problem Statement

As the scaling of the transistors introduced random variability, many statistical analysis have been carried out and suitable models have been introduced. Over the time with the suitable solutions some of the variability can be controlled, some will attain a saturation value and some of them cause more variability. The work [4] analyzes the impact of variability in nano-scale FinFET's such as Gate Edge Roughness (GER), Random Dopant Fluctuations (RDF), Fin Edge Roughness (FER) on the threshold voltage (V_{TH}) and [5] analyzes the effect of Metal Grain Granularity (MGG), Oxygen Vacancy(OV) variability on the threshold voltage (V_{TH}) of the transistor and compares all the variability together for different transistor dimensions. As it is evident, with the use of intrinsic channel, the variability induced by Random Dopant Fluctuations will be minimum and also Gate Edge Roughness maintain constant profile, but the variability by Fin Edge Roughness, Oxygen Vacancy and Metal Grain Granularity worsens as device dimension

shrinks. This invites new study to reduce the variability induced by them.

Hence, this work looks into the reasons for variability induced by Oxygen Vacancy and Metal Grain Granularity to propose a solution, which in turn reduces the overall variability.

1.2 Thesis Organization

This report is organized as follows-

- Chapter 2 gives necessary introduction to MGG induced variability.
- Chapter 3 explains the background related to Oxygen Vacancy induced Variability.
- Chapter 4 describes the core concept on which the proposed solution hinges on.
- Chapter 5 gives necessary background on the tool used and explains the simulation set up in detail.
- Chapter 6 reveals all the simulation results.
- Chapter 7 provides the conclusion.
- Chapter 8 states all the references.

CHAPTER 2

METAL GRAIN GRANULARITY

Metals remain in the pattern of periodic lattice structure where regular array of atoms form bond with adjacent atoms. But, this crystalline structure cannot grow unbounded due to inherent defects. So, in general the metallic films comprise of several grains with distinct orientations. The integrated circuit processing conditions such as temperature and deposition decide the grain size. The grain size extends with raise in the temperature[6]. In general, based on the metal type, the grains grow $\sim 4 - 22nm$[7].

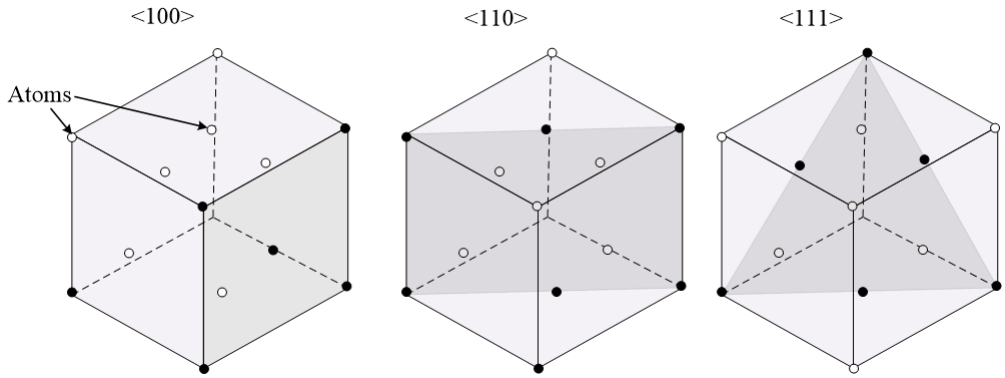


Figure 2.1: Unit cells of crystal structure

The construction of grains can be analyzed by understanding the type of unit cell which the crystalline structure repeats in different directions to form the grain. The commonly found unit cells such as hexagonal close pack(HCP), body centered cubic (BCC), face centered cubic (FCC) make most of the metal grains used in integrated circuits. During the formation of the crystals, the fashion which the unit cells end up decide the orientation

of the grain. Some of the grain orientations are shown in Fig.2.1 for the unit cell type FCC which has eight atoms at the cubic corners and one atom at the face center. Commonly, a normal vector plane of the form $< XYZ >$ used to represent orientation. In the Fig.2.1, the dark circles represent the atoms on the respective planes and white circles are the atoms which are not on the plane. The surface density is calculated as number of atoms of plane of interest per unit area. i.e for the given orientation, the number of atoms intersecting the plane divided by the intersection area.

The workfunction(eV) can be defined as the minimum energy required to knock off an electron from a solid. Bulk chemical potential and the surface dipole potential form the workfunction of a material[8]. The exchange interaction and electron-electron correlation form the bulk chemical potential. On the grains of metals, dipoles get formed. Such dipoles formed on such surface planes alter the metal workfunction [8]. This can be explained using Lang and Kohn's model stated in [9]. Generally, the negatively charged electron distribution spills out of the metal surface resulting positive charge accumulation inside the metal surface, balancing the neutrality. This form the dipole. The stronger the dipole created by the charges, stronger the field which opposes the removal of an electron. This results in increase in the original workfunction. So the surfaces shown in Fig.2.1 which has more number of atoms intersecting the surface create results in higher workfunction. For the FCC cube's surfaces shown in the Fig.2.1, highest atomic surface density is on the plane $< 111 >$ succeeded by $< 100 >$ and $< 110 >$ resulting in the workfunctions in the same decreasing order. This is proved experimentally by Gaillard *et al.*[10]. Hence, the workfunction of metal grains is higher for the orientation of the grain with highest surface density.

The effective value of workfunction of the metal tends towards the prob-

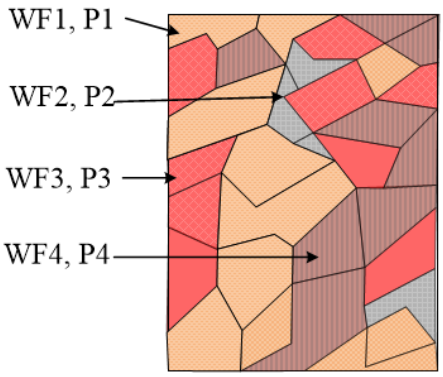


Figure 2.2: Metal grains with different orientation and probability

ability of occurrence of the particular orientation. A metal film structure will be more stable along this orientation hence that particular orientation is preferred orientation for the given metal. But these preferred orientations change with the temperature. For a selected gate formation temperature, the depositing metal gate will contain grains of random sizes, typically lower sizes as compared to grains generated during higher temperature[11] and shapes with different orientation probability as shown in Fig.2.2. So the workfunction is not deterministic. It changes during gate formation during IC fabrication, randomly. Banerjee *et al.*[7] have envisaged a model to calculate the effective workfunction based on the orientation and probability and listed out the implication on the process, device and circuits [11]. At the strong inversion region as shown in the Fig.2.3, the threshold voltage (V_{TH}) of a transistor is calculated as-

$$V_{TH} = V_{FB} + V_{OX} + \psi_S \tag{2.1}$$

where V_{FB} is flat band voltage, $\psi_S = 2 \times \psi_F$. The flat band voltage is calculated as,

$$V_{FB} = \phi_M - \phi_S - \frac{Q_f}{C_{OX}} \tag{2.2}$$

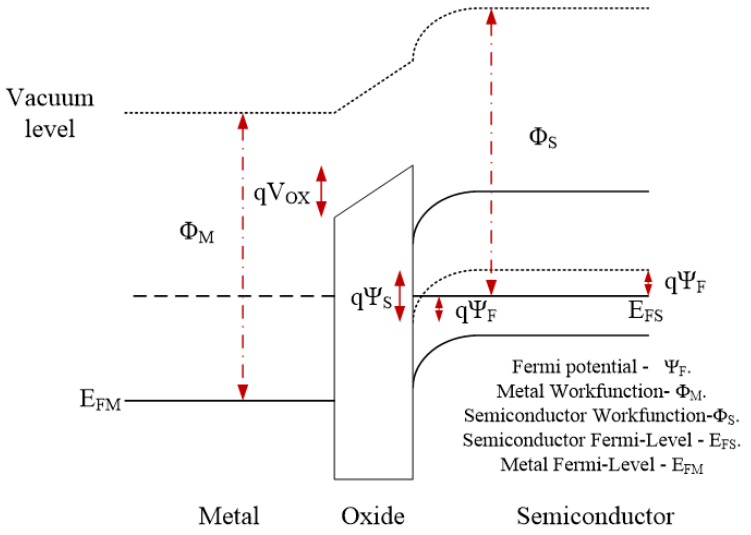


Figure 2.3: Band diagram indicating threshold voltage

where ϕ_M is the metal workfunction, ϕ_M is the semiconductor workfunction, Q_f is the fixed charge at the oxide/Si interface, and C_{OX} is the oxide capacitance. As the metal workfunction ϕ_M changes, so as the flat band voltage. This in turn fluctuates the threshold voltage causing variability[11].

Interestingly, for the current technology with the transistors of gate length of few nano-meters it can be noted that the gate formation end up containing just few metal grains and hence casing more variability[7]. As the grain size increases, the variability induced by it also increases[12]. Further, as the bulk CMOS transistors have single gate and FinFETs have multiple gate, the variability caused by metal grain is more in FinFETs than in bulk CMOS transistors. Also, the variability increases as the width of the channel decreases[12]. The variability caused by grains on the off current I_{OFF} increases as the transistor gets scaled down[13]. But, it appears that the variability caused by metal grain granularity does not impact much on the sub-threshold slope[11],[13].

Notably, there are multiple existing works suggesting reduction of grain induced variability. By scaling film thickness [14], by aligning grain's orien-

tation [15] the metal grain induced variability can be reduced. Ohmori *et al.* explored a way reduce the variability by tuning the crystal structure by converting it to amorphous form.

CHAPTER 3

OXYGEN VACANCY

The contact between Hafnium oxide(HfO_2) and Silicon was predicted to be thermodynamically stable[16]. But, later it was observed that HfO_2 freely forms silicate layer[17] when it was stacked on Silicon bulk. Though the formation of an interfacial silicate layer was assumed to be an endothermic reaction with positive Gibbs free energy change(ΔG), later it was proved that the overall reaction to be exothermic [18] with negative (ΔG). The reason was found to be the formation of thermodynamically driven point defect "oxygen vacancy".

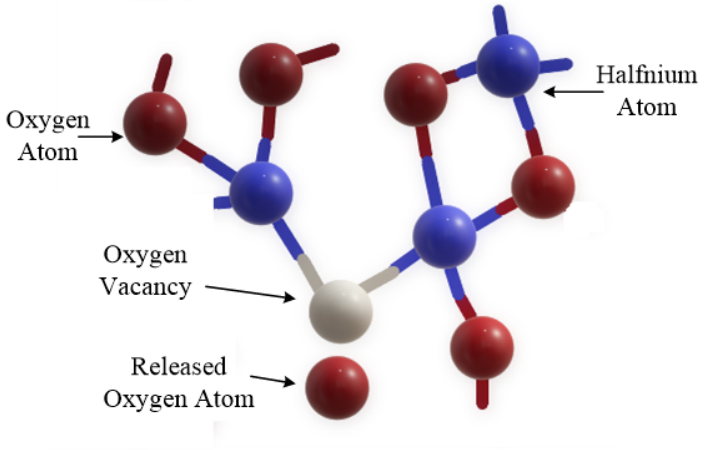
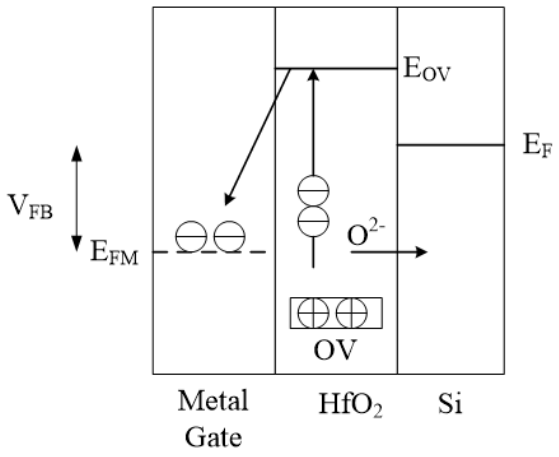
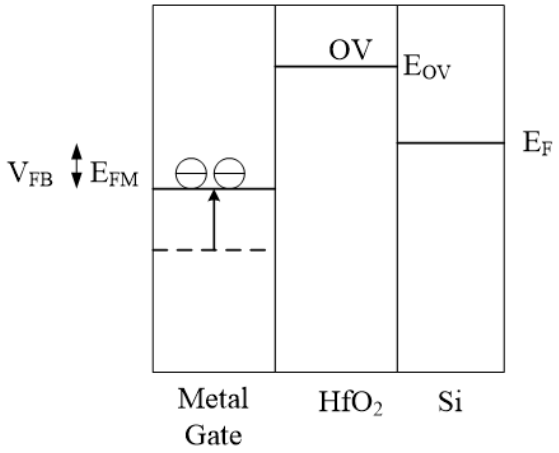


Figure 3.1: Oxygen Vacancy representation

To support the scaling of MOSFET's by replacing SiO_2 by high$-\kappa$ dielectric materials such as HfO_2 faced with many challenges such as charge trapping[19],[20], Fermi level pinning[21] and degradation of mobility[22]. The presence of oxygen vacancy defects within HfO_2 film was asserted in[23],[17]



(a) Oxygen Vacancy Formation



(b) Shift in V_{FB} due to dipole formation

Figure 3.2: Formation of OV causing change in V_{FB}

by observing an extra absorption peak within the band gap of HfO_2 detected by Spectroscopic Ellipsometry measurement data. The correlation between trap energy level determined[24] and the observed data of the energy level of the peak proved The existence of electron trap associated with oxygen vacancy. The Fermi level pinning at the Poly-Silicon/Oxide interface was described for the first time by C.Hobbs *et al.* in [21]. They confirmed the fact that the Hf based materials create interface dipoles which in turn pins the Fermi level below the Poly-Si conduction band.

K. Shiraishi *et al.*[18] theoretically explained the change in flat band voltage(V_{FB})

by formation of oxygen vacancies. The eviction of an oxygen atom from the HfO_2 crystal results in creation of two electrons. The subsequent transfer of the two surplus electrons to the p+ poly gate creates an interface dipole which alters the local electrostatics. Along with Fermi pinning[21], mobility degradation[22], the tendency of formation of interfacial oxide layer by Si and doubly charged oxygen atom on the both sides i.e p+ poly gate and Si bulk, forced the device designers to choose inert metal gates as shown in Fig.3.2(a). Further, for the high$-\kappa$ gate stack, the effect of oxygen vacancies on high$-\kappa$ was studied by [17]. It was proposed to choose optimal thermal process, and carefully selected gate stack to mitigate oxygen vacancy formation.

The effect of oxygen vacancies on the threshold voltage was demonstrated by E.Cartier *et al.* in[25]. They demonstrated that the flat band voltage (V_{FB}) of p-FET metal gates were dependent on the post processing annealing setting.It was found that for gate stack with Ru,Pt and Re, the flat band voltage changed $\sim 750mV$ with the change of temperature, p_{O2} during post deposition N_2/O_2 and annealing. The reason for change in the V_{FB} was found to be the formation of oxygen vacancies, and subsequent charge transfer to the gate as shown in Fig.3.2(b).

The concentration of oxygen vacancies and their spacial allocations differ in each manufactured device. This causes variability in the electrostatic field induced and in V_{FB}. This will in turn cause variability in the threshold voltage. The model to estimate oxygen vacancy concentration against the gate workfunction was proposed by Robertson *et al.*[26]. As stated earlier, Takeuchi *et al* measured the value of E_{OV} using absorption spectra, which was found to be $1.2eV$ below the conduction band of HfO_2. This was also measured by [25] using charge pump- based model. K.Shiraisi *et al.*[18] proved that the formation of oxygen vacancy was indeed an exothermic reaction for

p+ poly gates as compared to n+ poly gates for which the reaction was an endothermic. This modeling helped to understand the effective workfunction shift.

As explained earlier, the formation of oxide layer at the HfO_2/p+ poly gate with the released negative charged oxygen atom, and in turn increasing the effective oxide thickness lowered gate capacitance and also, the p+ poly gate was prone to Fermi level pinning. This compelled the device engineers to use p-metal gates. The work [27] extended the the theory[18] to metallic gates and confirmed V_{FB} modulation for metal/HfO_2 gate stack. The OV induced potential shift was modelled and experimentally validated against the oxygen partial pressure(p_{O2}) by Guha and Narayanan in [28]. The change in potential was inversely proportional to $p_{O2}^{1/2}$ and also, it was found that the shift in potential decreases linearly along the oxide thickness.

The study of OV induced threshold voltage variability was done by A.R.Trivedi *et al.*[5]. The simulation study was carried out by statistically modelling the oxygen vacancy concentration and their placements. As explained in [28],[17],[25] it was found that the oxygen vacancy concentration raises with the surging gate processing temperature, increase in workfunction and decrease in oxygen partial pressure. For Gate Last process with smaller temperature of $750K$ as the oxygen vacancy concentration accumulated towards HfO_2/Metal interface, $\sigma(V_{TH})$ was found to be lesser as compared to Gate First process. The oxygen vacancies present near the channel region were found to be inducing substantial local variability in the potential. Most importantly, it was found that as the channel length decreased, amount of change in threshold voltage decreased but variability of the threshold voltage increased for the same oxygen vacancy concentration. Hence the variability induced by oxygen vacancy has become an important source of variability

for the future technologies.

CHAPTER 4

CORE CONCEPT

As stated in Chapter 2 and Chapter 3, for the future technologies, the variability induced by oxygen vacancies and metal gate granularity aggravates. Hence there is a need of effective solution to contain and reduce the variability. This work proposes a novel methodology to reduce the variability.

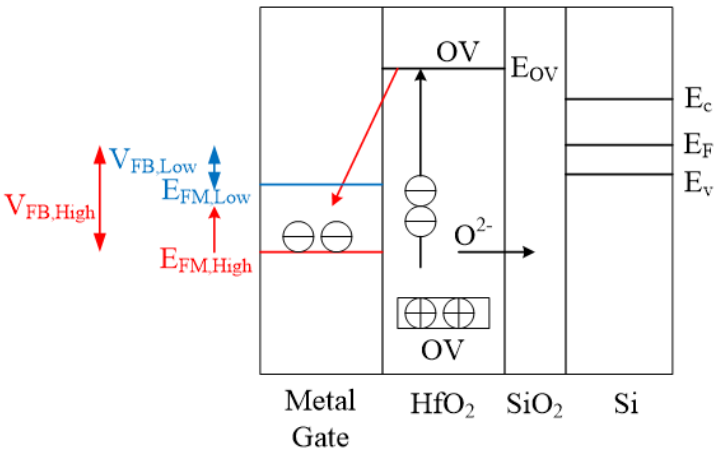
Thesis:

At an optimal condition, the variability induced by Metal Grain Granularity and Oxygen Vacancy will "cancel out" each other.

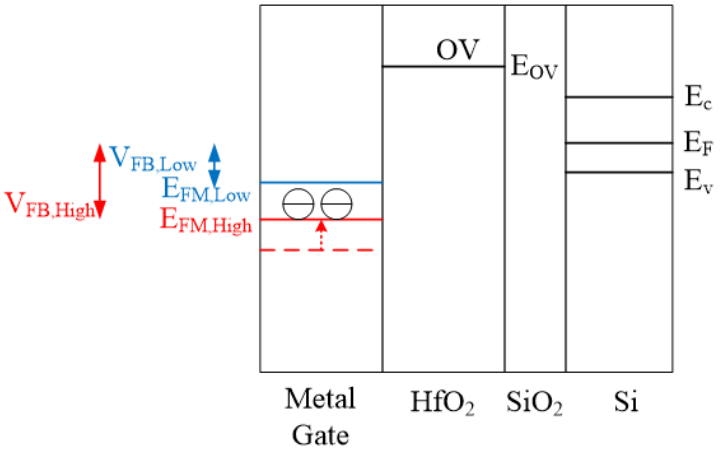
Reasoning:

The surplus electrons generated during oxygen vacancy formation will transfer to the lowest available energy level from E_{OV}. As explained in Chapter.3, the electrons get transferred easily to the gate metal with high workfunction. At the microscopic level, with the gate being granularized with grains containing different workfunctions, the surplus electrons tend to transfer to the grain with highest workfunction. i.e to the lowest energy level. Hence, it is expected that the formation of oxygen vacancies and hence the dipole only under the metal grain with high workfunction.

This transfer of surplus electrons will alter the electrostatic around the grain and eventually reduce the workfunction of the high workfunction metal



(a) Electron transfer to the grain with high workfunction



(b) Reduction of WF of the high WF metal grain

Figure 4.1: Formation of OV under grain with high WF

grain. Hence, it is expected that the overall flat band voltage V_{FB} will reduce when compared to the overall V_{FB} of the system with MGG variability only and also, the overall V_{FB} will be more than the V_{FB} of the system with OV variability alone.

To encapsulate, OV variability will reduce the V_{FB} and MGG variability will increase the V_{FB}. At an optimal condition, the effects get balanced out, causing less shift the V_{FB}, and in turn reducing the overall V_{TH} variability.

CHAPTER 5

SIMULATION METHODOLOGY

The simulation strategy involved generation of metal grain granularity, statistical modeling for oxygen vacancies and using these developed models simulate them in a designed device. The developed models were simulated in tri-gated SOI FinFET device.

5.1 Simulation Tools

Various tools have been used to generate the coordinates, simulating the electrical characteristics of the device and viewing corresponding results. To generate coordinates of metal grains granules, to generate coordinates of oxygen vacancies, to dynamically design the complete transistors based on generated coordinates of granules, oxygen vacancies and to automate whole process computing tool MATLAB was used. Based on generated coordinates, to design the transistor, simulate their electrical characteristics and view the results Synopsys's Sentaurus Technology Computer-Aided Design(TCAD) tools[29] were used. To extract the suitable results out of the generated results scripts were written in PERL and TCL.

5.1.1 Sentaurus TCAD

Synopsys's Sentaurus Technology Computer-Aided Design(TCAD) tools[29] are very powerful tool which helps user to design devices, optimize semicon-

ductor process parameters, technology and simulate the electrical characteristics. These TCAD tools are equipped to solve equations related to process, device such as physical equations, fundamental equations and various partial differential equations.

The tools can be divided into two entities: process simulators and device simulators.

Based on governing physical equations, the process simulators helps user to simulate the various steps such as etching, deposition, ion implantation, annealing , oxidation etc. The semiconductor wafer is discretized into multiple parts before applying suitable governing equations.

The device simulators are used to design the device, discretize them and simulate the electrical characteristics of the devices.

In this work following device simulators were used to simulate the proposed theory.

Sentaurus Structure Editor

Sentaurus Structure Editor is used to design either 2-dimensional or 3-dimensional devices using primitive shapes such as circle, rectangle, polygon, cube etc. Along with designing geometries of devices it also helps in process emulations. The doping profiles of the devices, the meshing precision are also given as input to the device.

The tool offers user to design devices either in GUI mode, which offers a state of art visualization or using specific commands of it's scripting language[30]. The scripting commands are written in a '.scm' file and given as input for compiling and designing.

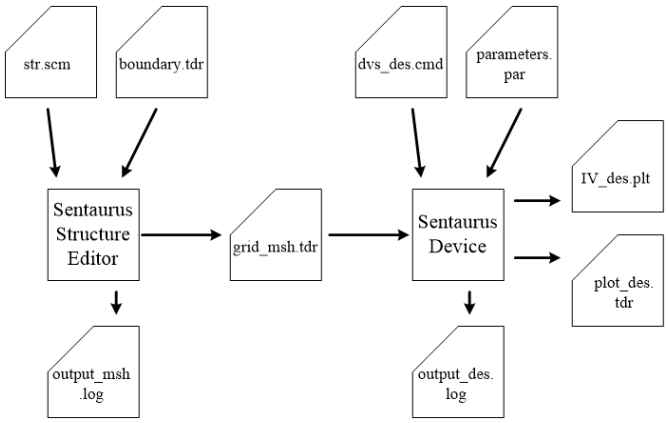


Figure 5.1: The tool flow of the device simulation

Sentaurus Mesh

The designed device needs to be discretized or 'meshed' to represent the entire device structure as a finite element structure. The tool has inbuilt axis aligned mesh generator and tensor product mesh generator which generate high quality discrete grids. It is also used in process simulators.

The meshing resolution is specified in '.scm' file. The resolutions can be given into complex 2-dimensional or 3-dimensional structures and also to define doping profiles whether they are uniform or has any steep gradients. Using these parameters, high quality Delaunay mesh grids are generated.

Sentaurus Mesh tool automate entire process of meshing based on the scripting commands[29]. This process of meshing generates '.tdr' file which is used to as an input to the device simulators.

Sentaurus Device

Sentaurus Device[31] is used to calculate thermal, optical and electrical characteristics of each input semiconductor device structure. It has comprehensive material,physical models which are applied during simulations.

The meshed finite element structure representation of the device is used

simulate and obtain it's electrical characteristics. These discretized mesh nodes have various properties such as material, doping concentration. So corresponding electrical characteristics such as electric fields, current density, electrostatic potential etc also other characteristics such as generation, recombination rates, carrier concentration at each nodes can be computed.

The electrodes defined on which the boundary conditions such as voltages, change in workfunction etc are applied. The mobility models, operating conditions, various other physical parameters are given in the input file of the format '.cmd '. The other external parameters can be given as input to the device as well using '.par' file. The tool mainly solves Poisson equation, carrier continuity equations using various numerical methods such as Newton-Raphson method etc and the resultant current, voltage characteristics are extracted via electrode contacts.

Using this an user can understand the working of the designed device under various electrical and environmental conditions. Hence the user can decide to optimize the device further based on the need also one can extract the SPICE model of the device.

As shown in the Fig.5.1, Sentaurus Device[31] takes input files of the meshed device in '.tdr' format, assigned boundary conditions in '.cmd' file, specific external parameter file in '.par' format. The current voltage characteristics are stored in '.plt' file and various other resultant electrical characteristics such as electrostatic potential, energy levels, doping levels etc and other physical characteristics such as temperature variation within the device etc are stored in '.tdr' file.

Sentaurus Visual

Sentaurus Visual is state of art interactive visualization tool. Many tasks such as viewing the designed device post meshing it, viewing the resulting electrical and physical characteristics once they are simulated can be carried out in 2D and 3D formats.

The tool takes input TCL script files and using the tool specific scripting command one can post process the output data, generate output images etc[29].

Sentaurus Inspect

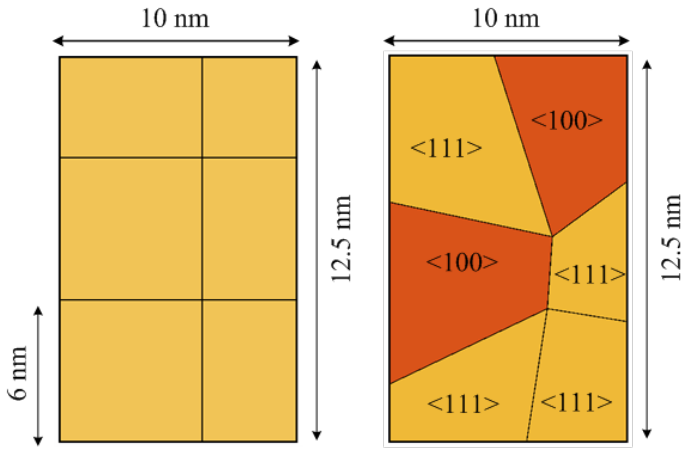
To plot doping profiles and electrical characteristics of semiconductor devices in X-Y format and analyse it the GUI tool Inspect can be used. Using scripting and inbuilt mathematical libraries the data can be processed for the further use.

5.1.2 MATLAB

The powerful computational tool was used to write scripts for generating various coordinates such as of metal grains, oxygen vacancies and automate entire process for all the physical, environmental and electrical conditions. The post processing of the data also has been carried out using matlab.

5.2 Simulation Set-up

The simulation set-up contains generation of metal grain granularity, statistical model for oxygen vacancy concentration and the placement of the oxygen vacancies, designing a tri-gated SOI FinFET and it's simulation.



(a) Uniform grains (b) Randomized grains

Figure 5.2: Creation of metal grain granularity

5.2.1 Generation of Metal Grain Granularity

As discussed in Chapter 2, for the nanometer sized transistors when a gate electrode is deposited with a metal such as TiN, they get deposited with as grains with random shapes, sizes and orientations. In a wafer containing thousands of chips and billions of transistors, each device has metal gate with different grain shapes, size and orientations and hence each device operates with different threshold voltage due to variability induced by grains.

As explained in [7],[32], for TiN metal, majority of the grains are aligned to $< 111 >$ and $< 100 >$ orientation. Hence, this work restricts the study of MGG variability only to $< 111 >$ and $< 100 >$ orientations.

In this work, quadrilateral shaped grains were chosen. To generate metal grains and to mimic the random sizes of the grains, initially the all around gate was divided into three slabs. One slab on the left of fin, one slab on the right of fin and another slab on the top of the fin. The gate surface area in 2D, say X-Y direction was uniformly discretized with grain of chosen edge length as shown in Fig.5.2(a). These discretized vertices were randomized around the original point to generate the random size and shapes as shown

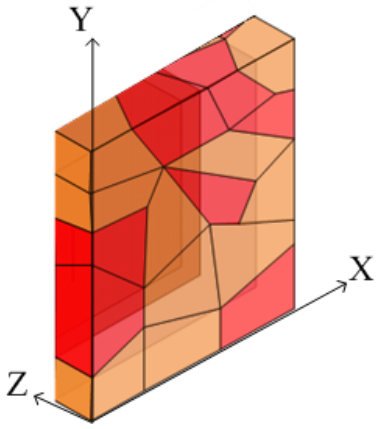


Figure 5.3: Extruding metal granularity to third dimension

in Fig.5.2(b). Then this 2D structure was extruded to third dimension using Sentaurus Structure Editor command as shown in Fig.5.3.

Based on the probability of generation, the grains were assigned one of the $< 111 >$ and $< 100 >$ orientations randomly. Now the the grains with different orientations are assigned workfunctions accordingly[32] as mentioned in Table I. These workfunctions in eV are assigned to the particular grain region 'r' in the input file of Sentaurus Device tool as shown below-

Physics (Region = "region.M(r)") MetalWorkfunction (Workfunction=5.0)

The step was repeated for remaining two other slabs to form a gate around the channel.This is shown in the Fig.5.4.

Table I: GRAIN ORIENTATION AND WORKFUNCTION

Grain Orientation	**Workfunction**
<111>	4.8eV
<100>	5.0eV

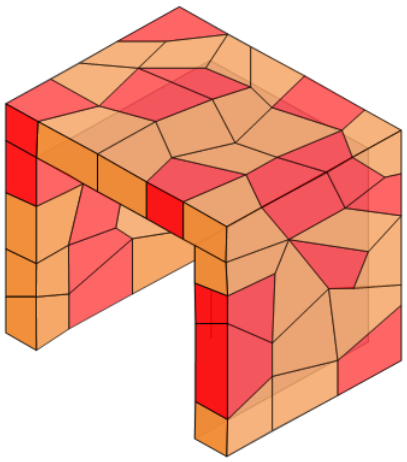


Figure 5.4: Forming gate around the channel

5.2.2 Statistical Modeling of Oxygen Vacancy Concentration

Statistical Modeling

The process of forming an oxygen vacancy V_O^{++} involves release of oxygen atom O_O^x from the HfO_2 dielectric and release of two surplus electrons 'e' as explained below [5].

$$O_O^x \leftrightarrow V_O^{++} + 2e + \frac{1}{2}O_2 - \Delta G_1^0 \tag{5.1}$$

where O_2 is the oxygen gas molecule, standard free energy of exchange is denoted by ΔG_1^0[5]. The surplus electrons are transferred to the gate metal electrode. So the electron concentration is expressed using Fermi-Dirac statistics as [33]-

$$[e] = \frac{1}{1 + exp\left(\frac{E_{OV(r)} - E_{F,m}}{kT_{G,form}}\right)} \approx exp\left(-\frac{E_{OV} - E_{F,m}}{kT_{G,form}}\right) \tag{5.2}$$

where k denotes the Boltzmann's constant, E_{OV} is the effective defect energy, metal Fermi energy is denoted by $E_{F,m}$, gate formation temperature repre-

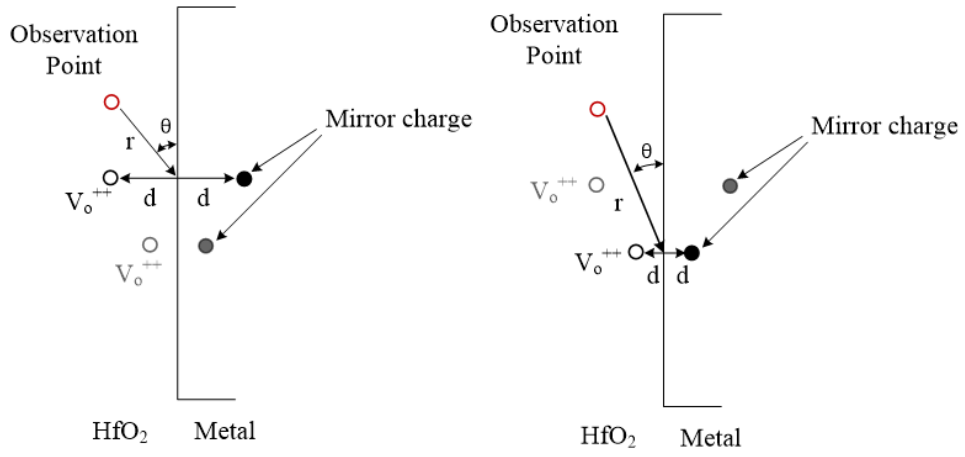


Figure 5.5: The mirror charge created by OV dipole

sented by $T_{G,form}$ and effective concentration of various terms are represented inside the [ ].

The effective OV concentration at equilibrium is expressed using law of mass action as [33]

$$\frac{[V_O^{++}]}{[O_O^x]}[e]^2 p_{O2}^{1/2} = exp\left(- \frac{\Delta G_1^0}{kT_{G,form}} \right) \tag{5.3}$$

where p_{O2} is the oxygen partial pressure. Using Eqn.5.2 and Eqn.5.3 we can arrive at the probability of generation as [5]-

$$P_{OV} = \frac{[V_O^{++}]}{[O_O^x]} = \frac{1}{p_{O2}^{1/2}} exp\left(- \frac{\Delta G_1^0}{kT_{G,form}} + 2 \times \frac{E_{OV}(r) - E_{F,m}}{kT_{G,form}} \right) \tag{5.4}$$

But, formation of oxygen vacancy which has positive charge affects the overall defect energy level E_{OV} around it and in turn affects formation of another oxygen vacancy nearby it[5]. Basically positive charged oxygen vacancy V_O^{++} and corresponding surplus electrons transferred to metal gate form a dipole and causes local variation in the energy level with respect to the metal Fermi energy which can be captured using method of mirror charges[34].

As shown in the Fig.5.5, this potential field of the dipole with respect to an observational point r is expressed as[5]-

$$\Delta V(r) \approx \frac{q}{4\pi\epsilon}\frac{2d \times sin\theta}{r^2} \tag{5.5}$$

where q is the unit electron charge, the notations d,r,θ are shown in the Fig.5.5.

For a general observation point, the net potential field caused by all the existing dipoles is expressed as-

$$\sum_i \Delta V(r_i) \approx \sum_i \frac{q}{4\pi\epsilon}\frac{2d_i \times sin\theta_i}{r_i^2} \tag{5.6}$$

When the metal gate is granularized and assigned different workfunctions, for the oxygen vacancy formation, the corresponding workfunctions of the nearest grain, $E_{f,m,grain}$ should be taken into account in the Eqn.5.4.

$$P_{OV} = \frac{1}{p_{O2}^{1/2}} exp\left(-\frac{\Delta G_1^0}{kT_{G,form}} + 2 \times \frac{E_{OV}(r) - \sum \Delta V(r_i) - E_{F,m,grain}}{kT_{G,form}} \right) \tag{5.7}$$

This equation is used to study the generation the random OV placements for the gate last process with the formation temperature of $750K$. When the ultra-thin films of HfO_2 layers used in the formation of gate, the resulting standard free energy of oxygen vacancy formation ΔG_1^0 is $3eV$ as given in [33]. Based on [35], the defect energy level E_{OV} is $\sim 1.2eV$ from the HfO_2 conduction band.

The values of the different variables used in eq.(5.7) to generate OV placements are listed in Table.II.

Table II: MODEL PARAMETERS

Parameters	**Values**
ΔG_1^0	3eV[33]
Electron affinity	2.45eV[36]
$\Delta(E_C - E_{OV})$	1.2eV[35]
High WF	5.0eV[32]
Low WF	4.8eV[32]
$T_{G,form}$	750K[5]

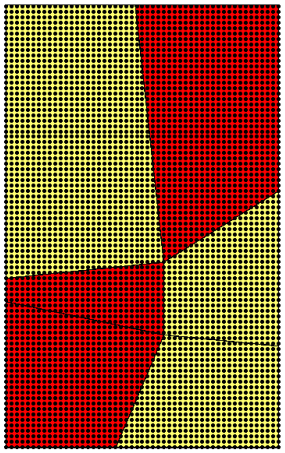


Figure 5.6: Meshing the HfO_2 layer

Oxygen Vacancy Placement:

To mimic the oxygen vacancy placements in the HfO_2 layer film, initially every node of oxygen atom is considered as a possible placement of oxygen vacancy. Hence the the film is meshed with node density of oxygen atom i.e $\sim 55/nm^{-3}$[37] as shown in Fig.5.6. This will result with uniformly placed nodes, i.e in crystalline form. As the HfO_2 film is of amorphous nature, to mimic it, each node is perturbed around it's original point. Also, the order of consideration of these points are also randomized.

Now the Eqn.5.7 is applied along with the parameters listed in table.II and the process parameters such as oxygen partial pressure p_{O2}.The resulting oxygen vacancies are represented as cubes of $0.2nm$ edge length and assigned charge of $2q$. The structure of cubes are generated in Sentaurus Structure

Editor. But assigning charge is done in the Sentaurus Device. Sentaurus Device defines q as the unit electron charge and uses it as a scaling factor for the input commands representing charge concentration. The electron concentration is represented in terms of cm^{-3} which is multiplied by the electron unit charge scaling factor q to get charge concentration in terms of cm^{-3}. In the current structure the oxygen vacancies are represented as cubes of volume $0.008nm^{-3}$. If we assign charge of $2q$ to each cube, the resulting electron concentration is $0.25 \times 10^{24} cm^{-3}$. This is represented in the Physics command for the OV region 'r' of the input file as shown below-

Physics (Region = "region.OV(r)region.HK") Charge (Conc = 0.25e24)

This procedure is repeated for all the gate slabs, to generate oxygen vacancies around the channel at random locations.

Tri-Gated SOI FinFET

The study of the proposed theory is simulated in 10nm channel length tri-gated SOI FinFET. The FinFET's gate stack consists of SiO_2, HfO_2, and TiN metal electrode which is granularized as shown in Fig.5.7(b). The channel is considered as undoped. The Fig.5.7(a) shows detailed structure and different electrodes of the FinFET. Table.III lists different structural and electrical parameters[5].

The electrical boundary conditions, mobility models, workfunctions of metal grains, charge of the obtained oxygen vacancy cubes are assigned in the input file of the Sentaurus Device. The mobility models of [38], mainly the doping dependent are used to simulate the device. The V_{DS} voltage was set to $0.1V$. The gate voltage was swept from $0V$ to $0.8V$ to get corresponding

Table III: FINFET PARAMETERS

Spec.	**Values**
L_{gate}(nm)	10
T_{OX}(nm)	0.34
T_{HK}(nm)	1.4
T_M(nm)	2
H_{FIN}(nm)	12.5
W_{FIN}(nm)	5
S/D doping(cm^{-3})	3×10^{20}
HfO_2 (ϵ_r)	22
SiO_2 (ϵ_r)	3.9
V_D (V)	0.1

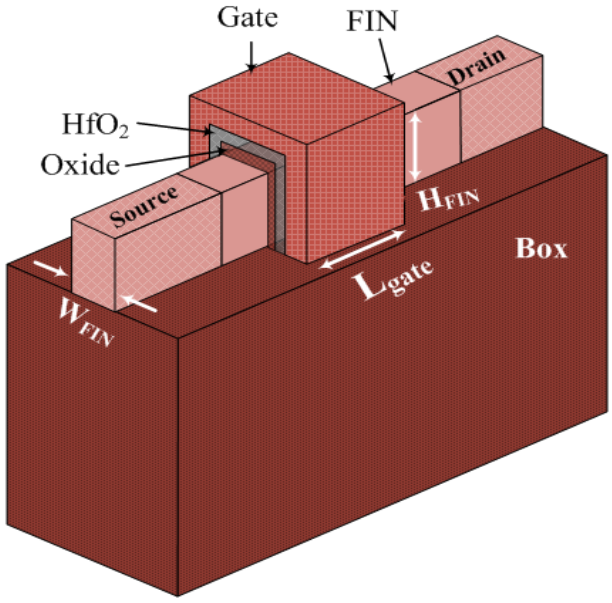
I-V characteristics. From the obtained I-V curve, the threshold voltage was calculated when the current reaches-

$$I(V_{TH}) = 300nA \times \frac{W}{L} \tag{5.8}$$

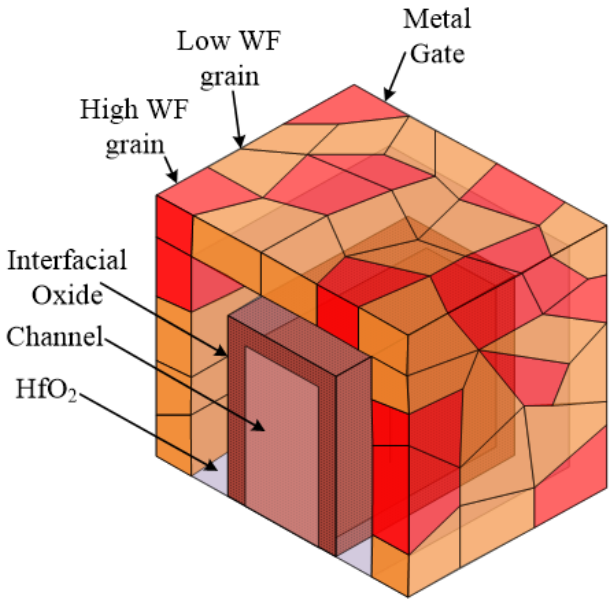
in the log scale. Here, W represents the width of the transistor and L represents the length of the channel. For FinFET the width of the transistor calculated as -

$$W = 2 \times H_{FIN} + W_{FIN} \tag{5.9}$$

Using above set up, the simulation exercise was carried out and the obtained results are explained in the next chapter.



(a) FinFET Transistor



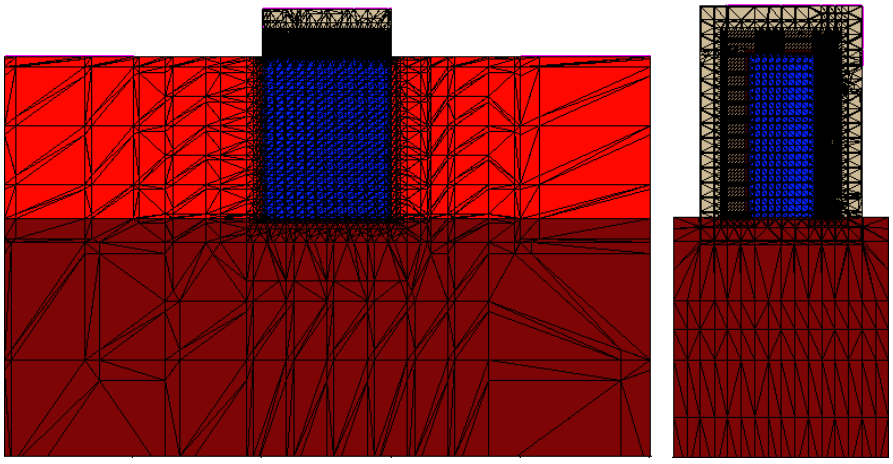
(b) Gate Stack

Figure 5.7: FinFET Schematic

CHAPTER 6

SIMULATION RESULTS

The simulations were carried out using the simulation set up explained in Chapter 5. A sample meshed transistor in Sentaurus TCAD tool is as shown in Fig.6.1. The simulations of the transistors were carried out at the chosen gate formation process, i.e gate last process with formation temperature of $750K$. To verify the theory proposed in the Chapter 5, the simulations were conducted by varying process parameter- oxygen partial pressure p_{O2}. The exercise was repeated for various grain sizes. The results stated in this simulation experiment has been extracted from 100 random samples.



(a) Along the length (b) Across the width

Figure 6.1: A sample transistor with meshed parts

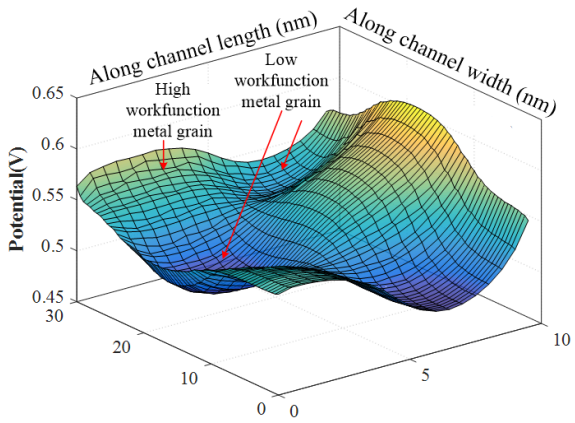
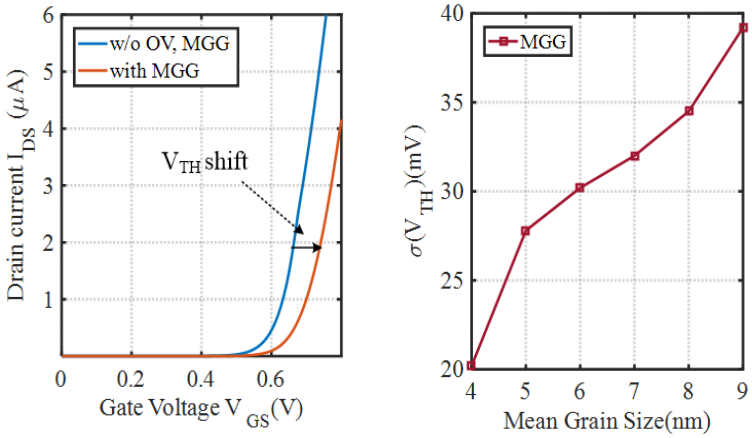


Figure 6.2: Surface potential of the channel induced by MGG



(a) $I_D - V_G$ curve (b) $\sigma(V_{TH})$ vs Grain Size

Figure 6.3: Variability induced by MGG

6.1 Metal Grain Granularity induced V_{TH} variability

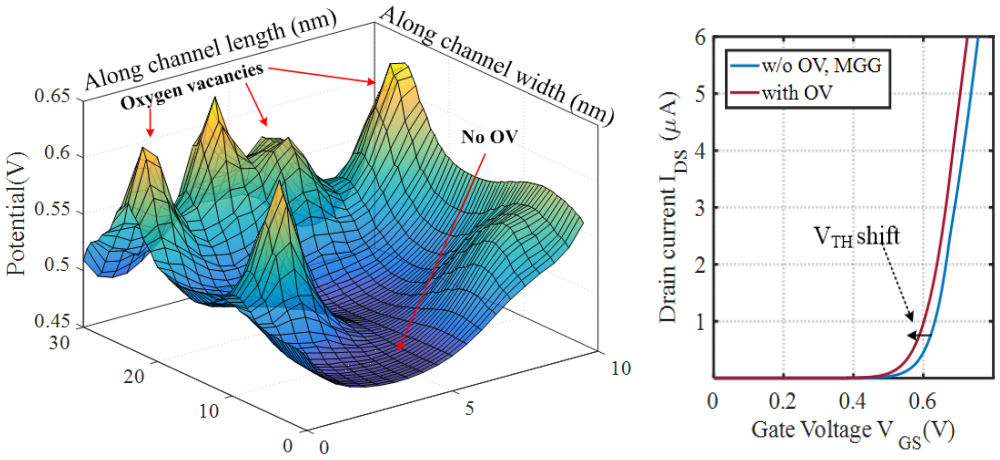
When the gate of the transistor was granularized and assigned different workfunctions, these induce V_{TH} variability due to change in the flat band voltage. This is evident from the surface potential plot as shown in Fig.6.2 where high workfunction metal grains induce localized depressions when compared to the potential induced by low workfunction metal grains. This change in the surface potential causes V_{TH} to shift to higher voltages as shown in the Fig.6.3(a)

Along with the randomness of each transistor during grain generation as the grain size varies, the profile of surface potential also changes due to the different area of the grains. This will also affects the V_{TH} variability. As the Fig.6.3(b) shows, for the sample orientation probability of 0.6, the variability induced by metal grain granularity increases with the increase in the metal grain size. Also, when the V_{TH} variability is observed for the different orientation probability, initially the variability increases until $50-60\%$ of orientation probability, later the V_{TH} variability tend to decrease as the most of the metal gate grains would be of similar orientation and workfunction and hence causing uniform surface potential in the channel. [5].

6.2 Oxygen Vacancy induced V_{TH} variability

As an oxygen vacancy carries positive charge of $2q$, this will raise the potential. The surface potential of the channel when effect of oxygen vacancies considered alone is shown in Fig. 6.4(a). As expected, the presence of OV is evident from the presence of spikes in the voltages on the surface of the channel. These voltage spikes in turn reduces the threshold voltage as show in Fig. 6.4(b).

The spacial distribution of OV concentration indicates increase in oxygen vacancy concentration with the reduction of oxygen partial pressure p_{O2}, increasing the gate formation temperature $T_{G,form}$ and increasing workfuntion for the gate metal as evident in [5]. The Gate Last process used in this exercise ($T_{G,form} = 750K$) generates less oxygen vacancies that the Gate First process ($T_{G,form} = 1300K$). This is also evident from eq.(5.7).



(a) Surface Potential (b) $I_D - V_G$ curve

Figure 6.4: V_{TH} shift induced by OV

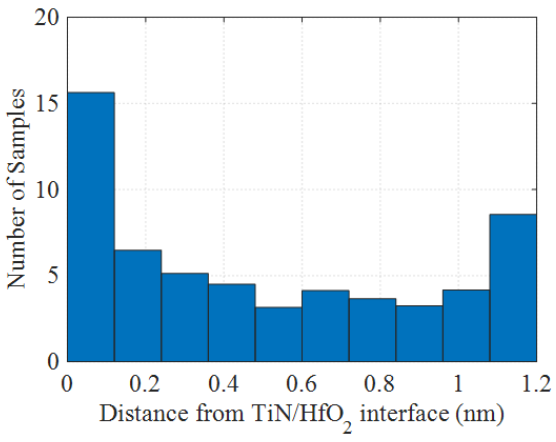


Figure 6.5: Oxygen Vacancy distribution along the depth of HfO_2

The Fig.6.5 shows the spacial distribution of oxygen vacancies along the oxide layer. As expressed in eq. 5.5, towards the HfO_2/Metal interface where $\theta \rightarrow 0$, the dipole potential decreases. This angular dependency of probability of oxygen vacancy formation P_{OV}, results in high oxygen vacancy concentration at the HfO_2/Metal interface. This is also evident in [5], also as observed experimentally in[28] in terms of linear decrease in potential change along the oxide due to varying oxide concentration.

The oxygen vacancies present closer to the channel causes more electric

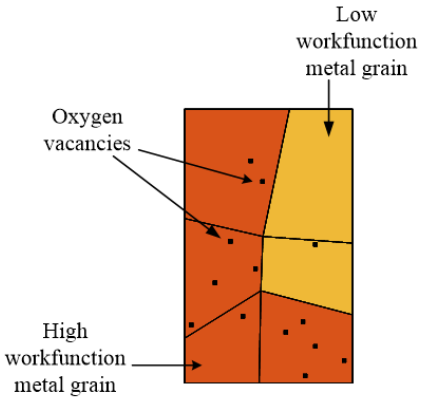


Figure 6.6: Formation of OV under metal grain with high WF

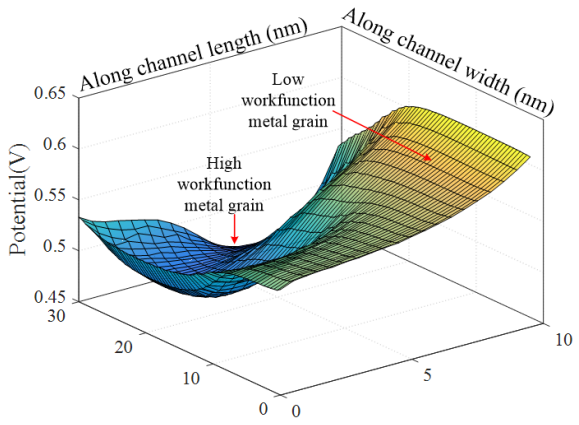
field and hence sharper spikes in the channel surface potential as shown in Fig.6.4(a).The larger the oxygen vacancy concentration, the larger the shift in the threshold voltage and higher the $\sigma(V_{TH})$[5].

6.3 Variability induced by OV and MGG

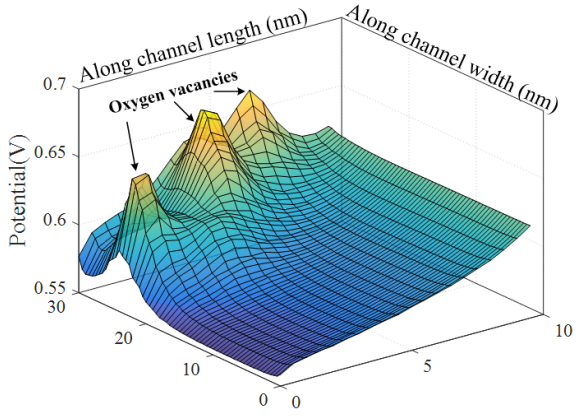
When both the oxygen vacancy and metal grain granularity variability are present, the oxygen vacancies tend to form under the metal grains with high workfunction due to ease of charge transfer. This can be observed in the Fig.6.6.

As evident in the figure, there is on zero probability of oxygen vacancy formation under grain with lower workfunction. This is also evident in the surface potential plot for a sample transistor with metal grain of edge length $6nm$ as shown in the Fig.6.7 , when plotted with the effects OV and MGG separately. The effective surface potential of the channel when both the oxygen vacancies and MGG are present is shown in the Fig.6.8

The oxygen partial pressure p_{O2} was swept from $10^{-5}atm$ to $10^{0}atm$ and variability in the threshold voltage($\sigma(V_{TH})$) was calculated for 100 random



(a) Surface potential with only MGG



(b) Surface Potential with only OV

Figure 6.7: Surface potential indicating formation of OV under the high WF grain

samples at each p_{O2} value. The data proved the proposed theory of the presence of a 'minima' in the curve as show in the Fig.6.10. The exercise was repeated for various grain sizes spanning from $4nm$ to $9nm$ and the corresponding data were plotted. For every grain size, the existence of a 'minima' was observed.

The carefully placed oxygen vacancies will reduce the variation of the potential of the channel created by MGG and hence they seem 'cancelling' each other as evident in the Fig.6.9 plotted at a distance $3.4nm$ from the

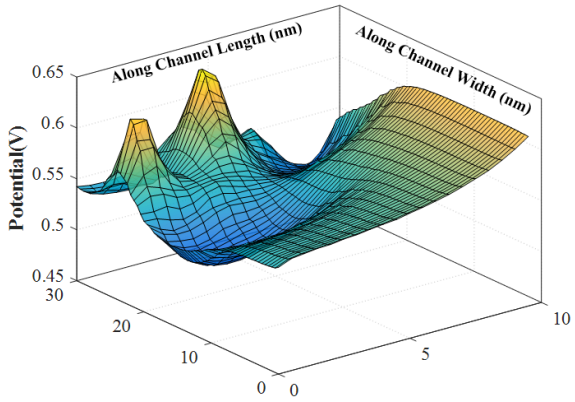


Figure 6.8: Surface Potential with both OV and MGG acting together

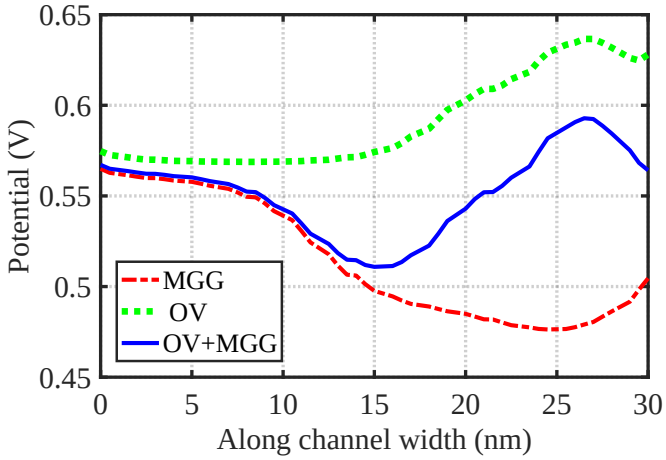


Figure 6.9: OV and MGG cancelling each other

Source/Channel interface for the sample transistor. The corresponding oxygen partial pressure value (p_{O2}) is the optimum value where, the number of oxygen vacancies is just enough to balance the MGG variability.

As explained earlier, at the lower oxygen partial pressure more oxygen vacancies get created causing variability which is dominated by OV variability and at the higher oxygen partial pressure very less oxygen vacancies get created, and in turn the variability is dominated by MGG, therefore these are the sub optimal conditions as shown in the Fig.6.10. Beyond certain higher value of oxygen partial pressure, oxygen vacancies will not get created

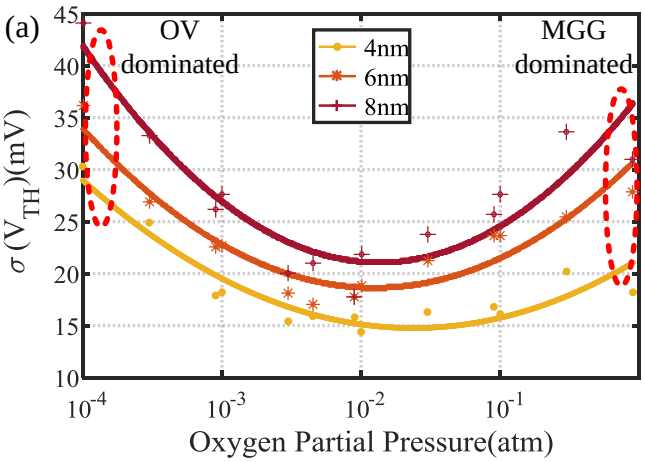


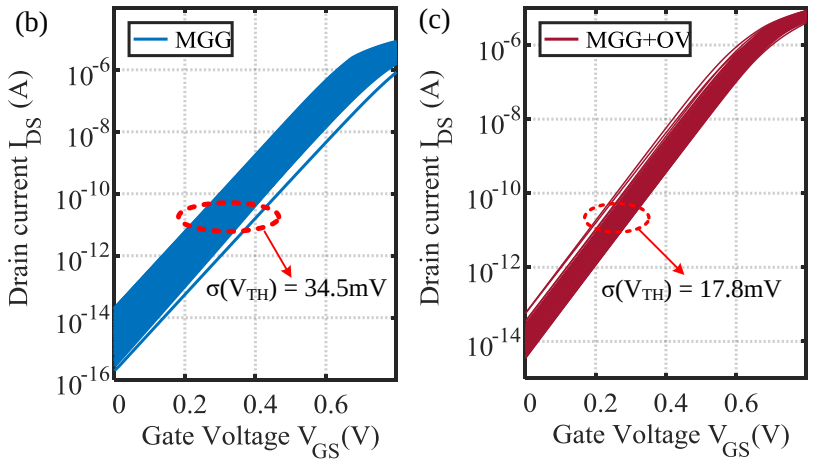
Figure 6.10: $\sigma(V_{TH})$ vs Oxygen partial pressure(p_{O2})

at all and variability will only be of MGG, hence will reach saturation value of $\sigma(V_{TH})$ for the given grain size. At much lower value of oxygen partial pressure, a very high oxygen vacancy concentration will get created even under the lower metal grain workfunction, which will induce more variability.

The Fig.6.11 shows the I_{DS}-V_{DS} curves for the ensemble of 100 sample transistors of metal grain edge length $8nm$. The Fig.6.11(a) shows the curves when MGG was acting alone inducing $\sigma(V_{TH})$ of $34.5mV$ and the Fig.6.11(b) shows the family of cures when both the MGG and OV variability acting together at optimum oxygen partial pressure. This condition reduces the $\sigma(V_{TH})$ to $17.8mV$ at the optimal p_{O2} value of $11.8 \times 10^{-3} atm$. Fig.6.12 shows the histogram of V_{TH} computed for MGG acting aline, and MGG, OV acting together at optimum and sub-optimum value of p_{O2} values. Clearly, under all conditions except at the optimal condition, $\sigma(V_{TH})$ increases.

$\sigma(V_{TH})$ for different grain sizes:

At the optimal condition, the value of $\sigma(V_{TH})$ for across the grain sizes do not vary much. But, as shown in the Fig.6.3(b), the value of $\sigma(V_{TH})$ increases with the increasing grain sizes of the metal deposited. When this was



(a) I_{DS}-V_{DS} curves of MGG (b) I_{DS}-V_{DS} curves of MGG and OV

Figure 6.11: I_{DS}-V_{DS} curves showing reduction in $\sigma(V_{TH})$

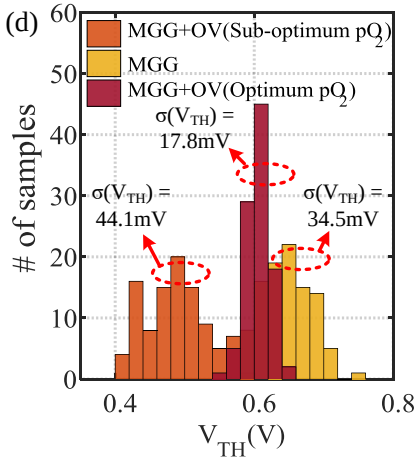


Figure 6.12: Histogram of V_{TH}

compared against the $\sigma(V_{TH})$ obtained for the case with both OV and MGG variations are present at the optimum condition, as shown in Fig.6.13(a), it can be concluded that with the increasing grain size , reduction in the $\sigma(V_{TH})$ value also increases. As evident in the Fig.6.13(b), more than 50% reduction in $\sigma(V_{TH})$ can be observed for the grain size of $9nm$.

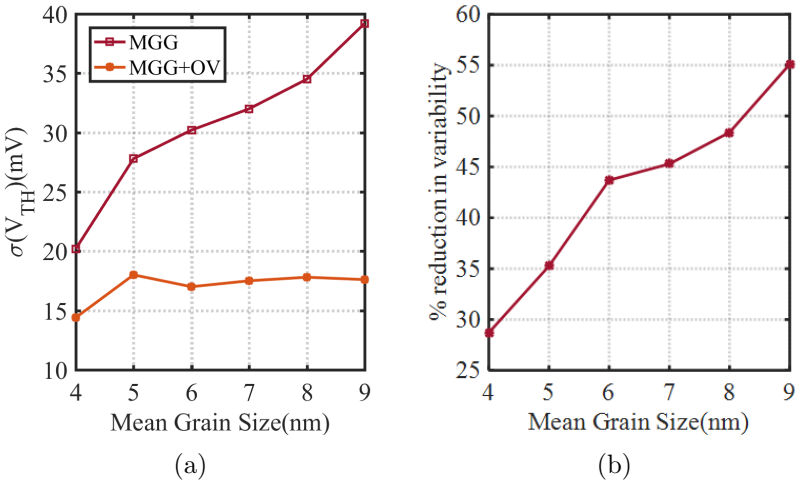


Figure 6.13: Comparison of $\sigma(V_{TH})$ for different grain sizes

Mean value of V_{TH} ($\mu(V_{TH})$):

Along with the $\sigma(V_{TH})$, the mean value of threshold voltage ($\mu(V_{TH})$) also reduces, at the optimal condition. This can be seen the Fig.6.14(b). At the lower value of oxygen partial pressure, as more number of oxygen vacancies get created causing reduction in the $\mu(V_{TH})$ value. As the value of oxygen partial pressure increases, less oxygen vacancies get formed. Hence $\mu(V_{TH})$ will be dominated by MGG variations, increasing the value of $\mu(V_{TH})$. This steady increase in the value of $\mu(V_{TH})$ can be observed in the Fig.6.14(b).

$\sigma(V_{TH})$ at different grain orientation probabilities:

When the orientation probabilities are changed by considering the metal grain granularity alone, at the low probability value and at high probability value the resulting MGG variability is low. This is due to the fact that the overall workfunction is dominated by one type of the grain orientation and hence similar workfunction exists across the gate. Beyond these extreme points, the variability will start increasing resulting highest variability at the

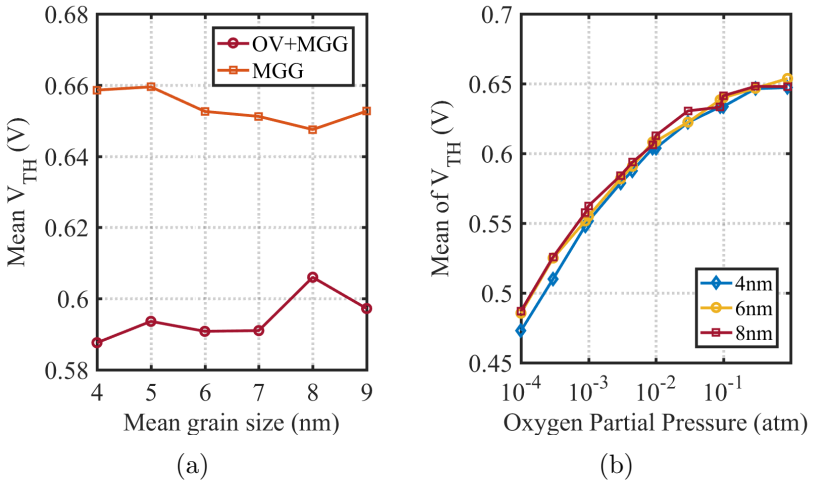


Figure 6.14: Mean Values of V_{TH}

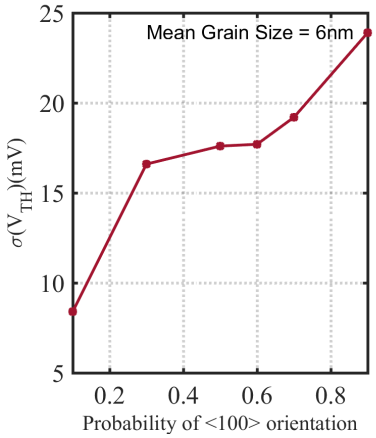


Figure 6.15: $\sigma(V_{TH})$ for various grain orientation probabilities

mid point.i.e. at 50%[5].

In the presence of both oxygen vacancy and metal grain granularity variability, at the optimal condition, low probability of grain orientation with high workfunction results in low variability. This is because as the low workfunction grain dominates the transistor gate and in turn there will not be many oxygen vacancies. As the probability of high workfunction grain gets increased, number of oxygen vacancy also gets increased, resulting increase in variability as shown in Fig.6.15. The histogram plot of threshold voltage

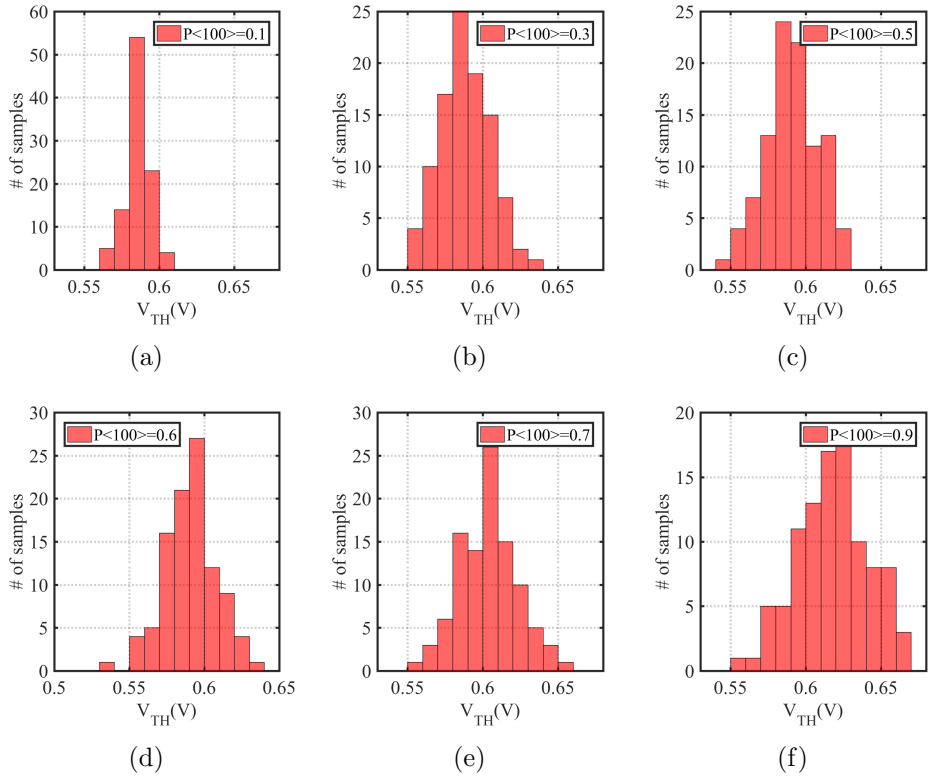


Figure 6.16: Histogram of V_{TH} for various grain orientation probabilities

at various grain orientation probabilities is plotted in Fig.6.16.

It is important to note that the variability values stated in 6.15 has been obtained at $750K$ and is a pessimistic value for higher probabilities. As stated in [7], the probability presence of high workfunction grain increases with increasing temperature.

This implies that the gate first process with $1300K$ is not an optimal condition because of following reasons:

- Higher gate processing temperature results in metal gate with grains in preferred orientation with high workfunction grains [7]. This results in higher variability as shown in Fig.6.15.

- As the gate formation temperature increases, the concentration of oxygen vacancies also increases than the obtained concentration for Fig.6.15.

Hence at $1300K$, the over all variability will be much more than the stated value.

CHAPTER 7

CONCLUSIONS

This work introduced an innovative methodology to study the interaction of oxygen vacancy and metal grain granularity. When the proposed model was simulated in FinFET, it was found that the variability induced by oxygen vacancy and metal grain granularity can balance each other.

Considering the fact that individually, oxygen vacancy and metal grain granularity affect threshold voltage in opposite directions and with the tendency of oxygen vacancy to form under high workfunction metal grain, carefully chosen concentration of oxygen vacancy can effectively "cancel out" the variability induced by metal grain granularity.

As the variability induced by oxygen vacancy and metal grain granularity aggravates with the scaling of transistor size and with the use of multi gated transistor, this novel methodology provides a solution to reduce the threshold voltage variability.

CHAPTER 8

REFERENCES

[1] "Tsmc and oip ecosystem partners deliver industry's first complete design infrastructure for 5nm process technology." [Online]. Available: https://www.tsmc.com/tsmcdotcom/PRListingNewsAction.do?action=detaillanguage=Enewsid=THPGWQTHTH

[2] "Itrs 2002." [Online]. Available: http://www.itrs2.net/

[3] S. S.Mukhopadhyay, *Low-power variation-tolerant design in nanometer silicon*. New York, NY, USA: Springer, 2011.

[4] C. B. TW. Xingsheng, A. R. Brown and A. Asenov, "Statistical variability and reliability in nanoscale finfets," *Proc. IEEE IEDM*, p. pp. 5.4.1–5.4.4, 2001.

[5] A. R. Trivedi, T. Ando, A. Singhee, P. Kerber, E. Acar, D. J. Frank, and S. Mukhopadhyay, "A simulation study of oxygen vacancy-induced variability in hfo_2/metal gated soi finfet," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1262–1269, 2014.

[6] H. T. G. H. C. R. M. Grovenor and D. A. Smith, "The development of grain structure during growth of metallic films," *Acta Materialia*, vol. 32, no. 5, p. pp. 773–781, May 1984.

[7] V. K. D. H. F. Dadgour, K. Endo and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—part i: Modeling, analysis, and experimental validation," *IEEE Trans. Electron Devices*, vol. 57, no. 10, p. pp. 2504–2514, Oct. 2010.

[8] A. Cottrel, *Introduction to the Modern Theory of Metals*. London, U.K.: Inst. Metals, 1998.

[9] N. Lang and W. Kohn, "Theory of metal surfaces: Charge density and surface energy," *Phys. Rev. B, Condens. Matter*, vol. 1, no. 12, p. pp. 4555–4568, June 1970.

[10] N. Gaillard et al., "Characterization of electrical and crystallographic properties of metal layers at deca-nanometer scale using kelvin probe force microscope," *Microelectron. Eng*, vol. 86, no. 11/12, p. pp. 2169–2174, Nov./Dec 2006.

[11] V. K. D. H. F. Dadgour, K. Endo and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—part ii: Implications for process, device, and circuit design," *IEEE Trans. Electron Devices*, vol. 57, no. 10, p. pp. 2504–2514, Oct. 2010.

[12] K. Ohmori et al., "Impact of additional factors in threshold voltage variability of metal/high-k gate stacks and its reduction by controlling crystalline structure and grain size in the metal gates," *Proc. IEEE IEDM*, p. pp. 1–4, June 2008.

[13] G.Indalecio et al., "Scaling of metal gate workfunction variability in nanometer soi-finfets," *ULIS Conf.*, 2014.

[14] O. B. J. M. López, F. J. Gordillo-Vázquez and J. M. Albella, "Low grain size tin thin films obtained by low energy ion beam assisted deposition," *Appl. Surf. Sci.*, vol. 173, p. pp. 290–295, March 2001.

[15] R. C. R. Banerjee and P. Ayyub, "Influence of the sputtering gas on the preferred orientation of nanocrystalline titanium nitride thin films," *Thin Solid Films*, vol. 405, p. pp. 64–72, Feb. 2002.

[16] K. Hubbard and D. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *Journal of Material Research*, vol. 11, no. 11, pp. pp. 2757–2776, November,1996.

[17] H. D. H. Takeuchi and T.-J. King, "Impact of oxygen vacancies on high-k gate stack engineering," *Proc. IEEE IEDM*, p. pp. 829–832., Dec.2004.

[18] K. Shiraishi et al., "Physics in fermi level pinning at the poly si/hfbased high-k oxide interface," *Proc. VLSI Technol. Dig. Tech. Papers*, p. pp. 108–109., 2004.

[19] A.Kerber et al., "Origin of the threshold voltage instability in sio2/hfo2 dual layer gate dielectrics," *IEEE Electron Device Letters*, vol. 24, no. 2, pp. pp. 87–89, 2003.

[20] A.Kerber et al., "Charge trapping and dielectric reliability of sio/sub 2/-al/sub 2/o/sub 3/ gate stacks with tin electrodes," *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. pp. 1261–1269, 2003.

[21] C.Hobbs et al., "Fermi level pinning at the polysi/metal oxide interface," *Symp. VLSI Technololgy*, 2003.

[22] Z.Ren et al., "Device design considerations for ultra-thin soi mosfets," *IEEE International Electron Devices Meeting 2003*, 2003.

[23] H. D. H. Takeuchi and T.-J. King, "Observation of bulk hfo2 defects by spectroscopic ellipsometry," *J. Vac. Sci., Technol. A, Vac.Surf., Films*, vol. 22, no. 4, p. pp. 1337–1341, 2004.

[24] W.Zhu et al., "Hfo/sub 2/ and hfalo for cmos: thermal stability and current transport," *IEDM Tech*, Dec.2001.

[25] E.Cartier et al., "Role of oxygen vacancies in vfb/vt stability of pfet metals on hfo_2," *Proc. Symp. VLSI Technology*, p. pp. 230–231, 2005.

[26] O. S. J. Robertson and A. A. Demkov, "Fermi level pinning by defects in hfo_2-metal gate stacks," *Applied Physics Letters*, vol. 91, no. 13, pp. pp. 132 912–1–132 912–3, 2007.

[27] Y. Akasaka et al., "Modified oxygen vacancy induced fermi level pinning model extendable to p-metal pinning," *Japanese Journal of Applied Physics*, vol. 45, no. 2, pp. 46–50, December 2006.

[28] S. Guha and V. Narayanan, "Oxygen vacancies in high dielectric constant oxide-semiconductor films," *Physical Review Letters*, vol. 98, no. 19, p. p. 196101, 2007.

[29] "Synopsys sentaurus tcad." [Online]. Available: https://www.synopsys.com/silicon/tcad.html

[30] "Sentaurus structure editor." [Online]. Available: https://www.synopsys.com/silicon/tcad/structure-editor.html

[31] "Sentaurus device." [Online]. Available: https://www.synopsys.com/silicon/tcad/device-simulation.html

[32] E.Cartier et al., "pfet vt control with hfo_2/tin/poly-si gate stack using a lateral oxygenation process," *Proc. Symp. VLSI Technol.*, p. pp. 42–43, 2009.

[33] S. Guha and P. Solomon, "Band bending and the thermochemistry of oxygen vacancies in ionic metal oxide thin films," *Appl. Phys. Lett.*, vol. 92, no. 1, pp. pp. 012 909–1–012 909–3, 2008.

[34] C.Kittel, *Introduction to Solid State Physics*. New York, NY, USA: Wiley, 1986.

[35] M. H. E. Cartier and M. Copel, "Oxygen passivation of vacancy defects in metal-nitride gated hfo2/sio2/si devices," *Appl. Phys. Lett.*, vol. 95, no. 1, pp. pp. 042 901–1–042 901–3, 2009.

[36] A. A. P. Broqvist and A. Pasquarello, "Band alignments and defect levels in si/hfo2 gate stacks: Oxygen vacancy and fermi-level pinning," *Appl. Phys. Lett.*, vol. 92, no. 13, pp. pp. 132 911–1–132 911–3, 2008.

[37] D. Ceresoli and D. Vanderbilt, "Structural and dielectric properties of amorphous zro2 and hfo2," *Phys. Rev. B.*, vol. 74, p. p. 125108, Sept.2006.

[38] P. K. K. K. Y. Toh and R. G. Meyer, "An engineering model for short-channel mos devices,," *IEEE J. Solid-State Circuits*, vol. 23, no. 4, p. pp. 950–958, August 1988.

VITA

Name	Madhu Padmanabha Sumangala
Education	M.S. Electrical and Computer Engineering 2017 – 2020 University of Illinois at Chicago
	B.E. Electronics and Communication Engineering 2007 – 2011 Visvesvaraya Technological University
Projects	Design and layout of two state operational amplifier in 180nm technology.
	Design and layout of SRAM in 28nm technology.
	Design of 64 bit MIPS processor using VHDL.
	Design of Low dropout regulator in 180nm technology.
Experience	Student Researcher at Advanced Electronics of Nano Devices (AEON) Laboratory, UIC
	Senior Software Engineer, HCL Technologies