Switching Sequence-and Switching Transition Control of Power Electronic Systems

BY

DEBANJAN CHATTERJEE

B.E., Jadavpur University, India, 2015

THESIS

Submitted as partial fulfilment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Chicago, 2021

Defense Committee:

Sudip K. Mazumder, Chair and Advisor
Mohammad Shadmand
Lina He
Danilo Erricolo
Jose Rodriguez, Andres Bello National University

Dedicated to my mom and dad

First and foremost, I would like to thank my PhD. advisor Prof. Sudip K. Mazumder for his guidance, time, financial support, and technical help. I would like to express my gratitude to my mom, Smt. Debjani Chatterjee, and my late father Shri. Kanchan Chatterjee for their unconditional support, love, and encouragement.

I would like to thank the Office of Naval Research (Award No. N00014-17-1-2695) for financial support. I would also like to thank my Ph.D. committee members, Prof. Jose Rodriguez, Prof. Mohammed Shadmand, Prof. Lina He, and Prof. Danilo Erricolo, for their valuable time.

I want to acknowledge the help of many past and present colleagues at the Laboratory of Energy and Switching Electronics System (LESES), namely Ankit Gupta, Harshit Soni, Abhijit Kulkarni, Nikhil Kumar, Moien Mohamadi, Shantanu Gupta, and Congbo Bao.

I would like to thank my friends Vikram Bhattacharjee, Saswata Gupta, Rahul Mallik, Sayantan Mahapatra, and Prolay Krishna Chanda for giving me strength throughout my PhD studies.

PREFACE

This dissertation is an original intellectual product of the author, D. Chatterjee. All the work presented here was conducted in the Laboratory for Energy and Switching-Electronics Systems (LESES) at the University of Illinois at Chicago.

The results of our research have been previously published as journal, conference, and workshop articles in:

- IEEE Transactions on Power Electronics (Debanjan et al., 2020,2021)
- IEEE Transactions on Power Electronics (Harshit et al., 2019)
- IEEE Energy Conversion Congress and Exposition (ECCE'2019) (Debanjan et al., 2019)
- Power electronics for Distributed Generation and Systems (PEDG'2016) (Debanjan et al, 2016)
- Power electronics for Distributed Generation and Systems (PEDG'2021) (Debanjan et al, 2021)

The results of our research are currently in review in:

- IEEE Access (Debanjan et al., 2021)

The copyright permissions for reusing the published materials are given in Appendix I.

Debanjan Chatterjee

June 2, 2021

CONTRIBUTION OF AUTHORS

Major parts of the results and discussions in this thesis are taken from my published or submitted papers with written permission from the journals (see Appendix K). Below, the contributions of all the co-authors are listed:

Authors' contributions in IEEE Transactions Power Electronics, 2020,2021, ECCE'18, PEDG'16, 21, IEEE Access'21: D. Chatterjee, and S. K. Mazumder conceived the main ideas and led the investigations. D. Chatterjee undertook the analytical analysis and experimental study. D. Chatterjee, and S. K. Mazumder contributed to the write-up of the manuscripts.

Authors' contributions in IEEE Transactions on Power Electronics, 2019 H. Soni, and S.K. Mazumder conceived the main idea and led the investigation. Harshit Soni undertook the initial circuit design and performed the experimental analysis. A Gupta, D. Chatterjee, and A. Kulkarni modified the experimental set-up to validate some control algorithms for different load conditions. D. Chatterjee did extensive stability analysis of the control algorithms. H. Soni, S. K. Mazumder, A Gupta, D. Chatterjee, and A. Kulkarni contributed to the review and write-up of the manuscript.

TABLE OF CONTENTS

CHAPTER PAGE

TABLE OF CONTENTS (Continued)

CHAPTER PAGE

TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF FIGURES

FIGURE PAGE

LIST OF FIGURES (Continued)

FIGURE PAGE

LIST OF FIGURES (Continued)

FIGURE PAGE

LIST OF FIGURES (Continued)

FIGURE PAGE

LIST OF FIGURES (Continued)

FIGURE PAGE

LIST OF ABBREVIATIONS

- AC: Alternating Current
- CC: Constant-current
- CCL: Constant-current load
- CCM: Continuous conduction mode
- CM: Common mode
- CPL: Constant-power load
- DC: Direct Current
- DM: Differential-mode
- DSP: Digital signal processor
- EMI: Electromagnetic interference
- FET: Field-effect transistor
- GaN: Gallium nitride
- MPC: Model predictive control
- PCB: Printed circuit board
- PCL: Pulsating-current load
- PES: Power-electronic system
- PI: Proportional integral
- PWL: Piecewise Linear
- PWM: Pulse-width modulation
- SS: Predictive switching sequences
- PSBC: Predictive switching sequence-based control
- SBC: Sequence-based control
- SS: Switching sequence
- STC: Switching transition control

- SiC: Silicon carbide
- WBG: Wide-band gap

SUMMARY

In this dissertation, an approach for switching sequence (SS)-based control (SBC) for a high-frequency higher-order power electronic system is delineated. This contrasts with a conventional linear-control design of a power-electronic system (PES) where the gains of the control laws are typically determined by small-signal analysis of the averaged model of the PES. The closed-loop control of such a PES using its small-signal model is often found to be unsatisfactory regarding the overall stability and performance. This is of relevance to the PES catering non-linear time-varying and reduced damped loads. To address the challenges in control design for a PES driving such challenging loads, this dissertation delineates an optimal switching-sequence-based control (SBC) scheme, which applies stability-bound switching sequence(s) to the PES. The SS based control design is multi-scale in nature. It encompasses slow-scale PES state regulation and fast-scale PES phenomenon like switching losses, device EMI etc.

Also, a novel method is formulated to ensure the reachability of the PES dynamics based on its switching sequence in terms of the time horizon of the switching sequence and the allocation of this time among the switching states of the same switching sequence. This is ascertained by modeling the PES and the pulsating load as a nonlinear map and then using this map and multiple Lyapunov functions determined by solving a set of linear-matrix inequalities (LMIs)) corresponding to each of the switching states of a given switching sequence. It is further shown that the knowledge of the stability bounds of a reachable switching sequence helps in reducing the online computation time for optimal SBC associated with solving the optimization problem by reducing the overall search space. To validate the optimal SBC, an experimental GaN-FET-based dc/dc HF Ćuk-PES is fabricated and tested. The overall SBC is implemented on a series of very low-cost industrial DSPs, which also implements an observer to preclude the need for a plurality of sensors for the higher-order Ćuk-PES. The overall performance of the SBC is found to be satisfactory under varied dynamical conditions.

After stabilizing fast time-varying and reduced damped loads, it was investigated whether such SBC laws can autonomously shape the conducted EMI spectra of a PES. This pushes the boundary of such controllers to encompass much faster scales. It is seen that the careful design of such control laws offers higher programmability to conventional PES design where bulky EMI filters have been traditionally used to reduce EMI of switching power converters. An EMI filter is always a less programmable solution since it is usually designed for the worst-case EMI mitigation and usually overkill for a PES operating at reduced load condition. The switching sequence-based control, hence, offers EMI mitigation across wide operating regions, without compromising PES regulation and tracking. Moreover, SBC does so using

switching sequences that guarantee the reachability of the PES dynamics. Hence, classical drawbacks related to conventional open-loop EMI mitigation techniques can be used as constraints in the SBC formulation to operate the EMI mitigated PES under a wide operating regime under desired conditions. The work may be of paramount importance for operating the ultra-fast-transition recent wide-bandgap semiconductor devices at higher power with increasing switching frequencies, which is usually desirable for increased power density and reduced switching losses. It is shown by experimental results how the switching sequences do complete differential-mode and reduced-scale common mode EMI mitigation for the PES while maintaining perfect state regulation for a higher-order non-minimum phase PES.

The final part of the thesis encompasses the design of a switching transition-based control scheme to shape the rise-fall times of the switching sequences of the WBG devices. To achieve a higher switching frequency of a PES, yet low switching losses, the speed of switching transitions of power semiconductor devices (PSDs) need to be increased. However, such fast transitions adversely affect PES performance in terms of electromagnetic interference (EMI) and device stress. Hence, a switching transition control scheme is developed to create optimality between switching PSDs with higher transitions yet maintaining good EMI performance and device stress. The switching transition control (STC) framework helps to maintain a target efficiency of an HF PES by controlling the high $\frac{di}{dt}$ and $\frac{dv}{dt}$ regions of a WBG device on the fly. It does so in a way that the increase in efficiency does not come at a cost of increased device stress/EMI. An HF Ćuk PES using a Cree SiC Mosfet half-bridge module is fabricated for the testing purpose of the STC framework. The work has ramifications in meeting the system-level requirements of a PES.

Chapter 1

1.INTRODUCTION

Parts of this chapter, including figures and text, are based on my following papers:

D. Chatterjee and S. K. Mazumder, “Optimal switching sequence-based control of a differential-mode inverter,” in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1–8.

D. Chatterjee and S. K. Mazumder, “Turn-on switching transition control using a GaN-FET based active gate drive,” in *2021 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, accepted.

D. Chatterjee and S. K. Mazumder**, “**Switching transition control to improve efficiency of a dc/dc power-electronic system,” *IEEE Access*, doi: 10.1109/ACCESS.2021.3092017.

H. Soni, S. K. Mazumder, A. Gupta, D. Chatterjee, and A. Kulkarni, “Control of isolated differential-mode single- and three-phase Ćuk inverters at module level,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8872-8886, 2018.

D. Chatterjee and S. K. Mazumder, “Switching-sequence control of a higher-order power-electronic system driving a pulsating load,” *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 1096–1110, 2020.

D. Chatterjee and S. K. Mazumder, "EMI Mitigation of a Ćuk Based Power-Electronic System using Switching-Sequence-based Control," *IEEE Trans. Power Electron*., vol. 36, no. 9, pp. 10627-10644, 2021.

D. Chatterjee and S. K. Mazumder, “Predictive switching sequence-based control for constant power load,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1574–1583.

1.1. Importance of switching sequence control for a power electronic system

Switching sequence-based control (SBC) laws, when designed based on topological switching behavior can positively affect the slow-scale, medium-scale and fast-scale dynamics of a PES[1]. The topological switching dynamics of a PES coupled with the load dynamics can be used to predict future control actions that can lead to desirable behavior of the PES. The slow and medium-scale dynamics can range from energy source optimization, dc output voltage regulation of a dc/dc PES[2] to input PFC of a rectifier[3]. The fast scale encompasses switching losses of a PES, device EMI spectrum, device stress levels, etc.[4]. Figure 1a shows the evolution of a PES state based on a switching sequence (SS). The spectrum of the SS shows the scales addressed by such control design where T_{kw} denotes the time horizon of the SS (i.e. the total time period of the SS), α_{k1} denotes the time allocation of a first generalized switching state in the SS (a SS can have multiple switching states 1-0-..-0-1, etc., α_{k1} denotes the on-time of the first switching state) , and t_r, t_f denotes the rise and fall times (switching transition times) of a switching state in the SS respectively. For an illustrative example, consider the switching sequence (SS) in Figure 1a to consist of only two states, 0 and 1. Consider T_{kw} =10 μs ($T_{kw}^{-1} = 100$ *k*Hz) and t_r, t_f to be 30 *n*s each (for WBG devices like GaN and SiC), the spectra of a SS encompass the follows: dc and slow scales that can lead up to 2-10 *k*Hz. Traditional small signal and averaged model-based controllers usually achieve a maximum control bandwidth of this order to do steady-state output voltage regulation as in case of dc/dc converters or rectifiers, or perform steady-state tracking like in case of inverters[5]; next comes faster scales at 100 *k*Hz and its higher sidebands. T_{kw} or the time horizon variation of the switching sequences affect these scales. They have a direct impact on conducted and radiated EMI signature of a SS, along with PES losses in form of switching loss, deadtime loss, etc; finally, the sideband of the switching transitions of the sequences comes at above 30 MHz for t_r, t_f to be 30 *n*s. They also directly affect common mode EMI and switching losses of the PES, along with reliability of the WBG devices by affecting $\frac{dv}{dt}, \frac{di}{dt}$ stresses. Figure 1b further explains the scenario. It shows that for the same averaged control command generated by a conventional (say PI) controller to maintain an average output voltage of a PES, two different switching sequences may result depending on modulation types, which may result in different fast scale response of the system.

Using PES switching behavior that addresses all the scales mentioned above to synthesize controllers is of importance for a PES catering challenging loads. Challenging loads include those which have very low damping and

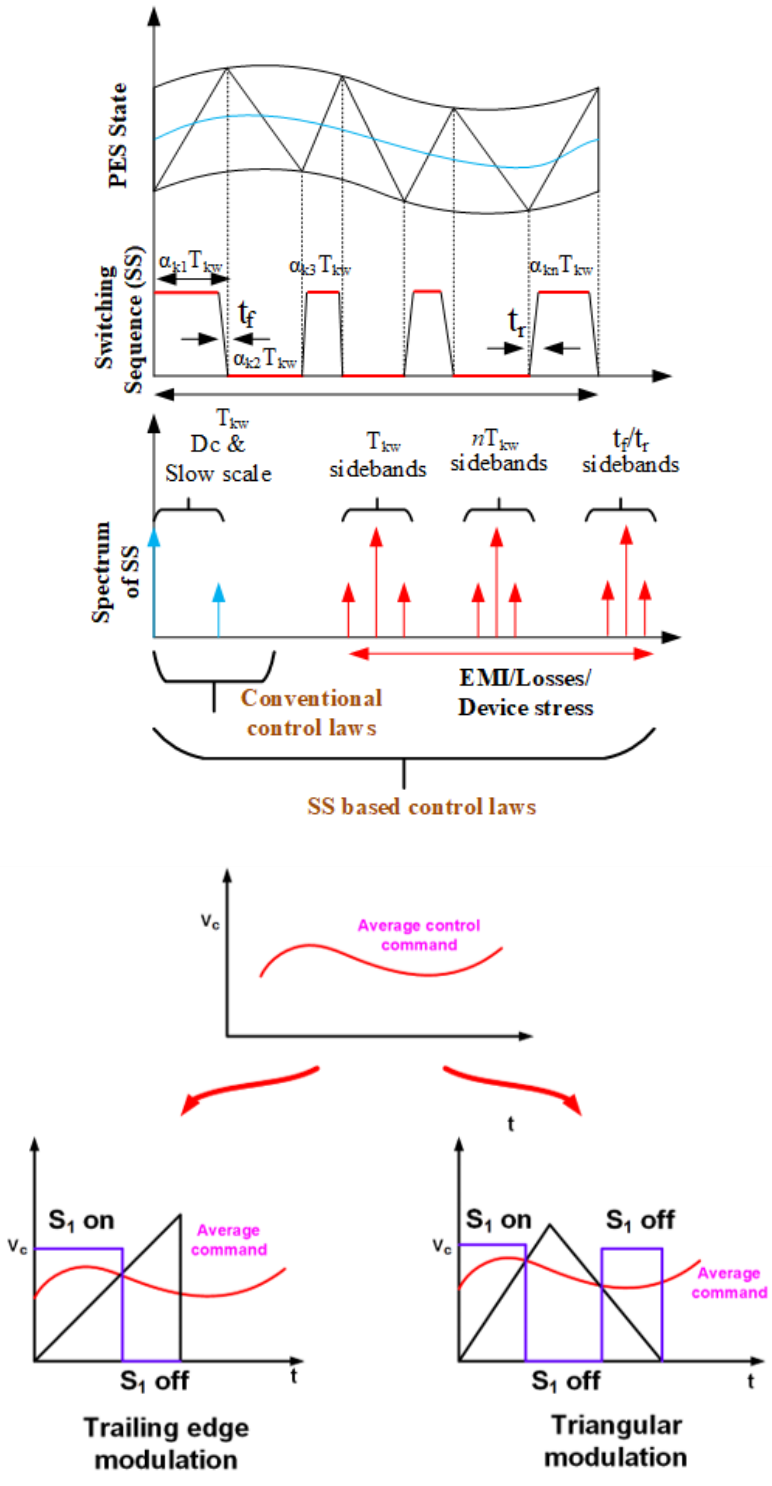


Figure 1. (a) Figure showing the scales addressed by switching sequence-based control laws. The spectra of the sequences range from dc/slow scales (PES dc average regulation, line frequency tracking of a PES) to faster scales like sidebands of the switching sequences and transition time of the sequences. (b) Figure showing how an average control command can lead to different switching states in a switching sequence which may lead to different fast-scale properties like switching losses, EMI, etc.

negatively affects PES stability margins. Hence, such fast control laws are required for higher-order power-electronic systems (PESs) that supply nonlinear time-varying and reduced damped loads with higher temporal scales [6], [7]. Such loads require careful attention in control design since large-signal variations in voltages and currents may lead to stability and power-quality issues. For such a PES, typical linear controllers (that are designed to operate in the vicinity of the system equilibrium) as well as several nonlinear controllers, are often unable to ensure large-signal stability and satisfactory performance. Figure 2 depicts a case illustration to justify the use of such SS based control/SBC design. It illustrates the performance of one such recently-outlined nonlinear control law [5] for a Ćuk PES feeding a 1 *k*Hz time-varying pulsating load. (The pulsating frequency is so chosen, such that resonance due to the presence of poles and zeros of the PES in the vicinity of 5 *k*Hz are not excited). The control law failed to regulate the output voltage of the PES at such higher temporal scales as shown in Figure 2. This is primarily because the gains of the nonlinear controller, synthesized using a reduced-order slow-scale model of the PES, are pushed to the limits causing instability. This implies that, for such a fast-varying-load application, SS based control strategy/SBC, that uses model of PES encompassing wider temporal scales, is needed so that satisfactory large-signal stability of the PES is ensured while exhibiting fast dynamic response.

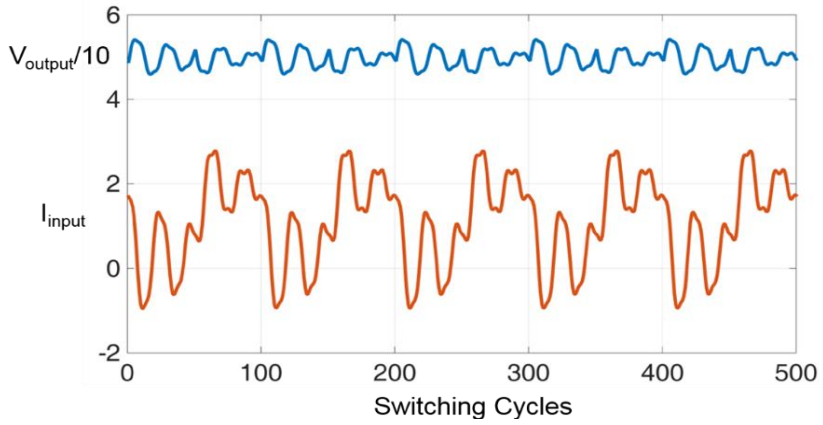


Figure 2. Illustration of the PES response using a nonlinear controller [3] feeding a pulsating load with a repetition rate of 1 *k*Hz. The upper and lower traces show instabilities in the scaled output voltage and the input inductor current, respectively. The results are for a Ćuk PES described in Chapter 2. The figure highlights inability of the controller to give the desired performance.

1.2. Use of optimal control theory for synthesis of the switching sequences

Advanced sliding-mode controllers [4], [5] may yield robust closed-loop PES feeding such nonlinear time-varying pulsating loads. Notwithstanding, for a higher-order PES, efforts leading to computation of the explicit control action

based on a Lyapunov function is non-trivial. Backstepping- and passivity-based control laws [10], [11] use smooth averaged models for control formulation that mitigate the range of temporal scales. Dynamic feedback linearization [12] may be a possibility as well; however, if the PES is a higher-order system, determining the convergence of the zeroth-order dynamics is challenging.

Optimal controllers, based on multiscale discontinuous models of the PES, demonstrate promise in constituting the SS. In that regard, model-predictive-control (MPC) laws solve the underlying optimal-control problems by controlling the switching states of a PES. As a result, the resulting switching sequence in a MPC problem when applied to a PES may result in satisfactory performance but, the stability of the PES is not always guaranteed [13]. This becomes an issue of importance for PES supplying reduced damped and fast time-varying loads exhibiting wide temporal scales. In contrast, optimal switching-sequence-based control laws (SBC), achieve optimality by directly controlling the stability-bound switching sequence(s) that yields robust performance of the PES even when it is driving a fast-switching or reduced damped load. Figure 3 delineates the distinction between a conventional linear-control synthesis and SBC formulation, which is devoid of a PWM modulator, as illustrated in [14], [15].

SBC underlies solution of an optimal control problem. References [16]–[22] outline how the modern optimal controllers, that underlie SBC, have evolved as attractive solutions for controlling PES that go beyond simple regulation to superior spectral shaping and switching-loss mitigation [16]. Reference [16] although discusses multi-

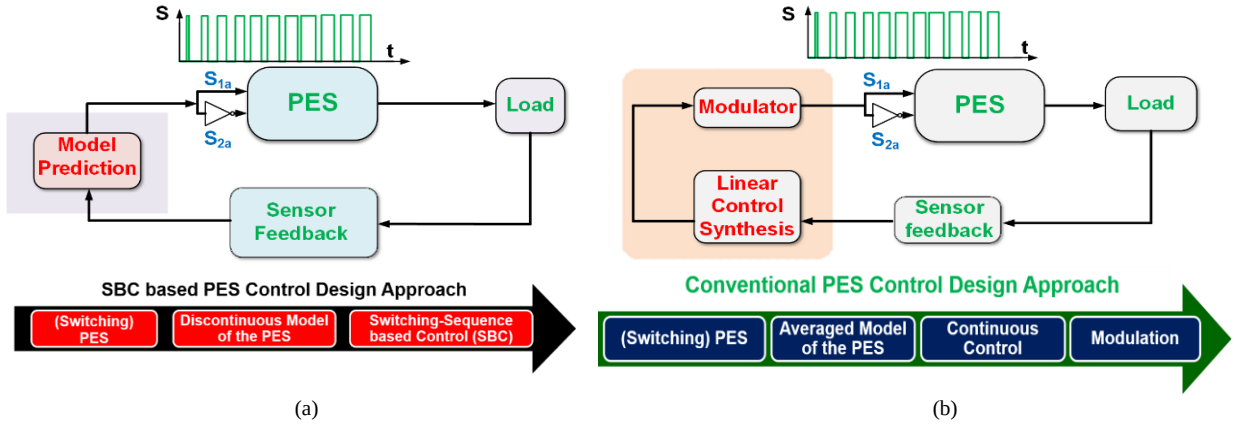


Figure 3. Illustration of (a) SBC scheme for PES and (b) a conventional linear control scheme. SBC precludes the need for a PWM modulator.

objective optimal control framework but adequate case illustrations are devoid in literature. References like [15], [23] on the other hand focus on another equally important objective: optimization techniques for high-frequency PESs so that the optimal solutions can be obtained online for ever-evolving switching frequencies of the PES.

Optimal controllers for lower-order non-minimum phase PES have been previously discussed in [15]-[19]; however, they do not take into consideration nonlinear loads for a higher-order PES operating at high frequency. References [20]-[22] primarily show deteriorated PES behavior with nonlinear reduced damped loads and the challenges in control formulation. The dissertation, hence, focusses on Ćuk based PES as an illustrative example to solve the issues related to PES control for such challenging loads seamlessly. Ćuk based PES is a non-minimum phase higher-order system that is difficult to control for non-linear loads and designing an SBC approach for this case scenario will make the control generalizable.

1.3. Choice of a higher-order PES prototype for sequence-based control

The choice of the Ćuk PES for dissertation study is twofold. Since SBC controllers are based on optimal control laws to create the SS for the PES, they require full-state feedback[15] which makes its application challenging in higher-order topologies and is an interesting research challenge. Optimal control laws as predictive controllers are generally used in topologies with higher switch count but lower PES state tally like VSI, buck, boost, buck-boost[15], [24], [32] to offset the requirement of a large number of sensor measurements. In boost-derived PES, usually, the output voltage is measured and estimation of the inductor current using simple Leuenberger observers is enough since the PES dynamics are usually observable with respect to the output voltage. However, for higher-order topologies like isolated Ćuk, linear observers cannot be used for state estimation easily as a higher number of sensors are required for observability. Hence, in this dissertation, it is shown how to design predictive controllers using non-linear Poincare map-based estimation to preclude sensor plurality.

Also, in recent literature, Ćuk PES modules are being used to create differential mode PES structures achieving modularity, reduced switch count, simple gate driver design due to low-side driven switches etc.[3], [33]. The modular Ćuk PES modules have been used to create differential-mode rectifiers, solid-state transformers, inverters, both single and three-phase. [3], [5], [33]. Since SBC is a modular control architecture in nature, once developed for a Ćuk PES dc/dc module, it can be used to seamlessly control all differential-mode structures.

1.4. Use of switching sequence-based control design to affect fast scale PES properties

In the 1st part of the dissertation, an SBC approach to mitigate the challenges associated with the control design of a higher-order non-minimum-phase PES supplying higher-frequency and reduced damped loads is undertaken. It is shown that this advanced controller outperforms conventional linear controllers in terms of performance since it can

achieve much higher bandwidth while maintaining the stability of the PES under consideration.

Apart from controlling fast temporal and reduced damped loads, it is then investigated whether SBC can impact fast-scale phenomenon like differential-mode (DM) and common-mode (CM) EMI of a PES.

Previous work in [16] shows how advanced controllers based on the model predictive control principle can affect fast scale properties of a PES like efficiency, shaping PES output/input spectrum. Using the same MPC principle, [19] shows how the switching behavior of the PES can be manipulated to decrease switching losses, while maintaining perfect state regulation at the output. This is because multiple switching sequences having different fast-scale response can result in the same dc average. Using a cost-function based approach which consists of both voltage/current regulation terms and switching loss terms, [19] proves that the control can select switching states in such a way that it can reduce losses and yet maintain good output characteristics of a PES. Although various literature like [16], [19] talk about improving PES efficiency on the fly, there is a dearth of work related to the use of such advanced control techniques for shaping the PES EMI spectrum. The motivation behind the use of such advanced control techniques to positively affect PES EMI is as follows:

1) Any PES when operated at higher power has a significant continuous input current which increases the magnetic size of the input differential-mode (DM) filter.

2) Also, the ultra-fast transition of the wide bandgap semiconductor devices makes input common-mode filters bulky and reduces the power density of the PES.

3) The EMI filter size hence offsets the power density of the PES that was supposed to increase many-fold with increasing switching frequency of these WBG systems.

Conventional EMI filters, based on guidelines delineated in [34], [35] are indispensable in PES design for conforming to the strict EMI standards. The filters reduce the PES design flexibility, and the DM EMI filter-PES interaction deteriorates the control performance of the system. However, this SBC, when applied to a PES, can directly affect the EMI spectrum and hence, they can be maneuvered to dictate the EMI signature of the PES. Hence, it is shown how the SBC based control architecture which solves an optimal control problem can incorporate the EMI standards in the system constraints to autonomously shape the EMI spectra of the PES. It is also investigated whether by doing so the SBC can bring down the size of the conducted EMI filter.

1.5. Beyond switching sequence to controlling the switching transitions

Till this point, SBC is used to control a higher-order non-minimum PES catering reduced damped and fast temporal loads, while also using the industrial EMI standards as multivariate PES constraints in the control problem to mitigate PES conducted EMI. So, the SS control, as explained in Figure 1a, till now, used only variation in the switching sequence, the time horizon T_{kw}, and time allocation of the 1-0,-01 states as $\alpha_{k1} - \alpha_{kn}$, for control. Using these control variables, SBC could affect (referring to Figure 1a) dc and slow scales (it could achieve higher control bandwidth while maintaining stability), and sidebands of the switching frequency (nT_{kw}). Hence, in the final chapter of the thesis, focus is shifted to control the switching transitions of WBG devices to shape the t_r, t_f sidebands as desired. The motivation behind controlling the switching transitions of the states in a SS is as follows:

The switching transition times of WBG devices are aggressively decreased [33], [36] to decrease switching losses at higher frequencies. The performance achieved by using fixed transition times of WBG devices prove inadequate in terms of common mode EMI spectrum, parasitic oscillations that may lead to increased device stress, and beyond a point hampers normal PES operation. Hence, an attempt is made to shape $\frac{di}{dt}$ and $\frac{dv}{dt}$ regions of a wide-band gap power semiconductor device (PSD) on the fly in the final chapter. It is done to create decreased device stress and EMI as the switching transitions of the PSDs are decreased. Previous work has been done on design of active gate drive techniques to control the transition of these devices [37], [38]. However, such literature seldom shapes the device transitions considering system-level requirements. In the current dissertation, depending on the device switching behavior, the switching transition control scheme (STC) maintains a PES target efficiency increment, across wide operating conditions while precluding excessive device stress. Hence, a unified control scheme is developed in this dissertation which takes care of slow-scale regulation to fast-scale control of the device switching transitions.

The dissertation has hence been organized as follows:

In the 2nd chapter, it is shown how the optimal SBC directly maneuvers the duration of switching states in a switching sequence of the Ćuk PES through minimization of an appropriate cost-function via effective case illustrations. A novel methodology to analyze the reachability of the PES dynamics in terms of the time horizon of a switching sequence has also been provided that in the long run may lead to the realization of such time-consuming control laws in industrial-scale processors by real-time computation time reduction. The approach delineated may benefit the solution of problems related to (but not limited to) electromagnetic launch systems [39], motor-drives with

pulsating current loads [40], design of controllers for linear induction motors [41] having pulsating current levels that can be used in launch systems, as well as PES networks in vehicular technologies feeding downstream PES.

Then in the 3rd chapter, the effect of such SS based control design on PES EMI is evaluated. It is shown how seamlessly the SS can be maneuvered to mitigate conducted emissions in a PES while maintaining perfect state regulation. The work has ramification in terms of a decrease in the EMI filter size of a PES, thereby increasing the efficiency and power density of the system.

Then in the 4th chapter, an STC scheme to shape the device switching transition is delineated. The chapter explains in considerable depth the synthesis of the STC network which has several design intricacies.

Finally, a conclusion is drawn in Chapter 5, with a brief explanation of some avenues of future research possibilities.

Chapter 2

2. SWITCHING-SEQUENCE CONTROL OF A HIGHER-ORDER POWER-ELECTRONIC SYSTEM

Parts of this chapter, including figures and text, are based on my following papers:

D. Chatterjee and S. K. Mazumder, "Optimal switching sequence-based control of a differential-mode inverter," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1–8.

D. Chatterjee and S. K. Mazumder, "Switching-sequence control of a higher-order power-electronic system driving a pulsating load," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 1096–1110, 2020.

D. Chatterjee and S. K. Mazumder, "Predictive switching sequence-based control for constant power load," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1574–1583.

This chapter is divided into two sub-parts. In Section 2.1 of this chapter, SBC design for fast-varying temporal loads is delineated. Such loads are extremely common in electromagnetic launch systems, induction motor drives etc. and the framework delineated in this chapter will provide a control approach to stabilize such loads. In Section 2.3, the same SBC will be used to control equally challenging and reduced damped constant power loads.

2.1. SBC for pulsating loads

For fast-varying pulsating loads, most of the existing literature delineates hardware modifications of PESs in terms of increased energy storage and lack proper control solutions. Reference [42] delineates topological advances required in a PES structure to power nonlinear pulsating loads, and [43] further adds on how to reduce pulsating load impacts on microgrids. Reference [44] uses coupled magnetics to improve PES dynamic response for pulsating loads. Similarly, [45] depicts modulation technique for a PES powering a pulsating load. In [6], aircraft generating systems supplying pulsating loads and their design guidelines, in terms of topology and control, have been outlined. Reference [46] describes high-power pulsating-load applications where large magnetics have been used for energy storage to deliver power to the load. Such systems operate at low pulse-repetition frequencies as reiterated in [47]. Similarly, [7] uses compensating devices for intermittent energy storage to improve PES dynamic response. Reference [48] also talks about using enhanced storage devices and simpler control techniques to supply pulsating load applications. Using minimal storage capabilities, [49] presents a neural-network (NN) based control framework to address problems related to pulsating loads in shipboards, but such systems operate at low switching frequencies which makes the use of NN techniques feasible. Also,[50] delineates advanced controllers to mitigate the effects of pulsed power loads, but the prediction models used are linearized about operating points and implemented in high-end processors that does not encompass online time savings in low-end digital processors.

To address the shortcomings in the work delineated in the above literature to provide a good framework for pulsating load control, three broad steps are undertaken in the SBC design procedure in the Section 2.1.

Section 2.1.1 outlines the first step regarding the discrete modeling of the PES feeding the pulsating load. Subsequently, Section 2.1.2 provides the method for reachability analysis of the PES in terms of its switching sequence. In the final step, outlined in Section 2.1.3, optimization of the PES using one or more of these reachable switching sequence(s) to ensure desired performance optimality. This section also provides the generalized framework for SBC architecture for a PES. Subsequently, Section 2.1.3.1 delineates the online optimal SBC synthesis for a

specific Ćuk PES, which includes the description of the discrete prediction model of the PES, the performance index for the control, and the observer design that precludes the full-sensor-feedback requirement for the higher-order PES. The results are discussed in Section 2.1.4.

2.1.1. Modeling of the PES driving a pulsating load

SBC is a closed-loop optimal policy, where given a k^{th} switching sequence with h switching states, its time horizon (T_{kw}) and the allocation ($\alpha_{k1}, \ldots., \alpha_{kh}$) of this time among each of its switching states are computed on the fly. Figure 4 portrays two such switching sequences of a PES, to explain the point, having time horizon T_{kw} and $T_{(k+1)w}$ respectively, along with the time allocation (($\alpha_{k1}, \ldots., \alpha_{kh}$) for the 1st sequence and ($\alpha_{k+1_1}, \ldots., \alpha_{k+1_{h1}}$) for the 2nd sequence) amongst the switching states (h switching states in the first switching sequence and $h_1$switching states in the second switching sequence). The optimal values of these sets of parameters in SBC are determined in two steps. Initially, the outer limits of these two sets of parameters are determined using a Lyapunov-based reachability analysis. This is detailed in Section 2.1.2, which requires a hybrid nonlinear model of the PES driving the pulsating load.

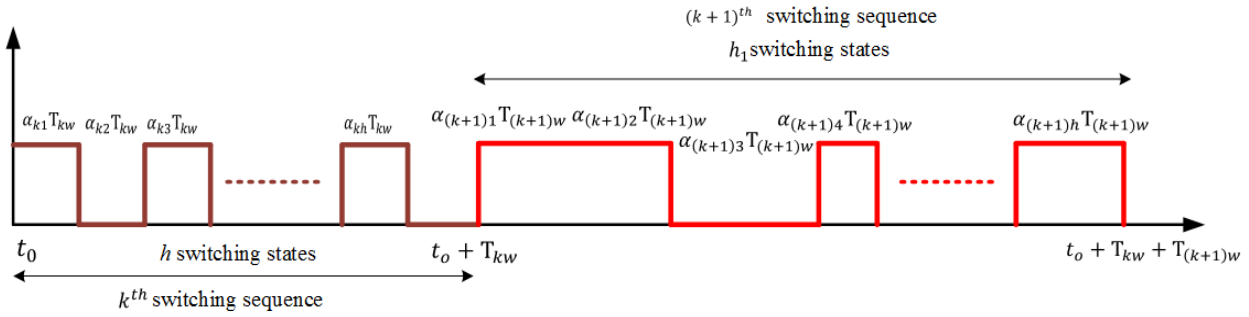


Figure 4. Illustration of the k^{th} and $(k+1)^{th}$ switching sequence of a PES comprising h and h_1 switching states, respectively.

Subsequently, the optimal values of these two sets of parameters from the above set are determined in real-time by solving an optimization problem outlined in Section 2.1.3. In this section, the nonlinear model of the PES driving a pulsating load is outlined.

Figure 5 depicts a pulsating load with the dynamics defined by the following harmonic series:

$$i_{load}(t) = \frac{1}{2} i_{load1} + \sum_{m=1}^{\infty} \{a_m \cos(w_m t) + b_m \sin(w_m t)\} \quad (1a)$$

$$\frac{1}{2} i_{load1} = \text{average}(i_{load}(t)) \quad (1b)$$

$$a_m = \frac{\sin(2m\pi D_{load})}{m\pi} \Delta i_{load} \quad (1c)$$

$$b_m = \frac{1-\cos(2m\pi D_{load})}{m\pi}\Delta i_{load} \tag{1d}$$

The physical meaning of the symbols in (1a) are depicted in Figure 4, where D_{load} denotes the duty cycle of the pulsating load, Δi_{load} denotes the magnitude of the load transition and T_{load} denotes the time period of the load pulse. Inverse of T_{load} gives the pulsating load frequency f_{load}.

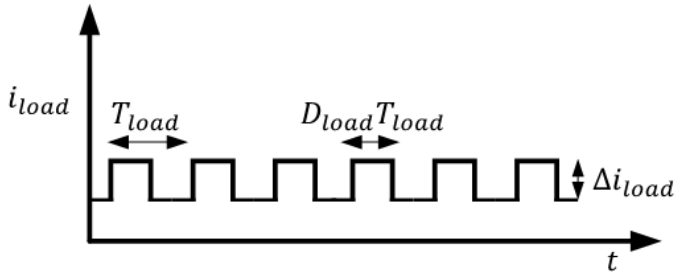


Figure 5. Illustration of a pulsating load with transition level denoted by Δi_{load}, duty cycle denoted by D_{load}, and the switching time period of the pulse denoted by T_{load}.

For a practical pulsating load with finite slew rate,

$$\dot{\hat{x}}(t) = \hat{A}_{kn}\hat{x}(t) + \hat{B}_{kn} + \frac{1}{2}i_{load1} + \sum_{m=1}^{\infty}\{a_m \cos(w_m t) + b_m \sin(w_m t)\} \tag{2}$$

where $\hat{A}_{kn}$ and $\hat{B}_{kn}$ are matrices that describe the PES without the pulsating load and have been defined in [5]. Equation (2) is rewritten in a compressed form as follows:

$$\dot{x}(t) = A_{kn}x(t) + B_{kn} \tag{3}$$

where A_{kn} and B_{kn} are functions of the pulsating-load dynamics and defined in Appendix A for a particular PES.

Next, (3) is translated to error coordinates using $e(t) = x(t) - x^*$, where $e(t)$ represents the error vector, while x^* represents the steady-state values of the PES states. In the error coordinate, (3) is modified as follows:

$$\dot{e}(t) = A_{kn}e(t) + \overline{B_{kn}} \tag{4}$$

where $\overline{B_{kn}} = -(B_{kn} + A_{kn}x^*)$. Discretizing (4), one obtains the following expression for j^{th} discrete sample:

$$e(j+1) = A_{knd}e(j) + B_{knd} \tag{5}$$

where

$$A_{knd} = \prod_{n=1}^{2h} exp^{A_{kn}T_{kw}\alpha_{k(2h-n+1)}} \tag{6a}$$

$$B_{knd} = [\left(\prod_{n\neq 1}^{2h} exp^{A_{k(2h-n+1)}T_{kw}\alpha_{k(i)}}\right)(exp^{A_{k1}T_{kw}\alpha_{k1}} - I)A_{k1}^{-1}\overline{B_{k1}} +$$

$$\left(\prod_{n\neq 1,2}^{2h} exp^{A_{k(2h-n+1)}T_{kw}\alpha_{k(i)}}\right)(exp^{A_{k2}T_{kw}\alpha_{k2}} - I)A_{k2}^{-1}\overline{B_{k2}} + \cdots \quad (exp^{A_{k2h}T_{kw}\alpha_{k2h}} - I)A_{k2h}^{-1}\overline{B_{k2h}} \tag{6b}$$

2.1.2. PES stability analysis

Reference [13] delineates the theory behind computation of the reachability analysis of a switching sequence of a PES. However, the theory does not explicitly consider the time horizon of the switching sequence. The reachability analysis that is laid forth, apart from creating a set of reachable switching sequences for the PES, helps in determining the range of the time allocation of the n^{th} switching state in the k^{th} switching sequence ($i.e., \alpha_{kn}$) and the length of the time horizon of the k^{th} switching sequence (i.e., T_{kw}) that aids in real-time execution of SBC. For the k^{th} switching sequence illustrated in Figure 3, with h switching states satisfying $0 \leq \alpha_{kn} \leq 1,\ \sum_{n=1}^{h} \alpha_{kn} = 1$, and $P_{kn} = P_{kn}^{T}$ being positive-definite matrices, a piecewise-discrete (multiple) Lyapunov function $V_k(j) = \sum_{n=1}^{h} e(j)^T P_{kn} e(j)$ is used to obtain the gradient of the multiple Lyapunov function:

$$\nabla V_k(e) = V_k(j+1) - V_k(j) = \sum_{n=1}^{h} \alpha_{kn} \left(e(j+1)^T P_{kn} e(j+1) - e(j)^T P_{kn} e(j)\right). \tag{7}$$

Using (6) and (7) it can be shown that: (the proper derivation is included in Appendix B)

$$\nabla V_k(e) = \sum_{n=1}^{h} \alpha_{kn} \begin{pmatrix} e(j) \\ 1 \end{pmatrix}^T \begin{bmatrix} (A_{knd}^T P_{kn} A_{knd} - P_{kn}) & A_{knd}^T P_{kn} B_{knd} \\ B_{knd}^T P_{kn} A_{knd} & B_{knd}^T P_{kn} B_{knd} \end{bmatrix} \begin{pmatrix} e(j) \\ 1 \end{pmatrix}. \tag{8}$$

According to Lyapunov-method of stability analysis for a discrete system, the PES state trajectories converge to (i.e., reach) an orbit if $\nabla V_k(e) < 0$ which results in the following linear matrix inequality (LMI):

$$\sum_{n=1}^{h} \alpha_{kn} \begin{bmatrix} (A_{knd}^T P_{kn} A_{knd} - P_{kn}) & A_{knd}^T P_{kn} B_{knd} \\ B_{knd}^T P_{kn} A_{knd} & B_{knd}^T P_{kn} B_{knd} \end{bmatrix} < 0 \tag{9}$$

Equation (9) is solved using the LMI tool in MATLAB. The flowchart shown in Figure 5 delineates how the LMIs are solved to get α_{kn} and T_{kw} that ensure PES reachability (i.e., orbital existence) given a range of pulsating load dynamics. To ensure periodic orbital stability the range of T_{kw} should always include $T_{kwmin} = T_s$, where T_s denotes the switching frequency of the PES. The bounds on Δi_{load}, f_{load}, and D_{load}, denoted by $\Delta i_{loadmax}$, $f_{loadmax}$, and $D_{loadmax}$, respectively, come directly from hardware limitations which will be discussed in Section 2.2.

2.1.3. SBC scheme

Figure 6 delineates the entire SBC scheme for a PES. The steps incurred in the SBC synthesis are delineated as follows:

1) Initially, depending on the PES topology and its switching behavior, a set of feasible switching sequences for

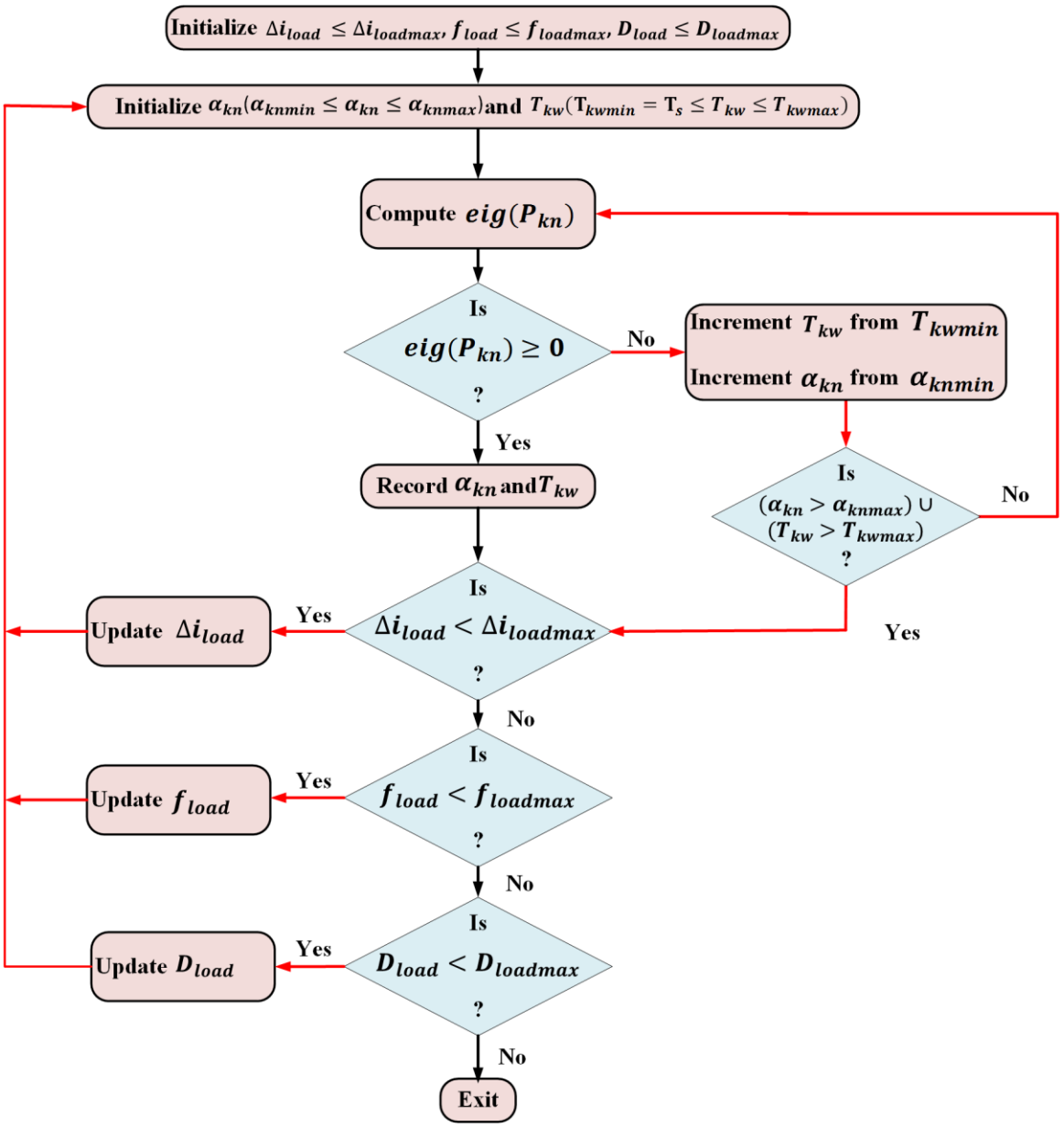


Figure 6. Flowchart of PES stability analysis methodology

the PES is determined following [9];

2) Subsequently, a comprehensive discontinuous dynamical model of the PES that incorporates the dynamics of the PES and the pulsating load is developed, as outlined in Section 2.1.1.

3) Subsequently, using the feasible switching sequences in "1", the model in "2", the PES parameters and the pulsating-load parameters (i.e., $\Delta i_{load}, f_{load}, D_{load}$), a subset of reachable switching sequences (that ensure the convergence of the PES dynamics) is determined offline using the stability-analysis methodology outlined in

Section 2.1.1. The goal of this analysis is to determine the bounds on α_{kn} and T_{kw} for the reachable switching sequences that are used for the online execution of SBC for optimally controlling the performance of the PES;

4) Subsequently, for fast real-time execution of the SBC, an online prediction model of the PES is synthesized that closely matches the dynamics of the model in "2". The prediction model is synthesized using a discrete map of the PES, which is obtained by combining the maps corresponding to each switching state. If the PES has h switching states in a reachable switching sequence, the prediction model can be synthesized as in (10), where $\hat{A}_{knd}$ and $\hat{B}_{knd}$ have been defined in (11a) and (11b).

$$\hat{x}(j+1) = \hat{A}_{knd}\hat{x}(j) + \hat{B}_{knd} \tag{10}$$

$$\hat{A}_{knd} = \prod_{n=1}^{2h} exp^{\hat{A}_{kn}T_{kw}\alpha_{k(2h-n+1)}} \tag{11a}$$

$$\begin{aligned}\hat{B}_{knd} = [&\left(\prod_{n\neq 1}^{2h} exp^{\hat{A}_{k(2h-n+1)}T_{kw}\alpha_{k(n)}}\right)\left(exp^{\hat{A}_{k1}T_{kw}\alpha_{k1}} - I\right)\hat{A}_{k1}^{-1}\hat{B}_{k1} + \\ &\left(\prod_{n\neq 1,2}^{2h} exp^{\hat{A}_{k(2h-n+1)}T_{kw}\alpha_{k(n)}}\right)\left(exp^{\hat{A}_{k2}T_{kw}\alpha_{k2}} - I\right)\hat{A}_{k2}^{-1}\hat{B}_{k2} + \ldots\ldots + \\ &\left(exp^{\hat{A}_{k2h}T_{kw}\alpha_{k2h}} - I\right)\hat{A}_{k2h}^{-1}\hat{B}_{k2h};\end{aligned} \tag{11b}$$

5) Next, a cost function, denoted by $C(\alpha_{kn}, T_{kw})$ is formulated and an online optimal control problem is solved online to perform online performance control of the PES. The optimization problem is used to determine α_{kn} and T_{kw} that minimizes the cost function:

$$C(\alpha_{kn}, T_{kw}) = (\hat{x}^* - \hat{x}(j+1))^T P(\hat{x}^* - \hat{x}(j+1)) \tag{12}$$

given the constraints on PES states and bounds on α_{kn} and T_{kw}. In (12), P is a positive-definite matrix that provides scaling of the terms in the cost function. As shown in Figure 7, the optimization problem yields reachable switching sequences with optimal values of α_{kn} and T_{kw} (i.e., $\alpha_{kn_{opt}}, T_{kw_{opt}}$) that are fed to the PES power stage;

6) Finally, and if full-state feedback is not possible to preclude the need for large number of sensors in a higher-order PES, a closed-loop state observer is synthesized as follows:

$$\bar{\hat{x}}(j+1) = \overline{\hat{A}_{knd}}\bar{\hat{x}}(j) + \overline{\hat{B}_{knd}} \tag{13}$$

$$\overline{\hat{A}_{knd}} = \prod_{n=1}^{2h} exp^{\hat{A}_{kn}T_{kw}(\alpha_{k(2h-n+1)} + \Delta(\alpha_{k(2h-n+1)}))} \tag{14a}$$

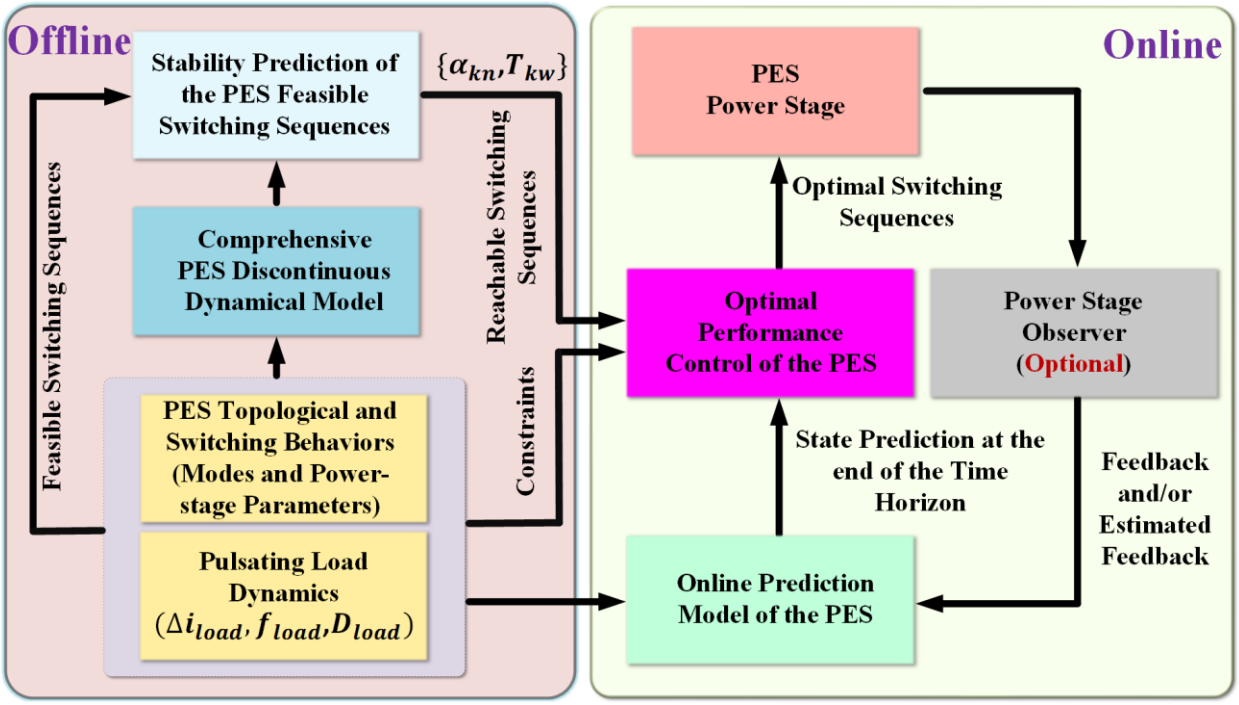


Figure 7. An illustration of the SBC scheme for the PES driving a pulsating load.

$$\overline{\hat{B}_{knd}} = [\left(\prod_{n\neq 1}^{2h} exp^{\hat{A}_{k(2h-n+1)}T_{kw}(\alpha_{k(n)}+\Delta\alpha_{k(n)})}\right)\left(exp^{\hat{A}_{k1}T_{kw}(\alpha_{k1}+\Delta\alpha_{k1})} - I\right)\hat{A}_{k1}^{-1}\hat{B}_{k1} + \left(\prod_{n\neq 1,2}^{2h} exp^{\hat{A}_{k(2h-n+1)}T_{kw}(\alpha_{k(n)}+\Delta\alpha_{k(n)})}\right)\left(exp^{\hat{A}_{k2}T_{kw}(\alpha_{k2}+\Delta\alpha_{k2})} - I\right)\hat{A}_{k2}^{-1}\hat{B}_{k2} + \cdots + \left(exp^{\hat{A}_{k2h}T_{kw}(\alpha_{k2h}+\Delta\alpha_{k2h})} - I\right)\hat{A}_{k2h}^{-1}\hat{B}_{k2h} \quad (14b)$$

where the correction terms, denoted by Δ, have been discussed for a PES in Section 2.1.3.3. Figure 8 shows a flowchart as used for the implementation of SBC online. To be precise, the algorithm minimizes, for a given set of reachable switching sequences, the cost function $C(\alpha_{kn}, T_{kw})$ with respect to α_{kn} and T_{kw}. For $T_{kw} > T_{kwmin}$, both α_{kn} and T_{kw} are optimized which ensures convergence of the PES dynamics from an initial condition to an orbit [9] using reachable switching sequence(s). Whenever $T_{kw} \leq T_{kwmin}$, we consider $T_{kw} = T_{kwmin} = T_s$ and only α_{kn} has to be optimized, which ensures convergence to the periodic orbit [9] or steady-state.

2.1.3.1. Case illustration: synthesizing SBC for a Ćuk dc/dc PES (Ćuk-PES)

To realize the SBC scheme online, a GaN-FET-based 100-kHz Ćuk-PES is fabricated and tested. The online SBC

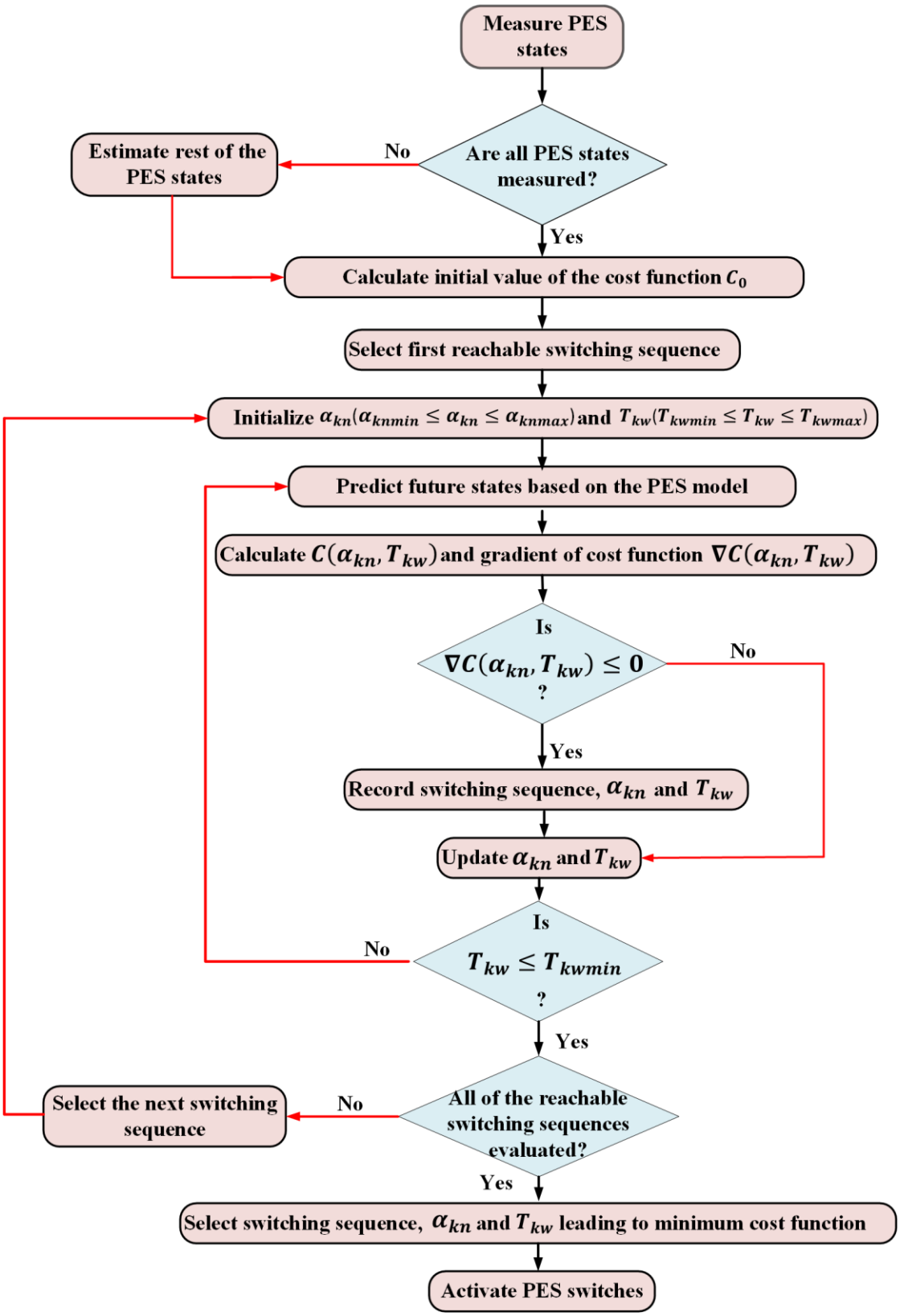


Figure 8. A flowchart for online implementation of the SBC

scheme for the Ćuk-PES as shown in Figure 9, which constitutes of an online prediction model synthesis, followed by cost function formulation and lastly, the observer design, is discussed below.

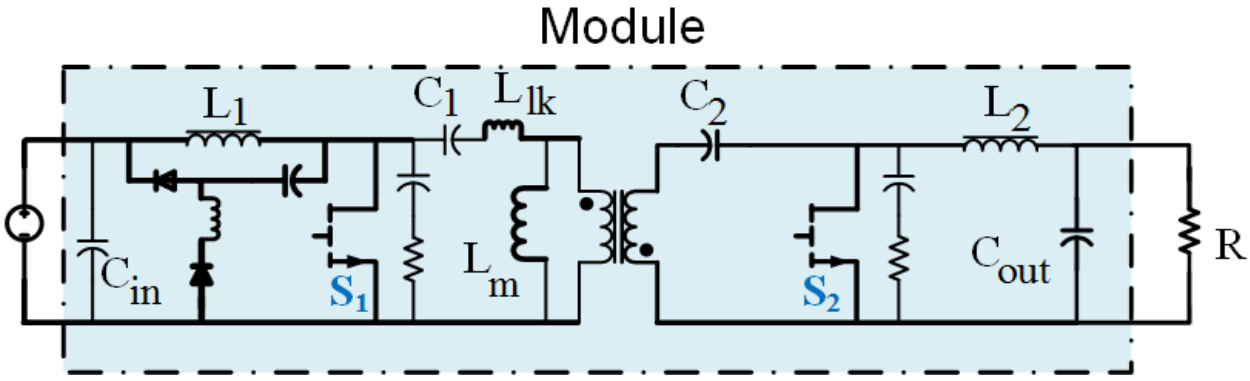


Figure 9. Schematic of the Ćuk PES with GaN-FET-based switches S_1 and S_2.

2.1.3.1.1. Prediction model

The higher-order isolated Ćuk-PES operates in the continuous-conduction-mode (CCM) of operation. The modes of operation have been shown in Appendix C to ease comprehension. For the fundamental switching sequence of the Ćuk-PES, if A_{k1} and B_{k1} and A_{k2} and B_{k2} are matrices in successive switching states having time allocations of α_{k1} and α_{k2}, respectively, and T_{kw} be the time horizon of the fundamental switching sequence, then by stacking together the following equations:

$$\hat{x}(j') = e^{A_{k1}\alpha_{k1}T_{kw}}\hat{x}(j) + (e^{A_{k1}\alpha_{k1}T_{kw}} - I)A_{k1}^{-1}B_{k1} \tag{15}$$

$$\hat{x}(j+1) = e^{A_{k2}\alpha_{k2}T_{kw}}\hat{x}(j') + (e^{A_{k2}\alpha_{k2}T_{kw}} - I)A_{k2}^{-1}B_{k2} \tag{16}$$

one obtains the following nonlinear map:

$$\hat{x}(j+1) = e^{A_{k1}\alpha_{k1}T_{kw}+A_{k2}\alpha_{k2}T_{kw}}\hat{x}(j) + e^{A_{k2}(\alpha_{k2})T_{kw}}\left((e^{A_{k1}\alpha_{k1}T_{kw}} - I)\,{A_{k1}}^{-1}B_{k1}\right) + (e^{A_{k2}\alpha_{k2}T_{kw}} - I){A_{k2}}^{-1}B_{k2} \tag{17}$$

where $\hat{x}(j')$ and $\hat{x}(j+1)$ denote the system states after time evolution $\alpha_{k1}T_{kw}$ and $\alpha_{k1}T_{kw} + \alpha_{k2}T_{kw}$, respectively, from initial value $\hat{x}(j)$. The system dynamics satisfy $\alpha_{k1} + \alpha_{k2} = 1$. The exponential terms in (17) is simplified using first-order Euler's approximation to form the following nonlinear prediction model:

$$\hat{x}(j+1) = (I + A_{k1}\alpha_{k1}T_{kw} + A_{k2}\alpha_{k2}T_{kw})\hat{x}(j) + (A_{k2}\alpha_{k2}T_{kw} + I)(\alpha_{k1}T_{kw}\,B_{k1}) + \alpha_{k2}T_{kw}\,B_{k2} \tag{18}$$

Given any set of initial conditions from the sensors/observers, this approximation is found to be viable for high sampling rates, as depicted in the first 100 switching cycles of the system in Figure 10 , sampled at 100 *k*Hz. The first

50 switching cycles encompass system start-up and hence the approximation is viable for both start-up and steady-state. The schematic of the Ćuk-PES, as shown in Figure 9 , includes more passive elements including the magnetizing and leakage inductance of the transformer, which have not been incorporated in the prediction model for reasons described in Appendix D.

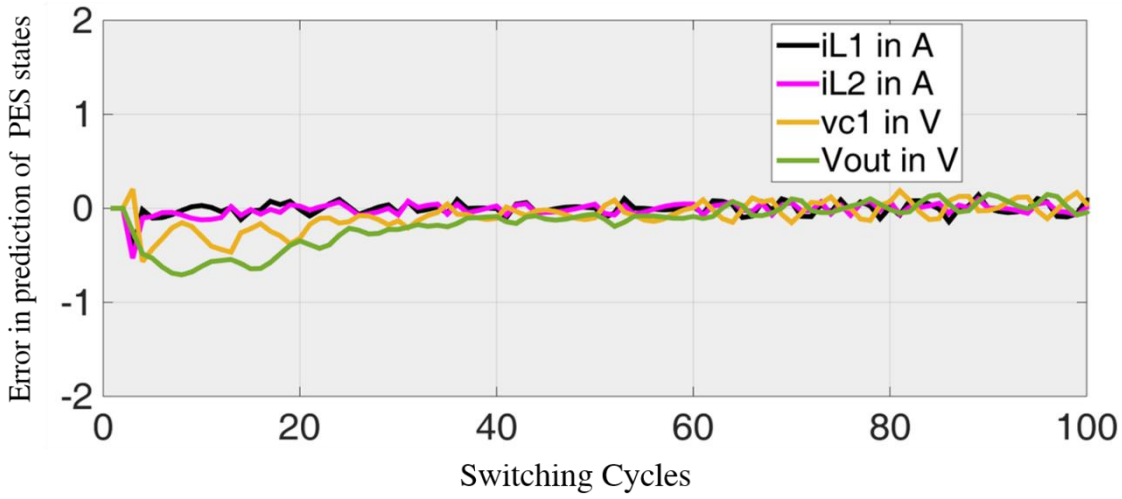


Figure 10. Error in the prediction of the PES states based on the nonlinear Ćuk-PES model (18) and the approximated nonlinear model (19). The legends from top to bottom represent the input and output inductor currents, blocking capacitor and output voltage. The y-axis denotes both voltage and current (a value of 0.25 corresponds to both -0.25 V and 0.25 A).

2.1.3.1.2. Cost function

The generalized framework for the discrete cost function of the non-minimum phase Ćuk-PES as a current regulation problem is outlined as follows:

$$C(\alpha_{k1}, T_{kw}) = \delta_1 \left({}^{1}/_{IL_{ref}}\right)^2 * \left(IL_{ref} - iL_1(j)\right)^2 + \gamma_1 * \left(\alpha_{k1}(j) - \alpha_{k1}(j-1)\right)^2 + \gamma_2 * \left(T_{kw}(j) - T_{kw}(j-1)\right)^2 \quad (19a)$$

$$IL_{ref} = G_p \left(V_{ref} - V_{out}(j)\right) + G_I \sum_j \left(V_{ref} - V_{out}(j)\right) T_{kw} + I_{ff} \quad (19b)$$

where IL_{ref} and V_{ref} are the references for the input inductor current $iL_1(j)$, and the output voltage $V_{out}(j)$, both defined at j^{th} discrete sample. The last two terms in $C(\alpha_{k1}, T_{kw})$ help in mitigation of control input chattering between two successive discrete samples. The terms G_p and G_I, along with the feedforward term I_{ff}, help in mitigation of steady-state error quickly. The cost function is designed based on the principles mentioned in [8], [25], [51], [52]. The terms δ_1, γ_1, and γ_2 effectively maneuver the control bandwidth and transient response, and their tuning process is

discussed in [53], [32].

2.1.3.1.3. Observer design

SBC when implemented on a higher-order PES may necessitate a state observer to reduce the cost associated with full-state feedback. A state observer for the Ćuk-PES is created using (17). Notwithstanding, the actual system dynamics may not precisely match the prediction of model (17) due to the parasitic, transformer nonlinearity, and switching dead time. Hence, a correction mechanism is needed to ensure that, the error between the observed and the actual system dynamics converges to zero. The equation of the observer is as follows:

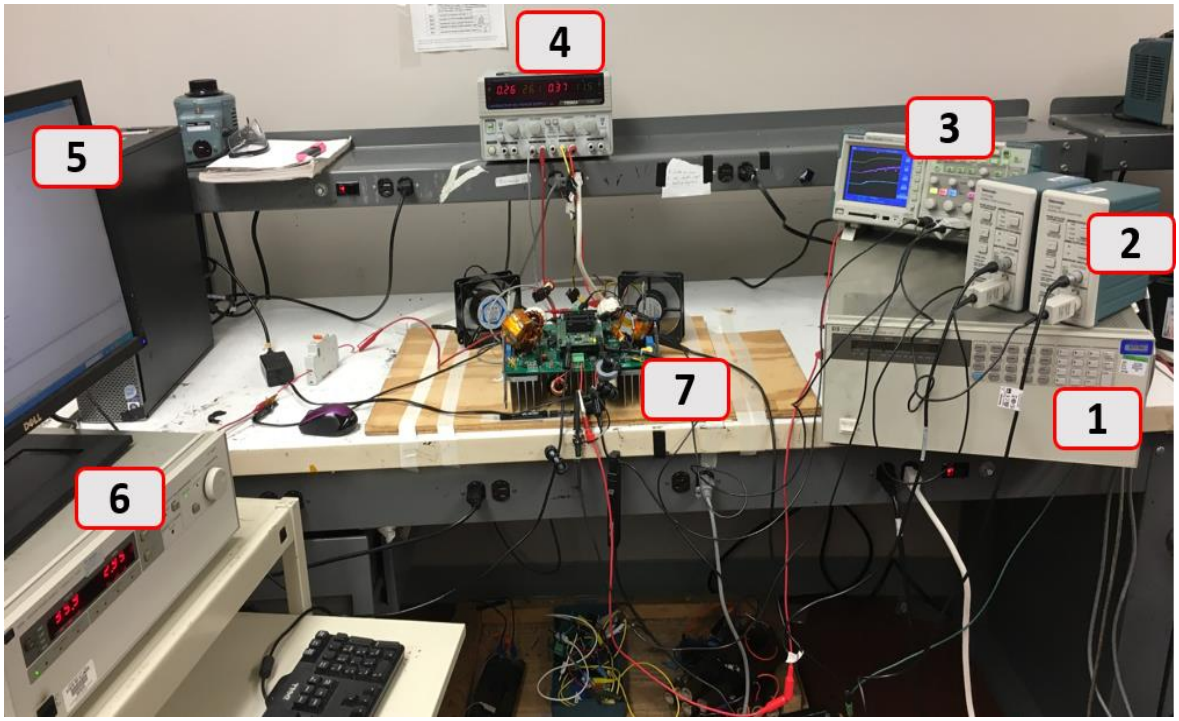
$$\bar{\hat{x}}(j+1) = e^{A_{k1}(\alpha_{k1}+\Delta\alpha_{k1})T_{kw}+A_{k2}(1-(\alpha_{k1}+\Delta\alpha_{k1}))T_{kw}}\bar{\hat{x}}(j)+ +e^{A_{k2}(1-(\alpha_{k1}+\Delta\alpha_{k1}))T_w}\Big(\big(e^{A_{k1}(\alpha_{k1}+\Delta\alpha_{k1})T_{kw}} - I\big)\,{A_{k1}}^{-1}B_{k1}\Big) + (e^{A_{k2}(1-(\alpha_{k1}+\Delta\alpha_{k1}))T_{kw}} - I){A_{k2}}^{-1}B_{k2} \tag{20}$$

$\bar{\hat{x}}(j+1)$ denote the observed system states after time evolution $T_{kw}+\Delta\alpha_{k1}T_{kw}$, where $\Delta\alpha_{k1} = K_p(V_{out}(j) - \overline{\hat{x_4}}(j))+K_I\sum_j\big(V_{out}(j) - \overline{\hat{x_4}}(j)\big)T_{kw}$, $V_{out}(j)$ is the sampled output voltage of the hardware Ćuk-PES at the j^{th} discrete instant, and $\overline{x_4}(j)$ is the output voltage of the observer at the same time instant. The observer takes $V_{out}(j)$ and $V_{in}(j)$ as the inputs and K_p and K_I are proportional and integral gains. Parameters α_{k1} and T_{kw} are varied across the operating range and the values of the closed-loop gains are computed taking into consideration the large-signal stability of the observer.

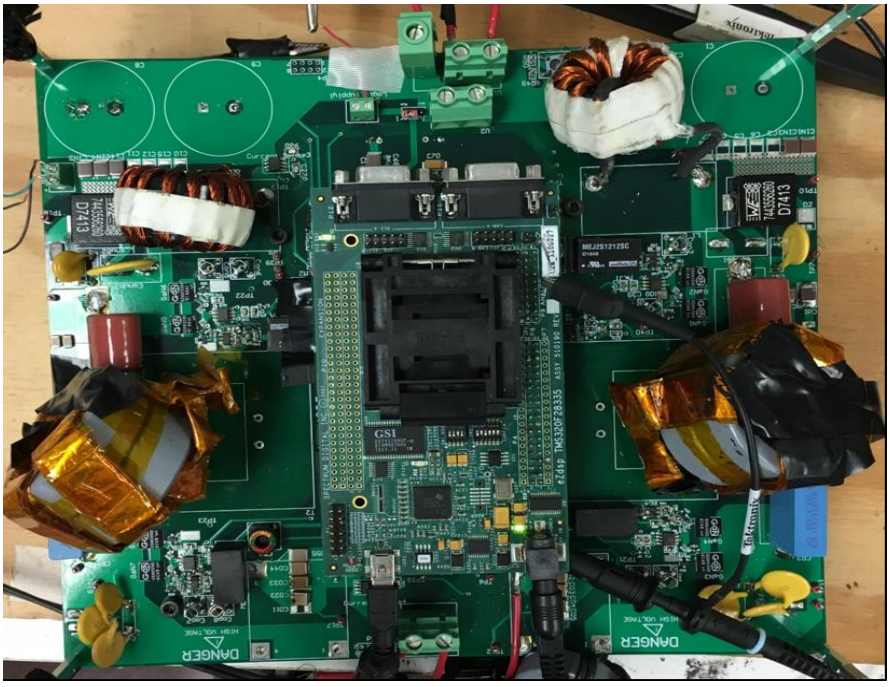
2.2. Results of SBC for pulsating load

The section is organized as follows. The hardware set-up, along with the higher-order Ćuk-PES experimental prototype, as shown in Figure 11a and Figure 11b, is discussed first. Next, the analytical-stability results for the system and how it helped in SBC execution online are delineated with experimental results.

The SBC algorithm is implemented on a TMS320F28335 digital signal processor (DSP) using code composer studio version 3.3, and the switching sequence, with the allocated switching states (α_{k1} and α_{k2}) and time horizon (T_{kw}), is used to drive the GS66508B GaN-FET-based Ćuk-PES operating at switching frequency ($f_s = 1/T_s$) of 100 *k*Hz. The power-stage parameters used are provided in Table I. The detailed hardware design is discussed in [33] and the advanced protection features in the hardware prototype that has not been covered in [33] is included in Appendix E.



(a)



(b)

Figure 11. (a) The entire experimental platform is shown. The components are (1) dc electronic load (2) current sensor (3) oscilloscope (4) the control supply (5) the PC running code composer studio version 3.3 (6) the input dc power supply (7) The experimental hardware PES. (b) The PCB realization (top view) of the GaN-FET-based Ćuk-PES.

The dc electronic load 6050A from HP is used to emulate the pulsating load, while hall current sensor TCP312A (30 A) with TCPA300 amplifiers (both two) from Tektronix is used for current measurements. Agilent 6030A dc power supply is used as regulated input power supply for the PES, while a bench power supply from Tenma is used as control supply. Isolated 4-channel oscilloscope TPS 2024B from Tektronix is used to capture experimental results for the PES.

Table 1. The Power-stage-Parameters for the Ćuk-PES.

Input voltage range (V_{in})	Output voltage range (V_{out})	Input inductance (L_1)	Output inductance (L_2)	Input capacitance (C_{in})	Output capacitance (C_{out})	Input blocking capacitance (C_1)	Output blocking capacitance (C_2)	Switching frequency ($1/T_s$)	Transformer turns ratio (N)
0-50 V	0-170 V	50 μH	100 μH	4.4 μF	5 μF	6. 8 μF	1.5 μF	100 kHz	2

Load-transition level (Δi_{load}) of up to 5 A and load duty cycle (D_{load}) of up to 90% is considered as they can be realized in the Ćuk-PES hardware prototype. The Bode plot of the open-loop transfer function from α_{k1} to V_{out} is shown in Figure 12 ; it shows, resonant poles and zeros of the higher-order Ćuk-PES located below 5 kHz. As such, to avoid the excitation of system resonance, an upper limit of f_{load} is considered to be well below 5 kHz. Since f_{load} of 2 kHz can be safely realized in hardware prototype, the reachability analysis derived in Section 2.1.2 is restricted to $\Delta i_{load} \leq 5$ A, $f_{load} \leq 2$ kHz, and $D_{load} \leq 90\%$.

The importance of the stability-criterion in the form of LMI is two-fold. Considering the fundamental switching sequence of the Ćuk-PES (with $\alpha_{k1}$and α_{k2} representing the time allocation of switching states in the sequence, T_{kw} as the time horizon of the switching sequence and given the constraint $\alpha_{k1} + \alpha_{k2} = 1$), the analysis aids in the following:

1) investigation of the impacts of $\Delta i_{load} \leq 5$ A, $f_{load} \leq 2$ kHz, and $D_{load} \leq 90\%$ on the reachability of the system dynamics;
2) determination of the allowable ranges of α_{k1} and T_{kw} that stabilize the Ćuk-PES across $\Delta i_{load} \leq 5$ A, $f_{load} \leq 2$ kHz, and $D_{load} \leq 90\%$.

All analytical results are for V_{in} = 30 V and V_{out} = 50 V. Using the afore-mentioned values of pulsating-load dynamics in the LMIs defined by (9), reachable ranges of α_{k1} and T_{kw} are computed for $\Delta i_{load} \leq 5$ A, $f_{load} \leq 2$ kHz, and

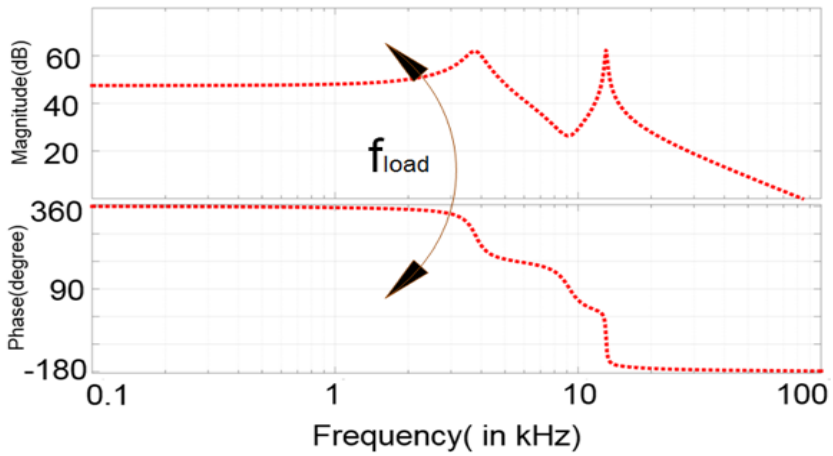


Figure 12. Illustration of open-loop Bode plot of $\hat{V}_{out}/\hat{\alpha}_{k1}$ of the Ćuk-PES where f_{load} denotes the pulsating load frequency, where $\hat{V}_{out}$ and $\hat{\alpha}_{k1}$ are the perturbed small-signal variables.

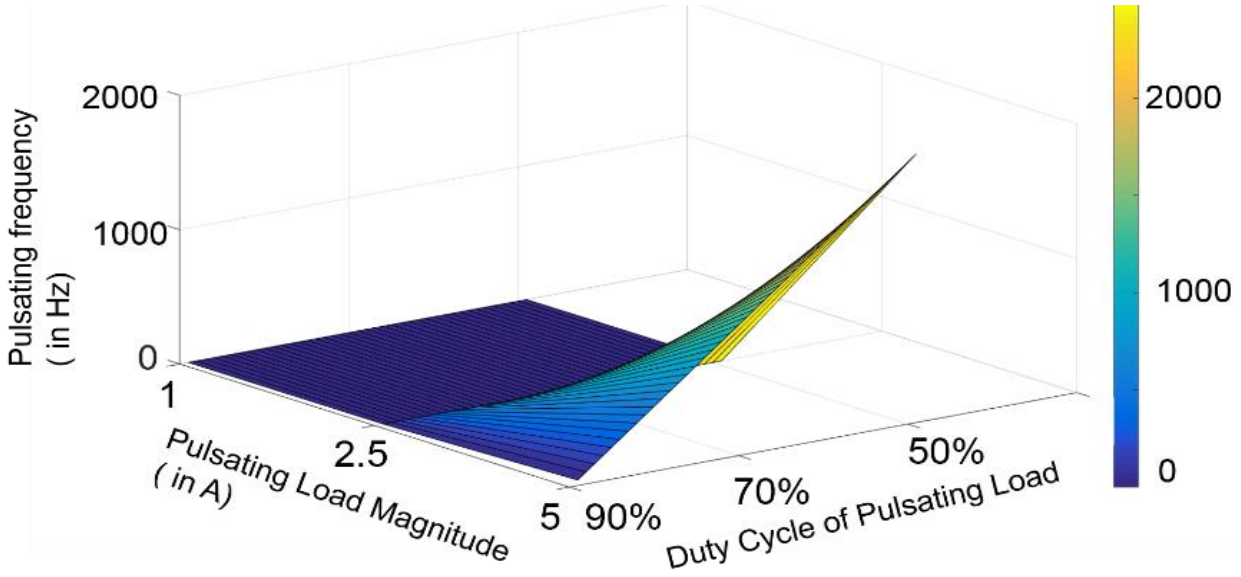


Figure 13. The region of reachable operation of the PES.

$D_{load} \leq 90\%$ that are used for real-time execution of SBC.

The impacts of load variations on the reaching conditions of the Ćuk-PES are investigated by solving (9). The region on the contour in Figure 13 represents operating conditions that ensure reachability of the system dynamics. The region of reachability denotes that there exists α_{k1} and T_{kw} with variation of D_{load}, Δi_{load} and f_{load} for which system dynamics can be stabilized. Figure 12 shows that for the Ćuk-PES, while the region of reachable operation remain unchanged with pulsating load magnitudes lower than Δi_{load} = 2.5 A for lower pulsating frequencies, for $\Delta i_{load} > 2.5$ A at higher pulsating frequencies, the region of reachable operation keeps on diminishing. As such, progressively

reduced pulsating duty cycles are attainable and further, beyond $\Delta i_{load} =$ 4 A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$, there exists no α_{k1} and T_{kw} that can make the system dynamics reachable.

The afore-mentioned theoretical analysis precludes control law formulation. However, to investigate whether the experimental results match the theoretical predictions, an SBC law, due to its fast-transient response and seamless control formulation is used and operation within and outside the reachability contour are investigated.

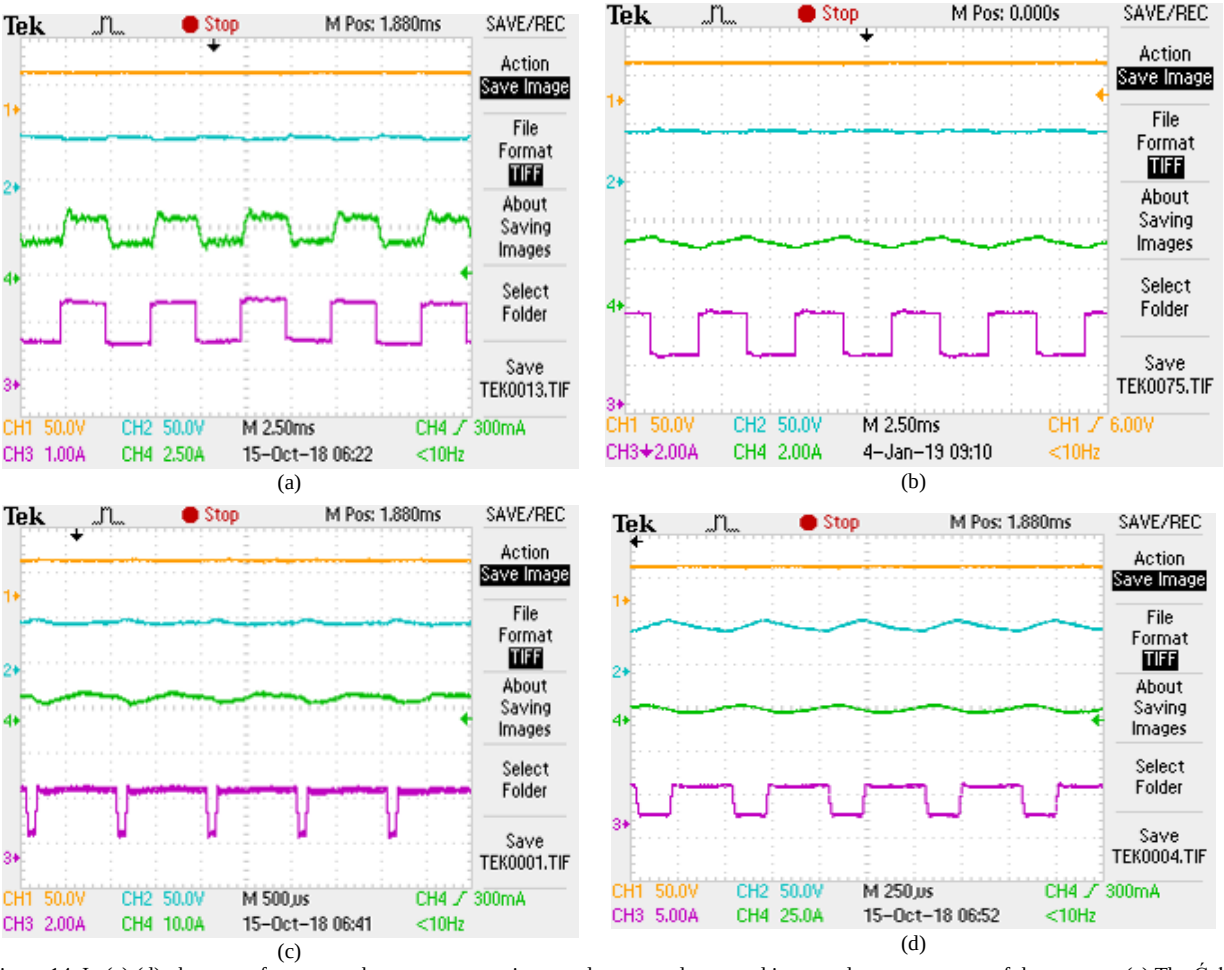


Figure 14. In (a)-(d), the traces from top to bottom represent input and output voltages and input and output currents of the system. (a) The Ćuk-PES response for $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$. (c) The PES response for $\Delta i_{load} =$ 2.5 A, $f_{load} = 1$ *k*Hz, and $D_{load} = 90\%$, respectively. (d) The Ćuk-PES response for $\Delta i_{load} =$ 4 A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$. (b) By increasing the input capacitance to 1 mF, the pulsation in the input ripple current in (a) (i.e., for $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$) is mitigated.

For validation of operation within the reachable contour, Figure 14a shows the Ćuk-PES response for the operating condition $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$. The system exhibits stable response as the operating point defined by f_{load}, D_{load}, and Δi_{load} lie on the reachable region in Figure 13. Figure 14b shows the Ćuk-PES response

at $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ kHz, and $D_{load} = 50\%$ when an electrolytic capacitor of 1mF is placed at the input. At increased input capacitance, the pulsating input current (shown by the green trace) gets smoothed off, which leads to uncorrupted input dc supplies. Figure 14c shows the system response for the more stringent operating condition $\Delta i_{load} =$ 2.5 A, $f_{load} = 1$ kHz, and $D_{load} = 90\%$, which lies on the boundary of the reachable region in Figure 12 as well. Figure 14d shows system response for the operating condition $\Delta i_{load} =$ 4 A, $f_{load} = 2$ kHz, and $D_{load} = 65\%$ which also lies on the boundary of the reachable region.

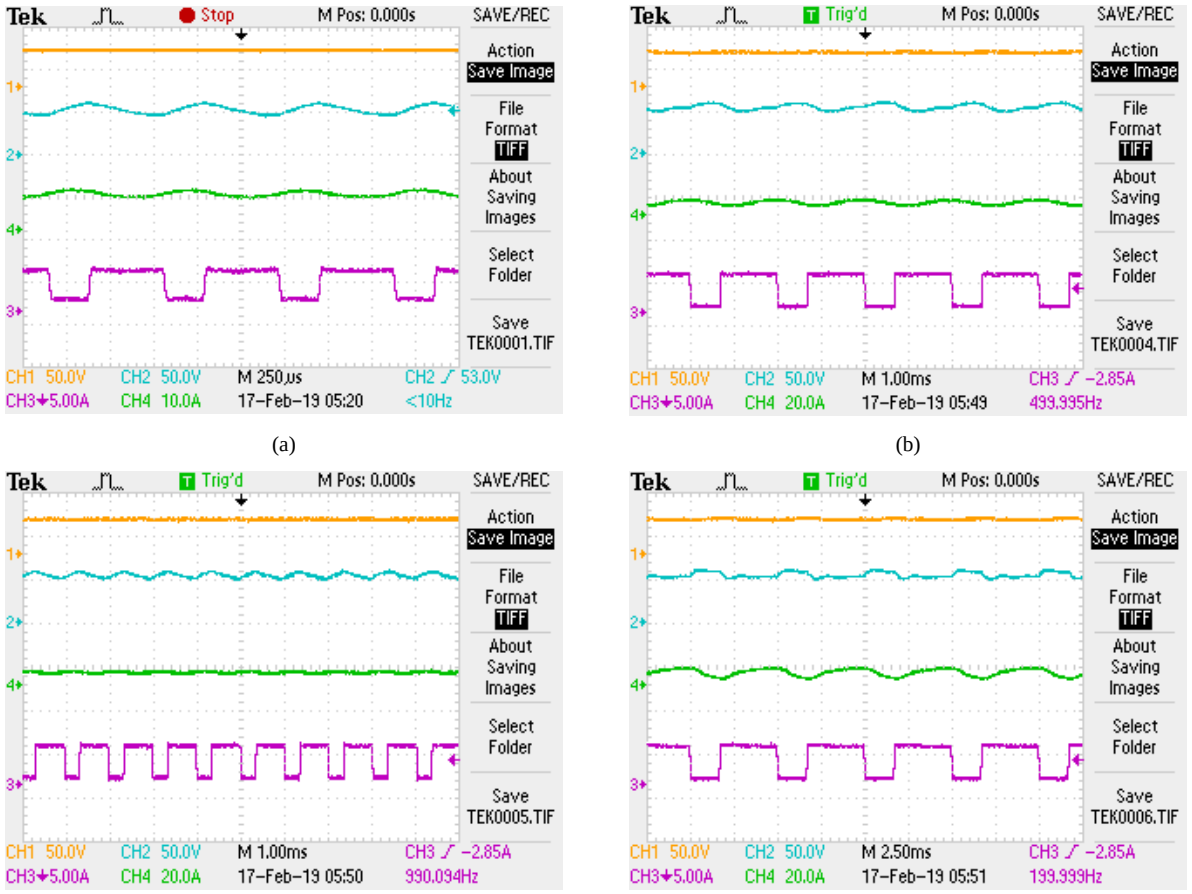
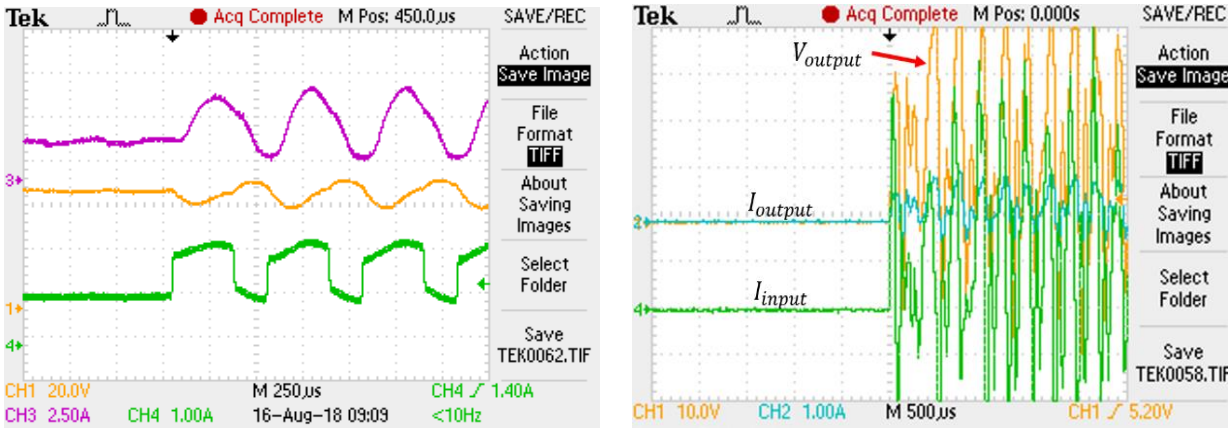


Figure 15. In (a)-(d), the traces from top to bottom represent input and output voltages and input and output currents of the system. The Ćuk-PES response for $\Delta i_{load} = 4$ A, $D_{load} = 65\%$ and (a) $f_{load} = 1.5$ kHz (b) $f_{load} = 1$ kHz, (c) $f_{load} = 0.5$ kHz (d) $f_{load} = 0.2$ kHz. The pulsating load frequency is changed from the worst-case load condition.

Finally, for further validation of operation within the reachable contour, a case illustration is demonstrated where the load-step (Δi_{load}) and duty cycle (D_{load}) have been kept at the value imitating the worst-case scenario, and only the pulsating frequency is gradually changed, and whether the proposed SBC could achieve satisfactory performance

is verified in Figure 15. SBC provided satisfactory performance given the limited computational capabilities of the low-end microcontroller used for implementation.

For validation of operation outside the reachable contour, Figure 16 shows the response of the Ćuk-PES for operating points that do not lie on the reachable contour in Figure 13. Operating the system beyond the reachable region at $\Delta i_{load} = 5$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$ yields an unstable system resulting in oscillatory currents and voltages. The oscillations eventually lead to the distorted output voltage and currents in the unstable system. The onset of the oscillations is highlighted in Figure 16a, where the Ćuk-PES is regulating its output voltage to 50 V before operation beyond the reachable regime. The analysis in Figure 13 also shows that for $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and D_{load} = 50%, operating the system for $T_{kw} > 20$ μs results in instability. In Figure 16b, the Ćuk-PES is operated by setting $T_{kw} = 26$ μs (> 20 μs) which, as predicted, yields an unstable system.



(a) (b)

Figure 16. (a) The Ćuk-PES response for $\Delta i_{load} = 5$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$ at the onset of instability. In (a) the traces from top to bottom represent input current, output voltage and output current. (b) The unstable operation of the Ćuk-PES is captured for operation at $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$ at T_{kw}=26 μs (> 20 μs). The traces from top to bottom represent output voltage, output current and input current.

Now that the region of reachable operation, as shown in Figure 13, is experimentally validated, we explore the following: if the Ćuk-PES has to operate at a certain Δi_{load},f_{load}, and D_{load}, the ranges of α_{k1} and T_{kw} that would ensure the PES reachability at every Δi_{load},f_{load}, and D_{load} can be determined. Figure 17 shows the maximum allowable α_{k1} for the Ćuk-PES with respect to T_{kw}. Increasing the T_{kw} limits the maximum duty cycle available to ensure reachability. Figure 17 shows the limits on α_{k1} and T_{kw} for extreme cases of the pulsating-load dynamics. Using this analysis, a bound on α_{k1} and T_{kw} is obtained for the PES operation. Operation beyond the limit of α_{k1} and

T_{kw} obtained may lead to unstable PES behavior.

The bounds on α_{k1} (which also set the bounds for α_{k2}) and T_{kw} help in saving computation time for online execution in SBC, which enables implementation using low-cost hardware realizable without the need for sophisticated algorithms in the high-frequency Ćuk-PES. Figure 17 shows that for loads with relatively slower scales of $\Delta i_{load} \leq$ 1 A, $f_{load} \leq 0.2$ *k*Hz, and $D_{load} \leq 50\%$, the maximum α_{k1} is capped at 0.61 and maximum T_{kw} is capped at 18 μs. Hence, any optimization algorithm to solve the online optimal SBC must look for values of $0 < \alpha_{k1} \leq 0.61$ and $T_{kw} \leq 18$ μs. The minimum value of T_{kw} is dictated by the Ćuk-PES switching time T_s which is 10 μs leading to $10 \leq T_{kw} \leq 18$ μs. For a simple brute-force search using a resolution of α_{k1} to be 0.02, and T_{kw} to be 1 μs, Figure 18a shows the saving in computation time for real-time execution of SBC.

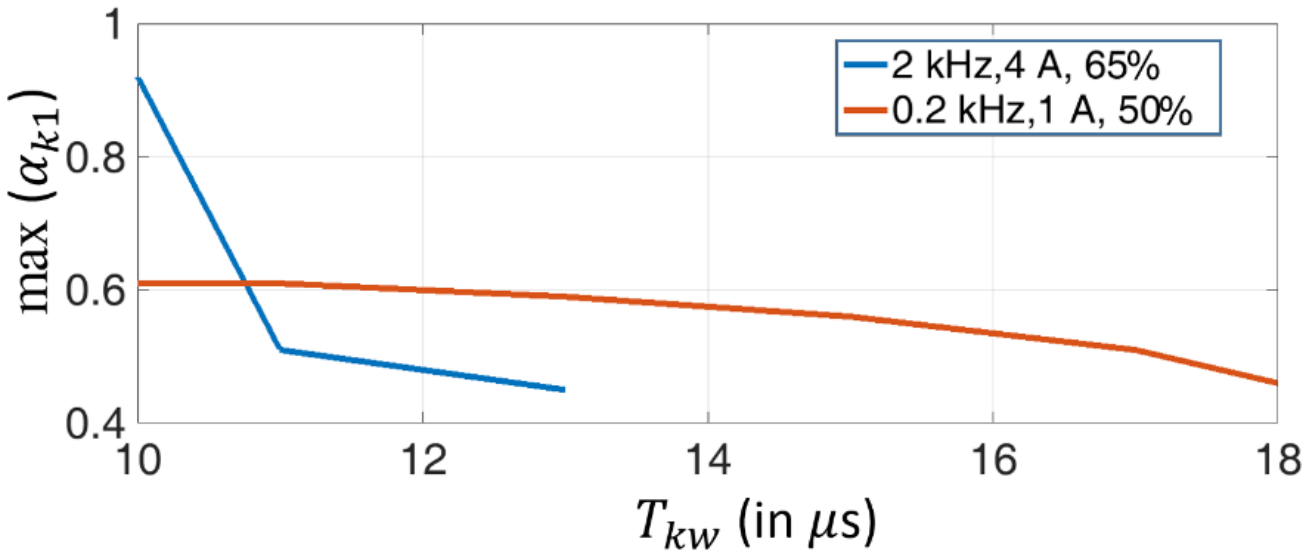
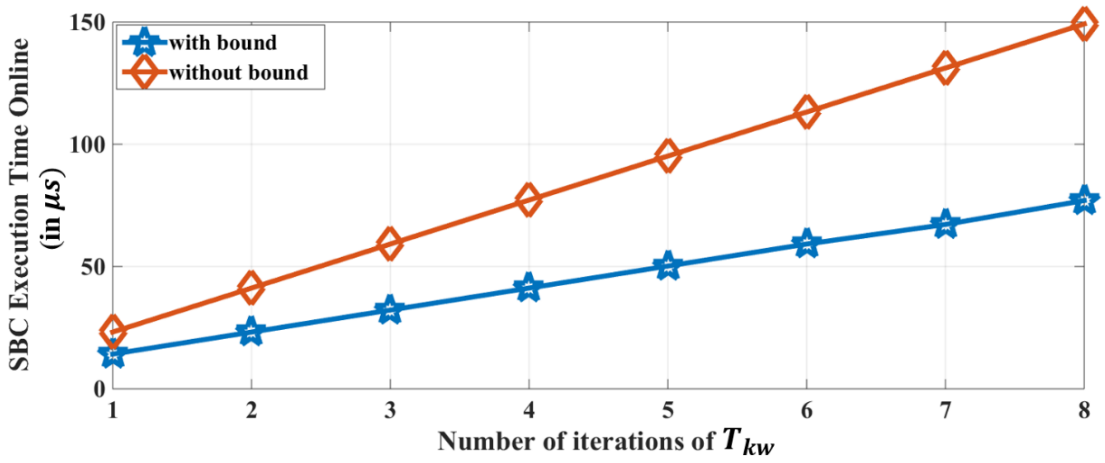
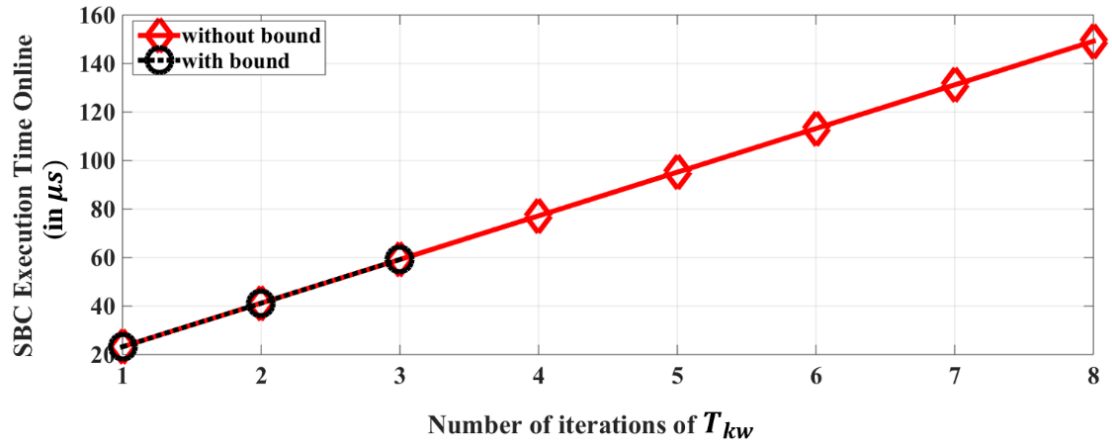


Figure 17. Variations of α_{k1} with T_{kw} for $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$ and $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$.

For the Ćuk-PES operating at $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$, the maximum allowable time horizon is $T_{kw} \cong 13$ μs beyond which there exists no α_{k1} for which the system can reach an output voltage of 50 V for an input voltage of 30 V. Hence, for $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$, the online optimal SBC has to look for values of $0 < \alpha_{k1} \leq 0.9$ and $10 \leq T_{kw} \leq 13$ μs, as shown in Figure 17. Figure 17, hence, shows that the blue trace which corresponds to $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$ stops at 13 μs which proves that no α_{k1} that can provide reachability for $T_{kw} \geq 13$ μs. Although the upper limit of α_{k1} has increased for this case, the range of T_{kw} has decreased, which saves online execution time for SBC. Hence, looking for admissible values of α_{k1} and



(a)



(b)

Figure 18. (a) Experimentally obtained online SBC execution time, with and without offline reachability analysis for number of iterations of T_{kw} for loads below $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$. (b) The experimental comparative study of the online SBC execution time for $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$ as a function of number of iteration of T_{kw}.

T_{kw} yields a computation time of 59.2 μs, as shown in Figure 18b. If the bound on T_{kw} is not obtained, then the search time to execute the online SBC increases considerably.

Next, it is investigated whether online execution of the SBC by limiting the ranges of T_{kw} and α_{k1}, ascertained using the reachability analysis, deteriorates the performance of the Ćuk-PES. Figure 19a and Figure 19b show the Ćuk-PES performance variation at $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$, with and without bounds on α_{k1} and T_{kw}, respectively. Figure 19c and Figure 19d show the same PES performance variation at $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$, with and without bounds on α_{k1} and T_{kw}, respectively. The start-up response shows no

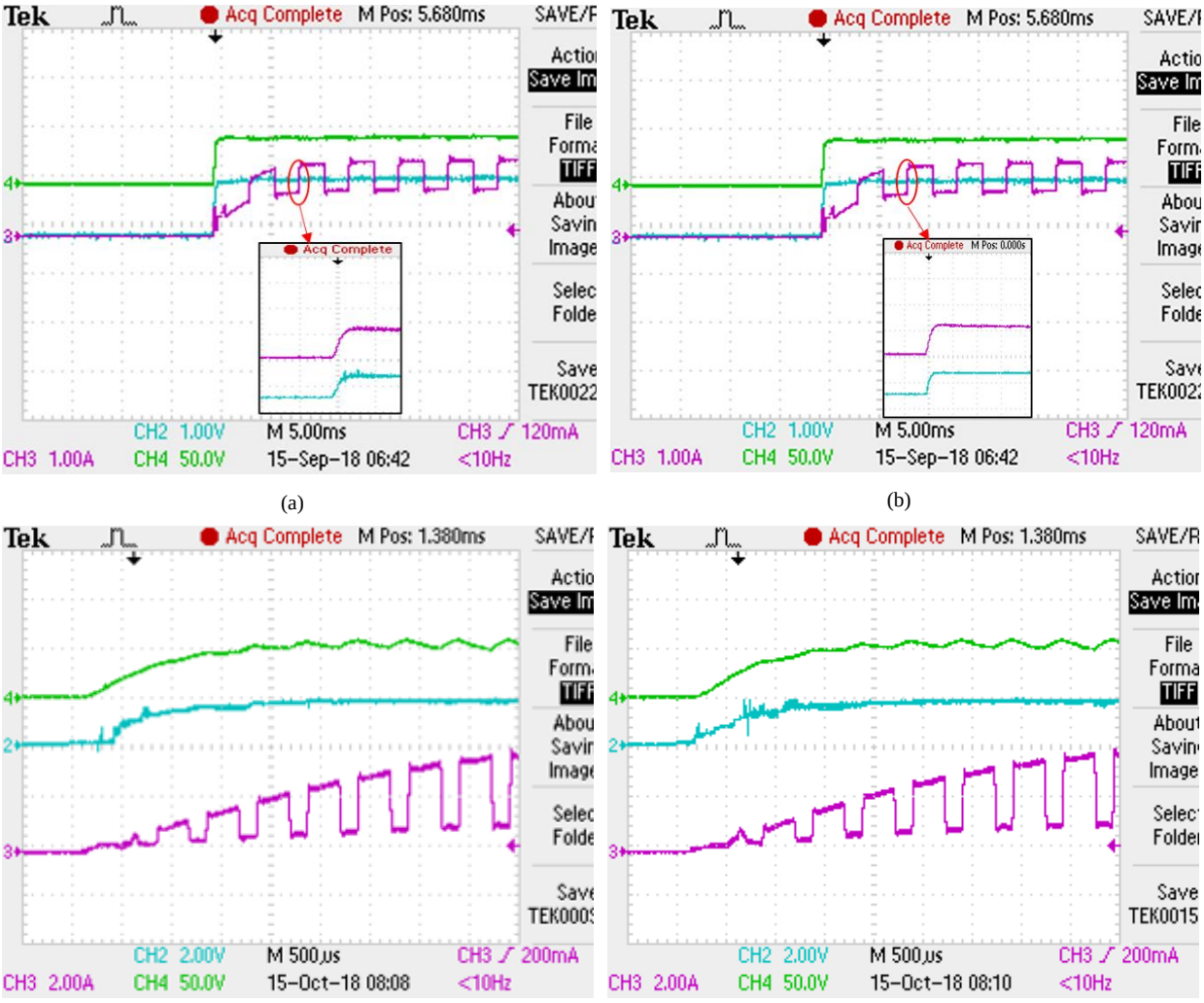
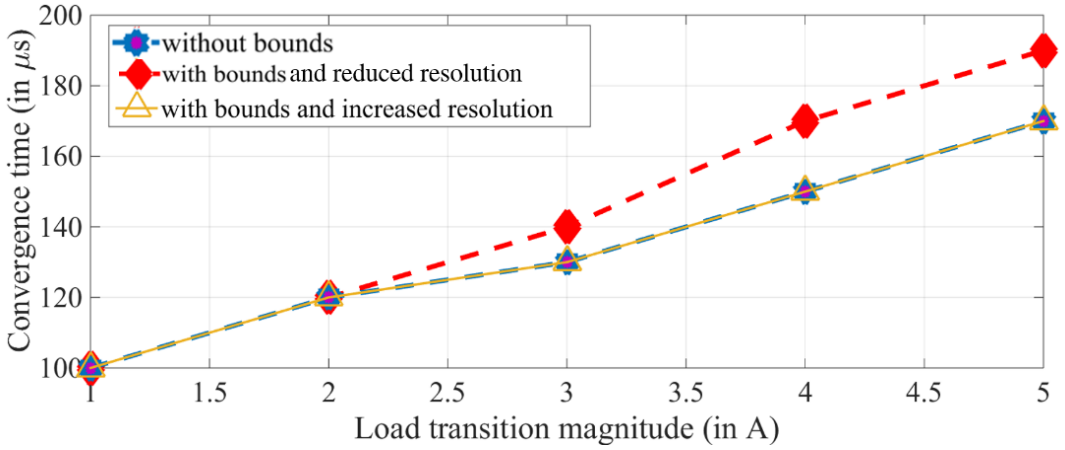


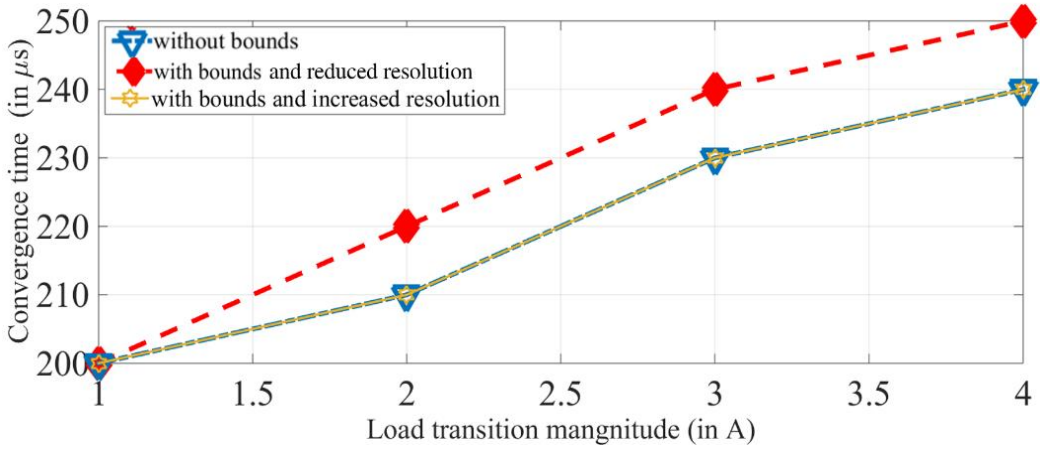
Figure 19. (a) and (b) The start-up response of the PES for $\Delta i_{load} = 1$ A, $f_{load} = 0.2$ *k*Hz, and $D_{load} = 50\%$ without and with bounds on α_{k1} and T_{kw}, respectively. The horizontal scale is 500 μs/div in the subplots in (a) and (b). (c) and (d) The Ćuk-PES start-up response without and with bounds on α_{k1} and T_{kw}, respectively, for $\Delta i_{load} = 4$ A, $f_{load} = 2$ *k*Hz, and $D_{load} = 65\%$. The channels 2, 3 and 4 represent α_{k1}, output current, and output voltage respectively in (a)-(d).

significant deterioration of the Ćuk-PES performance in the two cases. Thus, the savings in the computation time of SBC is realized without tangible performance degradation at the prediction extremities.

Figure 20a and Figure 20b further validate the fact that computational time savings do not come at much reduced PES performance by plotting the convergence time of the output voltage to its steady-state value after the load-transition event has occurred for $f_{load} = 0.2$ *k*Hz and $D_{load} = 50\%$ and $f_{load} = 2$ *k*Hz and $D_{load} = 65\%$. At the



(a)



(b)

Figure 20. (a) A comparative study of the experimental convergence time of the output voltage after load transition has occurred at f_{load} = 0.2 *k*Hz and D_{load} = 50% for gradually increasing load transition levels. (b) A comparative study of the experimental convergence time of the output voltage.

extreme load conditions possible for the Ćuk PES of f_{load} = 2 *k*Hz, D_{load} = 65% and Δi_{load} = 4 A, there is delay of as low as 20 μs considering the high switching frequency of the PES. It is a trade-off for implementing such computationally intensive control at low-end processors at high switching frequency. Due to limited computational capability of the low-cost industrial digital signal processor used, the resolution of the control commands T_{kw} and α_{k1} is fixed in the experiment to be 1 μs and 0.02 respectively. Hence, both the results with and without bounds, have been obtained at fixed resolution. However, the resolution of the control inputs can be further increased along with modifications of the coefficients (γ_1 and γ_2) in the cost function, to bridge the gap in convergence times, as shown in the comparative study in Figure 20.

2.3. SBC for reduced-damped constant power load

Next, SBC is delineated for constant power loads. Since the FFT of a switching sequence (SS) ranges from dc to several MHz, as shown in Figure 1, any disturbance that originates in PES state due to such reduced-damped loads can be suitably tackled by the intelligent synthesis of the switching sequence (SS) of a PES. The sequences can be designed based on a variety of conventional linear control principles. However, linear control principles fail to utilize such wide-scale of the SS since they perform small-signal perturbation of the averaged model. To cite an example, for

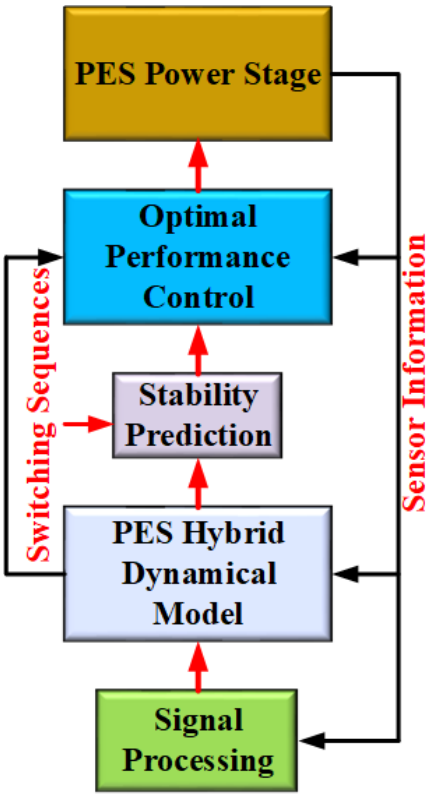


Figure 21. Illustration of SBC scheme for standalone PES.

an isolated Ćuk differential-mode inverter operating at 100 kHz[33], a controller designed by linearized analysis cannot attain a bandwidth of more than 0.6 kHz and cannot hence address fast scales. In this regard, SS, when designed based on non-linear optimal principles, can control all the scales suitably. Apart from being an advanced non-linear controller, optimal principles are predictive in nature. They can compute open-loop future actions[52] to seamlessly guide a PES response on the fly and then do trajectory correction based on sensor feedback as model predictive controllers[54]. Sequence-based controllers[2] (SBC) go a step further to do extensive offline analysis based on the

full-order PES non-linear piecewise affine models and Lyapunov stability methods for discontinuous systems[1] to narrow down the online search space of control actions, thereby reducing the computational burden on DSP. The Lyapunov methods, although deemed mathematically tedious, actually encompass solution of a set of simple LMIs in MATLAB[55]. The switching sequence (SS) generation for a PES is highlighted in Figure 21.

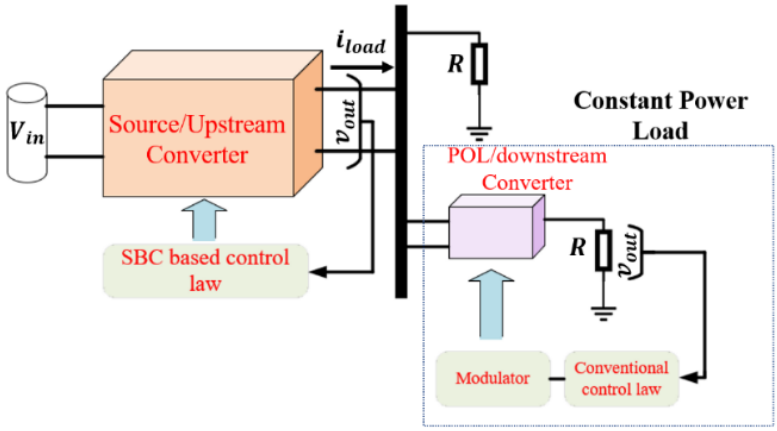


Figure 22.Schematic of an upstream Ćuk PES feeding a downstream PES.

The effectiveness of such control design is validated now for constant power loads (CPL) which are non-linear in nature. The non-linear CPLs have a negative incremental impedance which has a destabilizing effect on multi-converter PES systems[29]–[31], [56], [57]. Figure 22 shows a multi-converter system where the source upstream PES regulates its output voltage tightly, thereby emulating a CPL and provides power to downstream PES and loads. Since CPLs lead to a reduced damped PES, traditionally CPLs have been tackled by active and passing damping approaches. Passive impedance damping approaches[58] negatively affect PES power density, efficiency, etc. On the other hand, active damping approaches [59], [60]successfully emulates the effect of passive damping by resistive elements by incorporation of feedback loops that shape the PES input/output impedance. Reference [57] uses the load current as feedforward to effect the PES stability positively while driving a CPL. But the approaches make use of linear control laws by linearizing the PES dynamics around a fixed operating point and hence the control laws designed are not global in nature. To provide a case illustration: in [61], the active damping methodology to tackle the CPL can be designed for the PES for the worst-case operating point. However, when the PES operates at a fraction of rated power the control design lacks optimality. Also, the active damping methodologies are validated for lower-order PES

prototypes that can provide enough stability margins for conventional linear control design. However, for higher-order PES like Ćuk, Figure 23 shows the undamped PES small-signal response of the output voltage with respect to control input for CPL which makes it difficult for linear control designs to achieve enough stability margin at appreciable bandwidth. Hence for highly nonlinear loads like CPL, SBC can seamlessly synthesize sequences on the fly taking into consideration the global stability of the PES while exhibiting fast dynamic response.

This part of Chapter 2 delineating the SBC scheme for CPL is organized as follows; the SBC architecture for the isolated PES with constant power load is discussed in Section 2.3.1. Section 2.4 deals with simulation and experimental validation of the proposed approach. The chapter is concluded in Section 2.5.

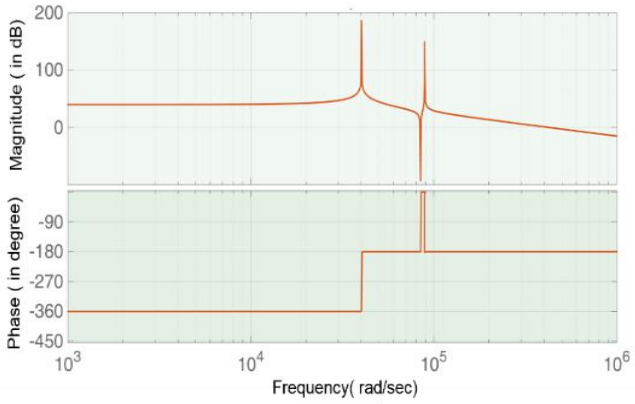


Figure 23. An undamped Ćuk PES model with CPL.

2.3.1. SBC architecture for constant power load

Open loop optimal policies predict the PES behavior in advance before firing the PES switches. The optimal policies are made closed-loop via sensor feedback considering the PES model-hardware mismatches. SBC is such a closed loop optimal policy, which starts with the synthesis of the piecewise-linear model (PWL) of the PES which depends on the PES topological and switching behaviors, and then the stability of the PES sequences is analyzed. Subsequently, discrete maps of the PES are synthesized and based on Lyapunov theory, stability bounds on time horizons (T_{kw}) of a switching sequence and time allocation of switching states in a sequence α_{kn} are computed. The switching sequences have definite horizons $T_{kw_1}, \ldots\ldots, T_{kw_n}$ with time allocations $\alpha_{k1}, \ldots\ldots, \alpha_{kn}$ with generalized rise and fall times t_r and t_f respectively. Choice of these parameters by SBC in a predictive manner shapes the PES spectrum from slow to ultra-fast scales. The steps in SBC synthesis is as follows:

2.3.1.1. PWL modeling of an isolated PES

The first step of SBC is to attain a full-scale model of the PES. The model will be used for offline stability analysis and online prediction model. Isolated PES topologies, in this regard, pose predicaments in construction of the PES model for SBC. This is due to complex model formulation owing to the presence of magnetizing (L_m) and leakage inductance (L_{lk}) of the high-frequency (HF) transformer, which creates extra states in the PES model. For discussion, we will consider an isolated Ćuk PES model as shown in Figure 24. For the control of the same Ćuk PES in [2][62], the isolated PES high-frequency transformer dynamics was replaced by flux-balance equations leading to reduced order PES dynamics, since the objective was only to perform output voltage regulation since the reduced order PES equations lead to correct input current and output voltage dynamics.

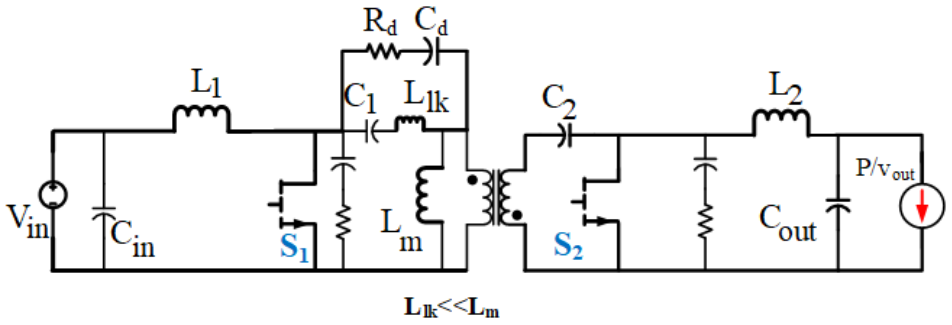


Figure 24. Isolated Ćuk PES schematic.

Notwithstanding, this results in severe shortcomings since the transformer significantly modifies the response of the blocking capacitors C_1 and C_2 (Figure 24) which is not captured by the reduced-order flux-balanced PES dynamics. The capacitor response may be used for PES constraints when dealing with reduced-damped loads and affecting wider scales and addressing fast-scale phenomenon like losses, EMI etc. Hence, a full-scale model is desired which considers HF transformer dynamics for correctly capturing converter dynamics. However, incorporation of the HF transformer dynamics leads to undamped oscillations in the prediction model due to the resonance of C_1 and C_2 with magnetizing inductance L_m. To dampen the oscillations, in the virtual isolated PES model, an RC damper branch was also considered as shown in Figure 24. This drastically improves the quality of predictions made by the prediction model. Figure 25 compares the Floquet multipliers of the isolated PES dynamics between case 1: with L_m only, case 2: with L_m and damper RC branch. The multipliers for the case 2 are further inside the unit circle which implies a more stable

system response over the wide operating region.

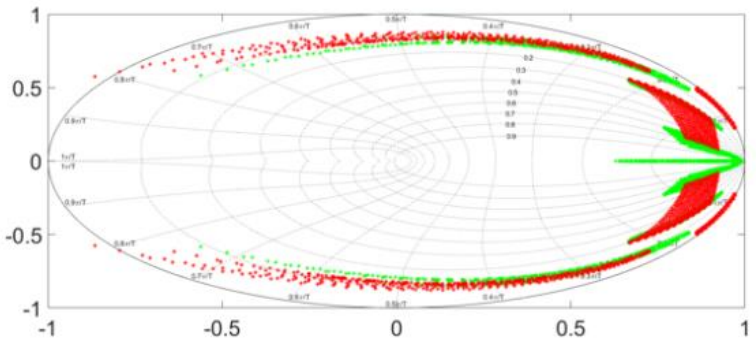


Figure 25. Floquet multipliers (represented on imaginary and real axes) obtained using period-one map of the isolated Ćuk PES. Comparison of the evolution of the Floquet multipliers (represented on imaginary and real axes) on the incorporation of magnetizing inductance (red) and on the introduction of passive damping using RC branch(green) for variation of α_{kn} and T_{kw}.

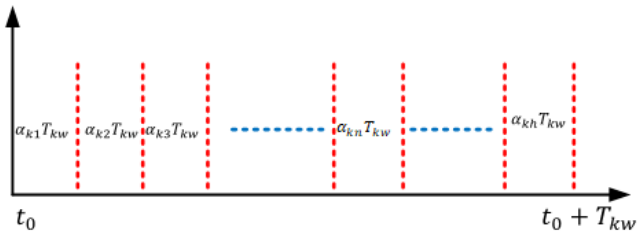


Figure 26. k^{th} switching sequence is shown with h states. Equation (1) corresponds to the n^{th} switching state.

Taking this into consideration the isolated PES model can be written as:

$$\dot{x}(t) = A_{kn}x(t) + B_{kn} \tag{21}$$

where A_{kn} and B_{kn} are matrices that describe the PES with the CPL for the n^{th} switching state in k^{th} switching sequence and have been defined in Appendix F. The total number of states in the k^{th} switching sequence is h. (say) as shown in Figure 26. The matrices A_{kn} and B_{kn} should be piecewise affine to preclude mathematical complexity for the modeling and stability analysis. A linear discontinuous state model eases the LMI complexity as derived in Section 2.1.

For the non-linear CPL load-based PES as shown in Figure 27, the downstream PES is modeled into the original system upstream PES leading to an integrated higher-order PES model. The downstream PES is controlled by a linear controller and hence the controller equation has also been incorporated considering a fixed switching sequence. This

leads to a comprehensive PES dynamical model that can be used for stability analysis.

Next, (21) is translated to error coordinates using $e(t) = x(t) - x^*$, where $e(t)$ represents the error vector, while x^* represents the steady-state values of the PES states. In the error coordinate, (1) is modified as follows:

$$\dot{e}(t) = A_{kn}e(t) + \overline{B_{kn}} \tag{22}$$

where $\overline{B_{kn}} = -(B_{kn} + A_{kn}x^*)$. Discretizing (22), one obtains the following expression for j^{th} discrete sample:

$$e(j+1) = A_{knd}e(j) + B_{knd} \tag{23}$$

The detailed matrix formulations have been shown in [2].

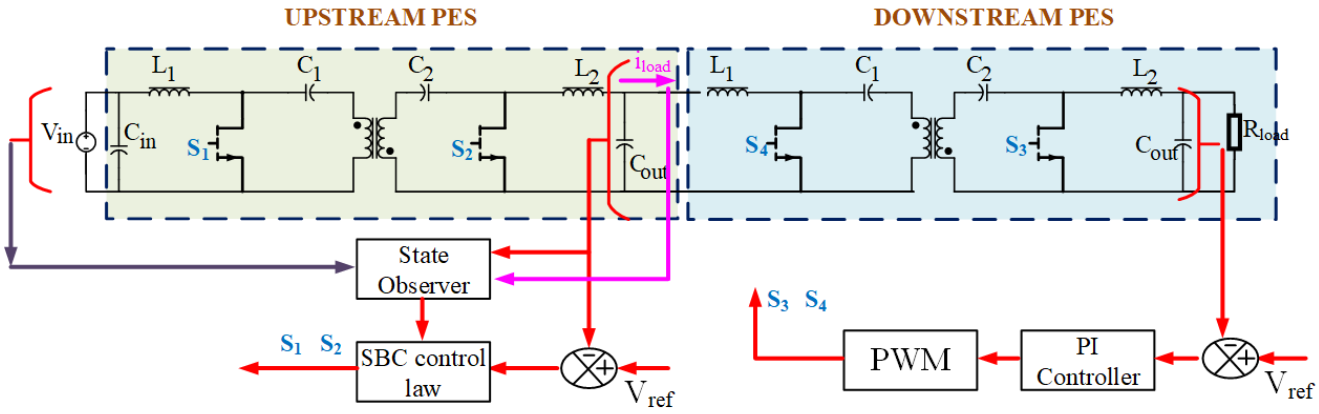


Figure 27. Two isolated Ćuk PES have been connected back-to-back. The SBC algorithm is applied to the 1st PES while the downstream PES is controlled by a PI controller whose switching sequence is fixed to the 1st module by the processor.

2.3.1.2. Stability analysis of the PES

Once the full-scale PES model is obtained, a piecewise-discrete (multiple) Lyapunov function $V_k(j) = \sum_{n=1}^{h} e(j)^T P_{kn} e(j)$ is used to obtain the gradient of the multiple Lyapunov function:

$$\nabla V_k(e) = V_k(j+1) - V_k(j) = \sum_{n=1}^{h} \alpha_{kn} \left(e(j+1)^T P_{kn} e(j+1) - e(j)^T P_{kn} e(j)\right) \tag{24}$$

This leads to the simple LMI : $\sum_{n=1}^{h} \alpha_{kn} \begin{bmatrix} (A_{knd}^T P_{kn} A_{knd} - P_{kn}) & A_{knd}^T P_{kn} B_{knd} \\ B_{knd}^T P_{kn} A_{knd} & B_{knd}^T P_{kn} B_{knd} \end{bmatrix} < 0$ which can be easily solved using [55]. The solution of the LMIs command practical significance. The LMI solutions present a feasibility

problem that helps to attain a bound of α_{kn} and T_{kw} that reduces DSP computational time.

2.3.1.3. Online SBC implementation

2.3.1.3.1. Prediction model and performance index

The online execution scheme of SBC encompasses the definition of an online model for prediction and optimization of the control actions based on PES constraints and a pre-defined cost function in the processor. The online prediction model of the PES is derived from the full-scale model in (1). Taking into consideration the DSP timing requirements, the model was simplified by considering i_{load} as the control input to the PES, along with α_{kn} and T_{kw}. Taking DSP samples as $j, j+1, ..$ we form the Euler approximated prediction model as:

$$x(j+1) = (I + A_r\alpha_{k1}T_{kw} + A_r\alpha_{k2}T_{kw})x(j) + (A_r\alpha_{k2}T_{kw} + I)(\alpha_{k1}T_{kw}\, B_r) + \alpha_{k2}T_{kw}\, B_r \quad (25)$$

Here, A_r and B_r are the matrices for the reduced-order online model and have been defined in Appendix F. The model takes input from the state observers and sensor measurements and explores its evolution over future control actions. The validity of such reduced models have been validated in [2].

The performance index revolves around voltage regulation of the upstream PES and takes the form already established for [2]. However, the design of the feedforward term I_{ff} in [2] is different from the current scenario. In order to improve the transient response of the controller, I_{ff} for the CPL application is modified to be $I_{ff} = \frac{V_{ref}I_{out}}{V_{in}}$ following [57]. Here, V_{ref} is the output voltage reference command of the PES, I_{out} is the measured output current and V_{in} is the input voltage.

2.3.1.3.2. Observer design and DSP implementation details

To bypass the plurality of sensor requirement for such a complicated higher-order system with many passive elements, state observers are required for optimal controllers. Traditional linear observers[63] based on Leuenberger theory, sliding mode principles, revolve around the generalized theory that the PES averaged dynamics should be observable given the number of sensing elements available. Such observer design requires sensing of plural states in the higher order Ćuk PES which is not practical. Hence a discrete Poincare non-linear map was used for observing the PES states. The map evolves in time-synchronized to the processor and the model-actual hardware inaccuracies are

eliminated by a PI loop as shown in [2].

The observer was implemented in a low-cost industrial-scale TMS320F28335 DSP with limited memory space. This was the most computationally intensive element in the design since the observer required a solution of exponential maps. Hence, a simple method was followed which will be discussed for the fundamental sequence of the PES. The terms $\gamma_{1-6}, \beta_{1(1-6)}, \gamma_{6-12}$ and $\beta_{2(1-6)}$ are precalculated in MATLAB. The terms are a function of $i_{load}, V_{in}, \alpha_{kn}, T_{kw}$. If x_{1-6} are initial states of the observer, the intermediate variables $x_{k_{1-6}}$ were calculated in the DSP. Using the variables $x_{k_{1-6}}$, the final states at the end of the horizon T_{kw} are calculated in the processor. The same procedure was used for the prediction model, too, as discussed in Section 2.3.1.3.1. The procedure helped in 70-80 per cent reduction in online computation time compared to generalized subroutines in C.

$$x_{k_{1-6}} = \gamma_{1-6} x_{1-6} + \beta_{1(1-6)} \tag{26}$$

$$x_{k_{6-12}} = \gamma_{6-12} x_{k1-6} + \beta_{2(1-6)} \tag{27}$$

Apart from the *(1) manipulated observer design* and *(2) the offline bounds on* $\boldsymbol{\alpha_{kn}}$ *and* $\boldsymbol{T_{kw}}$ *from the stability/reachability analysis,* a simple method was used to obtain an initial estimate of α_{kn} for each T_{kw} which cuts down computational time further. The initial estimate was based on the input-output non-linearity of the Ćuk PES (with N as the transformer turns ratio) as:

$$\alpha_{kn} = \frac{V_{ref}}{N * V_{in} + V_{ref}} \tag{28}$$

The initial estimate helped in simplifying gradient descent and brute force methods for online search space reduction.

2.4. Results of SBC for constant power load

The results section is organized as follows. First, through offline simulations, the isolated PES modeling justifications were validated. Next, the online computational savings due to the methods used in Section 2.3.1.3.2 are shown. Then, the results for the PES in CPL modes of operation were validated and discussed. The detailed hardware design is delineated in [33].

2.4.1. Effect of magnetizing inductance of the high-frequency transformer on PES modeling

Figure 28a and Figure 28b illustrates the steady-state oscillations of the PES states due to the inclusion of

magnetizing inductance (L_m) and leakage inductance (L_{lk}) of the high-frequency transformer. Resonance of L_m with the primary blocking capacitor of the PES (the Ćuk PES is shown in [5]) creates an undamped system model. An easy solution may seem to be the non-incorporation of L_m in the system model and hence modeling the high-frequency transformer as an ideal one. Although this leads to unchanged input inductor current and output voltage of the PES, it changes the two-input blocking capacitor responses, leading to faulty predictions of the capacitor voltages that can now never be used for PES hard and soft constraints[52]. This is of importance for driving CPL loads since SBC uses constraints on the PES states to ensure stable operation and preclude excessive device stress. Figure 29 compares the analytical solution of the Ćuk PES model against a full-scale simulation of the PES in Saber software for an operating point. Although the state-error values of the input inductor current and output voltage converged to zero, the blocking capacitor voltages on either side of the high-frequency transformer does not converge to zero.

Hence, to include L_m so as to eliminate this error, the PES model is modified to constitute a small parasitic included in series with the input inductor and an R-C damper network placed in parallel with the blocking capacitors. It dampens the oscillations in the PES model, also conserving the blocking capacitor response as shown by the comparisons in Figure 30a and Figure 30b for wide variations of α_{kn} and T_{kw}. The oscillations die away within 20-30 switching cycles, leading to damped PES response. This improves the efficacy of SBC predictions, leading to an optimal performance control.

2.4.2. Online computation time saving due to offline reachability bounds

SBC solves an online optimization problem with offline computed bounds on the control inputs. For any load under

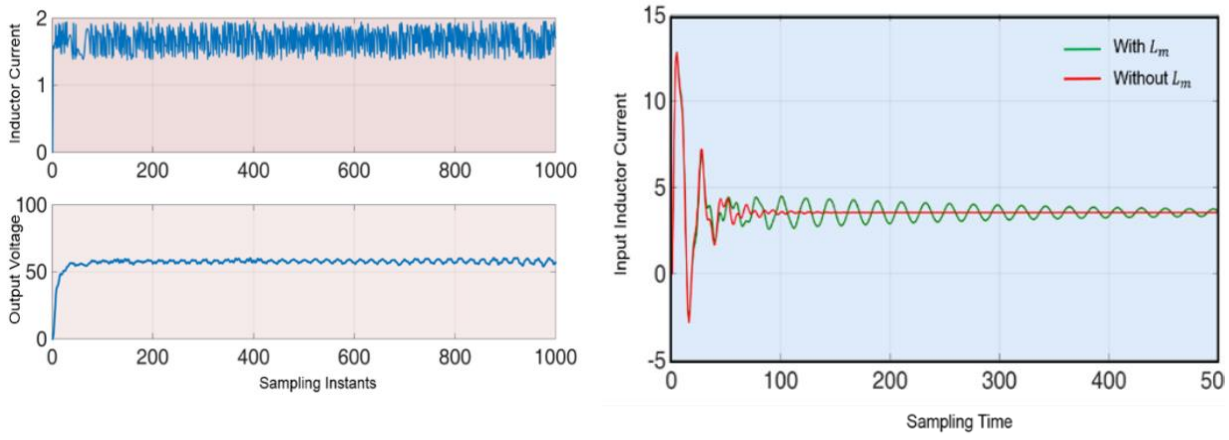


Figure 28. (a) Simulation results showing the effect of incorporation of magnetizing inductance in the prediction model for the SBC controller. It

leads to PES input current and output voltage oscillations. (b) The open-loop PES response (simulation result) with and without magnetizing inductance.

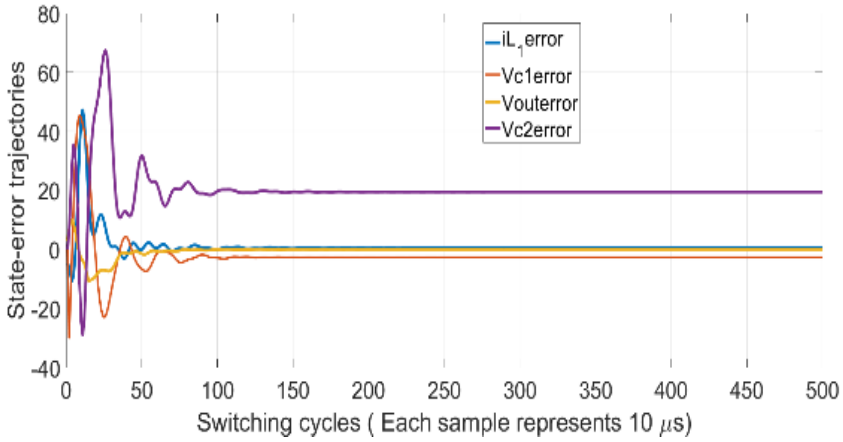
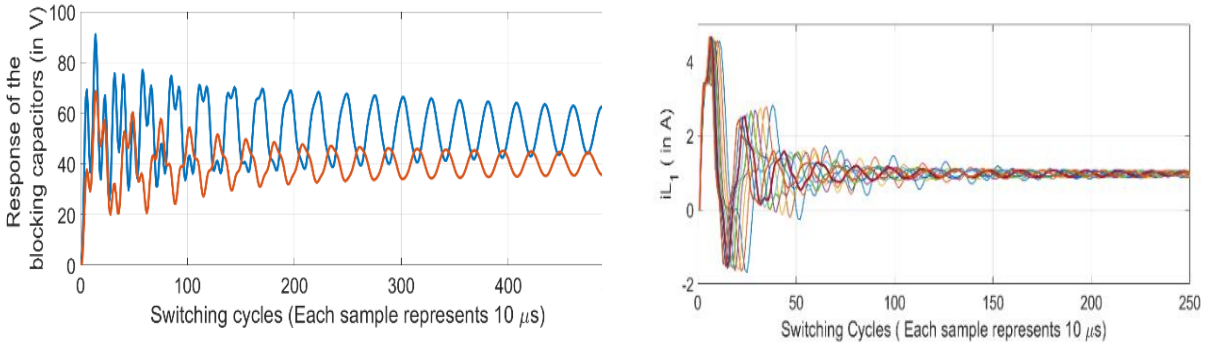
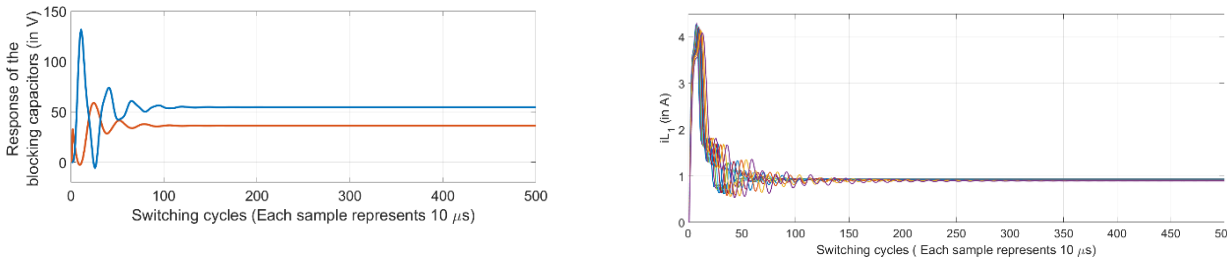


Figure 29. The state-error trajectories from start-up to steady-state for a full-scale model solution in Saber software and the PES analytical model without magnetizing inductance. The traces from top to bottom represent the errors in input inductor current (main control variable), the primary blocking capacitor voltage, the output voltage and secondary blocking capacitor voltage respectively.

consideration (CPL for the current case), SBC computes an offline reachable space for α_{kn} and T_{kw} that can provide reachability to the PES dynamics for any given V_{in}, V_{out} and P_{out}.The reachability bounds help in the execution of this dual-control problem in a low-cost processor by decreasing the online search space. Figure 31 shows the online execution time required to execute the SBC algorithms online using all the search-space reduction tools delineated in Section 2.3.1.3.1 for CPL operation. Of the execution time divisions in Figure 31, the state observer and signal processor timings have been heavily optimized. The exhaustive search space (ESS) is traversed using low



(a)



(b)

Figure 30. (a) Figure showing the deteriorated input inductor current and blocking capacitor responses of the Ćuk PES prediction model on the incorporation of the magnetizing inductance (L_m) only. (b) Figure showing the improved responses of the Ćuk PES virtual prediction model on the incorporation of the passive damping mechanism for magnetizing inductance (L_m).

complexity brute force method. By use of sophisticated interior points and advanced gradient descent methods aided by the initial point choice in Section 2.3.1.3.1, the ESS can be further reduced by half, making SBC possible in PES with switching frequencies of greater than 100 kHz.

2.4.2.1. PES supplying constant power load

Start-up response: Figure 32a shows the experimental hardware prototype of the Ćuk PES used for the constant-power load of operation. The SBC control algorithms have been executed on the TMS320F28335 digital signal processor on module 1, while a simple PI controller is used to drive module 2. The hardware prototype consists of two Ćuk dc-dc modules connected back-to-back with $V_{in} = 30$ V for module 1. Figure 32b shows the drain to source

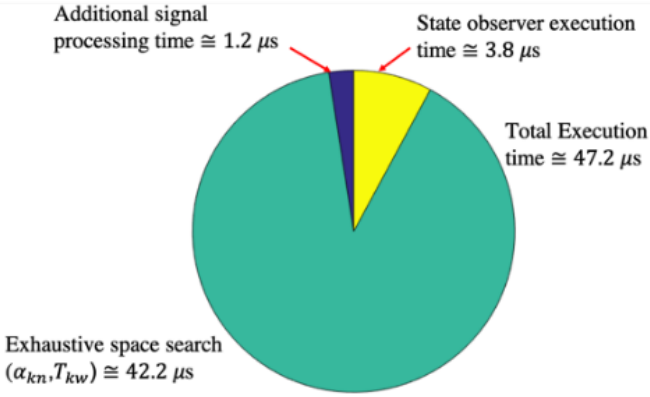
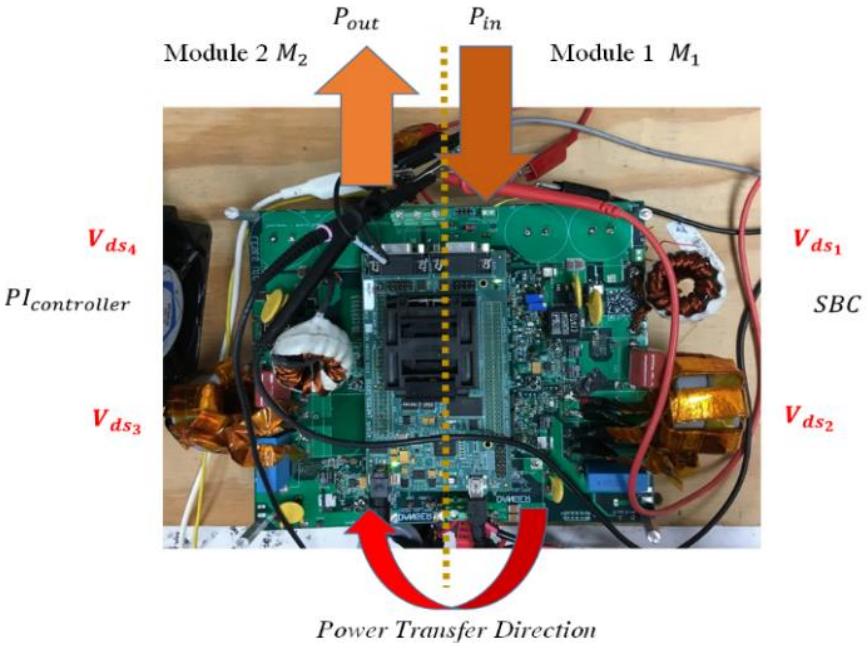
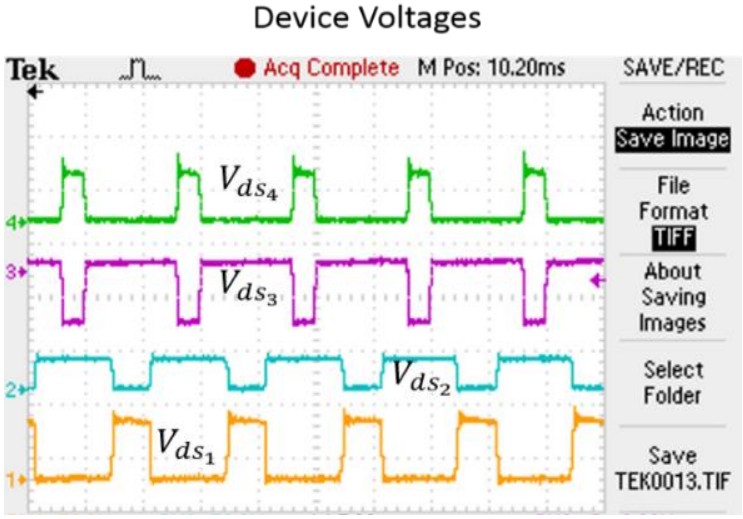


Figure 31. Figure showing the total execution time required to solve the SBC problem in the low-cost industrial processor. The implementation methodology delineated in Section 2.3.1.3.1 helped in online time reduction.

voltage waveforms of all the GaN FETs used in the PES modules. Figure 33 shows the start-up response of the output voltages of the two modules. $V_{output_{M_2}} = 60$ V and $V_{output_{M_1}} = 50$ V voltages seem to converge to steady-state without any disturbance and without any significant overshoot, thereby proving that the SBC algorithm in module 1 provided good performance in maintaining the constant-power load. Figure 34 further illustrates the time evolution of some of the states of the PES for CPL operation.



(a)



(b)

Figure 32. (a) Illustration of the hardware set-up for CPL. Two Ćuk PES modules have been connected back-to-back. Module 1 being the upstream PES and module 2 being the downstream PES. All the devices are GaN-FETs operated at 100 kHz. No passive resistors have been connected between the modules to aid damping. (b) The device voltages of the four GaN-FETs in CPL operation have been shown. Scales 50V/div.

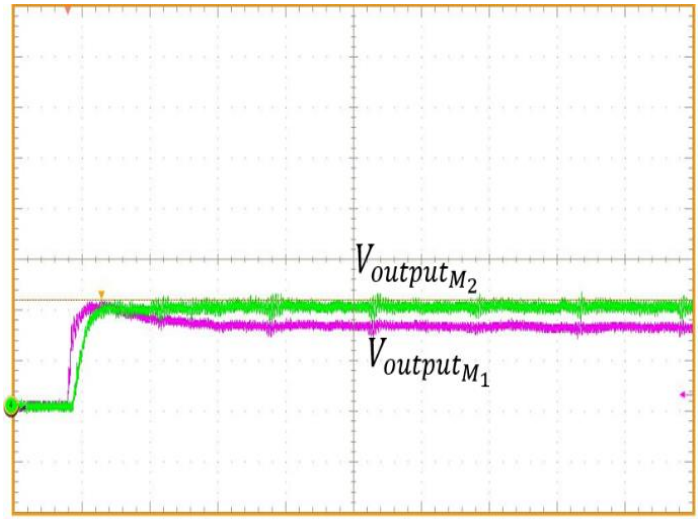


Figure 33. Illustration of the start-up response of the Ćuk PES modules. $V_{output_{M_2}}$(60V) and $V_{output_{M_1}}$ (50V) denotes the responses of module 2 and module 1, respectively. The scale is 30 V/div.

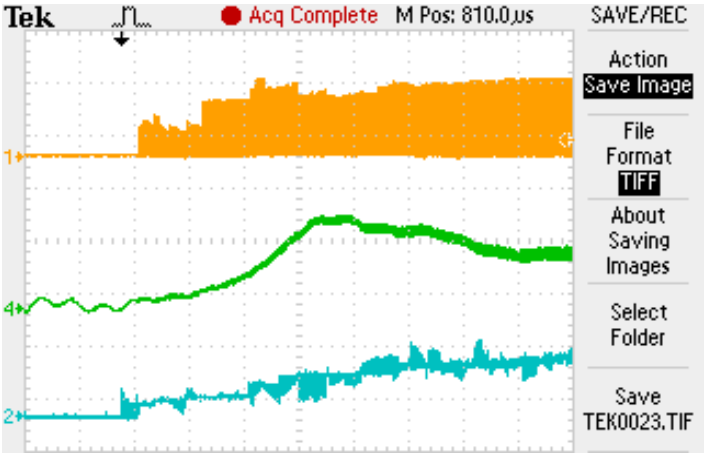
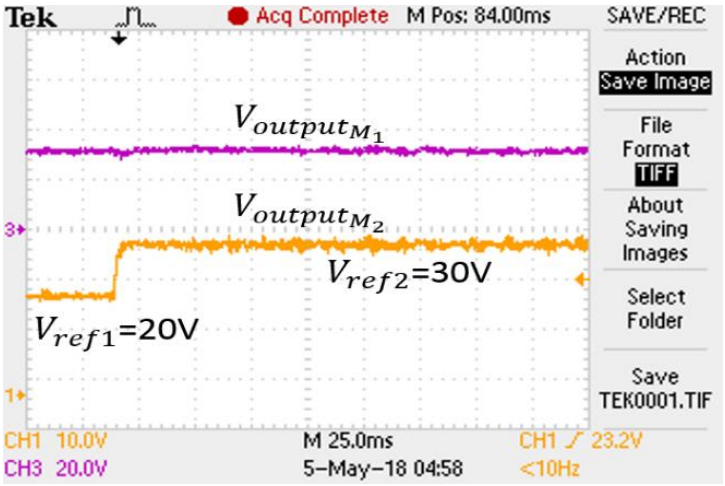


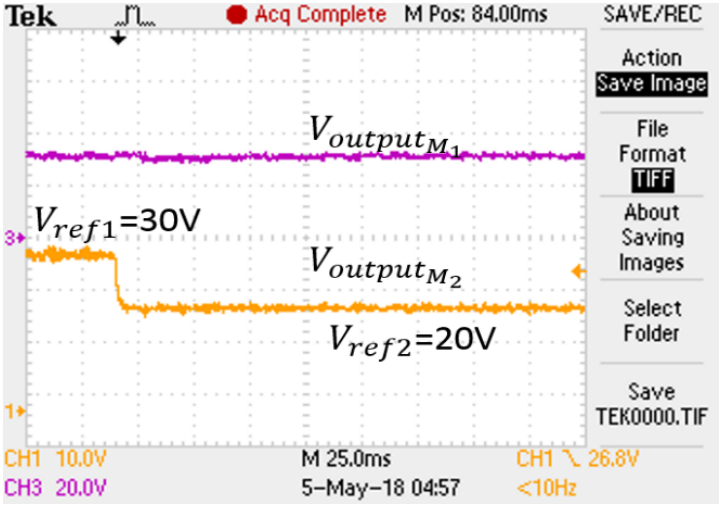
Figure 34. Illustration of the start-up response of the Ćuk PES drain to source voltage V_{ds_1}(from Figure 14a), the current i_{load} from Figure 7 and the evolution of the switching state α_{k1} from top to bottom. The vertical scales from top to bottom are 50 V/div, 4A/div and 2 V/div. The horizontal scale is 100 μs /div.

Step-response: When a step change in output voltage reference was given to the module 2, there was a negligible deviation in the module 1 voltage, which increased the current output to cater to the increased power demand as shown in Figure 35, proving the robustness of the control strategy for such higher-order non-minimum PES.

***Load transient response*:** Also, the 1st module with SBC maintained its bus voltage perfectly on the application of a pulsating load at the output of the 2nd module as shown in Figure 36. The pulsating load had transition magnitude of 2 A, the duty cycle of 65 % and frequency of 1 kHz. This further proves the robust nature of such control strategies.



(a)



(b)

Figure 35. (a) and (b) Perturbation in module-1 voltage that supplies the CPL to module 2. Despite the V_{ref} transient in module 2 voltage reference, there is negligible perturbation in the module-1 voltage, thereby proving it maintains its voltage, on event of a change in power demand.

2.5. Conclusions

Control of a higher-order PES driving pulsating and reduced damped CPL load using SBC, which solves an underlying optimal-control problem using pre-determined reachable switching sequences of the PES, is delineated in

this chapter. Initially, using an integrated nonlinear map of the PES with the load, a discrete multiple-Lyapunov-function-based methodology to ascertain the reachability of the PES dynamics, in terms of its switching sequence and the time duration of the sequence and the allocation of that time among the switching states of the same sequence, is determined. Subsequently, an online optimal SBC formulation is outlined that uses these pre-determined limits on the reachable-switching-sequence duration and its distribution among the switching states of the same sequence. By doing so, the overall computation time for online SBC execution is expected to be reduced without affecting the overall control performance of the PES.

Subsequently, the theoretical predictions are experimentally validated executing an online SBC on a GaN-FET-based higher-order high-frequency non-minimum-phase Ćuk-PES. To begin with, time-domain experimental results that validate the offline reachability predictions of the Ćuk-PES are conducted. Next, it is shown experimentally, how the theoretical predictions of the reachability analysis for the Ćuk-PES enable a tangible reduction in computation time for online execution of the SBC without any appreciable compromise in system performance and convergence time. Overall, the outlined work has broader ramifications. First, the nonlinear-map-based reachability-analysis

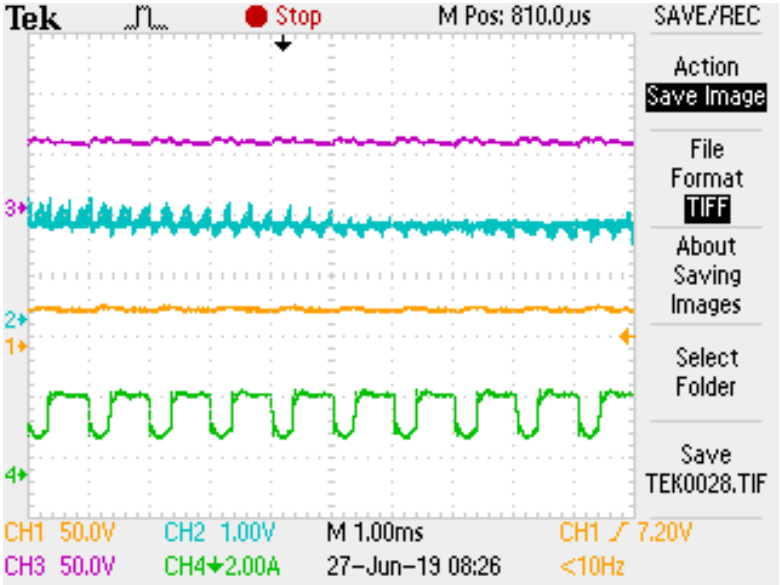


Figure 36. Illustration of the steady-state response of the Ćuk PES output voltage of module 2, the evolution of the switching state α_{k1},the output voltage of module 1, and the pulsating current at the output of module-2., from top to bottom.

approach in terms of a switching sequence of a PES is extendable to other PESs driving pulsating and other types of loads. Second, the reduction in online computation of the SBC, using stability-bound reachable switching sequences, implies that lower-cost processor can be used while retaining quality large-signal response expected of optimal

controllers.

The SBC approach outlined in this dissertation is generalizable. A PES is typically designed for CCM, boundary control mode (BCM), or discontinuous-conduction mode (DCM). For the first two cases, the methodology outlined in this chapter and explained for the specific Ćuk-PES applies as is. If, however, the PES is designed only for DCM, then, the modeling and stability Sections for the PES and loads considered must encompass an additional switching state corresponding to inductor-current invariance. The reachability analysis and optimization methodology remain the same as outlined in respective Sections with the exception that the search for the time allocation of the switching states of a switching sequence will involve an additional search space to assess the impact of duration inductor current discontinuity or invariance on PES reachability.

Chapter 3

3. ELECTROMAGNETIC INTERFERENCE MITIGATION OF A POWER ELECTRONIC SYSTEM USING SWITCHING SEQUENCE CONTROL

Parts of this chapter, including figures and text, are based on my following papers:

D. Chatterjee and S. K. Mazumder, "EMI Mitigation of a Ćuk Based Power-Electronic System using Switching-Sequence-based Control," *IEEE Trans. Power Electron*., vol. 36, no. 9, pp. 10627-10644, Sept. 2021.

.

Rapid switching transition of wide-bandgap semiconductor devices like GaN has made higher switching frequencies realizable at higher power [1][2], which helps in the synthesis of a power-dense/compact power-electronic system (PES). However, rapid switching at increasingly higher frequencies negatively affects electromagnetic-interference (EMI) performance of a PES. Hence EMI input filters need to be designed to fulfil the strict regulatory standards on differential-mode (DM), common-mode (CM) and radiative noise spectrum. The EMI regulatory standards [65] become stricter at progressively higher ends of the frequency spectrum, which challenges higher-frequency operation at enhanced power levels. The situation can be explained by the following case illustration for conducted noise (CM and DM) : operating one of the GaN-FET based PES modules in [33] at 500 W for rated input and output voltages and for a switching frequency of 200 kHz, will result in the violation of the less strict CISPR/EN 55022/32 Class A EMI limit by a margin high enough to necessitate EMI filter that increases space [66], [67]. Use of

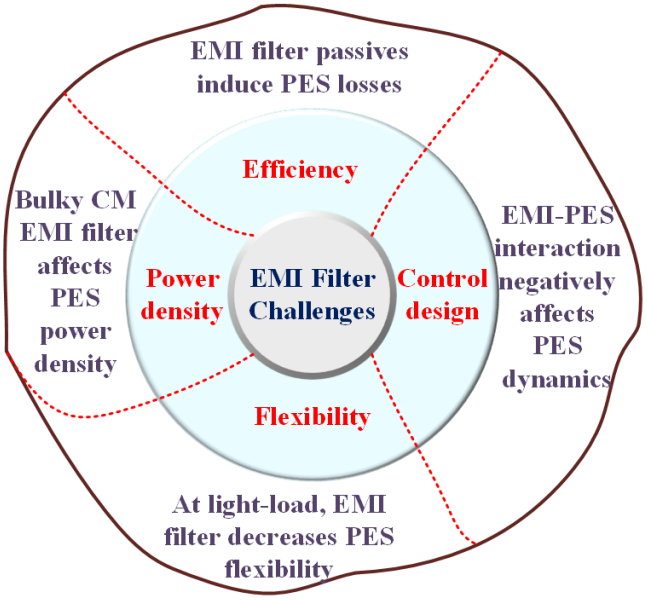


Figure 37. Illustration of the shortcomings of the traditional EMI filter.

multistage EMI filters [35] may preclude the use of higher valued passive components, thereby reducing EMI filter size and boosting power density of the PES. Notwithstanding, this causes a predicament in the design of a PES that has relatively low stability margins in closed loop, since the EMI filter may incorporate additional phase lag which may lead to instability and degraded PES overall control performance [68]. This adversely affects the power density of the PES that is supposed to increase with the use of fast switching transition GaN-FETs operating at very high frequencies. It also negatively impacts the efficiency of the PES due to extra losses incurred in the EMI filters

[34], [68], [69].

Due to the stringent limits on the size of the CM capacitor based on the leakage current allowance of the PES [70]–[73], CM EMI filter adversely affects the size of a PES more than DM filter. In DM filter the size of the DM capacitor can be increased to keep the inductor size down for high-current applications. But CM filter precludes this flexibility [70]–[73], which results in high inductance values for CM EMI cut-off.

In order to address the issues related to EMI filter design as portrayed in Figure 37, control-hardware integrated solutions must be woven fine for GaN-FET based wide bandgap (WBG) PES to realize higher frequency operation at increased power levels. This is because reliance on an increased size of EMI filters alone will impede high-frequency operation of a WBG PES.

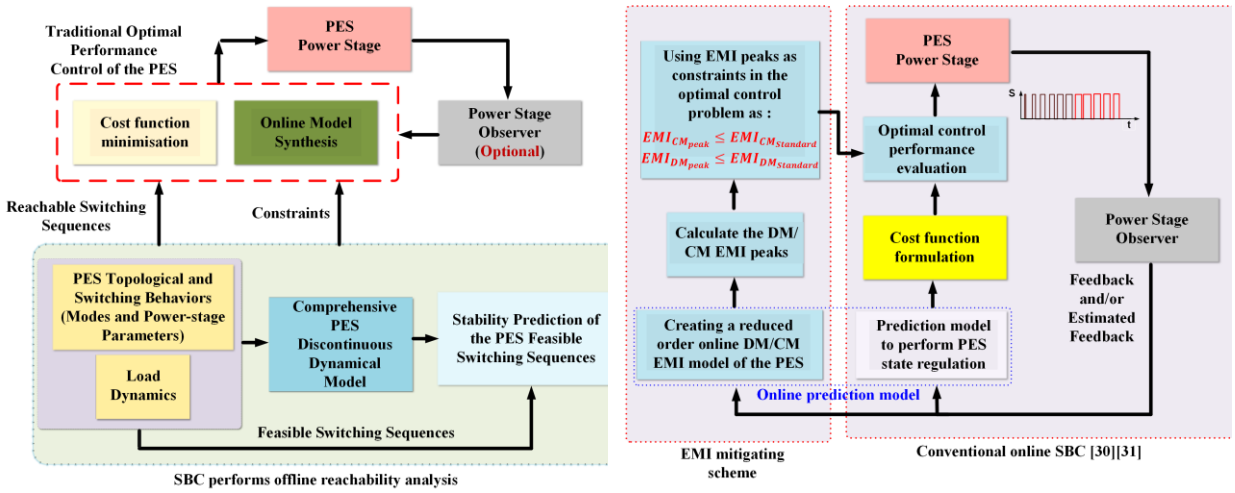
Frequency modulation techniques with open-loop control have been studied previously to decrease the EMI levels of a PES. The theory is based on [74] which derives the differential equations to show how frequency modulation impacts the spectrum of a signal. The effectiveness of these methods for EMI reduction of PES for different modulation profiles is discussed in [75]–[77]. Reference [76] focusses its discussion on how to create modulation profiles, with extensive analysis, to have a positive effect on both CM and DM EMI of a PES, while [78] provides a generalized assessment of how the depth and breadth of the modulation profiles impact PES EMI. Reference [78] also talks about the significant generalized side effects, such as audible noise due to frequency variation, and poor converter output voltage regulation obtained due to the modulation techniques. However, most of the abovementioned literature determines the effect of the modulating techniques based on open-loop principle, so that the distribution of the even and odd harmonics is pre-defined. The literature preferred non-variation of the PES duty cycles, in order not to disturb the observability of the desired modulation effect on the PES. Also, the impact of the modulation on PES behavior on EMI filter design and output filter size has not been discussed. Reference [79] outlines the benefits of the open-loop frequency modulation techniques against the drawbacks in increased output voltage ripple but it does not provide any quantitative analysis on how much the output filter size needs to be altered to support constant output voltage against decreased EMI filter size across wide switching frequency range. Moreover, it mainly comments on the open-loop behavior only with pre-defined constant time allocated switching sequences. Reference [80] further highlights the deterioration of the PES state response due to the low-frequency perturbation introduced by frequency modulation under the closed-loop linear controller but precludes detailed analysis on the controller tuning parameters for the experimental responses.

Practically a PES may be required to operate most of the times in closed loop under wide operating ranges. Hence, it is necessary to undertake studies related to PES behavior in closed loop under the influence of EMI mitigating switching sequences. Switching sequences affect the PES switching behavior, which in turn influences the EMI signature of a PES. They can be synthesized by a model/data-driven intelligent controller to positively affect the PES EMI signature, which can reduce the EMI size requirements or preclude the need for EMI filters up to some desired power levels.

The SS can be synthesized based on model-predictive-control (MPC) theory [15], [19], [22], [24], [27], [81]–[83] that can solve multi-objective optimal-control problems by careful manipulation of the switching states of a PES based on a predefined cost. Reference [4] shows how optimal controllers can control the switching states of a PES to achieve objectives ranging from limited switching loss reduction to the shaping of PES low-frequency spectrum along with standard PES state regulation. SBC goes a step further to formulate an advanced MPC that controls fast and slow-scale PES objectives but with SS that are stability bounded [2], [13], [14]. Figure 38a shows how SBC is distinct from conventional MPC. SBC uses offline stability/reachability analysis on the feasible switching sequences of a PES [13] to yield reachable switching sequences, which ensure PES stability in real-time and under challenging loading conditions and saving online computation time. The reachable switching sequences help to solve an online optimization problem to come up with direct control actions and preclude the need for a modulator. Also, SBC uses piecewise discrete maps of a PES since they can be written easily for digital processors and can increase control bandwidth. Switching state is controlled in a planning horizon in MPC, while the switching sequence evolves; SBC in contrast, directly controls the stability-bound switching sequence.

SBC design is delineated in detail in [2], [14] with adequate case illustrations, where the switching sequences evolve to control slower scale output voltage regulation and tracking. Figure 38a illustrates the difference between the conventional SBC scheme (as delineated in Chapter 2), with this new work that does PES EMI mitigation.

This chapter, hence, following the guidelines of SBC, constitutes a closed-loop controller that serves dual-objective: (1) steady state voltage regulation/ tracking of a PES; and (2) constituting DM and CM (conducted) EMI mitigating switching sequences in a predictive manner. These two broad steps in constructing the SS is delineated in detail in Section 3.1. Section 3.1 starts with the discrete modelling of the PES and goes forward in using an optimal control framework to constitute the SS, which ensures reachability of the PES dynamics, along with performing conducted EMI noise mitigation. Section 3.2 delineates the SS synthesis for a specific Ćuk PES. The results are discussed in



(a) (b)

Figure 38. Illustration of SBC based SS synthesis scheme for PES. The optimal performance control of the PES constitutes the switching sequences that can be changed on the fly based on definite goals.

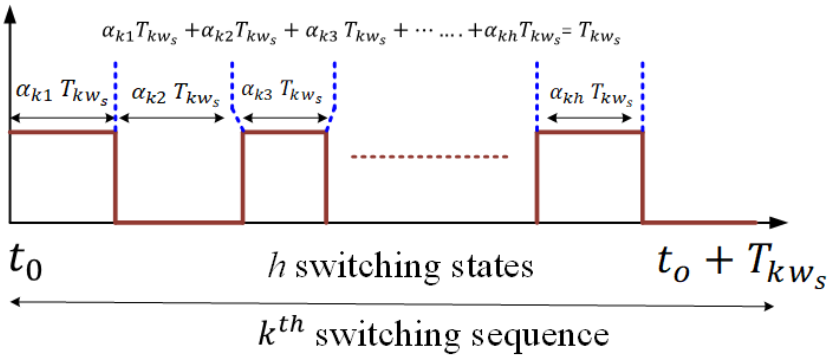
detail in Section 3.3, while conclusions are drawn in Section 3.4. The SS design provided good flexibility in the design of PES by incorporation of enhanced programmability, which is discussed in detail in the chapter and constitutes its main contribution.

3.1. SBC synthesis for EMI mitigation

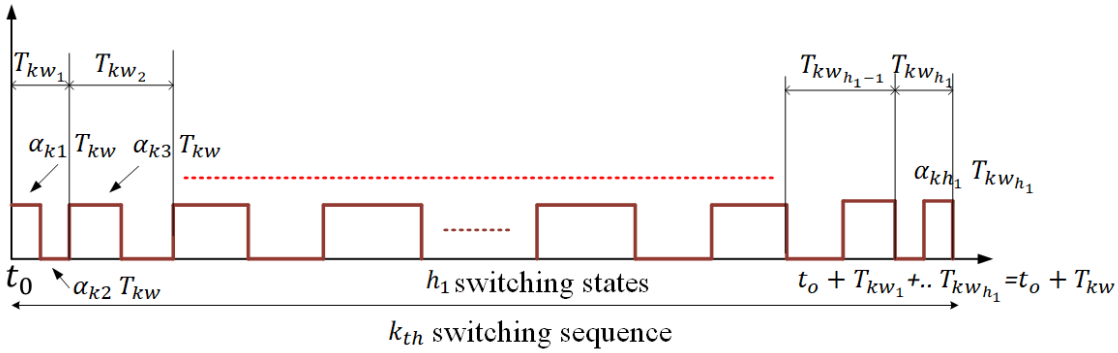
Figure 39a and Figure 39b portrays two predictive switching sequences (SS) synthesized by SBC for a generalized PES. The first SS has a constant time horizon of T_{kw_s}, while the second SS has a variable time horizon given by $T_{kw} = \left(T_{kw_1} + \ldots + T_{kw_s} + \ldots + T_{kw_{h_1}}\right)$, where $T_{kw_i}^{-1} = T_{kw_s}^{-1} + \Delta T_{kw}^{-1}\, \mathrm{v}_m(w_m t) \;\; \forall\, i \in \{1, n\}$, $\Delta T_{kw} = kT_{kw_s}, k \in R$, and v_m is a periodically varying function with w_m as its angular frequency. The symbols $\alpha_{k1}, \ldots., \alpha_{kh}$ in Figure 3 denote the time allocation of the switching states (h switching states in Figure 39a and h_1 switching states in Figure 39b) in the SS. Figure 3c illustrates the difference in the conducted-EMI spectrum of the PES in steady state subjected to these two SSs. We observe that, by modulating the T_{kw} of the SS for case illustrated in Figure 39b instead of repeating the same T_{kw} (= T_{kw_s}) for the case illustrated in Figure 39a yields EMI peak reduction as illustrated in Figure 39c.

While the control of a SS modulates the fast EMI-scale dynamics, it may also affect slower-scale PES dynamics that impact state regulation. Hence, an SBC formulation that controls the fast- and slow-scale dynamics of a PES

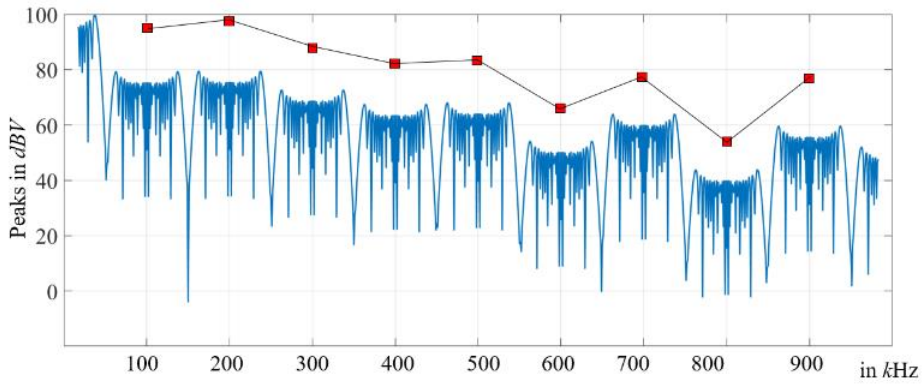
yielding conducted-EMI mitigation and voltage regulation is synthesized and outlined in the following subsections.



(a)



(b)



(c)

Figure 39. (a) and (b) Illustrations of two different SSs having different time horizons leading to (c) different EMI levels when applied to the same PES.

3.1.1 PES modelling

For the PES supplying a passive load, the PES dynamics for the n^{th} switching state in the k^{th} switching sequence can be expressed in the form:

$$\dot{x}(t) = A_{kn}x(t) + B_{kn} \tag{29}$$

where the load specific A_{kn} and B_{kn} are defined in Appendix G for the PES under consideration.

Next, (1) is translated to error coordinates using $e(t) = x(t) - x^*$, where $e(t)$ represents the error vector, while x^* represents the steady-state values of the PES states. In the error coordinate, (1) is modified as follows:

$$\dot{e}(t) = A_{kn}e(t) + \overline{B_{kn}} \tag{30}$$

where $\overline{B_{kn}} = -(B_{kn} + A_{kn}x^*)$. Discretizing (30), one obtains the following expression for j^{th} discrete sample:

$$e(j+1) = A_{knd}e(j) + B_{knd} \tag{31}$$

where

$$A_{knd} = \prod_{n=1}^{2h} exp^{A_{kn}T_{kw}\alpha_{k(2h-n+1)}} \tag{32a}$$

$$B_{knd} = [\left(\prod_{n\neq 1}^{2h} exp^{A_{k(2h-n+1)}T_{kw}\alpha_{k(i)}}\right)(exp^{A_{k1}T_{kw}\alpha_{k1}} - I)A_{k1}^{-1}\overline{B_{k1}} + \left(\prod_{n\neq 1,2}^{2h} exp^{A_{k(2h-n+1)}T_{kw}\alpha_{k(i)}}\right)(exp^{A_{k2}T_{kw}\alpha_{k2}} - I)A_{k2}^{-1}\overline{B_{k2}} + \cdots + (exp^{A_{k2h}T_{kw}\alpha_{k2h}} - I)A_{k2h}^{-1}\overline{B_{k2h}} \tag{32b}$$

3.1.2 PES stability analysis

For the k^{th} switching sequence illustrated in Figure 39a , with h switching states satisfying $0 \leq \alpha_{kn} \leq 1$, $\sum_{n=1}^{h}\alpha_{kn} = 1$, and $P_{kn} = P_{kn}^T$ being positive-definite matrices, a piecewise-discrete (multiple) Lyapunov function $V_k(j) = \sum_{n=1}^{h} e(j)^T P_{kn} e(j)$ is used to obtain the gradient of the multiple Lyapunov function:

$$\nabla V_k(e) = V_k(j+1) - V_k(j) = \sum_{n=1}^{h}\alpha_{kn}\,(e(j+1)^T P_{kn} e(j+1) - e(j)^T P_{kn} e(j)). \tag{33}$$

According to Lyapunov-method of stability analysis for a discrete system, the PES state trajectories converge to (i.e., reach) an orbit if $\nabla V_k(e) < 0$ which results in the following linear matrix inequality (LMI) for any generalized PES:

$$\sum_{n=1}^{h}\alpha_{kn}\begin{bmatrix}(A_{knd}^T P_{kn} A_{knd} - P_{kn}) & A_{knd}^T P_{kn} B_{knd} \\ B_{knd}^T P_{kn} A_{knd} & B_{knd}^T P_{kn} B_{knd}\end{bmatrix} < 0 \tag{34}$$

The equation (34) is solved using the LMI tool in MATLAB. Hence, depending on the PES topology and its switching behavior along with the knowledge of the specific load, once a reachability set of α_{kn} and T_{kw} is obtained from the extensive offline analysis, they can be used to solve the SBC online problem. The detailed derivation is delineated in [2].

3.1.3 SBC online problem

The SBC online problem is divided into two modes of operation:

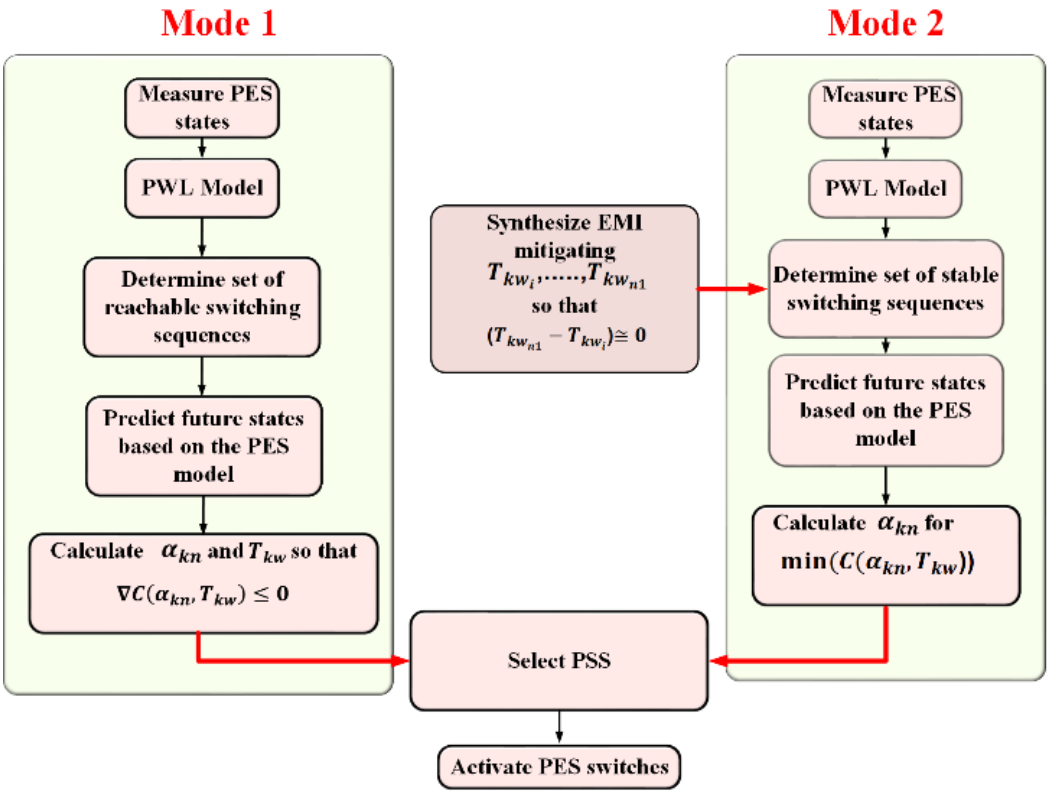


Figure 40. Dual-objective SBC online problem

1) Mode 1: During the transient conditions like a start-up or sudden load change, an online cost function $C(\alpha_{kn}, T_{kw})$ is minimized with respect to α_{kn} (n is a switching state in a given SS) and T_{kw} to synthesize a SS that guides the PES to its steady state.

2) Mode 2: During the PES steady state, as shown in Figure 40, to satisfy the EMI standards, a certain value of the time horizon $T_{kw_i} = T_{kw_s} + \Delta T_{kw} f(w_m t)$ that causes EMI mitigation is calculated and applied to the PES. The new value of T_{kw_i} is used in the online cost function $C(\alpha_{kn}, T_{kw})$ which is minimized with respect to α_{kn} only to maintain voltage regulation. The cases will be described in more detail in the following subsections.

3.1.4. Online prediction model (Mode 1 and Mode 2)

For fast real-time execution of the SBC, an online prediction model of the PES is synthesized that closely matches

the dynamics of the full-scale PES model used by the reachability analysis. The prediction model is synthesized using a discrete map of the PES, which is obtained by combining the individual maps corresponding to each of the switching states. If the PES has h switching states in a reachable switching sequence, the discrete prediction model for the $i+1$ sample can be synthesized as in (35), where $\hat{A}_{knd}$ and $\hat{B}_{knd}$ are the reduced-order PES and are derived similar to the process followed in Chapter 2:

$$\hat{x}(i+1) = \hat{A}_{knd}\hat{x}(i) + \hat{B}_{knd} \tag{35}$$

3.1.5. Cost function formulation (Mode 1 and Mode 2)

Next, a cost function, denoted by $C(\alpha_{kn}, T_{kw})$ is formulated and an optimal control problem is solved online to perform online performance control of the PES. The online optimization problem determines α_{kn} and T_{kw} that minimizes the following cost function:

$$C(\alpha_{kn}, T_{kw}) = (\hat{x}^* - \hat{x}(i+1))^T P(\hat{x}^* - \hat{x}(i+1)) \tag{36}$$

given the constraints on PES states and bounds on α_{kn} and T_{kw}. In (36), P is a positive-definite matrix that provides scaling of the terms in the cost function. The optimization problem yields reachable switching sequences with optimal values of α_{kn} and T_{kw} (i.e., $\alpha_{kn_{opt}}$, and $T_{kw_{opt}}$) that are fed to the PES power stage.

3.1.6. Observer design (Mode 1 and Mode 2)

Finally, if full-state feedback is not possible to preclude the need for a plurality of sensors for a higher-order PES, a closed-loop state observer needs to be synthesized. If $\bar{\hat{x}}$ are the observed PES states, the expression for the closed-loop observer is given for the (i+1) discrete sample by:

$$\bar{\hat{x}}(i+1) = \overline{\hat{A}_{knd}}\bar{\hat{x}}(i) + \overline{\hat{B}_{knd}} \tag{37}$$

where $\overline{\hat{A}_{knd}}$ and $\overline{\hat{B}_{knd}}$ are derived similar to the process in Chapter 2.

3.1.7. Constraints in SBC (Mode 1 and Mode 2)

Controllers [15], [19], [22], [24], [27], [81]–[83] that solve an optimal-control problem like SBC, minimize cost functions as shown in Section 3.1.5, based on constraints and compute α_{kn} and T_{kw}. The constraints can be set on individual PES states like voltage, currents etc. as in the form $\hat{x}(i) \leq x_{max}$, where x_{max} denotes the limit set on the

PES voltages, currents, or duty cycles. In this paper, constraints have been used to reduce the PES DM and CM EMI peaks below EMI standards as follows:

(1) For a generalized PES, the DM input current, which mainly contributes to the DM EMI peaks is used to create the DM EMI model. Similarly, the drain-to-source transitions of the PES devices that impact the charging the various parasitic capacitances of the PES set-up are used to form the CM EMI model;

(2) For a PES operating in steady state with a time horizon T_{kw_s}, (or constant switching frequency $T_{kw_s}^{-1}$) the DM/CM current waveforms can be expressed as periodic time series (shown in Appendix H) with C_{n_1} as the magnitude of the $n_1{}^{\text{th}}$ harmonic of $T_{kw_s}^{-1}$. For this $n_1{}^{\text{th}}$ harmonic, if C_{n_1} is below the limiting harmonic peak $C_{EMI_{n_1}}$ of the CISPR/EN 55022/32 Class-A EMI standard [65] (that is, $C_{n_1} < C_{EMI_{n_1}}$), then T_{kw_s} is not changed;

(3) However, if $C_{n_1} > C_{EMI_{n_1}}$ for the $n_1{}^{\text{th}}$ harmonic, then, a new time horizon T_{kw} is chosen that reduces PES EMI. It has already been established in Figure 39, how two different SSs having different time horizons can lead to different EMI levels for a PES.

It is ensured that for EMI peaks corresponding to the new time horizon T_{kw} (say $C_{n_{1_{new}}}$, detailed in Appendix H), $C_{n_{1_{new}}} < C_{EMI_{n_1}}$ is satisfied. The synthesis of this new time horizon T_{kw} is based on the basic principle laid forth by Van der Pol in [84], which demonstrates that when the frequency (inverse of the time horizon i.e. T_{kw}^{-1}) of a signal, such as the DM/CM current in the present case, is periodically modulated, the individual spectral peaks of the original signal are reduced.

Figure 41 shows the synthesis of this new T_{kw} for our case. It starts from a time horizon T_{kw_s} (or frequency $T_{kw_s}^{-1}$), spans a certain time horizon ΔT_{kw} (or frequency ΔT_{kw}^{-1}) on either side of T_{kw_s}, and comes back to T_{kw_s}. The periodicity of the T_{kw}^{-1} is taken as a sinusoid for ease of implementation. If the new time horizon T_{kw} contains h_1 switching states, the net reduction of the spectral peaks obtained depends on the values of T_{kw}, the depth ΔT_{kw}, and $\frac{T_{kw}}{h_1}$ [84]. All of these three parameters are shown in

Figure 41, while Appendix H briefly shows the mathematical formulation for the method and calculation of EMI peaks C_{n_1} and $C_{n_{1_{new}}}$.

Figure 42 shows the algorithm for online EMI mitigation. Depending on the present operating condition, and using an optimal framework, SBC calculates the EMI peaks of the PES using a DM/CM internal prediction model. If the

peaks violate the standards, SBC calculates the new values of T_{kw}, the depth ΔT_{kw}, and $\frac{T_{kw}}{h_1}$, that can reduce PES EMI below the EMI standards, and applies this time horizon to the hardware PES. Subsequently, once the new T_{kw} to meet the EMI standards is fixed, SBC minimizes cost function $C(\alpha_{kn}, T_{kw})$ given in (2) to find the optimal α_{kn} in the steady state. For any operating condition variation, the EMI peaks are recalculated, and the process repeats using the algorithm shown in Figure 42.

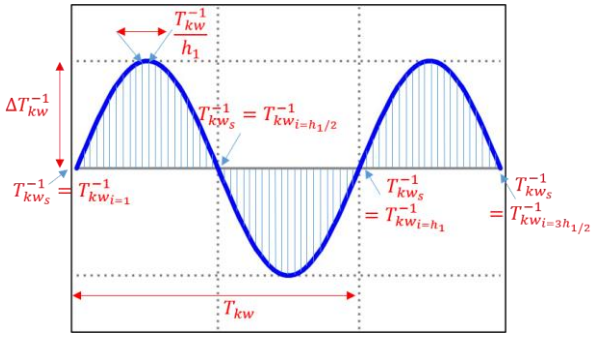


Figure 41. Figure showing how T_{kw} is formed in steady state to reduce EMI spectrum.

3.2. SBC implementation for EMI mitigation of Ćuk PES

For SBC, first, a full-scale model of the Ćuk PES is synthesized offline that is used to perform a reachability analysis as elucidated in Section 3.1.2 to come up with a stable range of α_{kn} and T_{kw} that can be used to solve the real-time SBC problem.

Next for the real-time part, Section 3.1.3 was followed for the PES. The real-time SBC problem is formulated for the Ćuk PES into two-steps as depicted in Mode 1 and Mode 2. The detailed case illustration for Mode 1 for the Ćuk PES, along with the non-linear state observer design is depicted in [2], which encompasses cost function formulation and observer design guidelines for the PES up to the steady state. During the steady state, the cost-function is modified as follows:

$$C_{Mode-1}(\alpha_{kn}, T_{kw}) = \gamma_1 C_{vreg}(\alpha_{kn}, T_{kw}) + \gamma_2 \left(\Delta\alpha_{kn}(i)\right)^2 + \gamma_3 (\Delta T_{kw}(i))^2 \tag{38}$$

$$C_{Mode-2}(\alpha_{kn}, T_{kw}) = \gamma_1 C_{vreg}(\alpha_{kn}, T_{kw}) + \gamma_2 \left(\Delta\alpha_{kn}(i)\right)^2 \tag{39a}$$

where $$C_{vreg}(\alpha_{kn}, T_{kw}) = (G_p \left(V_{ref} - V_{out}(i)\right) + G_I \sum_j \left(V_{ref} - V_{out}(i)\right) T_{kw} - iL_1(i))^2 \tag{39b}$$

where the terms $IL_{ref}, V_{ref}, V_{out}(i), iL_1(i)$ denote the input PES inductor current and output voltage references, output

sensed voltage, and predicted inductor current sample, respectively. The weight-tuning factors $\delta_1, G_p, G_I, \gamma_1, \gamma_2$ and γ_3 have all been synthesized based on guidelines defined in [2], [8], [51], [53]. Leading up to the steady state, SBC finds α_{kn}, and T_{kw} to make $\Delta C_{Mode-1}(\alpha_{kn}, T_{kw}) < 0$. During steady-state SBC synthesizes T_{kw} depending on EMI

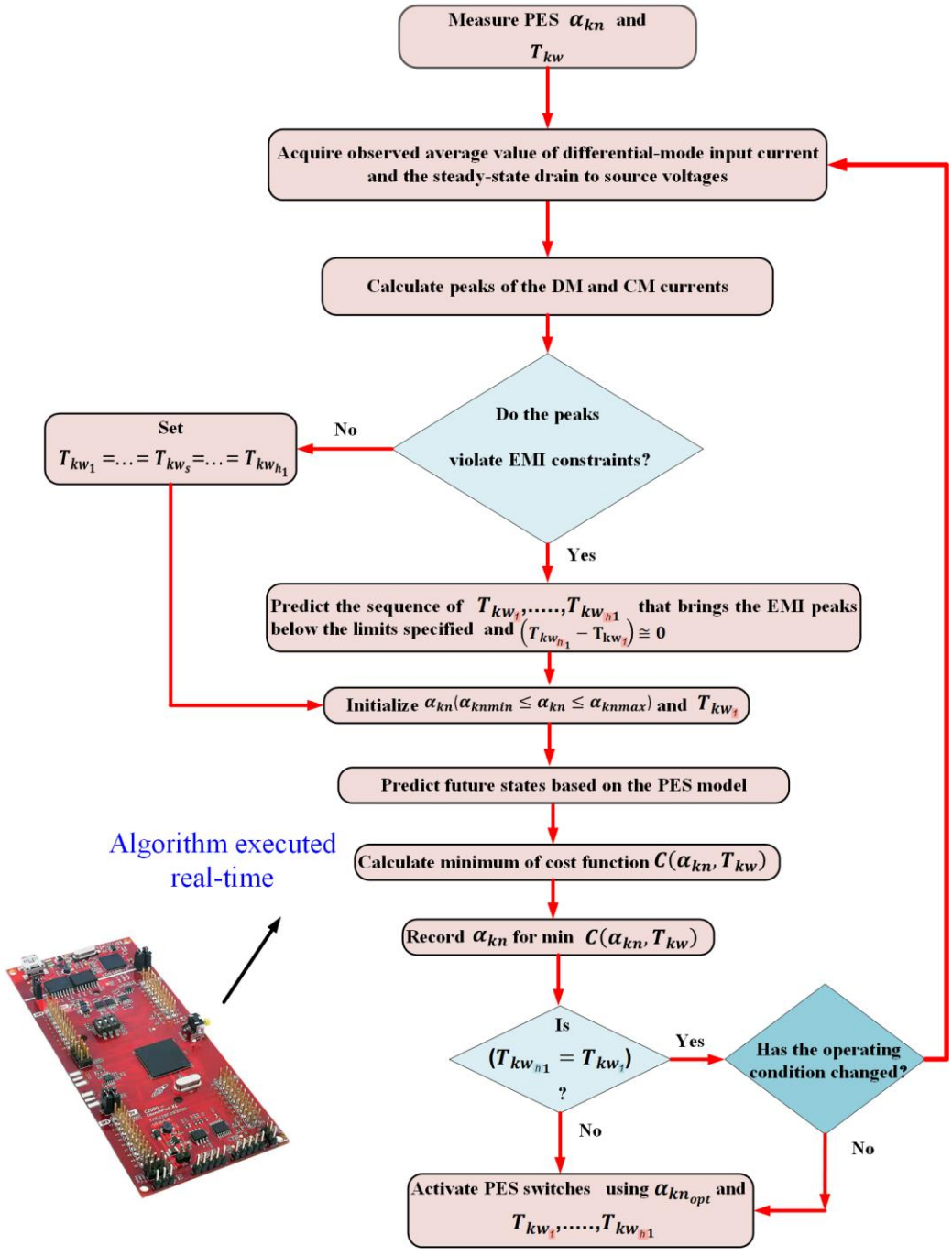


Figure 42. The online SBC algorithm that performs conducted-EMI mitigation.

mitigation, while $C_{Mode-2}(\alpha_{kn}, T_{kw})$ is minimized with respect to α_{kn} to maintain PES voltage regulation.

During the steady state in Mode 2, SBC synthesizes EMI-mitigating sequences, following the constraints on the EMI standards as delineated in Section 3.1.7. This helps in autonomous reduction of conducted EMI peaks of the PES. However, due to T_{kw} variation, the output voltage of the power supply gets affected negatively. Due to the low-frequency variation of the time horizon (T_{kw}) introduced by the SSs in steady state to reduce EMI, low-frequency harmonics are reflected in the output voltage. This results in output voltage deviation from the steady state value if SBC is applied without output voltage regulation. Hence, in steady state, SBC minimizes the cost objective $C_{Mode-2}(\alpha_{kn}, T_{kw})$ to keep the low-frequency deviation within bounds. Figure 43 explains the scenario by considering two consecutive SSs with different time horizons $T_{kw_{i+1}}$ and $T_{kw_{i+1}}$. Due to $T_{kw_{i+1}} > T_{kw_i}$, the output voltage ripple falls further for the 2nd SS leading to a drop in average output voltage (say $V_{out_{avg}}$). To avoid this droop, SBC provides a steady-state correction $\Delta\alpha_{ki}T_{kw_i}$ by minimizing (4b) to prevent output voltage deviation.

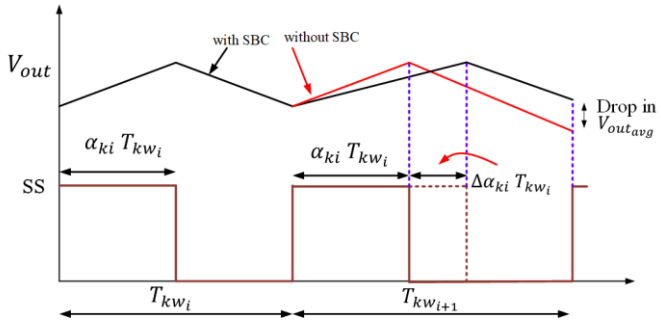


Figure 43. Steady-state correction $\Delta\alpha_{ki}T_{kw_i}$ provided by SBC using cost function (39) to reduce low-frequency output-voltage fluctuation due to time horizon variation for EMI mitigation.

3.2.1.DM EMI model synthesis for constrained optimal control

The CM- and DM-noise propagation paths of the Ćuk PES are shown in Figure 44. It shows the equipment under test (EUT) (i.e., the Ćuk PES), any CM and DM filters that may be used for adhering to industrial EMI standards (CISPR/EN 55022/32 Class A and Class B conducted emissions for this case) and the LISN circuit which separates the EMI of the PES from the input power supply. The conducted CM noise generated by the GaN-FET transitions flows into the ground via the parasitic capacitances, and then picked up by the R_{LISN1} resistors back to the GaN FETs. The main DM noise path is highlighted in red, while the CM noise paths have been highlighted in green.

The EMI measurements are taken using two LI-325C LISNs, named LISN1 and LISN2. The LISN circuits have also been delineated in Figure 44. In the LISN circuit, $L_{LISN1} = L_{LISN2} = 5\ \mu$H, C_{LISN1} =0.1 μF, $C_{LISN2} = 1\ \mu$F and

$R_{LISN1} = R_{LISN2} = 50\ \Omega$. Over the frequency range of the EMI standards, $L_{LISN1}$and L_{LISN2} and C_{LISN1} and C_{LISN2} which are close to line to neutral (LN) in Figure 44 are open circuits for LN; and the source V_{in} allows dc current to pass through to the PES. The other set of C_{LISN1} and C_{LISN2} close to the PES gives short circuit to the DM current and

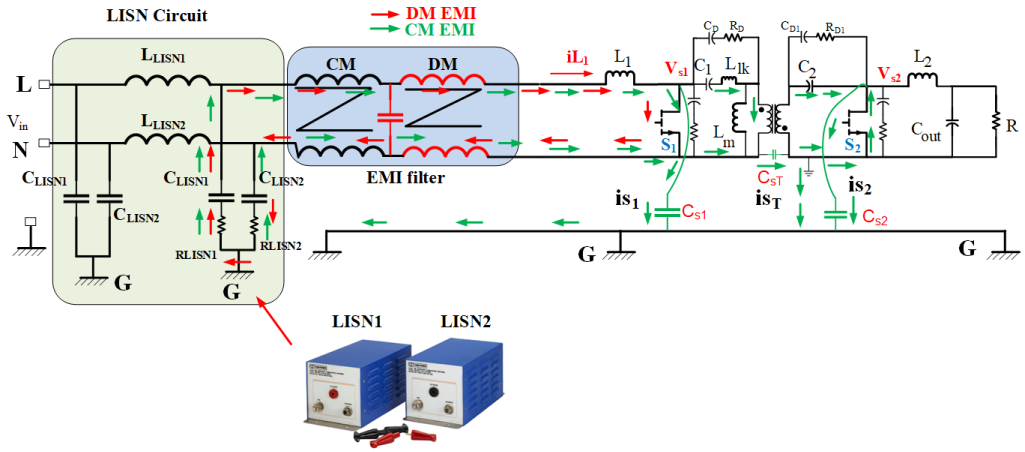


Figure 44. The CM and DM EMI propagation paths of the Ćuk PES is shown with the LISN circuit.

hence, impedances seen by the EUT between LG and NG (where G denotes ground/earth in Figure 44 are R_{LISN1} and R_{LISN2}.

To derive the EMI peaks for DM and CM noise, the EMI filter in Figure 44 is neglected. Now, in the Ćuk PES, the (DM) triangular input current that mainly contributes to the DM EMI peaks is used for the DM model and is predicted by the closed-loop state observer as described in Section 3.1.6. The input inductor current is denoted by $iL_1(t)$ which consists of an average component (iL_{avg}) and a high-frequency ripple component ($\Delta iL_1(\mathrm{t})$), as illustrated in Figure 45.

The DM input noise is primarily attributed to this time-varying ripple component ($\Delta iL_1(\mathrm{t})$), which can be written in the form of a Fourier series as follows:

$$\Delta iL_1(t) = \sum_{n_1=1}^{\infty} C_{dm} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} \tag{40}$$

where

$$C_{dm} = \Delta iL_{pp} * \frac{|sin(\pi n_1 \alpha_{kn})|}{n_1^2 \pi^2 \alpha_{kn}(1-\alpha_{kn})} \tag{41}$$

In (40) and (41), C_{dm} is the amplitude of the n_1^{th} harmonic component of the DM EMI spectrum and ΔiL_{pp} is the magnitude of the peak-to-peak inductor-current ripple for particular operating conditions, also highlighted in Figure

45. As discussed in Section 3.1.7, when the DM peaks (C_{dm} in (5)) of the Ćuk PES exceed the DM EMI standards [65] (say $C_{EMI_{dm}}$) i.e., $C_{dm} > C_{EMI_{dm}}$, a new SS with a time horizon $T_{kw} \in \{T_{kw_i}, \dots T_{kw_s}, \dots, T_{kw_{h_1}}\}$ that can minimize the DM peaks of the Ćuk PES below the EMI standards is chosen and applied to the PES. With this new SS, $\Delta iL_1(t)$ gets modified as follows:

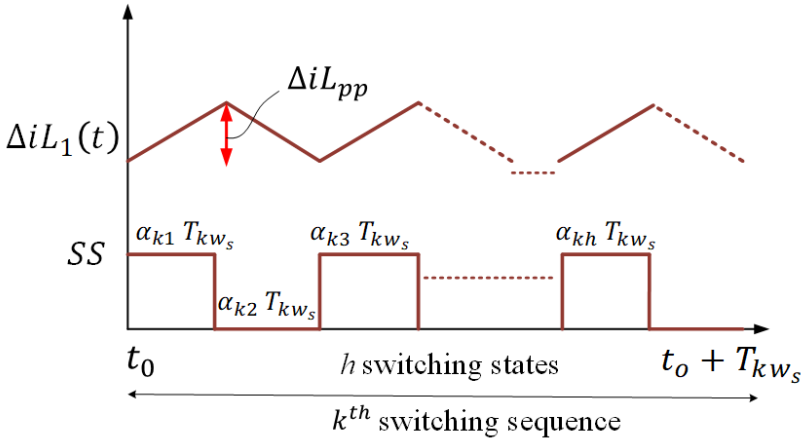


Figure 45. Figure showing the steady-state SS without DM EMI peak reduction and the corresponding $\Delta iL_1(t)$ in (40).

$$\Delta iL_{1_{new}}(t) = \sum_{n_1=0}^{\infty} \sum_{m_1=-\infty}^{\infty} C_{dm_{new}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1} + m_1 T_{kw}^{-1}\right)t)} \quad (42)$$

where $C_{dm_{new}}$ are the reduced amplitudes of peaks of the DM EMI spectrum with the new T_{kw}. The derivation of $C_{dm_{new}}$ and the abbreviations used in (42) used have been derived and defined in Appendix H. Figure 46 shows $\Delta iL_{1_{new}}(t)$ with the new SS that performs EMI mitigation.

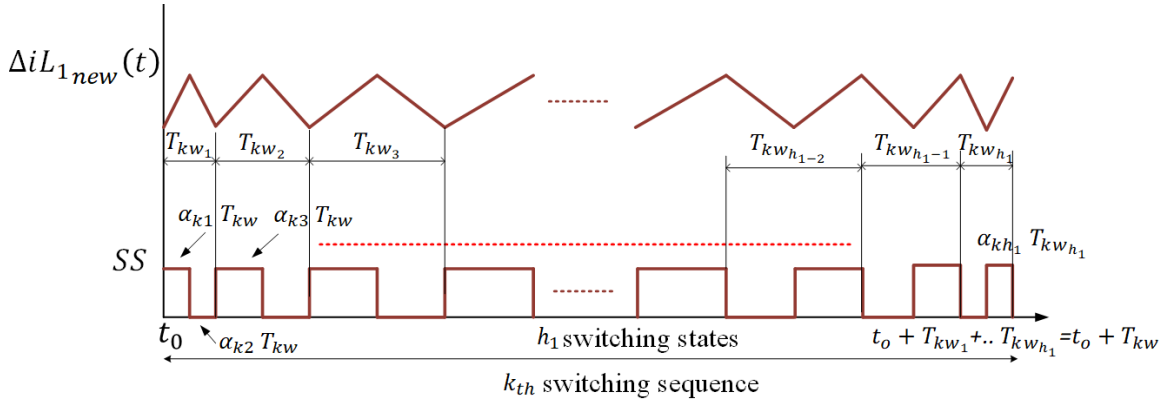


Figure 46. Figure showing the new SS to reduce the DM EMI peak and the corresponding $\Delta iL_{1_{new}}(t)$ in (42).

3.2.2. Physical DM EMI model synthesis considerations for actual hardware PES

To begin with, in the GaN-FET-based hardware prototype, the parasitic in the path of the DM current are not all accounted for while modelling the PES. The PES model precludes, for instance, high-frequency DM leakage inductances and PCB trace inductances some of which have been lumped together and shown as $L_{LK_{1,2,..,4}}$ in Figure 47a. Hence, the DM peaks predicted based on the online PES model, may deviate from those obtained using the actual hardware prototype. However, it happens at very high frequencies since $L_{LK_{1,2,..,4}} \ll L_1$, and the DM EMI in the sidebands of the PES switching frequency is dominated by the inductor L_1. (since $L_1 + L_{LK_{1,2,..,4}} \cong L_1$). As illustrated in in Figure 47b, the DM EMI peaks of a PES violate the EMI standards in the vicinity of the switching frequency (lower-order harmonics of the switching frequency) where the DM peaks can be calculated with reasonable accuracy and the effect of the parasitic $L_{LK_{1,2,..,4}}$ inductances on the DM EMI peaks are negligible. Hence, since the DM harmonics due to parasitic $L_{LK_{1,2,..,4}}$ dominate the spectrum around the higher order of the switching frequency, they are not considered for prediction purposes.

We perform sensitivity analysis in hardware set-up on this assumption and thereby attempt to validate experimentally, that by the reduction of the DM EMI peaks in the proximity of the lower order switching sidebands, the DM EMI standards can be satisfied. Moreover, the inductor L_1 does not remain fixed in actual hardware prototype across wide operating power and varies depending on the dc bias or the average input inductor current $\overline{\imath L_1(t)}$. The state observer in Section 3.1.6 predicts $\overline{\imath L_1(t)}$ and corrects the value of L_1 used in the online prediction model in real-time.

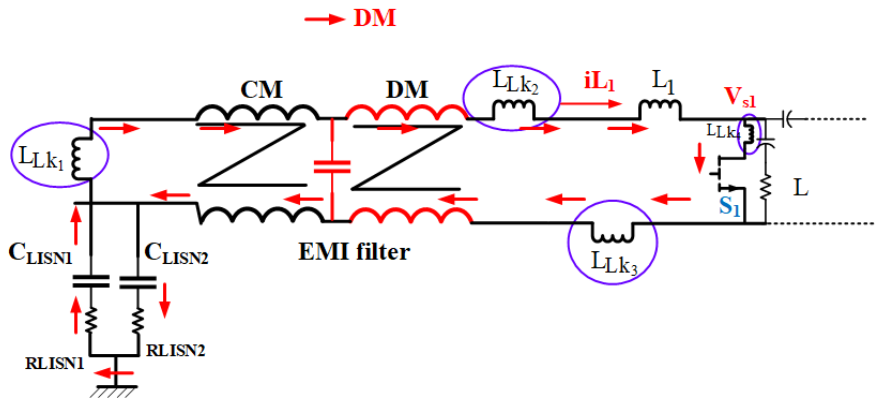
Yet another issue pertains to the finite deadtime associated with the GaN-FET based complementary devices of the Ćuk PES. Hence, if the time allocated to a switching state in a SS is α_{kn}, then considering the deadtime, the allocation becomes $\alpha_{kn} - \delta_{deadtime}$. This affects the DM EMI peak prediction since the peaks predicted by (41) depend on the value of α_{kn}. Any modern industrial processor has deadtime modules and hence $\delta_{deadtime}$ is preset and known in advance. Hence, the above-mentioned steps were incorporated for better DM EMI prediction.

3.2.3. CM EMI model synthesis for constrained optimal control

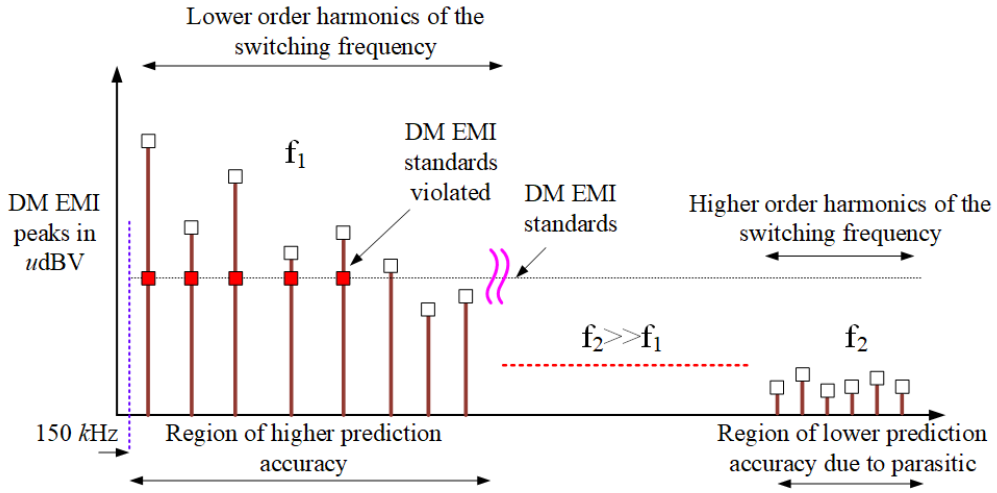
Unlike the DM current, the CM currents have more indeterministic coupling paths. Hence, to synthesize a CM PES

model that can predict the CM peaks with reasonable accuracy, yet is simple enough for real-time optimal control, an analytical model is created for the main CM coupling paths, which have been shown in Figure 44 for the isolated Ćuk PES under consideration.

Two primary CM noise sources are primary (S_1) and secondary (S_2) GaN FETs. The drain-to-source voltages of the GaN FETs are denoted by V_{s_1} and V_{s_2}. The dv/dt caused by the FET switching transition charges the parasitic



(a)



(b)

Figure 47. Illustrations of (a) high-frequency parasitic that have not been considered for DM EMI model and (b) region in the DM EMI spectrum of the PES that violates the DM EMI standards.

capacitances (say C_{s_1} and C_{s_2}, respectively) between the drain of the FET and the earth (G in Figure 44) and this, in essence, constitutes the CM noise. The stray capacitance is mainly formed between the drain of the device and heatsink, as the insulating materials have considerable dielectric constant.

Another major CM EMI source is the parasitic interwinding capacitances between the primary and secondary windings of the transformer. In the Ćuk PES, as shown in Figure 8, the voltages on primary and secondary sides of the transformer are denoted by V_{T_p} and V_{T_s}, respectively. For non-unity turns ratio of the HF transformer and unequal voltage distribution across the windings, the switching transition of $V_{T_p} - V_{T_s}$ charges the interwinding capacitance to cause a displacement current from the primary to the secondary side of the transformer and the earth.

Figure 48 shows a typical transformer structure where the primary and secondary sides have N_p and N_s turns and P_n and S_m layers, respectively. Due to the voltage difference between layer P_n and layer S_1, the interwinding

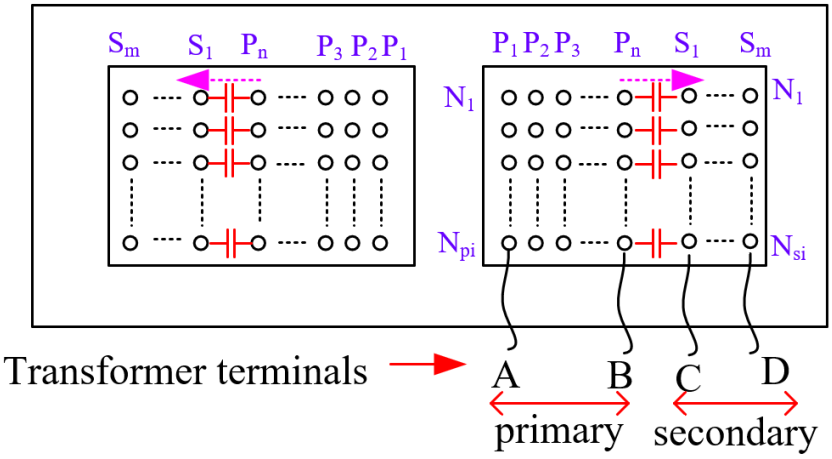


Figure 48. A typical HF transformer structure with the parasitic interwinding capacitance that results in CM noise.

capacitance between these two layers will result in a displacement current that can be written as $i_{S_T} = C_{dis}\,(N_{p_n} - N_s/N_{s_1})/2N_p\; dV_{T_p}/dt = C_{s_T}\; dV_{T_p}/dt$, where C_{dis} are the discrete capacitances between the primary layer P_n and secondary layer S_1, N_{p_n} and N_{s_1} are the number of turns in layer P_n and layer S_1, and $C_{dis}\,(N_{p_n} - N_s/N_{s_1})/2N_p$ is the total lumped inter-winding capacitance. These three-time varying voltages V_{s_1}, V_{T_p} and V_{s_2}, shown in Figure 13, are the major contributors to the CM noise spectrum of the PES. Figure 49 also shows the first derivatives of these time-varying voltages, which cause three CM currents i_{s_1}, i_{s_2}, and i_{s_T}. The currents, expressed as $i_{s_1} = C_{s_1}\; dV_{s_1}/dt$, $i_{s_2} = C_{s_2}\; dV_{s_2}/dt$, and $i_{s_T} = C_{s_T}\; dV_{T_p}/dt$, have been shown in Figure 44. Since V_{s_1}, V_{T_p}, and V_{s_2} are all periodic, their derivatives which lead to the CM currents i_{s_1}, i_{s_2} and i_{s_T} are also periodic and can be expressed using Fourier series like DM noise for peak prediction. The CM capacitors C_{s_1}, C_{s_T}, and C_{s_2} are usually very small in tens of pF and can be computed in detail by an impedance analyzer or using printed-circuit-

board modeling for a given PES. References [73], [85] highlight some of the peak-prediction procedure for CM EMI, by modeling PES in considerable detail. But, for our present application, such detailed models cannot be easily used in industrial digital signal processors (DSPs). Hence, we use some practical PES behavioral considerations and weave fine a data driven-analytical approach to predict CM noise for our application.

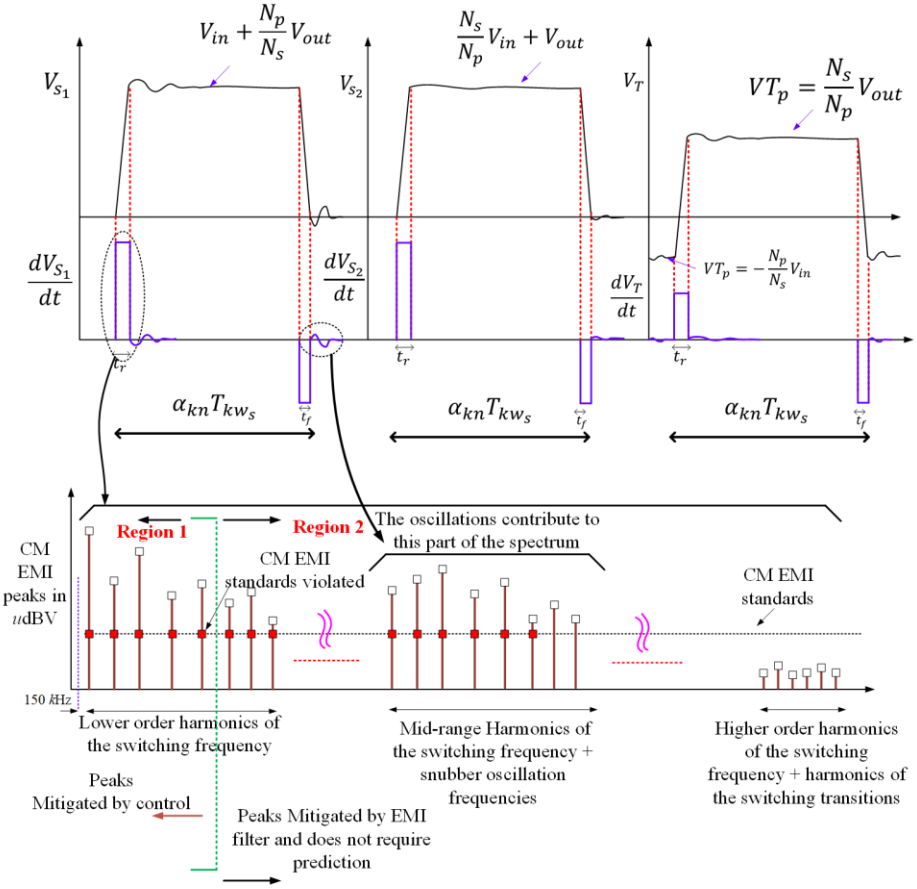


Figure 49. Figure showing the switching voltages of the Ćuk PES that mainly contribute to CM EMI. Also, the regions in the CM EMI control are shown.

3.2.4. Physical CM EMI model synthesis considerations for actual hardware PES

Figure 49 shows the CM EMI spectrum, with the typical V_{s_1}, V_{T_p} and V_{s_2} of a Ćuk PES. The CM EMI spectrum consists of the switching-frequency components, the frequency components due to parasitic oscillations caused by the leakage of the transformer discharging into the device capacitance that rides on the V_{s_1}, V_{T_p} and V_{s_2} signals. It also consists of the frequency components induced by the switching transition of the GaN FETs. Even though the main paths of the CM EMI have been highlighted, the CM current can find indeterministic paths to the earth (G, shown in

Figure 44) and hence, the spectra cannot be predicted with accuracy all the way to the switching-transition components without exact knowledge of the practical-PES model.

In the CM EMI spectrum shown in Figure 49, it is observed that the CM EMI standards for the Ćuk PES are violated for lower-order harmonics of the switching frequency and in the mid-range frequencies due to the parasitic oscillations induced by transformer leakage. So, for the case under consideration, the peaks in the lower-order harmonics are predicted and mitigated by control. We denote this region as Region 1. All the mid-range and higher-order peaks are mitigated by designing a CM EMI filter by observing the experimental peaks in a spectrum analyzer during experimentation; hence, they will not be predicted. We denote this region as Region 2. By mitigating the lower-order CM EMI peaks using control, the frequencies at which the CM EMI standards are violated are pushed to the higher end of the spectrum, which thereby reduces the size of the CM EMI filter.

Now, the CM current for the PES can be written in the form:

$$i_{CM_{total}} = i_{s_1} + i_{s_2} + i_{s_T} \tag{43}$$

$$= C_{s_1}\frac{dV_{s_1}}{dt} + C_{s_2}\frac{dV_{s_2}}{dt} + C_{s_T}\frac{dV_{T_p}}{dt} \tag{44}$$

In (44), dV_{s_1}/dt, dV_{s_2}/dt, and dV_{T_p}/dt are periodic waveforms, and hence $i_{CM_{total}}$ can be written in terms of a Fourier series as

$$i_{CM_{total}} = \sum_{n_1=1}^{\infty} C_{cm_{V_{s_1}}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} + \sum_{n_1=1}^{\infty} C_{cm_{V_{s_2}}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} + \sum_{n_1=1}^{\infty} C_{cm_{V_{s_T}}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} \tag{45}$$

$$= \sum_{n_1=1}^{\infty} C_{cm} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} \tag{46}$$

In (45), $C_{cm_{V_{s_1}}}$, $C_{cm_{V_{s_2}}}$ and $C_{cm_{V_{s_T}}}$ are the CM EMI peaks due to dV_{s_1}/dt, dV_{s_2}/dt, and dV_{T_p}/dt and in (46), $C_{cm} = C_{cm_{V_{s_1}}} + C_{cm_{V_{s_2}}} + C_{cm_{V_{s_T}}}$. Here the process of derivation of only $C_{cm_{V_{s_1}}}$ is delineated and the derivations of $C_{cm_{V_{s_2}}}$ and $C_{cm_{V_{s_T}}}$ are similar.

From Figure 49, one observes that V_{s_1} transits between zero and the value given by $V_{in} + N_p/N_s V_{out}$. Hence, if the rising and falling edges of V_{s_1} are given by t_r and t_f, then, the function $C_{s_1}\, dV_{s_1}/dt$ can be written as $C_{s_1}\frac{V_{in}+\frac{N_p}{N_s}V_{out.}}{tr}$ between zero to t_r, zero in between t_r to $\alpha_{kn}T_{kw_s} - t_f$, $C_{s_1}\frac{V_{in}+\frac{N_p}{N_s}V_{out.}}{t_f}$ between $\alpha_{kn}T_{kw_s} - t_f$ to $\alpha_{kn}T_{kw_s}$, zero in between $\alpha_{kn}T_{kw_s}$ to T_{kw_s}. Hence, the periodic function can be broken down into Fourier components and the peaks

of $C_{s_1}\, dV_{s_1}/dt$ denoted by $C_{cm_{V_{s_1}}}$ are expressed by the following:

$$C_{cm_{V_{s_1}}} = \sqrt{A^2_{cm_{V_{s_1}}} + B^2_{cm_{V_{s_1}}}} \tag{47a}$$

$$A_{cm_{V_{s_1}}} = \frac{(2\left(\left(T_{kw_s} a_2\left(\frac{\sin(y)}{T_{kw_s}}\right) - \frac{\sin\left(t_f + y\right)}{T_{kw_s}}\right)\right)}{2\pi p_1} + z)/T_{kw_s} \tag{47b}$$

$$B_{cm_{V_{s_1}}} = \frac{-(2\left(\left(T_{kw_s} a_2\left(\frac{\cos(y)}{T_{kw_s}}\right) - \frac{\cos\left(t_f + y\right)}{T_{kw_s}}\right)\right)}{2\pi p_1} - z)/T_{kw_s} \tag{47c}$$

$$y = 2\pi n_1\left(t_r + T_{kw_s}\alpha_{kn}\right), \tag{47d}$$

$$a_1 = C_{s_1}\frac{V_{in} + \frac{N_p}{N_s}V_{out}}{tr},\ a_2 = C_{s_1}\frac{V_{in} + \frac{N_p}{N_s}V_{out}}{t_f} \tag{48e}$$

$$z = \frac{T_{kw_s} a_1 \sin((2\pi n_1 t_r)/T_{kw_s})}{2 n_1 \pi} \tag{48f}$$

Even though C_{s_1}, C_{s_T}, and C_{s_2} can be calculated via use of impedance analyzer and PCB modeling based approaches [86], the process can prove tedious for different hardware setups and transformers. Hence, an easier experimental data-driven approach is used here for estimating the parasitic capacitances. For different V_{in} and V_{out} of the Ćuk PES, obtained for the experimental PES hardware using a spectrum analyzer, the real-time peaks of the CM EMI are measured. Let the experimental peaks be denoted by $C_{cm_{exp_i}}$ and the ones calculated from analytical model be C_{cm_i}. Now, using the simple algorithm delineated in

Figure 50, we tune the values of C_{s_1}, C_{s_T} and C_{s_2} that minimizes the function ($|C_{cm_{expi}} - C_{cm_i}|$). As shown in

Figure 50, the order of the harmonic n_1 for the CM spectrum up to which the EMI peaks will be mitigated by control is chosen such that the error in the prediction of these peaks is below a programmable pre-defined threshold ε.

Finally, following the methodology in Section 3.1.7, when the CM peaks (of the Ćuk PES) C_{cm} in (46) exceed the amplitudes ($C_{EMI_{cm}}$) of the CM harmonics specified by the EMI standards [65] (i.e., $C_{cm} > C_{EMI_{cm}}$), a new SS with a time horizon $T_{kw} \in \{T_{kw_1}, \ldots T_{kw_s}, \ldots, T_{kw_{h_1}}\}$ that can minimize the CM peaks to an acceptable level are chosen. When the new SS is applied, $i_{CM_{total}}$ modifies to the following form:

$$i_{CM_{total_{new}}}(t) = \sum_{n_1=0}^{\infty}\sum_{m_1=-\infty}^{\infty} C_{cm_{new}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1} + m_1 T_{kw}^{-1}\right)t)} \tag{49}$$

where $C_{cm_{new}}$ are the reduced amplitudes of peaks of the CM EMI spectrum. Derivation of $C_{cm_{new}}$ and the abbreviations used in (49) have been provided in Appendix H.

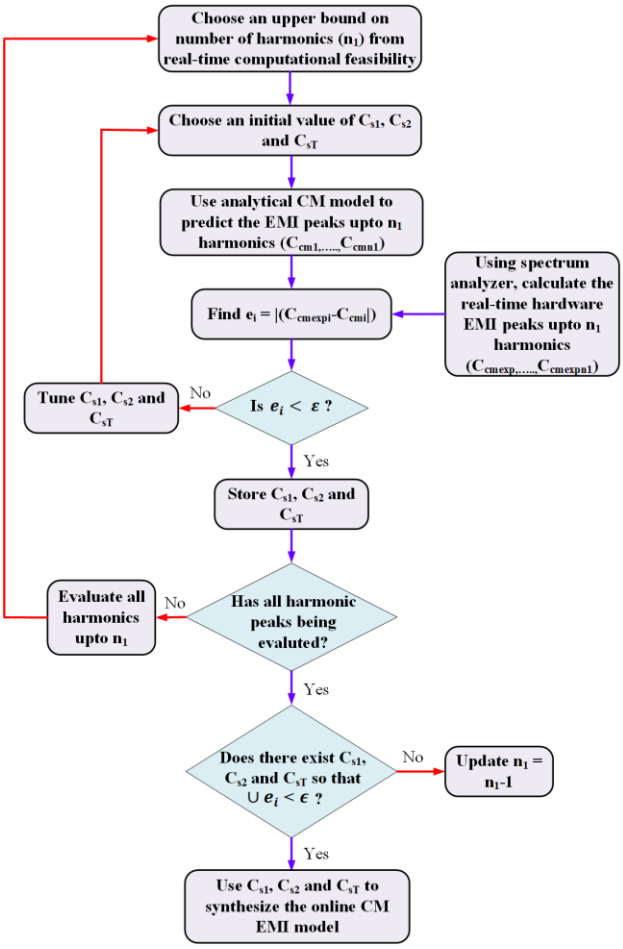


Figure 50. The offline algorithm in MATLAB to compute the value of common mode capacitors C_{s_1}, C_{s_T} and C_{s_2} based on expe rimental data. ε denotes a programmable pre-defined threshold.

3.3. Results

The section is organized as follows:

(1) First, the hardware set-up is explained in Section 3.3.1.

(2) Then, Section 3.3.2 delineates the time-domain experimental validation of the proposed approach in controlling the PES in terms of the steady state and transient waveforms. In Mode 1, SBC synthesizes switching sequences that guide the PES to steady state, and in Mode-2 does steady-state regulation and EMI mitigation.

(3) Section 3.3.3 shows how SBC autonomously mitigates the DM EMI, and its effect on the DM filter size in the

PES.

(4) Section 3.3.4 shows CM EMI mitigation and the subsequent CM EMI size reduction.

(5) Finally, it is experimentally demonstrated in Section 3.3.5 how the EMI mitigating SBC affects PES efficiency compared to traditional EMI filter losses. It also shows SBC based low-frequency distortion control results.

3.3.1. Hardware prototype and set-up description:

The hardware prototype consisting of the higher-order GaN-FET based Ćuk-PES is shown in Figure 51a. The PES hardware prototype is used to perform the EMI experiments using the set-up depicted in Figure 51b and Figure 51c.

The SBC algorithm is implemented on a low-cost dual-core TMS320F28379D digital signal processor (DSP) (LaunchXL-F28379D) using code composer studio version 8, and the switching sequence, with the allocated switching states (α_{kn}) and time horizon (T_{kw}), is used to drive the GS66508B GaN-FET-based Ćuk-PES operating at the

Table 2. The Power-stage-Parameters for the Ćuk-PES

Input voltage range (V_{in})	Output voltage range (V_{out})	Input inductance (L_1)	Output inductance (L_2)	Input capacitance (C_{in})	Output capacitance (C_{out})	Input blocking capacitance (C_1)	Output blocking capacitance (C_2)	Switching frequency ($1/T_s$)	Transformer turns ratio (N)
30-60 V	0-90 V	50 μH	100 μH	4.4 μF	5 μF	6. 8 μF	1.5 μF	100-250 kHz	2

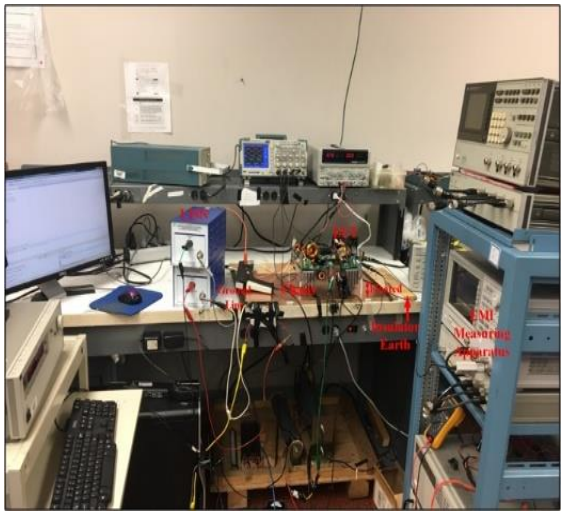
maximum power of 350 W. The power-stage parameters used are provided in Table 2. The detailed hardware design is discussed in [33]. The PCB layout in terms of the power, control and gate loops have been further optimized, than that discussed in [33], to minimize stray CM EMI noise. The EMI measurements are taken using LI-325C LISNs and 4395A Agilent Network/ Spectrum/ Impedance Analyzer. The set-up is implemented taking into consideration CISPR/EN 55022/32 Class A and Class B conducted emissions measuring standard.

3.3.2. PES autonomous EMI mitigation

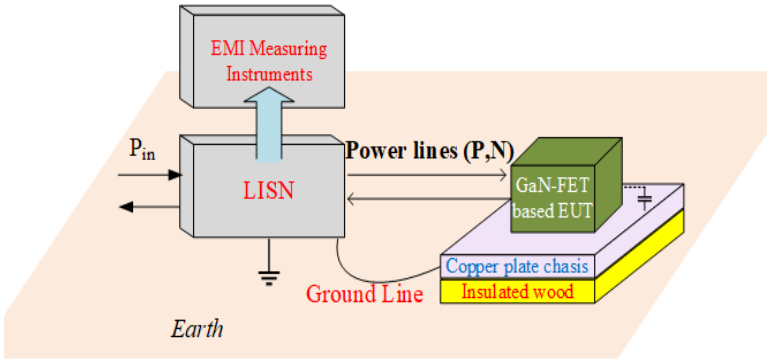
The online SBC consists of two parts:

(1) Mode 1-operation during transient operation leading up to the steady state where SBC determines the switching

(a)



(b)



(c)

Figure 51. (a) The PCB realization of the GaN-FET-based Ćuk-PES. (b) The PES experimental set-up for performing the EMI tests. (c) Set-up for

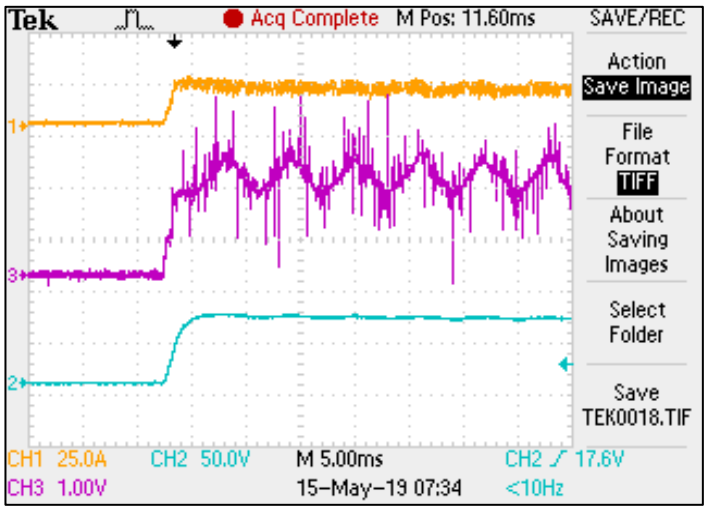
conducted emission measurement.

states (α_{kn}) and time horizon (T_{kw}) on the fly via minimization of the cost function defined in (38a).

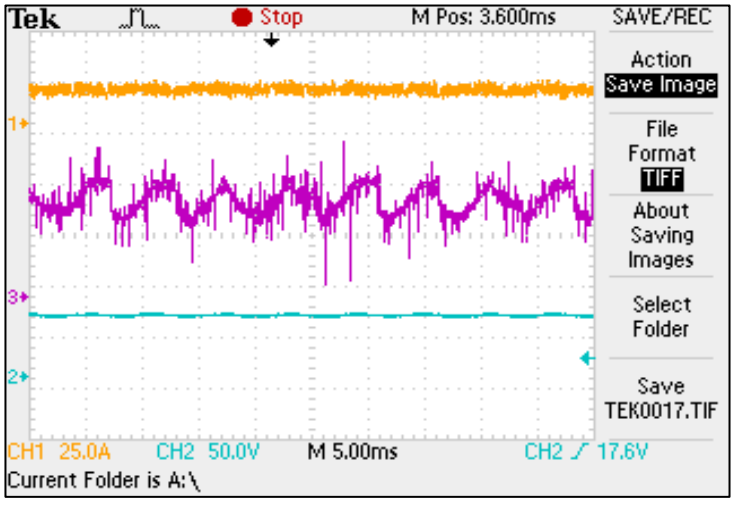
(2) Mode 2-operation in the steady state. Here the switching states (α_{kn}) of the switching sequence are synthesized to perform voltage regulation via minimization of the cost function defined in (38b), while $T_{kw} \in \{T_{kw_1}, \ldots\ldots, T_{kw_{h_1}}\}$ that does EMI mitigation at the specific PES operating condition is found out and applied to the PES. The algorithm outlined in Figure 42 is followed.

Figure 52a and

Figure 52b show the experimental PES start-up and steady state time-domain response obtained with SBC at 350 W.



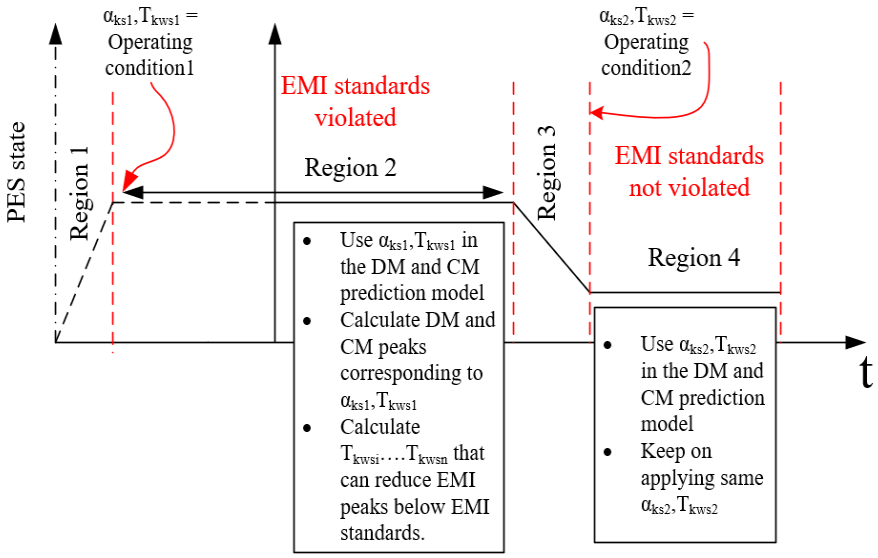
(a)



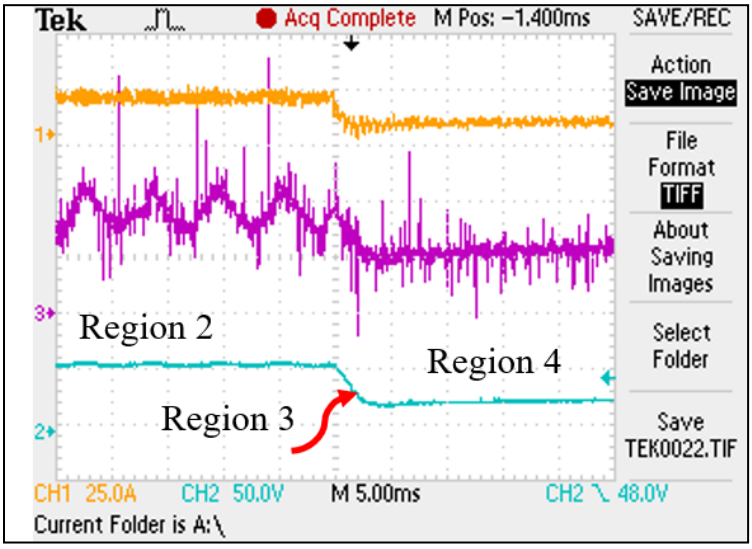
(b)

Figure 52. (a) Figure showing the PES start-up response. (b) Figure showing the PES steady state response. Both the results are taken at 350 W. The traces from top to bottom show the input PES current, $\alpha_{k1}T_{kw}$ variation (plotted as DAC output), and the output voltage of the PES.

Figure 53a and Figure 53b further show the PES response for a step change in reference power for the PES from 350 W to 20 W. The $\alpha_{kn}T_{kw}$ variation (plotted as DAC output) is of importance here. In Figure 53 the PES reaches



(a)



(b)

Figure 53. (a) and (b) Automatic adjustment of the switching sequences by SBC on change of operating condition. The traces from top to bottom in (b) show the input PES current, $\alpha_{kn}T_{kw}$ variation (plotted as DAC output), and the output voltage of the PES.

steady state power of 350 W in Region 2 via Region 1. Then the operating condition shifts to 20 W in Region 4 via Region3. The regions are so chosen that EMI standards [66] are violated in Region 2 and not in Region 4.

As shown in Figure 53b, at 350 W, SBC in Mode-2 synthesized a SS (α_{kn} and $T_{kw} \in \{T_{kw_1}, \ldots\ldots, T_{kw_{h_1}}\}$) that does EMI mitigation in Region 2 and minimizes the cost-function in (4b). In Region 2, SBC varied the $\alpha_{kn}T_{kw}$ to keep output voltage constant as shown in the middle trace in Figure 53b.

On changing the operating point to 20 W, SBC stops synthesizing EMI mitigating sequence in Region 3 and minimizes the cost function in (38a) to reach the new-steady state in Region 4. On reaching the new-steady state at significantly lower power, SBC using the algorithm in Figure 42 does not perform EMI mitigation since EMI standards [66] are not violated. The $\alpha_{kn}T_{kw}$ variation in trace-2 shows that the SBC, hence, adapts its switching sequence (α_{kn} and $T_{kw} \in \{T_{kw_1}, \ldots T_{kw_s} \ldots, T_{kw_{h_1}}\}$) autonomously in the steady state depending on the change of operating condition.

3.3.3. PES DM EMI mitigation with sensitivity analysis

Figure 54 shows the maximum error (across wide operating conditions) between the experimental and analytical DM EMI peaks. The online prediction model for DM EMI is made by using up to ten DM peaks above the EMI limits of 150 kHz. This is because (i) the DM EMI standards are usually violated below this range, as discussed in Section 3.2.2 (ii) the error in DM peak prediction in this region is appreciably low (usually less than 2% of the steady state peaks).

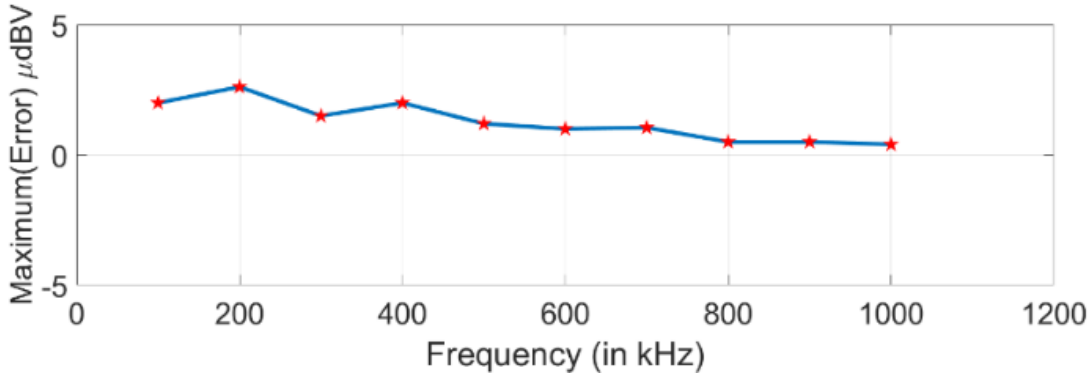
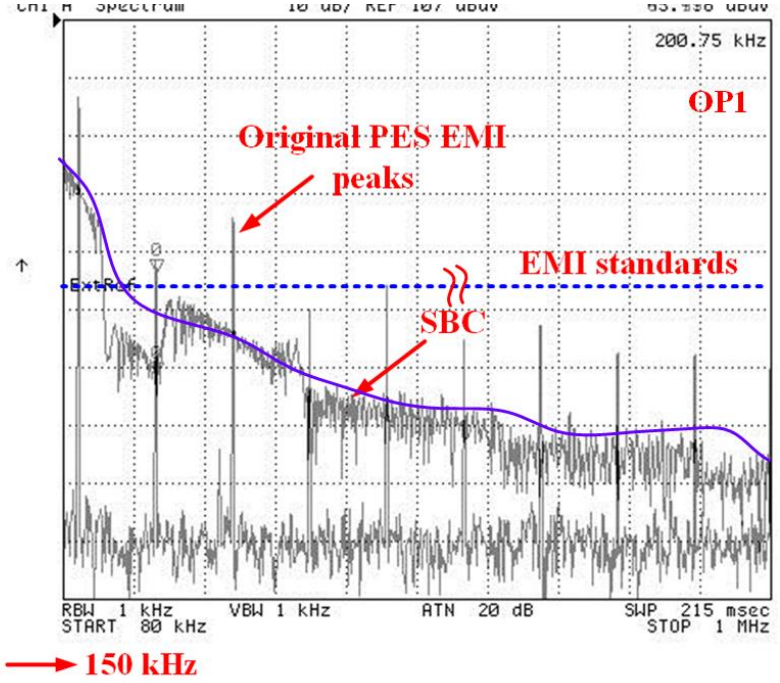


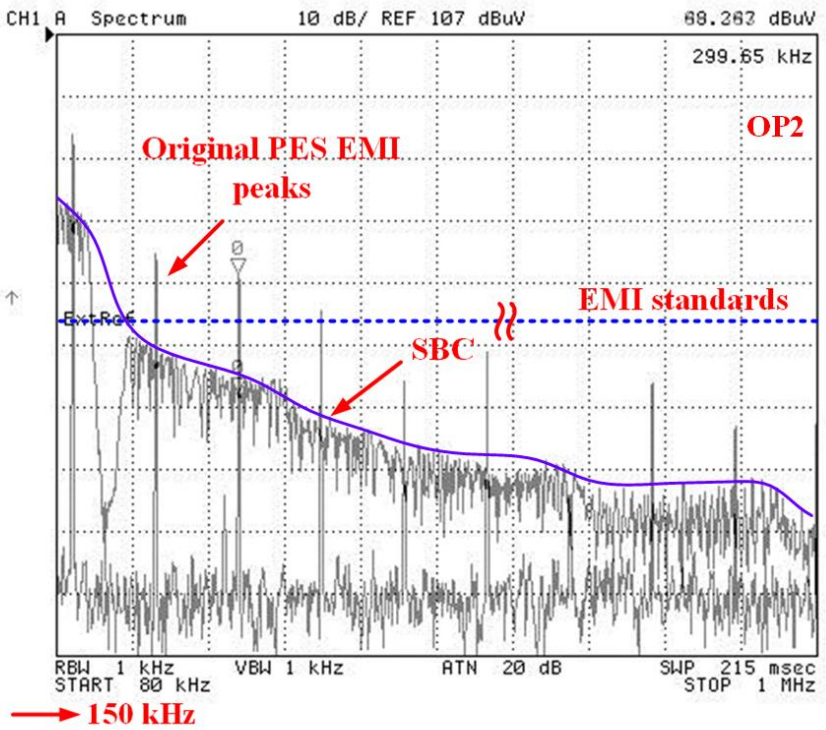
Figure 54. Worst-case error in DM peak prediction due to the hardware/PES model mismatches as discussed in Section 3.2.2.

Figure 55 shows the SBC-based DM EMI-mitigation across various operating conditions of the PES and plots the output voltage corresponding to those points. Figure 55a to Figure 55c show three operating points of the PES, chosen

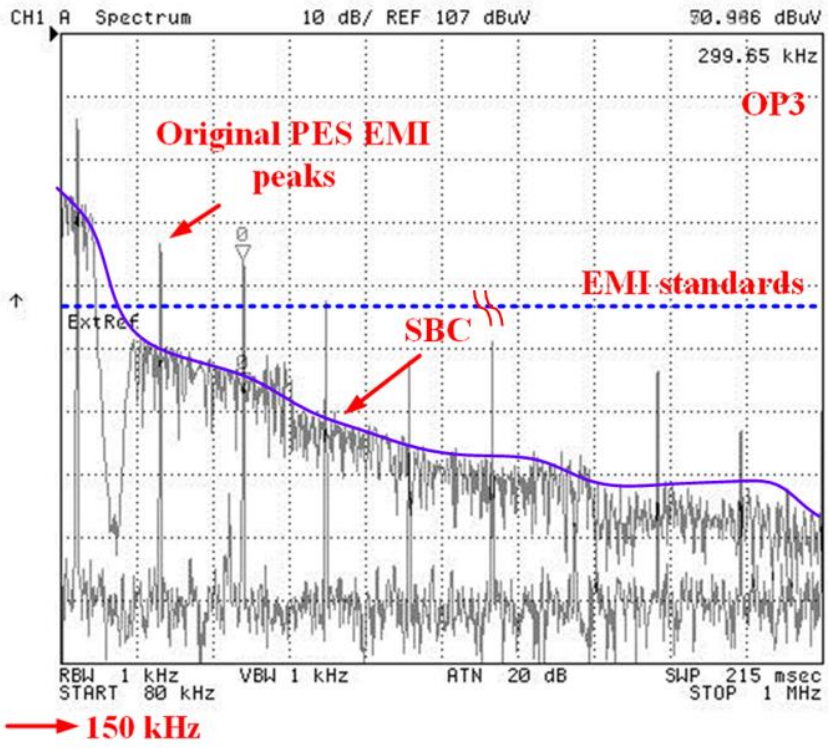
at random as OP1: V_{in}= 45 V, V_{out}= 100 V, P_{out} =300 W, OP2: V_{in}= 40 V, V_{out}= 80 V, P_{out} = 200 W OP3: V_{in}= 55



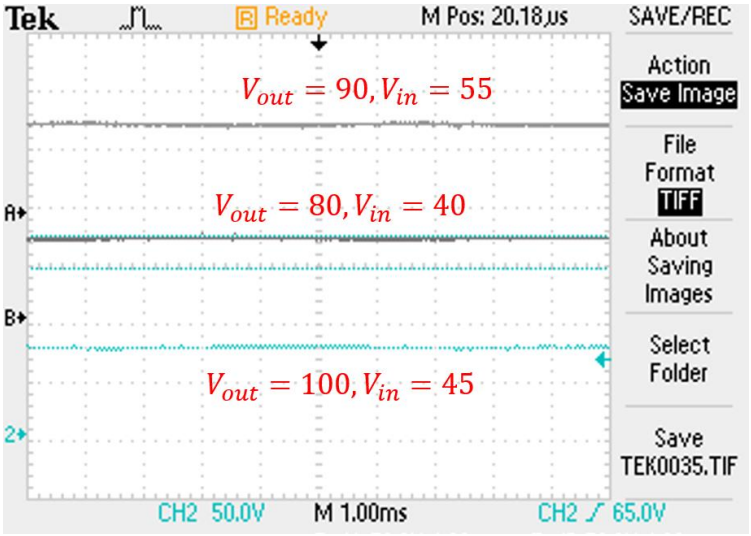
(a)



(b)



(c)



(d)

Figure 55. Experimental PES spectrum showing the DM EMI peak reduction using SBC across various operating conditions as (a) V_{in}= 45 V, V_{out}= 100 V, and P_{out} = 300 W (OP_1) , (b) V_{in}= 40 V, V_{out}= 80 V, and P_{out} = 200 W (OP_2). and (c) V_{in}= 55 V, V_{out}= 90 V, and P_{out} = 210 W. (d) Figure showing the output voltages for the operating points.

V, V_{out}= 90 V, P_{out} = 210 W. In all these three cases, the effect of the application of the SBC with DM EMI mitigating sequences (the reduced peaks with higher EMI floor in Figure 55) is compared against SBC without DM EMI mitigation (the isolated/islanded discrete DM EMI peaks in Figure 55). On violation of the EMI standards [66] in the steady state, SBC selects a new value of T_{kw}, the depth ΔT_{kw} and T_{kw}/h_1 (refer to Figure 41) that can reduce DM EMI peaks below the DM EMI standards leading to an entirely autonomous DM EMI mitigating system. A small safety margin is used to account for the PES model/hardware DM EMI peak mismatches shown in Figure 54. Figure 55d shows the output voltage of the PES for the three operating points.

3.3.4. DM EMI size mitigation

SBC provides programmable DM EMI suppression which reduces the size of EMI filter and in some cases precludes the need for it as is the case with the PES under consideration. For visual depiction and quantitative analysis, an EMI filter to suppress the DM peaks is designed following [4], [6],[34] for the worst-case operating point for DM EMI for the Ćuk PES. The designed EMI filter is shown in Figure 56. The DM EMI inductor has to carry the full input current and is designed accordingly by keeping the inductance less and capacitance higher as specified in [34] for higher input currents. The inductor/capacitor combination is hence determined to be 50 μH and 5 μF, respectively, for providing the attenuation required with some overcompensation.

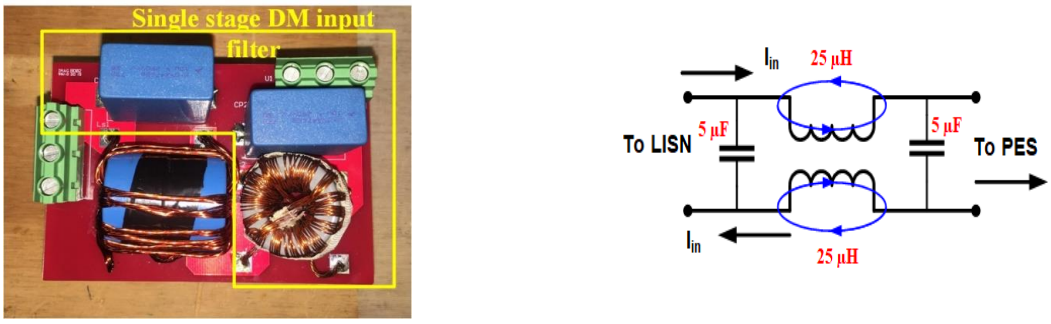


Figure 56. The DM EMI filter at the input side to suppress the DM noise peaks that are mitigated by SBC.

For the same worst-case DM EMI, Figure 57 provides a comparative analysis via experimental results, showing

(1) EMI peak suppression by DM EMI filter designed.

(2) SBC based DM EMI mitigation.

(3) The original unsuppressed DM EMI peaks.

Thus, SBC with DM EMI mitigating sequences eliminated the need for the DM EMI filter shown in Figure 56 for the Ćuk PES. This also resulted in a decrease in the weight of the PES by 0.45 kg.

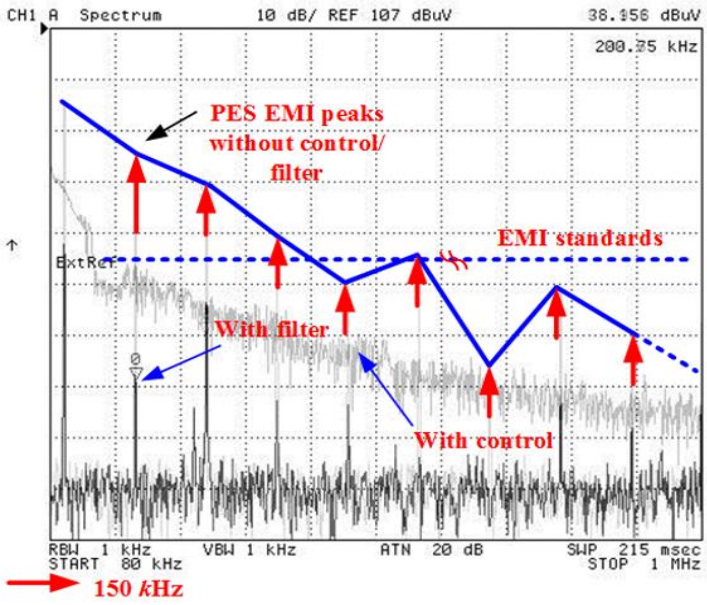
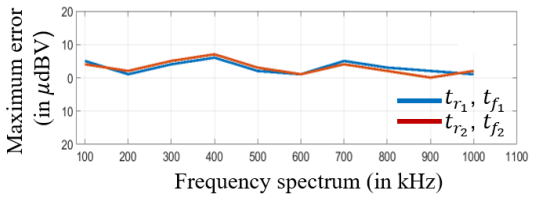


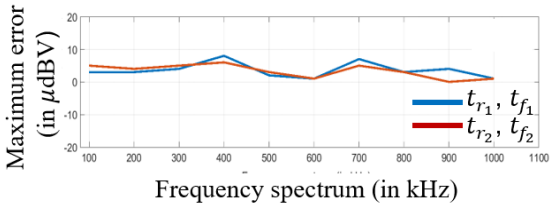
Figure 57. Figure showing comparative analysis of the EMI filter based peak reduction (bottom trace), SBC based peak reduction (middle trace) and original EMI DM peaks without EMI filter and without EMI mitigating SBC (top trace-red). The EMI standards are specified in blue.

3.3.5. PES CM EMI mitigation with sensitivity analysis

Since CM cases are heavily dependent on indeterministic parasitic coupling paths, an analytical model was created, and experimental data was used to find reasonable C_{s_1}, C_{s_T} and C_{s_2} to reduce PES model/hardware inaccuracies and a CM model for the PES was formed. For finding feasible values of the common mode capacitors using the algorithm in Figure 50, $\varepsilon \leq 10$ μdBV was used. The methodology is delineated in detail in Sections 3.2.3. Figure 58a shows the efficacy of the CM EMI peaks predicted by the CM model so constructed by plotting the maximum error ($|C_{cm_{expi}} - C_{cm_i}|$) for wide range of operating conditions. $C_{cm_{expi}}$ denotes the real-time CM EMI peaks of the hardware PES, while C_{cm_i} are the peaks predicted by the CM EMI model. Figure 58a also shows the error for two different values of switching transitions t_r (rise time) and t_f(fall time), namely t_{r_1} =30 ns, t_{f_1} =10 ns, and t_{r_2} = 80 ns, t_{f_2} = 30 ns. The rise and fall times for the 2nd case is chosen to show the validity of the proposed approach for devices with slower transitions respective to GaN-FETs like Si MOSFETs. Thus, the proposed CM EMI model works for different dv/dt



(a)



(b)

Figure 58.(a) Worst-case error in predictions for the CM EMI for hardware PES set-up 1 for two different values of switching transitions. (b) Worst-case error in predictions for the CM EMI for hardware PES set-up 2 for two different values of switching transitions. The worst-case error never exceeds $\varepsilon = 8$ μdBV.

transitions, as well with reasonable accuracy.

Because CM cases are parasitic modeling dependent, Figure 58a shows the error ($|C_{cm_{expi}} - C_{cm_i}|$), for a different PES hardware set-up to show the sensitivity of the CM EMI model. Instead of GS66508B GaN-FETs, a previous generation GaN-FET board using GS66508P GaN-FETs (same rating) was used. The previous generation GaN-FET board has changes in layout, gate drive design (isolated/non-isolated) and an extra LC snubber on the primary side. Also, the transformer structure was varied by using different number of layers for the primary and secondary windings, keeping the turns ratio and number of turns on each side same. Like Figure 58a, Figure 58b also plots $|C_{cm_{expi}} - C_{cm_i}|$ for two different values of $\frac{dv}{dt}$ transition rate.

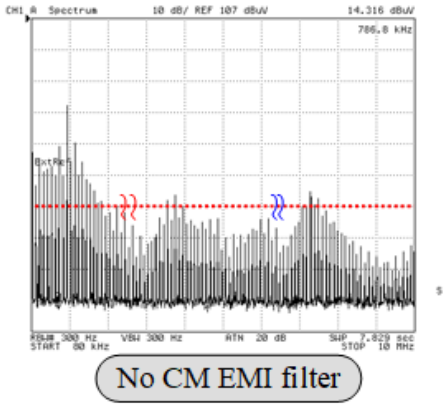
Now with reference to Figure 49, we hence define two regions:

1) Region 1: In this region, SBC is synthesized in a predictive manner due to reasonably accurate predictions of the CM EMI. Any CM noise peaks below the 10th harmonic of the switching frequency will be addressed by SBC.

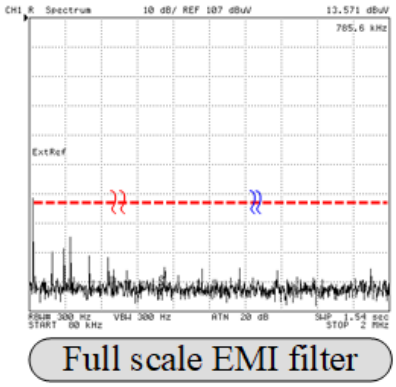
2) Region 2: In this region, the peaks will not be predicted. A CM EMI filter is designed based on guidelines of [34], which will address the CM EMI peaks.

Figure 59 shows the experimental results obtained by SBC using the online CM EMI model. Figure 59a shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating switching sequences for the worst-case CM EMI point. Referenced to Figure 49, the spectrum is dominated by the lower order harmonics of the switching frequency and mid-range harmonics due to parasitic oscillations.

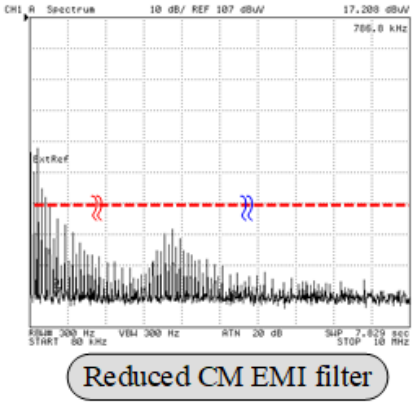
Figure 59b shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating sequences but with a full-scale CM EMI filter[34]. The spectrum meets the CM standards across the entire range. Figure 59c shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating sequences and reduced-size EMI filter. The EMI filter



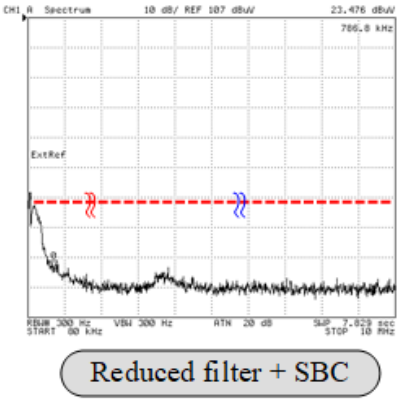
(a)



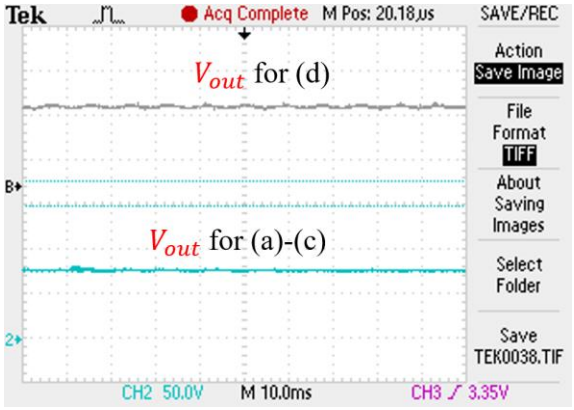
(b)



(c)



(d)



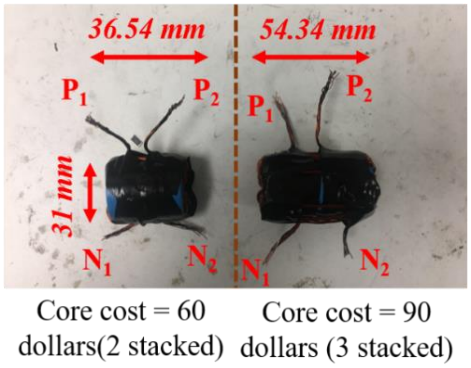
(e)

Figure 59. (a) Figure shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating sequences. (b) Figure shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating sequences and full-scale EMI filter. (c) Figure shows the CM EMI spectrum of the Ćuk PES for SBC without EMI mitigating sequences and reduced-size EMI filter. (b) Figure shows the CM EMI spectrum of the Ćuk PES for SBC with EMI mitigating sequences and reduced-size EMI filter. The CM EMI standards [3] have been highlighted in red. (e) The output voltages of the

above four cases have been compared.

is designed for higher cut-off frequency thereby reducing the size. However, the CM EMI peaks still violate the standards around the lower order harmonics. Figure 59d then shows the spectrum of SBC with EMI mitigating switching sequences which brings all the peaks below the EMI standards. The output voltage for the above four cases is shown in Figure 59e.

Figure 60 shows the reduction in EMI filter size and cost due to SBC based EMI mitigation. HITACHI FINEMET cores with very high permeability have been used as core materials for CM filter design. For the full-scale EMI filter for Figure 59b, three FINEMET cores each costing 30 dollars[87] have been stacked to create the CM EMI filter of 16 mH considering the window area for the required number of turns. The CM filter did not consist of any CM capacitor. For the reduced size CM EMI filter for Figure 60c and Figure 60d, two cores are stacked together to create 5 mH of CM inductance in conjunction with SBC based EMI mitigation to satisfy the CM standards. This results in 33.33% reduction in core cost for the CM inductor design. The FINEMET cores used for the CM filter have very high permeability thereby providing high inductance value in limited size and weight. Hence, CM filter size reduction does not lead to an appreciable specific weight variation of the PES. However, the use of alternative low-cost low-permeable cores for CM filter will lead to appreciable specific weight decrement of a PES due to huge inductance of CM filters.



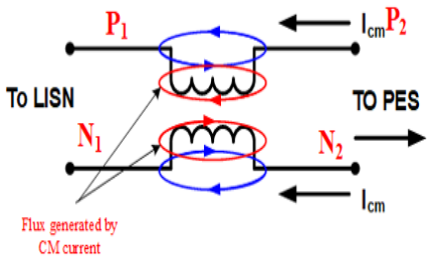


Figure 60. Comparative figure showing the designed full-scale and reduced-order EMI filter for the worst-case CM EMI mitigation. The EMI filter is designed with high-cost high permeability FINEMET cores.

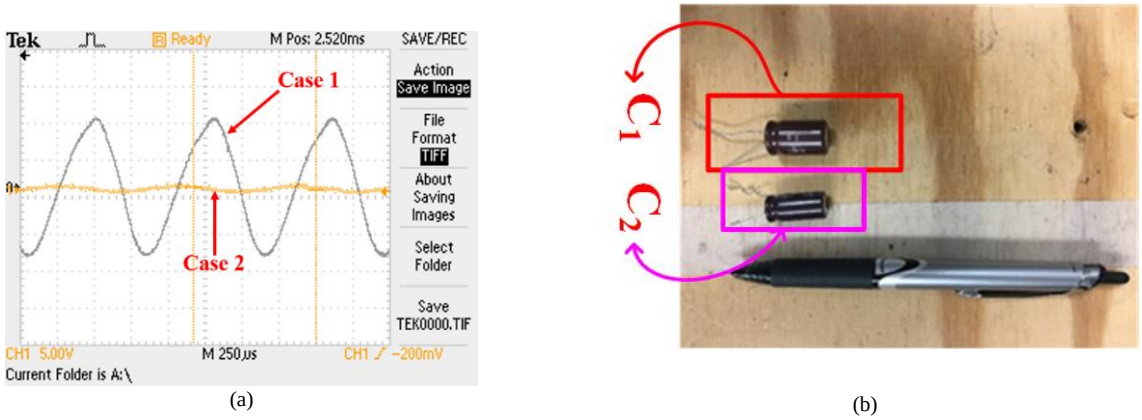
3.3.6. Low-frequency distortion, PES efficiency and effect of ADC resolution and delays:

3.3.6.1. Low-frequency distortion

As shown in Figure 43, T_{kw} variation in steady state to perform EMI mitigation results in output voltage fluctuation. SBC systematically controls $\alpha_{kn}T_{kw}$ of a SS to keep the low-frequency deviation within bounds. Figure 25a shows a comparative analysis of two situations to validate it experimentally:

(1) The grey trace signifies the scenario (Case 1) when the steady state EMI mitigating sequences are applied without performing output voltage regulation using SBC in steady state with capacitor $C_2 = 10\ \mu$F, in Figure 61b. The output voltage fluctuations are considerable.

(2) The yellow trace signifies the scenario when the SBC minimizes a cost-objective (38) of the output voltage fluctuations even in steady state, but with a slightly bigger capacitor $C_2 = 30\ \mu$F as shown by the comparative analysis in Figure 61b. It causes negligible output voltage deviations. From a power density and specific weight perspective, the capacitor size increment for the Ćuk PES is less considered to EMI filter size reduction.



(a) (b)

Figure 61. (a) Comparison of the output voltages in Case 1 and Case 2. Case 1 can be alternatively thought of as a scenario when the output voltage regulation feature of the control is disabled. The vertical scale signifies 5 volts/div and the average output voltage is 90 V. (b) The output capacitor size increase used by SBC for negligible output voltage deviations.

3.3.6.2. PES efficiency

In addition to the decreased EMI size and autonomous EMI mitigation, SBC has a positive effect on the operating efficiency of the PES. With an operating point of V_{in}= 30 V, V_{out}= 90 V, the power throughput of the PES is gradually increased by increasing the load for the below scenarios:

(1) First, without the CM/DM EMI filter, SBC is used to synthesize the switching sequences, both transient and steady state. In transient, SBC performed optimization of α_{kn} and T_{kw} to provide the desired response. Secondly, in steady state the SBC held on to the steady state output value providing good regulation;

(2) Second, the 1st case is repeated with the full-scale EMI filter [34][67] to do the DM/CM EMI peak reduction;

(3) Third, instead of using the full-scale EMI filter, SBC reduces DM and CM EMI peaks and uses a reduced-order CM filter. SBC also provides on-time variation of the switching sequences to keep output voltage constant.

Figure 62 shows the difference in efficiencies of case 1 with that of cases 2 and 3. SBC based EMI reduction provided better efficiency results than the case with EMI filter, even for such moderate power systems.

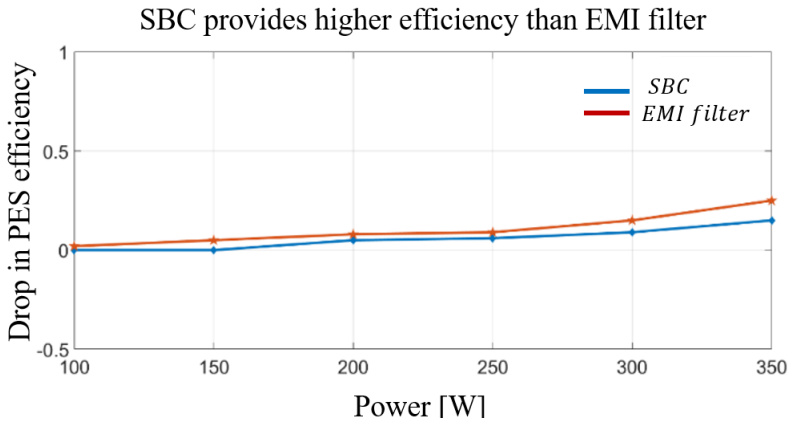


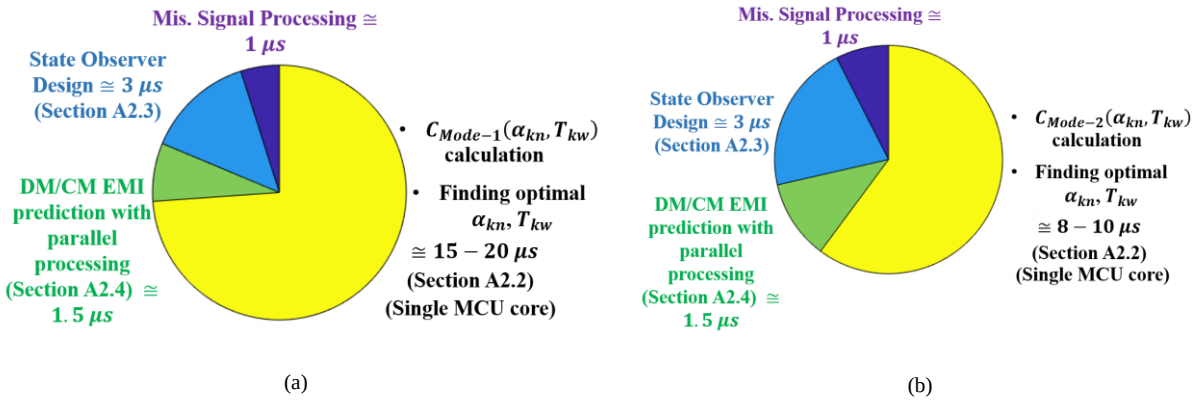
Figure 62. Figure showing that decrease of EMI filter size using SBC does not come at a price of decreased PES efficiency.

3.3.6.3. Comments on sensors, ADC acquisition and delays, and execution time

SBC uses a comprehensive high-frequency (HF) PES model to predict the EMI peaks for a PES for different operating conditions. It uses the EMI peaks to solve a constrained online optimal problem. For DM EMI, an open-loop HF PES model was used with safety margins to account for PES model/hardware mismatches, while for CM EMI a data-driven HF analytical model was formed. Both the models were used by SBC to reduce PES EMI autonomously, as shown experimentally. Alternate to the approach taken, the EMI peaks could have been measured real-time for SBC. For a case illustration for the CM EMI, for $T_{kw_s} = 10\ \mu s$, to capture the components up to 10th to 15th harmonic would have necessitated greater than 10 MHz ADC sensing. Additionally, computation of n-point FFT to calculate the EMI peaks for CM/DM current would have gone beyond the computational capabilities of low-cost digital processors.

Hence, using internal HF DM/CM models preclude the need for extremely high-bandwidth ADC sensing and saves DSP computation time. The real-time EMI peaks calculated depends on HF EMI model and steady-state values of the V_{in} and V_{out} voltage sensors, using (41) and (47). The voltage sensors are low-bandwidth and acquired digitally using the 16-bit ADCs of F28379D, at a sampling rate of 2 MHz. Considering ADC acquisition of V_{in} voltage sensor, decreasing the ADC bit resolution to 12 and 8 instead of 16, would lead to slight errors in EMI peak prediction of 0.03 μdB, and 0.69 μdB respectively, and deteriorated control performance.

The execution time of the SBC also affects control performance. For processors with faster instruction cycle time, SBC execution takes less computational time, which positively affects control performance in areas like output state regulation etc. because of the increased resolution of the control actions that can be achieved. Hence, for slow instruction cycle at a high switching frequency, to close the control loop in each switching cycle, the control resolution will become poor, thereby negating the effectiveness of such controllers. For the TMS320F28379D MCU which is a high-performance industrial DSP for general power converter control, the execution time breakdown for the overall SBC control in Mode-1 and Mode-2 of operation is shown in Figure 63.



(a) (b)

Figure 63. Figure execution time and/or time-breakdown for the overall SBC control in Mode-1 (a) and Mode-2 (b) of operation, respectively.

3.4. Conclusion

SBC that does EMI mitigation is discussed in this paper. SBC, in addition to synthesizing reachable sequences that ensures global stability for the PES, does DM and limited CM EMI mitigation.

The importance of SBC is as follows:

(1) By use of comprehensive HF PES model, SBC precludes need for complex sensing and high bandwidth ADCs, which simplifies PES design;

(2) Secondly, it reduces and, in some cases, precludes the need for EMI filters that negatively affects the power density and efficiency of the PES;

(3) It gives high programmability to PES design. A PES operating at 10-50 per cent of the rated condition does not necessitate bulky EMI filter to do overcompensation of EMI peaks at lighter loads. At higher power levels, when only the control will not be enough to mitigate the EMI peaks, an EMI filter-control in integrated combination may provide good flexibility.

Moreover, SBC does perfect on-time regulation of the switching sequences which limits the slower-scale deterioration as evident from the experimental results. This approach is particularly useful for the ever-evolving fast-transition devices like the GaN FETs with high dv/dt. Devices like these can be switched at higher frequencies under high power due to their low device capacitances, yet higher voltage and current ratings. The high $\frac{dv}{dt}$ of these devices also lead to lower switching losses at higher frequencies. However, operation at high power at higher frequencies may lead to bulky EMI filter or higher-order EMI filter to provide the desired attenuation. This is because of the strict contemporary EMI standards. Even though a higher-order EMI filter yields a robust option to meet the EMI targets and provide higher cut-off rate, it may affect the stability margin of a PES negatively in non-minimum phase systems which can impede their application. Hence, a hybrid SBC-EMI-filter synthesis for a PES may enable operation using these fast-transition devices at high dv/dt and at higher power.

Chapter 4

4. SWITCHING TRANSITION CONTROL OF A ĆUK BASED POWER ELECTRONIC SYSTEM

Parts of this chapter, including figures and text, are based on my following papers:

D. Chatterjee and S. K. Mazumder, "Turn-on switching transition control using a GaN-FET based active gate drive," in *2021 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, accepted.

D. Chatterjee and S. K. Mazumder**, "**Switching transition control to improve efficiency of a dc/dc power-electronic system**,"** IEEE Access, doi: 10.1109/ACCESS.2021.3092017.

Increasing the switching frequency of the power semiconductor devices (PSDs) reduces the size and cost of the

passive elements, thereby positively affecting the power density of a high-frequency (HF) power electronic system (PES). To achieve a higher switching frequency of a PES, yet low switching losses, the speed of switching transitions of PSDs need to be increased. However, such fast transitions adversely affect PES performance in terms of electromagnetic interference (EMI) and device stress. Hence, a switching transition control (STC) scheme is developed to create optimality between switching PSDs with higher transitions yet maintaining safe levels of parasitic oscillations, that result from reducing the transition time of these devices. The switching transition control (STC) framework helps the HF PES achieve a target efficiency improvement by controlling the high di/dt and dv/dt regions of a PSD on the fly. Results are shown to validate that this improvement of efficiency is not feasible with a passive gate drive. An HF Ćuk PES using Cree SiC Mosfet half-bridge module is fabricated for testing purpose of the STC framework. The STC network is based on a simple switched resistor network, synthesized using high-speed GaN-FETs and built across two generations, Gen-1, and Gen-2. The practical problems associated with the Gen-1 board (mainly due to the high-speed GaN-FETs) are addressed with design modification in Gen-2.

The work has ramifications in meeting a system level goal of a HF WBG PES, like a target efficiency increment, while not deteriorating the EMI performance and PSD stress levels that result due to parasitic oscillations in such PES**.**

4.1. Introduction

To reduce PES losses while increasing power densities (by increasing switching frequencies), the switching transitions of the PSDs need to be significantly improved as is evident from the recently used WBG PSDs like GaN-FETs and SiC FETs [2], [5], [33], [88]–[90]. These new-generation devices facilitate miniature chip design leading to small parasitic capacitances. This enables higher frequency operation at increased power. However, increasing the switching transitions of these new generation devices to decrease the switching losses using fixed gate drive results in non-optimal performance resulting in excessive device stress and electro-magnetic interference (EMI). As an illustrative example, if we consider SiC FET based high power half-bridge modules [91] that are fabricated to aid higher frequency operation at higher power ratings, reducing the on-time resistance of the low-side FET to reduce switching losses, results in reverse recovery induced oscillations [92] due to the body diode of the high-side FET. So, instead of reduced switching losses, these oscillations increase the *V-I* overlap at the turn-on switching transition even further, resulting in decreased PES efficiency. Over and above, these oscillations lead to unstable PES gate drive

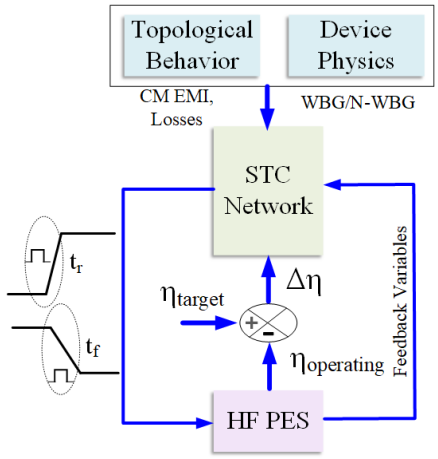


Figure 64. Figure showing how STC scheme can meet system-level goals for an HF PES.

operation, that does not let the PES operate across a wide operating range. In such HF PES, where there is a need of an optimality between switching losses (by using lower gate resistances) and device stress/ oscillations (that results due to use of lower gate resistances), a switching transition scheme, as shown in Figure 64, can be synthesized. Depending on a particular topology and an online operating point, with the device physics under consideration, it can create rise and fall times of the devices of the HF PES to meet a specific goal (η) for the topology. The specific goal (η) can range from efficiency increment to common mode EMI reduction for the PES.

Passive gate circuits cannot achieve this feat. They use fixed gate resistances which decrease transition times at the cost of increased power loop and gate loop oscillations and hence, optimized switching performance is not achievable over wide power levels. Active and passive snubbers, as well as active clamp circuits, are then used to reach optimality between switching loss EMI and device stress of a PES [33], [93]. This introduces additional components in the power stage in form of semiconductor switches, and passive elements which add to the PES losses. Also, the snubber values are difficult to optimize, and a desirable trade-off is seldom obtained.

A good strategy in attaining a tradeoff is to design an active gate drive that controls the switching transitions of a PES. The STC scheme in Figure 64 uses such an active gate drive. Active gate circuits were first used to dynamically adjust the turn-on/turn-off transition of slower transition IGBTs [88], [94] for series connection of such devices. It helped replace the conventional voltage-sharing snubbers, as well as reduce switching losses while maintaining admissible voltage/current stresses of the devices. References [38], [95]–[97] extend the use of active gate drive circuits for WBG SiC Mosfet applications. The literature [95][38] proposes switched resistor-based gate drive modulation to improve the current and voltage transitions of SiC PSDs and achieves controllability and performance

optimization in terms of EMI and switching losses. However, both the references encompass limited transitions of the switched resistor network, resulting in lower flexibility to affect different regions of the switching transition in a single turn on/turn-off event. Moreover, the switched resistor-based gate drive synthesis is not touched upon in detail in the abovementioned literature. Also, reference [96] uses the switched resistor approach to decrease turn-off losses only of the SiC FET, while during turn-on, EMI issues and device stress due to body-diode reverse recovery is focused upon. Reference [97] on the other hand could achieve higher granularity in switching transition control using a mixed-signal design approach. But the approach suffers from higher complexity, and the design parameters are not easy to replicate.

Recently, active gate circuits have been used for high-speed GaN-FETs with less than 10 *n*s switching transients [98]. Although the gate driver altered multiple drive parameters per switching event, however, the gate current peaks are significantly less than that needed for SiC Mosfets having large gate to source capacitances. Reference [98], although designed for low power applications, need to be extended to higher power scenarios where drive parameter variations per switching transition will lead to optimality between high EMI/device stress levels of a PSD at higher power and PES switching losses. Also, the specific application altered drive parameters in a switching transition using an integrated ASIC which is understandable since the switching transition of GaN-FETs is very fast. The complexity of the approach is bound to preclude its use in industrial applications.

The recent works in references [95]–[98] thus show active gate drive design for WBG PSDs that evaluate the effects of varying switching transition of devices on PSD turn-on/turn-off energy losses, device stress and EMI. They do so mainly using a double pulse set-up [95], thus creating a cause/effect relationship mainly. However, how these schemes can be extended to improve converter level performance, or meet a converter level goal, as shown in Figure 64, is not clearly described. Also, most of the literature that increases the granularity of these active gate drives uses complicated mixed-signal schemes that are difficult to replicate.

Contrary to these prevalent approaches, this chapter delineates a switching transition control (STC) framework, which, depending on modes of operation (CCM/DCM) of a Ćuk WBG PES set-up using Cree QPM3 SiC Mosfet half-bridge module (having high input capacitance that results in higher peak gate currents), shapes the turn-on/turn-off of the HF PES using an online processor. It does so to help the PES achieve target efficiency increment across wide

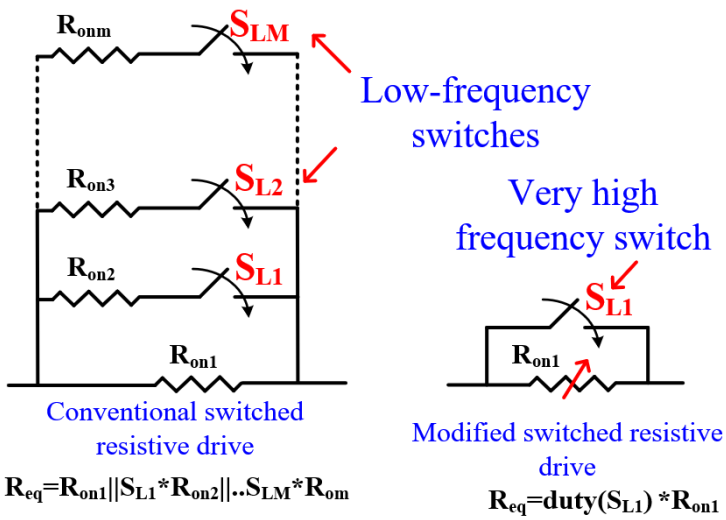


Figure 65. Figure showing the difference between conventional[38], [95] vs modified switched resistor-based gate drive approach.

operating conditions while precluding excessive device stress. The approach is scalable/replicable because: 1) it uses a switched resistor scheme for the STC circuit. It is the simplest form of active gate drive. Contrary to approaches in [95][38],which requires multiple gate resistors in the switched resistor drive to achieve granularity, the proposed approach makes use of a single resistor with a HF GaN switch in parallel. The pulses to the GaN device are selected to create an averaged gate resistance. The conventional vs proposed approach is compared in Figure 65. The approach dramatically reduces the gate footprint and complexity of the drive.

Moreover, the STC scheme uses discrete components that are easy to procure. The scheme is easy to synthesize with the increased reliability of high-speed GaN devices and their drive techniques that can switch a resistor with enormous speed without the need for integrated ASICs. 2) it uses an industrial-scale processor, F28379D, to realize the circuit without any significant computational burden or complex control.

The chapter is organized as follows: Section 4.2 delineates the STC framework and its application to the Ćuk based PES. Section 4.3 describes the hardware set-up synthesized to perform STC, along with experimental results. Some appendices have been incorporated to ease comprehension.

4.2. Switching transition behavior and control

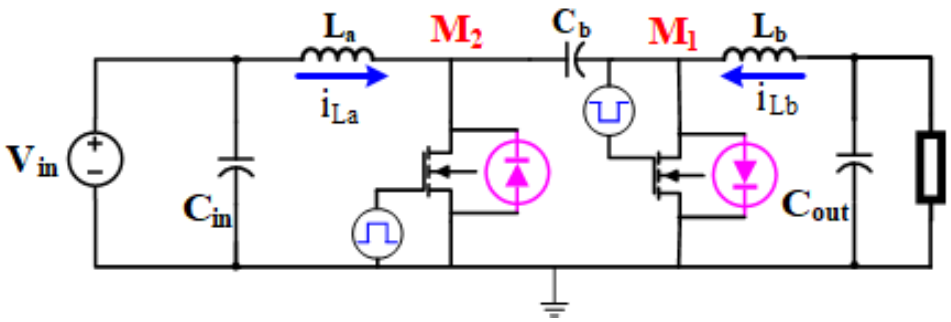
4.2.1. Motivation behind STC for the Ćuk PES

In this section, the motivation behind the switching transition control framework for a Ćuk PES is delineated. Figure 66a shows the schematic of the Ćuk PES. The Cree QPM3 SiC Mosfet half-bridge module (the details of the module cannot be stated due to Non-disclosure Agreement) used for the PES constitutes of two HF SiC switches denoted by M_1 and M_2 in Figure 66a. According to the modes of operation of the Ćuk PES in CCM operation (shown in Appendix I), the body-diode of Mosfet M_1 operates during both turn-on/turn-off transitions in deadtime and leads to near zero-voltage switching of Mosfet M_1. So, the switching losses of the PES are mainly associated with the hard-switched transition of switch M_2. Operating the Ćuk PES at 5 kW for $V_{ds_{M2}} = V_{ds_{M1}} = 500$ V results in the power loss distribution shown in Figure 66b, which is dominated by the switching loss of the switch M_2 of the SiC module. (Of the total switching losses of switch M_2, 70% is the turn-on switching loss). The Cree QPM3 SiC Mosfet half-bridge module is usually driven by an industrial Cree gate driver with fixed gate resistances and two isolated channels for each of the SiC Mosfets M_1 and M_2. Each of the gate-loop channels being a 2nd order LC system, the net gate resistance in the gate drive loop should damp any resonance arising in the loop. The net required gate resistance, from a damped gate-loop perspective (or the minimum gate resistance that is required for damping the gate resonance), can be calculated from the equation [99]:

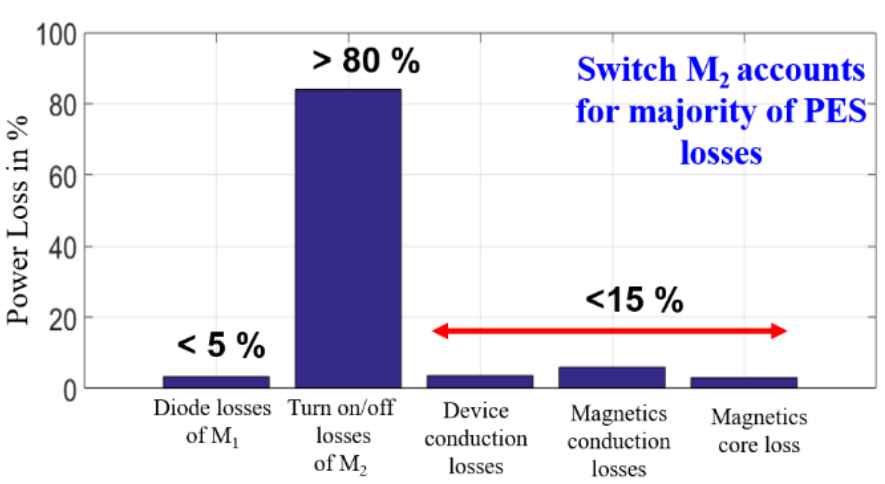
$$R_{init} + R_{ext} \geq 2\rho_{SiC}\sqrt{\frac{L_{int}+L_{ext}}{C_{iss}}} \tag{50}$$

In (50), R_{init} denotes the internal gate resistance of the SiC module, and R_{ext} denotes the external gate resistance in the driver circuit of each of the Mosfets M_1 and M_2. Also L_{int} and L_{ext} denote the parasitic inductance internal to the SiC module, and external to the module in the gate drive loop, respectively. C_{iss} denotes the input capacitance of the Mosfets M_1/M_2. For avoiding any resonance in the gate loop, ρ_{SiC} should be greater than unity. For the Cree SiC half-bridge modules chosen for hardware validation, with available values of L_{int} and L_{ext}, R_{init} is set at 1 Ω (internal to the SiC module and fixed) to avoid oscillations for zero R_{ext}. After that, R_{ext} should be set accordingly to limit switching losses of Mosfet M_2 while taking into consideration the stress on the devices because of high di/dt and dv/dt due to faster turn-on.

For the Ćuk PES under consideration, the turn-on is more problematic Using a fixed $R_{ext} = R_{on_1}$ at turn-on, as



(a)



(b)

Figure 66. (a) Figure showing a Ćuk PES. (b) Figure showing the loss breakdown of a Ćuk PES.

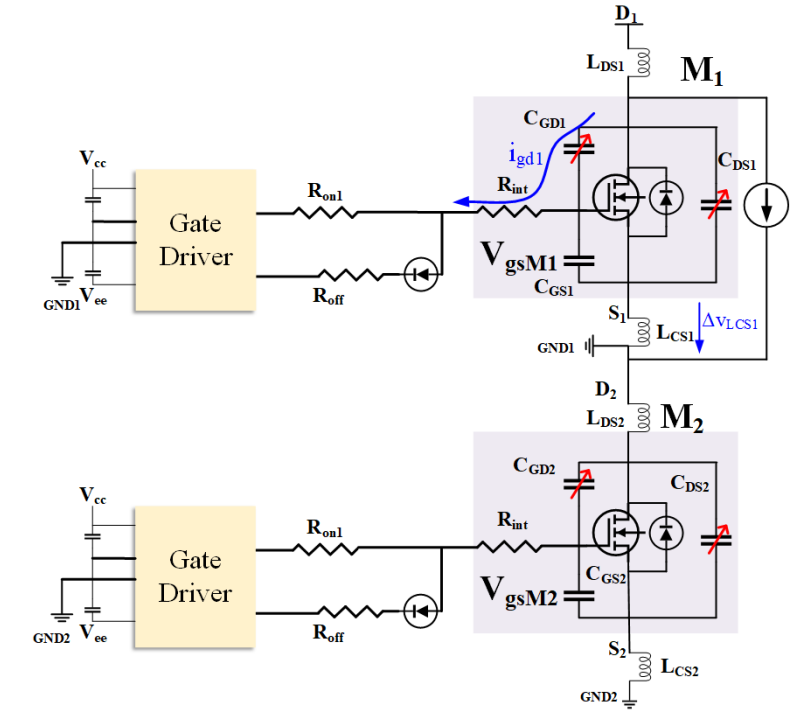
shown in Figure 67a, admissible power loop and gate driver performance is achieved only for higher values of the gate resistance R_{on_1}. When a lower R_{on_1} is applied to decrease the switching losses in a half-bridge set-up like Figure 67 two noticeable problems arise at turn-on:

1) due to higher dv/dt across switch M_1 when the lower

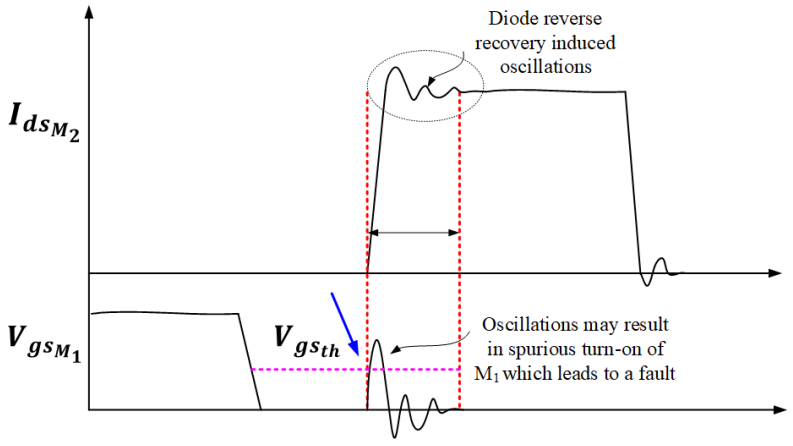
Mosfet M_2 is turning on, the rapid charging current (i_{gd_1}) of the Miller capacitance can lead to spurious turn-on of the high-side switch M_1.

2) due to higher dv/dt at the onset of the Miller region in the lower Mosfet M_2, the body diode of Mosfet M_1 reverse recovers at a very high rate, leading to higher di/dt rates. This results in a voltage drop across the common source inductance $\Delta v = L_{cs_1}\frac{di}{dt}$ across the gate of the upper Mosfet which may also lead to spurious turn-on and oscillations. Both (1) and (2) have been highlighted in Figure 67b.

Traditionally (1) is taken care of by decreasing the turn-off gate resistance of switch M_1. However, this reduces damping in the gate path and the voltage drop due to Δv (point 2) causes considerable current flow in the gate loop path which is undesirable. Hence to take care of (2), a larger gate resistance is desired. Such optimality is difficult to reach for modules with have large common source inductance. Also, for boosting the efficiency of the HF Ćuk PES



(a)



(b)

Figure 67. (a) Figure showing the schematic of the SiC half-bridge module with the passive gate drive circuit. (b) Figure showing spurious turn-on of the high side switch M_1 due to diode reverse recovery induced oscillations.

by decreasing the switching losses on lower Mosfet M_2 (since switching loss of M_2 accounts for the majority of losses of the PES as shown in Figure 66a) the turn-on resistance needs to be decreased which will lead to the problems delineated in points (1) and (2).

Hence, an STC method is adopted here to explore whether using variable gate resistance use during the SiC Mosfet transition can help the Ćuk PES meet a target efficiency improvement by reducing the switching losses while precluding excessive parasitic oscillations that result due to reduced turn-on resistance.

4.2.2. STC for turn-on transition of Ćuk PES

Figure 68a shows the switched resistor-based circuit synthesis for STC network, and Figure 68a shows the STC circuit when applied to the Ćuk PES.

The STC network controls the gate resistances of both the turn-on and turn-off path of the SiC module for both switches M_1/M_2. The external resistance of the turn-on path can be expressed as:

$$R_{ext} = R_{on_1} + \overline{S_{L1}} R_{on_2} \tag{52}$$

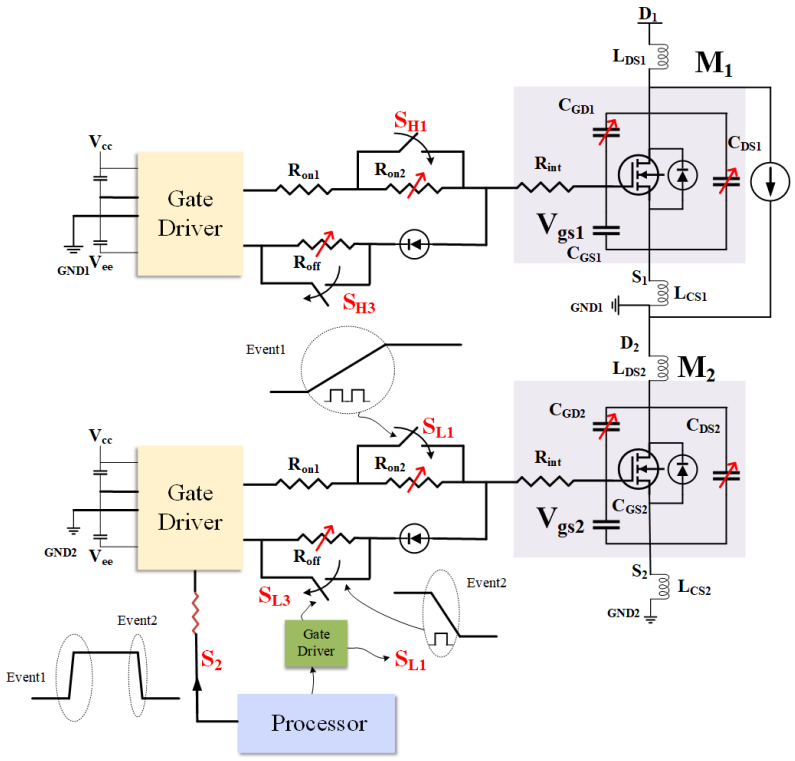
The turn-off path resistance can be expressed in the form:

$$R_{ext} = \overline{S_{L3}} R_{off} || \overline{S_{L1}} R_{on_2} + R_{on_1} \tag{53}$$

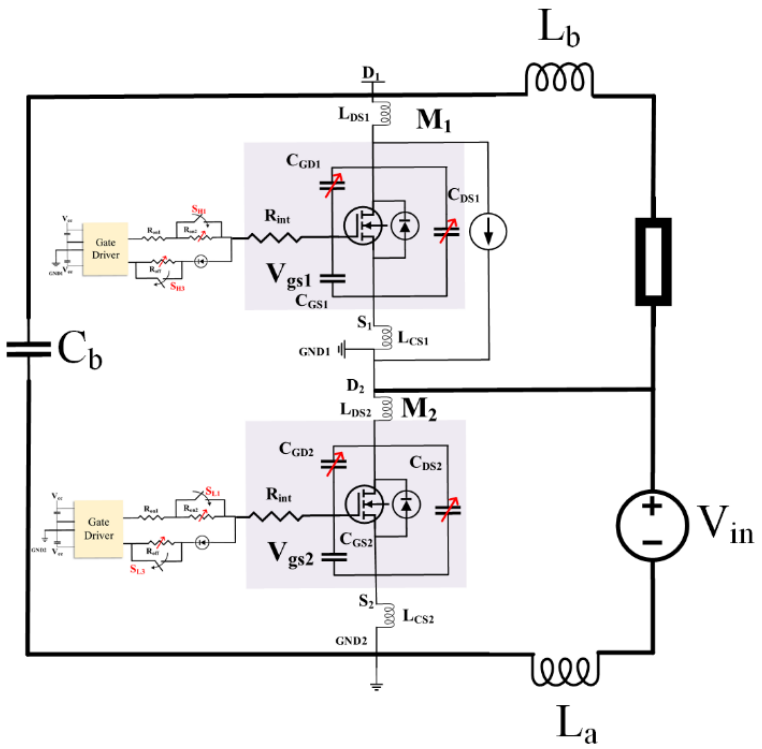
In (52) and (53), R_{on_1} is a fixed gate resistor in the gate drive path, while $\overline{S_{L1}} R_{on_2}$ and $\overline{S_{L3}} R_{off}$ are the dynamic values of the turn-on and turn-off gate resistances. As such, S_{L1} and S_{L3} switch at extremely high frequencies and are 1000-fold faster than the Cree SiC module switching frequency. The pulse-widths of S_{L1} and S_{L3} can be controlled to create an affective gate resistance in a transition region.

4.2.2.1. Following a pre-defined turn-on trajectory

As an illustrative example, for turn-on control, the STC network modulates the switching sequence of the HF switch S_{L_1}(both duty cycle and time period), as shown in Figure 69, to create an average gate resistance in between $R_{ext} = R_{on_1} + R_{on_2}$ and R_{on_1}. This is done to follow a pre-defined V_{ds} trajectory. R_{on_1} is a smaller value of gate resistance that is chosen to create optimal gate damping [99]. R_{on_2} is a higher value of the gate resistance that is chosen in a way to give higher controllability to the turn-on STC scheme. For the SiC module under consideration, due to higher value of transconductance (the term is explained in [90]) , the time from V_{th} to start of the Miller region is very small and the device current reaches steady state very fast. The main switching loss, as shown in Figure 69, is thus dominated



(a)



(b)

Figure 68. (a) Figure showing the switched resistor based STC framework to control the transitions of the SiC device. (b) The Ćuk PES with the

STC network.

by the Miller region due to the higher parasitic capacitances of the SiC module under consideration. Optimally shaping this region leads to efficiency improvement. Again, the Mosfet capacitance that controls the Miller Region [90] is non-linear. Due to the non-linear nature, at the onset of $V_{ds_{M_2}}$, the dv/dt slope is very high and the slope progressively decreases with decreasing value of $V_{ds_{M_2}}$. As shown by the varying pulse-widths in Figure 69, the switching sequence of S_{L_1} can be chosen in a way to create higher resistances during onset of $V_{ds_{M_2}}$ fall to reduce dv/dt, while progressively applying lower resistances as the voltage gradient reduces to save switching losses.

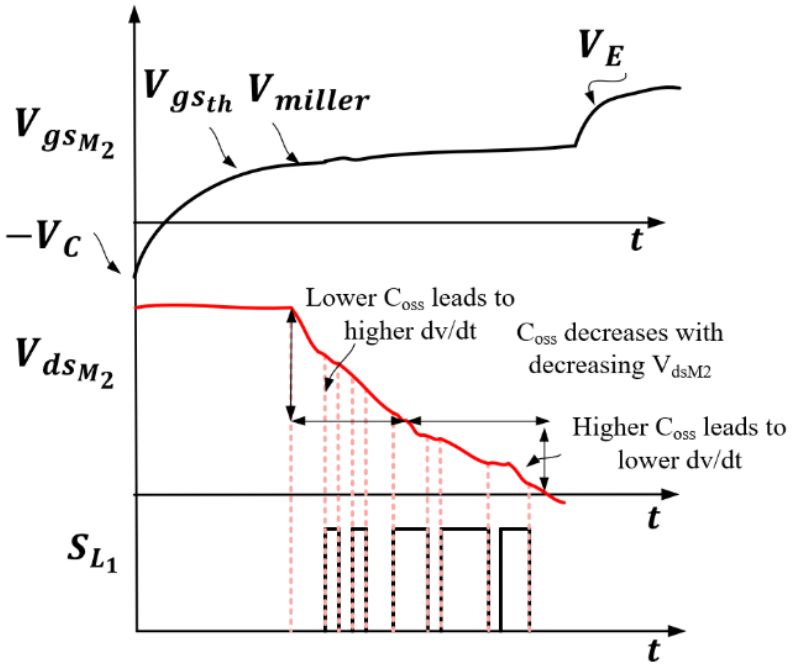


Figure 69. Figure showing the turn-on Vds trajectory control using STC.

4.2.2.2. Reducing diode reverse recovery-based oscillations to boost PES efficiency

Figure 70 further highlights the SiC Mosfet M_2 turn-on waveforms and the STC control scheme for the switch S_{L1}. The three variables T_{w_1}, T_{w_2} and T_{w_3} for the switch S_{L1} control the turn-on transition.

During turn-on of the SiC Mosfet M_2, the reverse recovery of the diode of SiC Mosfet M_1 is of importance as it affects the turn-on loss of M_2. Before the onset of Mode 2 in the Ćuk PES (shown in Appendix I), during Mode 1 the body diode of M_1 was conducting during deadtime. It was carrying a net current of $I_{L_a} + I_{L_b}$(See Figure 66a). As the

gate to source voltage of M_2 rises above the V_{th}, (shown by the point t_1 in Figure 70 the current $I_{L_a} + I_{L_b}$ flowing through the body diode of M_1 starts shifting to M_2. During the onset of the Miller region at t_2, the current overshoot increases beyond $I_{L_a} + I_{L_b}$ to $I_{L_a} + I_{L_b} + I_{dsrr} + C_{ds_{M_2}} \frac{dV_{ds_{M_2}}}{dt}$ at t_3, where I_{rr} is the reverse recovery current of the diode, and $\Delta i_L = I_{dsrr} + C_{ds_{M_2}} \frac{dV_{ds_{M_2}}}{dt}$ as shown in Figure 70. Due to high $\frac{dV_{ds_{M_2}}}{dt}$ during $t_3 - t_4$, the rate of decay of stored charge in the body diode increases, leading to the diode current falling to zero at high $\frac{di}{dt}$ rates. This high $\frac{di}{dt}$ results in voltage drop across the common source inductance L_{CS_1} (as shown in Figure 68b) which may lead to spurious turn-on of the high side device. Moreover, the high $\frac{di}{dt}$ may lead to voltage drops across the drain to source inductance of M_1/M_2, which may lead to additional oscillations that result in excess common mode EMI and device conduction losses. Appendix J derives the analytical equations for the time duration $t_1 - t_6$. As such, the analytical timings achieved by the dynamical equations are in close proximity to the experimental timings for SiC Mosfets, as shown in numerous literature like [90][100].

To perform STC for this turn-on transition, a unique switching scheme for the switch S_{L1} is followed, which is shown in Figure 70. Post V_{th}, and before the onset of the Miller region at t_2, the STC scheme sets the external gate resistance for a period T_{w_1} as:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}\, R_{on_2} = R_{on_1} \tag{54}$$

This is the region $t_1 - t_2$ (Appendix J). From SiC device dynamics[90], [99], [100], decreasing the region $t_1 - t_2$ causes $I_{L_a} + I_{L_b}$ to rise faster. This results in decreased switching losses for the PES by reducing the V-I overlap.

After the onset of the Miller region, a higher gate resistance is applied by STC by giving a low duty cycle to S_{L1}. The gate resistance is given by:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}\, R_{on_2} = R_{on_1} + (50\text{-}100\ \%)\, R_{on_2} \tag{55}$$

This is done for a period T_{w_2} to decrease the $\frac{dV_{ds_{M_2}}}{dt}$ fall rate to cause slower diode reverse recovery, which in turn will lead to less $\frac{di}{dt}$ induced oscillations by the reverse recovery current. After the pre-calculated period T_{w_2} in the Miller region when the diode reverse recovery has ended (Appendix J and [90], [100] derives the timings), STC applied a lower gate resistance by modulating the duty cycle of S_{L1}. The lower gate resistance is given by:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}\, R_{on_2} = R_{on_1} + (0\text{-}50\ \%)\, R_{on_2} \tag{56}$$

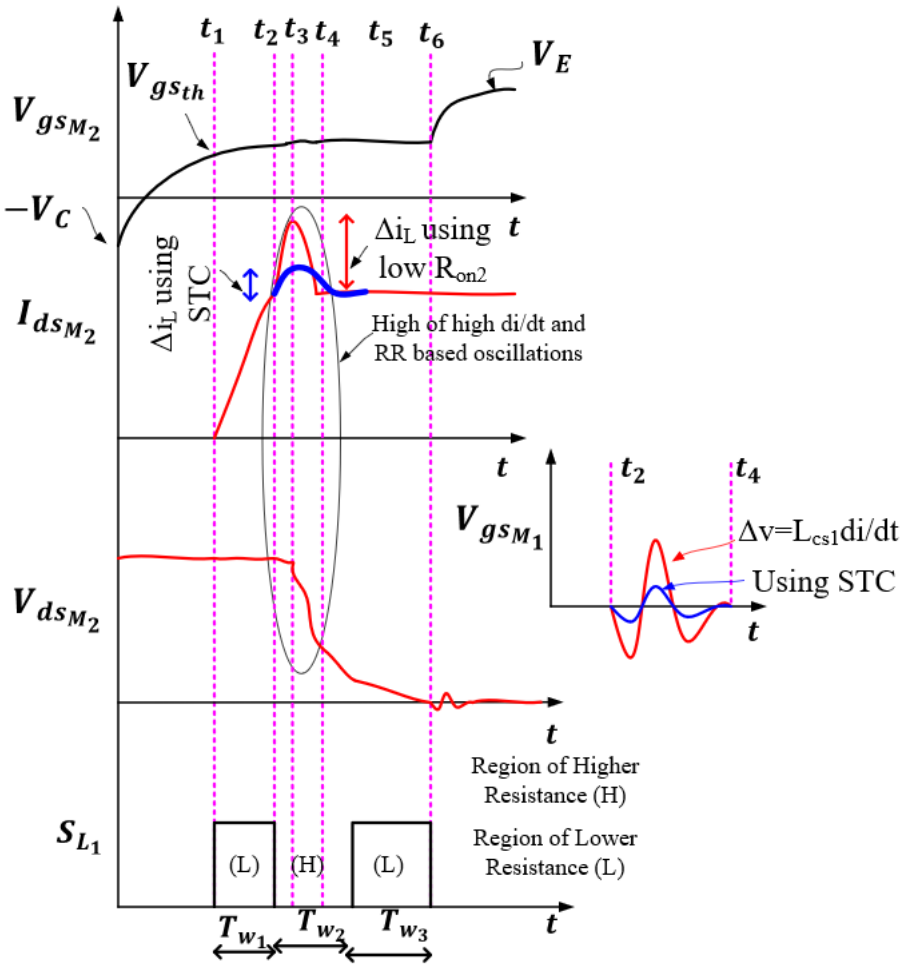


Figure 70. Waveforms for Mosfet turn-on and STC scheme for the switch S_{L_1}.

STC applies this lower gate resistance for a period T_{w_3} as shown in Figure 70 until the end of the Miller Region. This results in an enhanced rate of $\frac{dV_{ds_{M_1}}}{dt}$ fall, thereby decreasing the transition region post t_4 which leads to switching loss reduction. If a constant gate drive resistance R_{on_1}(that gives optimal damping, (1) and reference [99], [100])is used throughout the transition region, the diode reverse recovery-based oscillations lead to high current overshoot rates, which leads to the issues discussed in Section 4.2.1.

Hence, the STC scheme helps achieve optimality of Ćuk PES operation. For any operating point, depending on a particular desired dv/dt profile, STC can shape the $V_{ds_{M_2}}$ trajectory that can optimize switching losses and parasitic

oscillations that in normal cases result from decreasing switching transitions.

4.2.3. STC for turn-off transition of Ćuk PES

Contrary to the turn-on transition, the turn-off transition for the SiC module under consideration is not plagued by any diode reverse recovery effects. Also, the turn-off losses of the SiC Mosfets are much smaller than the turn-on losses. This is primarily due to the lower time constant of the turn-off phenomenon than the turn-on. For the current PES behavioral dynamics and for the test scenario, a STC scheme is not required for efficiency improvement during device turn-off mainly because of these reasons:

1) keeping a low value of the passive gate resistance results in very low overall turn-off losses for the Ćuk PES. There are two issues of using a lower value of turn-off gate resistance. First, the higher dv/dt during turn-off can lead to high common-mode currents in the PES. It can charge the parasitic capacitances between the switching node and earth, and the common-mode EMI can violate the EMI standards. It can increase the CM EMI filter size of the PES. The turn-off gate resistance for the PES was chosen accordingly and was fairly easy to optimize between CM EMI level and turn-off switching losses.

Secondly, for the current fall period (depending on SiC device physics [90], [100]), the presence of high values of L_{ds_2} in the drain-source path (Figure 68), can result in $L_{ds_2}\frac{di}{dt}$ based voltage overshoots which may cause excessive voltage stress on the device. However, for the experimental set-up under consideration, L_{ds_2} and currents are low enough not to create issues with device overvoltage stress.

2) Very importantly, the turn-off losses are less susceptible to gate resistance variation than turn-on losses. Since the gradient across the gate resistor is much smaller during the turn-off transition regions [18], a larger value of gate resistor variation is required to modify the voltage rise and current fall trajectories. Hence, the effect minor gate resistance variation provides during turn-on is not present during turn-off.

4.2.4. STC scheme and DSP implementation

The STC scheme is implemented using a simple mixed signal circuit with low complexity. For the digital signal generation, the E_{PWM} modules of TMSF28379D, a low-cost industrial-scale digital processor is used. An external combinational logic circuitry is used to affect a particular transition region. Figure 71 shows an illustrative example.

For turn-on transition control, E_{PWM1} is set as master module and is used to generate the main gate pulses of the SiC half-bridge module. To generate the S_{L1} signal, E_{PWM} modules 2,3 ad 4 are used as slave modules. All the E_{PWM} modules are positive edge triggered. The slave modules 2,3 and 4 create three phase staggered signals ($\emptyset = X_1, X_2, X_3$) having pulse widths (or turn-on time) of T_1, T_2, and T_3 respectively, with their periods being same as that of E_{PWM1} master module.

External to the processor, the three phase staggered signals from $E_{PWM2,3,4}$ are sent to a combinational logic drive to generate the final STC signals. Two important delays are considered while constituting the signals 1) $Delay_1$: denote the transmission delay between the main gate signal generated by the processor and the actual triggering of the SiC switches. 2) $Delay_{2,3,4}$: denote the transmission delay of the switching sequence between the STC signal generated by the processor and the actual triggering of the STC switches. Both these delays are mainly due to the drive stages and remain constant.

4.3. Experimental work

4.3.1. Hardware design of the STC network

The STC network is designed using low-cost discrete integrated circuits to modify the SiC device switching transitions (rising and falling) on the fly from the command of the F28379d processor. The GaN-FET switched resistor network, the schematic of which is shown in Figure 68, can modulate the switching pattern of GaN-FET based switches S_{L1} and S_{L3} (/S_{H1} and S_{H3}) to affect the net gate resistance in the gate drive turn-on and turn-off paths, respectively. For a particular operating condition of the PES, the corresponding modulating waveform guiding $S_{L1}/S_{L3}/S_{H1}/S_{H3}$ is calculated inside the F28379D processor (DSP) and sent to the gate driver of the GaN-FETs. For the switched resistor network, the GaN-FETs are chosen because:

1) The GaN-FETs have very low parasitic capacitances which can make them attain very low pulse widths. The pulse widths are much lower than the transition regions of the main SiC FET.

2) For test values of load current and blocking voltages, the SiC device transition region varies in the vicinity of 120-130 *n*s. Hence, the HF GaN-FET based switched resistor network can make multiple transitions inside the turn-on and turn-off times of the main SiC device to shape the V_{ds}-I_{ds} trajectory.

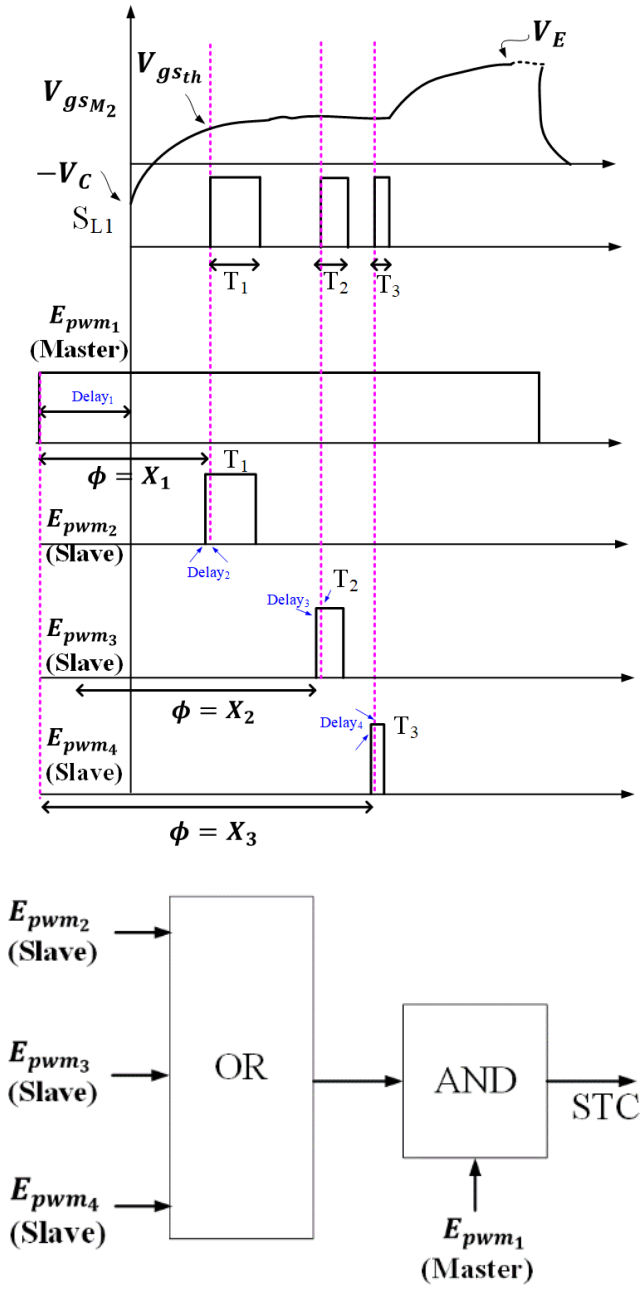
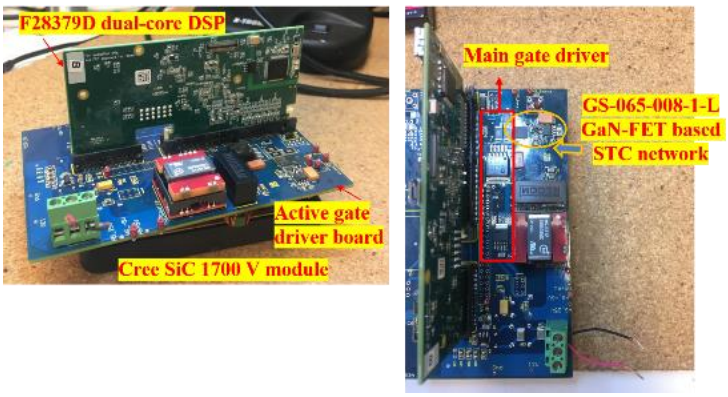


Figure 71. Figure showing the DSP implementation of the proposed STC scheme.

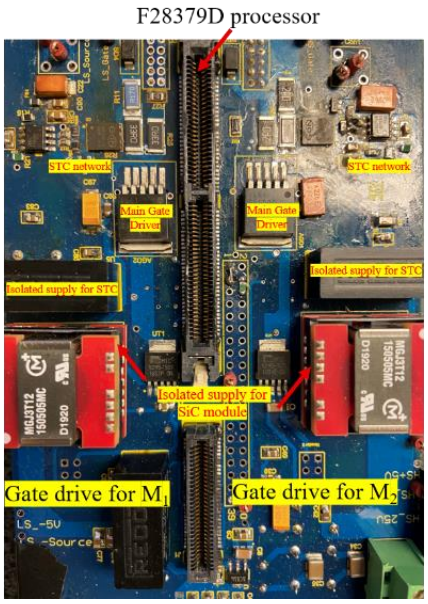
The gate driver is developed across two generations which is described below:

4.3.1.1. Gen-1 gate driver prototype (hardware description)

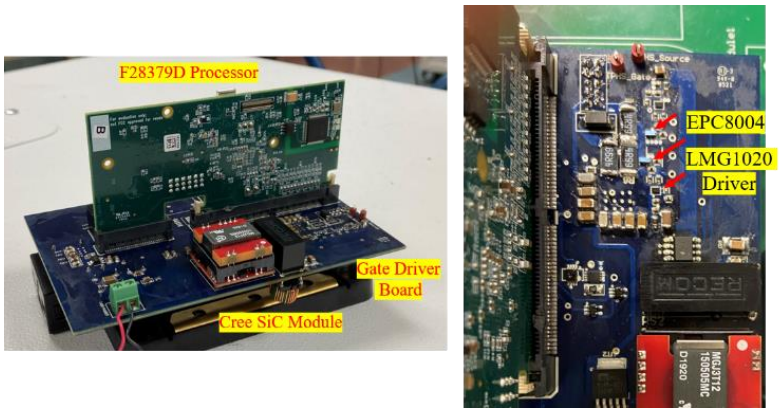
The Gen-1 and the Gen-2 design mainly differs in the design of the STC network. Faster GaN-FETs and more state-


F28379D dual-core DSP
Active gate driver board
Cree SiC 1700 V module
Main gate driver
GS-065-008-1-L GaN-FET based STC network

(a)


F28379D processor
STC network
Main Gate Driver
Isolated supply for STC
Isolated supply for SiC module
Gate drive for M1
Gate drive for M2

(b)


F28379D Processor
Gate Driver Board
Cree SiC Module
EPC8004
LMG1020 Driver

(c)

Figure 72. (a) The Gen-1 gate driver prototype. (b) Figure showing the layout of the important functionalities of the Gen-1gate driver board (c) The Gen-2 gate driver prototype.

of-the-art gate drivers are used in Gen-2 compared to Gen-1.

Figure 72a shows the Gen-1 gate driver board containing the STC network. The gate driver board houses components encompassing two separate isolated gate drive paths for each of the SiC Mosfets in the half-bridge module along with the STC network for each Mosfet in the module, along with an integrated processor to give online commands to the STC network. These important functionalities of the gate driver have been highlighted in Figure 72b.

The STC network in Gen-1 uses GS-065-011-1-L GaN-FETs with C_{rss} < 10 pF, and C_{oss} < 150 pF for the gate drive blocking voltage under consideration. The GaN-FETs are driven Si8271GB gate drivers from Silicon Labs, with separate turn-on and turn-off paths. The external gate resistance for turn-on and turn-off are set at 1 Ω each. The idea behind the design is to drive the GaN-FETs as fast as possible using low-gate resistances to attain fast transitions. Since the gate driver blocking voltages and currents are much lower than the ratings of the GaN-FETs used, the fast transitions will always ensure the operation of the device within the thermal limits. The design leads to rise transitions of 8-10 *n*s for the GaN-FETs and fall transitions of 2-3 *n*s. Hence pulse widths below 10 ns are not possible with the Gen-1 board.

4.3.1.2. Gen-2 gate driver prototype (hardware description*)*

Figure 72c shows the Gen-2 gate driver board. Like Gen-1, the new board also houses components encompassing two separate isolated gate drive paths, and the F28379D processor.

The STC network in Gen-2 uses EPC8004 GaN-FETs with C_{rss} < 2 pF, and C_{oss} < 50 pF for the gate drive blocking voltage under consideration. The EPC GaN-FETs are driven by a state-of-the-art gate driver from Texas instruments, LMG1020. The drivers and switches in the STC network is compared in Table 3.

The driver LMG1020 is used in LiDAR applications to drive fast GaN-FETs at 1 *n*s pulse-width. The external gate resistance for turn-on and turn-off are set at 10 Ω and 5 Ω respectively. The design leads to rise and fall transitions in the vicinity of 1 *n*s for the GaN-FETs. Hence the new design can achieve pulse widths well within 10 *n*s, leading to greater granularity of the STC framework.

4.3.1.3. Gen-2 v/s Gen-1

Synthesis of the GaN-FET based STC network encompasses some major HF loops which require careful design considerations. Figure 73a and Figure 73b compares the STC device and gate driver design of the GaN-FET based switches S_{L1} and S_{L3} in terms of PCB footprint and size.

As previously discussed, the switching of S_{L1} which is a GaN-FET based device, controls the dynamic resistance

Table 3. Comparison of the STC network.

	Gen-1	Gen-2
STC Device	GS-065-011-1-L	EPC8004
Device Dimensions	5, 6 mm	820, 2080 μm
STC Driver	Si8271-GB	LMG1020
Operating C_{iss}	80 pF	25 pF
Operating C_{rss}	10 pF	1.2 pF
Operating C_{oss}	150 pF	45 pF

R_{on_2} to modulate the gate current. The recommended main gate driver IC of each of the Mosfets M_1 and M_2 in the half-bridge module is rated for 14 A peak current. Hence the GaN-FET based switch was chosen for this application since it is amongst few commercially available options that can conduct the high gate current when S_{L1} is on, and due to its low parasitic capacitance can attain very low pulse widths.

However, the GaN-FET switches pose predicaments in gate and power loop design. The FETs have very low threshold voltage and a very low margin between optimal and maximum allowable gate voltage. An ill-designed gate and power loop may cause a false turn-on of the device, defeating the key objective of STC. Figure 73c identifies two key loops, Loop-1 and Loop-2 that requires careful design considerations both in the Gen-1 and Gen-2 boards.

(a) *Loop-1:* Loop-1 mainly involves the gate drive design for the GaN-FET network. The GaN-FET in Gen-1 is driven by an isolated gate driver, with separate turn-on and turn-off paths. To reduce PCB design complexity, a single positive supply gate driver was used, and the PCB design was carefully optimized to reduce spurious swings of the gate to source voltage waveforms. Also, the GaN-FET is chosen to have a dedicated Kelvin source that perfectly

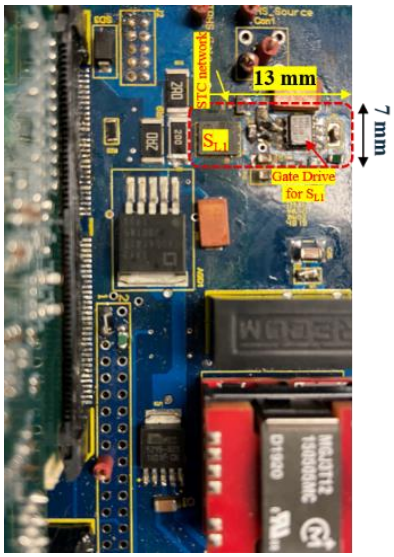
decouples the gate and the power loop. Using the relation $R_{init_{GaN}} + R_{ext_{GaN}} \geq 2\rho_{GaN}\sqrt{\frac{L_{int}+L_{ext}}{C_{iss}}}$, the gate loop was designed for minimum $R_{ext_{GaN}}$ to get the fastest transition times possible [99]. $R_{init_{GaN}}, R_{ext_{GaN}}$ denote the internal and external values of the resistances in the gate drive circuit (lumped together as R_g in Figure 73c), while $L_{int_{GaN}}, L_{ext_{GaN}}$ (lumped together as L_{gs} in Figure 73c) denote the internal and external values of the parasitic inductances in the gate

Table 4. Comparison of the Gate Drivers

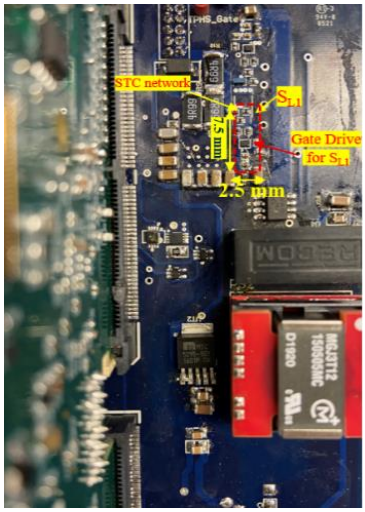
	Gen-1	Gen-2
Gate Driver	Si8271-GB	LMG1020
Dimensions	3.9,4.9 mm	0.8,1.2 mm
Source *I*	4 A	7 A
Sink *I*	2 A	5 A
Rise time	6 *n*s	400 *p*s
Propagation Delay	60 *n*s	4.5 *n*s (max)

drive circuit. In the Gen-1 board, using a 5 V constant gate drive supply, and a very low gate resistance of $R_g < 2\ \Omega$, theoretically transition times of less than 5 *n*s can be achieved. However, for the gate drive circuit shown in Figure 73a, the gate source inductance L_{gs} (due to larger GaN-FET package) and common source inductance L_{cs} slowed down the switching transitions considerably, resulting in rise transitions of 8-10 *n*s and fall transitions of 3 *n*s. This put a limit on the maximum pulse width of the GaN-FETs that can be achieved in the Gen-1 board, and thus limited the STC granularity.

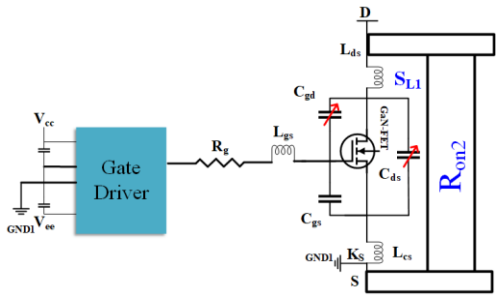
The shortcomings of Gen-1 is addressed in Gen-2 by carefully designing the gate drive loop. Gen-2 uses EPC8004 GaN-FETs (from EPC) which has much smaller footprint than GS-065-011-1-L GaN-FETs from GaN Systems (the comparison is shown in Figure 73a and Figure 73b). Compared to the Gen-1 gate drive design which used 0603 resistors for R_g, Gen-2 uses even smaller 0402 footprints, thereby considerably limiting the inductance L_{gs}. Also, due to smaller package of EPC8004 GaN-FETs, the common source inductance L_{cs} is bound to have smaller value in Gen-2, although both the designs uses Kelvin source connections.



(a)



(b)



(c)

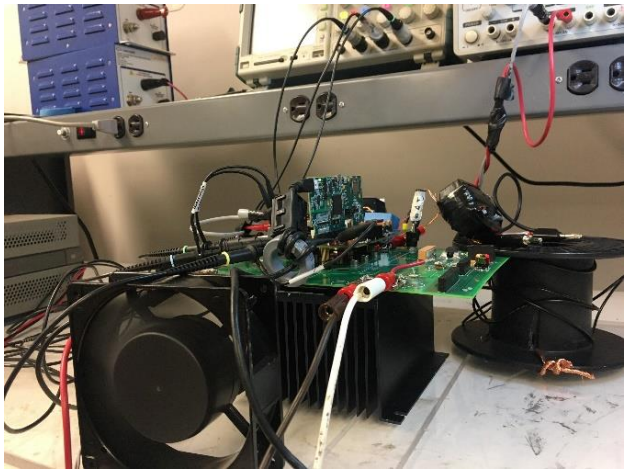
Figure 73. (a) and (b) Figure showing the turn-on switching transition schematics involving the high-speed GaN-FETs in Gen-1 and Gen-2 gate

driver boards. (c) GaN-FET gate drive for STC.

Gen-2 encompasses another important design change in choice of the gate driver. Gen-2 makes uses of LMG1020 gate driver. The miniaturized gate driver specialized for Lidar applications can create pulse widths of about 1 *n*s (driving an input capacitance like EPC8004 GaN-FETs) and has greater source/sink current capability than the Si8271-GB counterpart. Using a 5 V constant gate drive supply like Gen-1, and a gate resistance of R_g = 10/5 Ω for turn-on/off, theoretical, and practical rise times of 600 *p*s/ 1 *n*s are achieved, respectively.

Hence, use of EPC8004 FETs and LMG1020 driver gives greater granularity to the change of the gate resistance in the transition region compared to Gen-1. The most important parameters of the gate driver are compared in Table 4.

(b) *Loop-2:* The Loop-2 mainly dictates the maximum slew rate of the GaN-FETs that can be achieved. Loop 2 inductance is quite critical since it affects the FET switching behavior the most. The gate resistors, as shown in Figure 73a and Figure 73b, are placed close to the GaN-FET switches to minimize the stray inductance L_{ds} (Figure 73c). Loop-2 is a relatively high current loop and makes/breaks currents as high as 4-6 A in nanoseconds. This causes relatively high $\frac{di}{dt}$ of about 4-6 A/*n*s. The high $\frac{di}{dt}$ can couple with the common source inductance L_{cs} creating a negative feedback loop, thereby slowing down the GaN-FET and deteriorating the performance of the STC network. Hence the use of Gen-2 STC network is quite important in this regard in creating a design with minimal common source inductance L_{cs} (Figure 73c).



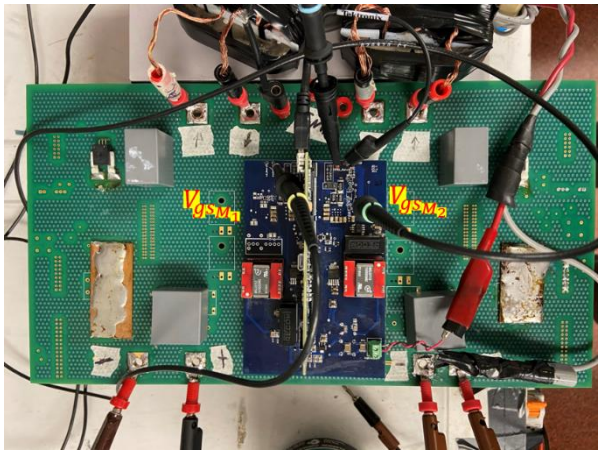
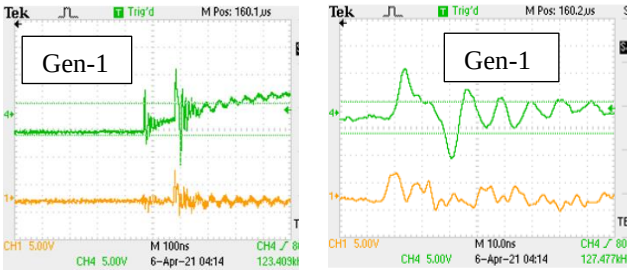


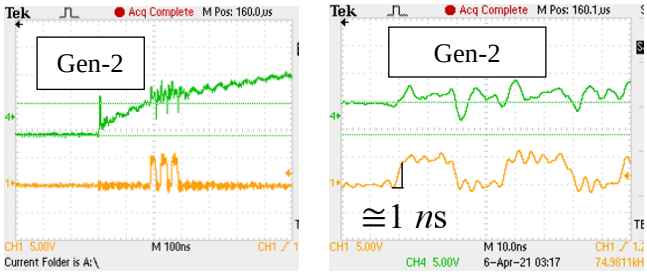
Figure 74. Figure showing the STC hardware validation platform. The V_{gs} signals (probed) of the SiC half-bridge module in the actual hardware platform is shown. The hardware is tested up to 5 kW and switching frequency of 50 *k*Hz.

4.3.2. Hardware platform for experimental validation

Figure 74 shows the hardware platform of the WBG Ćuk PES set-up that is used to test the gate drivers, Gen-1, and Gen-2. It consists of Cree SiC half-bridge modules driven by the STC based gate driver board. Figure 74 also shows the V_{gs} signals (probed) of the SiC half-bridge module in the actual hardware platform. $V_{gs_{M_2}}$ refers to the gate to source voltage of the low-side SiC Mosfet in the half-bridge module (in Figure 68), while $V_{gs_{M_1}}$ refers to the high-side SiC Mosfet gate to source voltage (in Figure 68). Referring to Figure 68, the resistive parameter values of the gate drive path are given $R_{on_1} = 1\ \Omega$, $R_{on_2} = 6.2\ \Omega$, and $R_{off} = 2\ \Omega$. As discussed in Section 4.2.2, R_{on_1} is fixed, while R_{on_2} and R_{off} can be modulated by GaN-FET based switches S_{L1} and S_{L3}. (Here only modulation of S_{L1} is considered as discussed in Section 4.2.2 and 4.2.3).



(a) (b)



(c) (d)

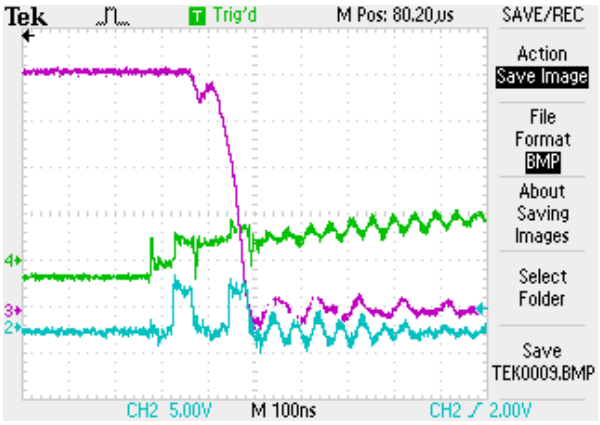
Figure 75. (a)-(d) Comparison between Gen-1 and Gen-2 gate driver board performances. The traces from top to bottom show $V_{gs_{M_2}}$ and S_{L_1}. (a), (b) and (c),(d) show same waveform but with different time resolutions. $V_{gs_{M_1}}$(5 V/div), S_{L_1}(5 V/div). Test levels, $V_{ds_{M2}} = V_{ds_{M1}}$ = 500 V, $I_{ds_{M2}} = I_{ds_{M1}}$ = 20 A.

Figure 75 shows the difference in performance between Gen-1 and Gen-2 gate driver boards. S_{L1} is switched to create a pulse width of 10 *n*s on, and 10 *n*s off. Figure 75a and Figure 75b shows the performance of Gen-1 gate driver board at time resolution of 10 *n*s and 100 *n*s, respectively. Gen-1 gate driver gives poor performance for the reasons discussed in Section 4.3.1.2 and Section 4.3.1.3. Figure 75c and Figure 75d shows the performance of Gen-2 gate driver. It gives satisfactory system performance in gate resistance variation. Figure 75d shows that the Gen-2 design can indeed achieve rise time of 1 *n*s. Pulse widths of less than 10 *n*s is a limitation on the part of F28379D processor, and with faster digital processors with higher clock speeds, even 2-3 ns pulse widths can be obtained leading to more granularity of the STC network.

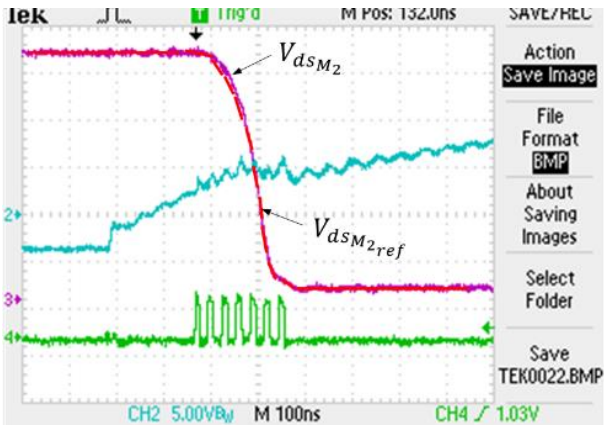
4.3.3. Turn-on transition control

In Figure 76, the effect of controlling the turn-on switching transition is shown. Figure 76a and Figure 76b compares the performance of Gen-1 and Gen-2 board in controlling the $V_{ds_{M2}}$ falling transitions for the same operating point $V_{ds_{M2}} = V_{ds_{M1}}$ = 500 V, $I_{ds_{M2}} = I_{ds_{M1}}$ = 20 A. As discussed in Section 4.3.1.3, due to several design modifications in Gen-2 gate drive, STC achieves better granularity in control of the STC pulse widths and achieves better noise immunity. Compared to only two transition events for the Gen-1 board, Gen-2 could achieve far more transitions that results in tighter control for a pre-defined $V_{ds_{M2}}$ trajectory.

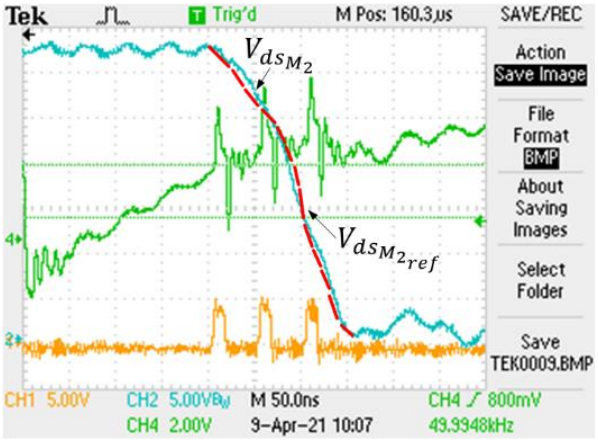
In Figure 76b, $V_{ds_{M2ref}}$ denotes a reference $V_{ds_{M2}}$ trajectory. The trajectory denotes the $V_{ds_{M2}}$ transition for R_{ext}= 4 Ω. Now, STC modulates the switch SL_1 to create the same trajectory using dynamic resistance $R_{ext} = R_{on_1} +$



(a)



(b)



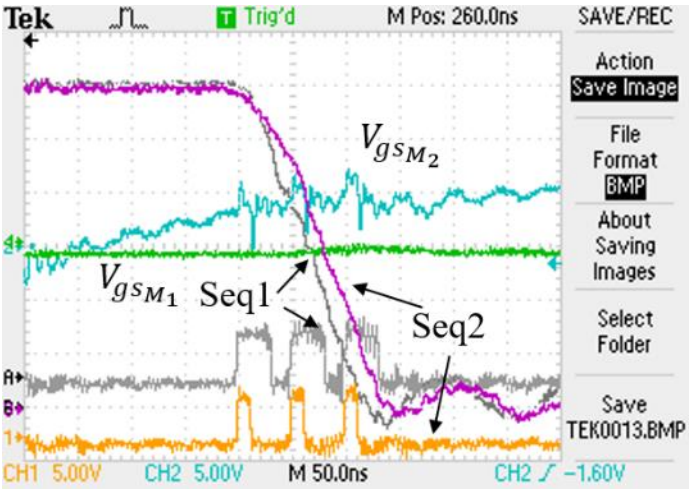
(c)

Figure 76. (a) Figure showing the turn-on transition control using STC for the Gen-1 board. The traces 2,3 and 4 show the $V_{ds_{M_2}}$ (100 V/div), $V_{gs_{M_2}}$ (5 V/div), and SL_1(5 V/div), respectively. Figure showing the turn-on transition control using STC for the Gen-2 board to follow a $V_{ds_{M_2}}$ trajectory (a) for 7 transition levels (b) for 3 transition levels. The traces 1, 2 and 4 in (a) show SL_1(5 V/div), $V_{gs_{M_2}}$ (5 V/div) and $V_{ds_{M_2}}$ (100 V/div), respectively, and in (b) show SL_1(5 V/div), $V_{ds_{M_2}}$ (100 V/div) and $V_{gs_{M_2}}$ (2 V/div), respectively.

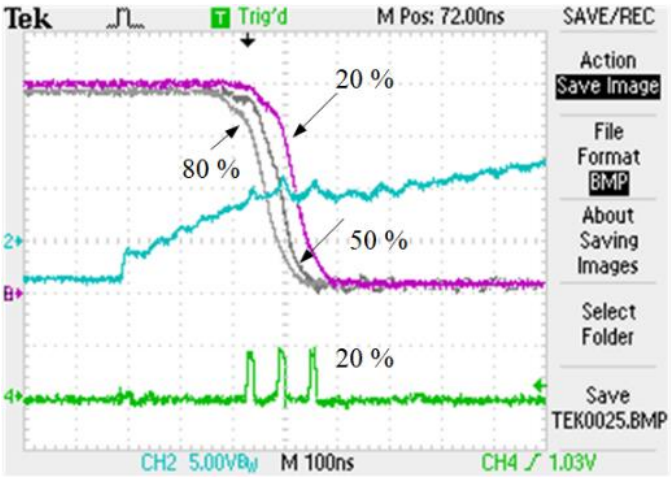
$\overline{S_{L1}}\ R_{on_2}$. Since R_{on_1}= 1 Ω, and R_{on_2}= 6.2 Ω, STC selects the switching sequence for switch SL_1 in a way to create an average resistance of $R_{on_1} + 0.4R_{on_2}$= 4 Ω. Figure 76c also shows a $V_{ds_{M2}}$ trajectory tracking using STC, but with decreased granularity of the switch SL_1. Increased granularity of the STC drive, achieves more smoother tracking of $V_{ds_{M2}}$, as depicted in Figure 76b compared to Figure 76c. In Figure 76c, the switch SL_1 has 35 % duty cycle, which coarsely leads to an external resistance of 5 Ω. $V_{ds_{M2ref}}$ denotes a reference trajectory for fixed R_{ext} = 5 Ω.

Figure 77a further shows how two different sequences of STC switch S_{L_1} (namely Seq1 and Seq2) can generate different $V_{ds_{M2}}$ falling trajectories. A higher duty cycle for the STC switch results in lower gate resistance and higher

transition speeds (Eqn. 2). Several such $V_{ds_{M2}}$ falling trajectories are shown in Figure 77b as the duty cycles for the STC switch are varied.



(a)



(b)

Figure 77. (a) Figure showing how different sequences can create different V_{ds} slopes during the turn-on transition. Seq_1 and Seq_2 denote the state of STC switch S_{L_1}. The scales are as follows: $V_{ds_{M_2}}$ (100 V/div), $V_{gs_{M_2}}$ (5 V/div), and SL_1(5 V/div), respectively. (a) Figure showing different $V_{ds_{M_2}}$ transition slopes as function of duty cycle of STC switch S_{L_1}. Traces 3,2,4 show $V_{ds_{M_2}}$ (100 V/div), $V_{gs_{M_2}}$ (5 V/div), and SL_1(5 V/div), respectively.

4.3.3.1. Reduction in gate loop oscillations due to common source inductance and efficiency improvement

As discussed in Section 4.2.1, decreasing the gate resistance to decrease the switching losses causes severe dv/dt and di/dt induced oscillations in the gate drive of the high-side switch M_1 (Figure 68) in the Ćuk PES. For the SiC module and topology under consideration, the oscillations due to the common source inductance (L_{CS1}) (di/dt induced)

is a bigger issue than the Miller charging current (dv/dt induced). Figure 78a shows the gate drive signal of the high-side switch M_1 ($V_{gs_{M1}}$) when the low-side switch is turning on ($V_{gs_{M2}}$) at $R_{ext} = R_{on_1} + \overline{S_1}\, R_{on_2} = R_{on_1} = 1\ \Omega$. It shows severe ringing which persists even in Figure 78b, when an active Miller clamp is applied to the high-side switch M_1 which proves that the oscillations are due to the large common source inductance L_{CS1}(di/dt induced). Using the STC scheme, as delineated in Section 4.2.2 (methodology), Section 4.2.4 (DSP implementation), and Section 4.3.3.1

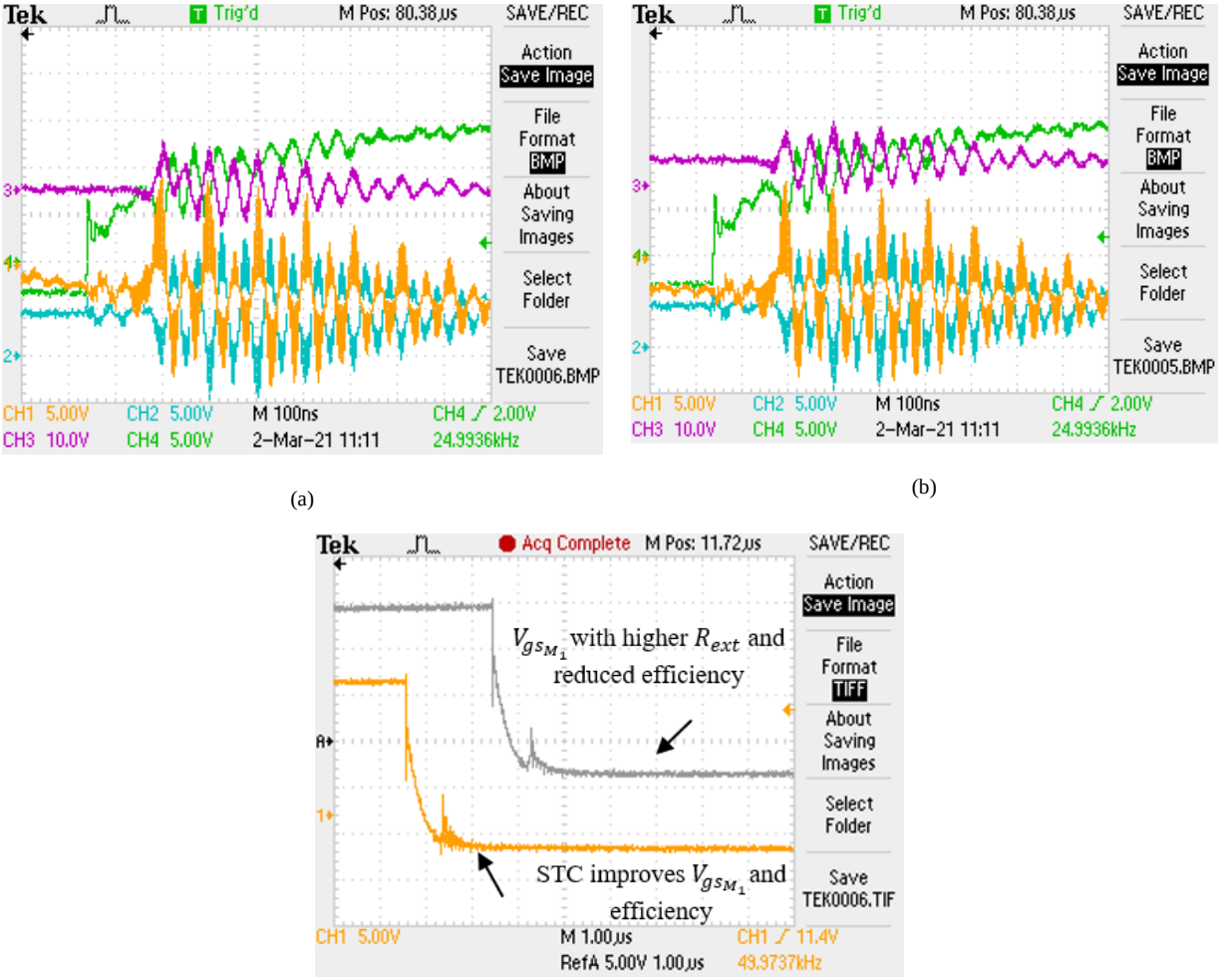


Figure 78. (a) Figure showing the gate source oscillations resulting due to reduced gate resistance. (b) Figure showing persistent gate oscillations even with implementation of active Miller clamp. The traces 1-4 show V_{gs_2}, V_{gs_1}, SH_3 and SL_1. SH_3 is turned on to give a low impedance path to the current discharging C_{gd_1}. In (a) and (b), SL_1 is turned on decrease the turn on resistance of switch M_2.(c) Figure showing reduced oscillations in gate source due to the STC scheme.

(V_{ds} tracking results), the gate drive response of high-side switch M_1 in Figure 78c is obtained (lower trace). It is

compared to the upper trace in Figure 78c which shows the scenario when a higher gate resistance $R_{ext} = R_{on_1} + \overline{S_{L1}}\, R_{on_2} = R_{on_1} = 7\ \Omega$ is applied. Hence, STC creates a scenario where a lower gate resistance can be applied to parts in the SiC transition region to increase PES efficiency while reducing gate-source oscillations.

4.3.3.2. STC improves PES efficiency

Figure 79 shows the constant efficiency increment of over 1% with increasing power levels achieved by the STC turn-on control scheme for the Ćuk PES, as delineated in Section 4.2.2. For the experimental result in Figure 79, with the drain to source voltage of 500 V of the lower side switch M_2, the switch currents are gradually increased. The improvement of efficiency is compared to a fixed gate resistance of R_{ext} = 7.2 Ω. When a smaller value of the gate resistor R_{ext} =1 Ω is used, the gate source oscillations increase to such high levels that the PES cannot be operated above 10 A peak, as shown in Figure 79. From an efficiency standpoint, although a fixed gate resistor R_{ext} =1 Ω will give higher efficiency numbers than STC initially, however, the severe di/dt induced oscillations will cause extra conduction losses in the system. Moreover, the oscillations lead to more V-I overlap, at the transition leading to increased switching losses too.

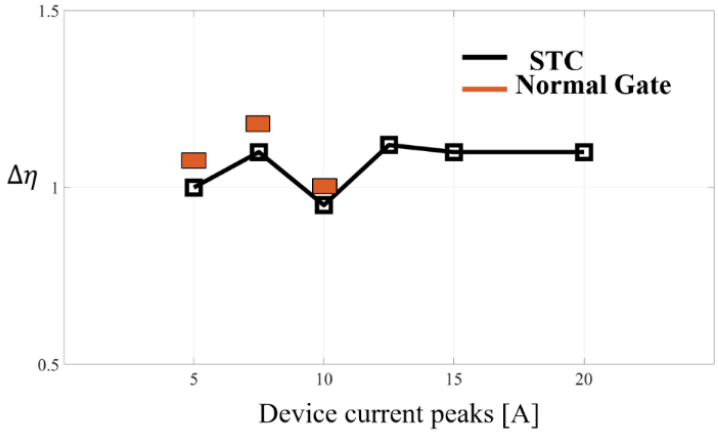


Figure 79. Figure showing improvement of PES efficiency at V_{ds_2} = 500 V.

4.4. Conclusion

An STC framework is created to affect turn-on transition of a WBG PSD and to meet a PES level target (which in this case is an efficiency increment). First depending on PES topological behavior and device physics, optimization areas to meet this target are identified and then the STC scheme is synthesized accordingly. For the test HF Ćuk PES,

the STC network achieved optimality of performance in terms of switching losses and diode reverse recovery stresses to meet the system level target. STC network achieved this optimality and gave satisfactory performance for the test operating conditions.

Contrary to a contemporary analog technique based active gate drives, the proposed STC takes a simple mixed-signal approach in driving a GaN-FET switched resistor-based gate drive using commands from an industrial scale processor, and easily procurable discrete components. The STC network differentiates itself from conventional switched resistor network based on the operational principle. Instead of using multiple resistors in a gate drive to achieve granularity that increases PCB gate drive footprint to the point of infeasibility, the STC network uses an extremely HF device and state of the art fast gate drivers to create an averaged gate resistance in a targeted transition region.

5. CONCLUSIONS AND FUTURE WORK

5.1. Summary of Contributions

In this dissertation, approaches for switching sequence-based and switching transition control for a high-frequency higher-order power electronic system is delineated. The control architectures are multi-scale in nature. In contrast to conventional control schemes in power electronic systems that are based on averaged PES models, switching sequence-based architecture goes beyond average dynamics control of a system to controlling fast-scale PES properties like switching losses, EMI etc. However, such controllers face issues with high computational burden as switching frequencies of wideband gap system are continually increasing. This dissertation helps in making such controllers mainstream by implementing them in low-cost industrial processors and at relatively high frequencies. The dissertation also shows how such controllers can go beyond control of challenging loads in higher-order non-minimum PES, to superior spectral shaping of the converters. The work of PES spectral shaping reduces EMI filter size which may be of importance for operating the ultra-fast-transition recent wide-bandgap semiconductor devices at higher power with increasing switching frequencies, that is usually desirable for reduced power density and switching losses.

Having established the superior nature of such switching sequence control architectures, the dissertation also tries to control the switching transition of WBG power electronic system to meet system level requirements of a converter. The following sections summarize the contribution of each chapter succinctly.

5.1.1. Switching sequence control for non-linear loads

In this chapter, to address the challenges in control design for a PES driving challenging pulsating and constant power loads, an optimal switching-sequence-based control scheme is formulated which applies stability-bound switching sequence(s) to the PES. To reduce the real-time computation time requirements of such optimal controllers, detailed reachability analysis is performed. The overall control scheme is implemented on a series of very low-cost industrial DSPs, which also implements an observer to preclude the need for plurality of sensors for the higher-order PES. The overall performance of the controller is found to be satisfactory under varied dynamical conditions. It is shown how the switching sequence controller stabilized systems when the normal controllers failed.

5.1.2. Using control as solution to affect fast scale PES properties

After stabilizing fast time-varying and reduced damped loads, it is investigated whether such SS based control laws can shape the conducted EMI spectra of a PES. The motivation behind the work is as follows: the switching frequencies of WBG power converters are increased to reduce the size of passives. Notwithstanding, this increases the DM and CM EMI of the PES which leads to larger CM/DM filter. This negatively impacts the power density of the WBG PES which was supposed to increase with higher switching frequencies.

It is seen that the careful design of such SS based control laws offers higher programmability to PES design where EMI filters have been traditionally used to reduce EMI of switching power converters. The SS control offers EMI mitigation across wide operating regions, without compromising PES regulation and tracking. The work has ramifications in reducing the EMI filter size of WBG power converters when they are operated at higher frequencies.

5.1.3. Going beyond switching sequence to switching transition

The final chapter of the dissertation encompasses design of a switching transition-based control scheme to shape the rise-fall transitions of the switching sequences of the WBG devices. The transitions are shaped in a way as to create optimality between increased device stress and switching losses of a PES. Contrary to prevalent schemes, where the effect of varying the switching transition of devices is studied under a double-pulse set-up, the STC scheme developed helped meet system level requirements of a HF PES.

5.2. Future research possibilities

The work done in this dissertation is based on a dc/dc Ćuk PES. One major future possibility is to extend it to other quadrants of PES operation. The work can be seamlessly extended to control battery chargers, and solar inverter applications. Also, such controllers can be used to control networked systems. For battery charging applications in electric vehicle, such control applications can result in far better transient and steady state performance. It is still a research issue on how the computational burden of these controllers will evolve with higher number of switches, and how to implement such controllers in low-cost processors. For networked systems, using monolithic cost objective, these controllers can manage satisfactory current and voltage sharing. For such systems, future research can be carried out on how to synthesize such controllers.

Another major research issue is the synthesis of the cost objective for such controllers. Since such controllers can

incorporate terms ranging from voltage regulation to loss minimization in the cost-objective, tuning the weighing terms in the cost-objective remains a challenge. Limited literature is available on tuning the cost objectives of such controllers. In this dissertation, the cost-objectives have been tuned online for a particular application and objective, but a more generalized procedure is required.

When it comes to switching transition controllers, the work done in this dissertation can be extended in two possible ways:

1) The present work makes use of industrial scale digital processor to realize the STC scheme. Although experimental results show that the STC network devices can achieve 1 *n*s transition speeds, but the pulse widths are limited by the processor to around 10 *n*s. Hence a faster processor can be used to achieve even higher level of granularity of the STC scheme.

2) The present work delineates an open-loop STC scheme. Pre-calculated transition times are used by the processor to achieve some system level goals. Hence, in future, there lies an opportunity to create a closed-loop STC controller, which depending on an online transition trajectory and real-time HF sensing, can control the STC network to perform closed-loop operation.

6. APPENDICES

Chapter 2

Appendix A

The matrices $\hat{A}_k$ and $\hat{B}_{kn}$ for the two switching states of the Ćuk-PES, expressed as $\hat{A}_{kn1}$ and $\hat{B}_{kn1}$ and $\hat{A}_{kn2}$ and $\hat{B}_{kn2}$, respectively, are defined below, where the symbols of the passive components have been defined in Figure 9.

$$\hat{A}_{kn1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_1}\left(2 + \frac{C_1}{2\,C_2}\right) & \frac{-1}{L_2} \\ 0 & \frac{-2}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_{out}} & 0 & -\frac{1}{RC_{out}} \end{bmatrix}, \hat{B}_{kn1} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \hat{A}_{kn2} = \begin{bmatrix} 0 & 0 & \frac{1}{L_1}\left(-1 - \frac{C_1}{4C_2}\right) & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{out}} & 0 & -\frac{1}{RC_{out}} \end{bmatrix}, \hat{B}_{kn2} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The pulsating load dynamics are incorporated into the system state-space to form the matrices A_{kn} and B_{kn} for a switching state. The pulsating load dynamics are expressed as harmonic series as in (A1). The states of the dynamics of the m^{th} harmonic component can be expressed as follows:

$$y_{m1} = \{a_m \cos(w_m t) + b_m \sin(w_m t)\} \tag{A1}$$

$$\frac{dy_{m1}}{dt} = \{-a_m w_m \sin(w_m t) + b_m w_m \cos(w_m t)\} = y_{m2} \tag{A2}$$

$$\frac{dy_{m2}}{dt} = \{-w_m a_m w_m \cos(w_m t) - w_m b_m w_m \sin(w_m t)\} = -w_m^2 y_{m1} \tag{A3}$$

Using (A2) and (A3), the states of the harmonic components are combined with $\hat{A}_{kn}$ and $\hat{B}_{kn}$ to form the state-space for the entire system. Matrices A_{kn} and B_{kn} for the two switching states of the system, expressed as $A_{kn1}$and B_{kn1} and A_{kn2} and B_{kn2}, respectively, have been written below, where m can vary from 1 to ∞:

$$A_{kn1} = \begin{bmatrix} \hat{A}_{kn1} & 1 & 0 & . & . & 1 & 0 \\ 0 & 0 & 0 & . & . & 0 & 0 \\ 0 & -w_1^2 & 0 & . & . & 0 & 0 \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ 0 & 0 & 0 & . & . & 0 & 1 \\ 0 & 0 & 0 & . & . & -w_\infty^2 & 0 \end{bmatrix}, B_{kn1} = \begin{bmatrix} \hat{B}_{kn1} + (1/2) i_{load1} \\ 0 \\ 0 \\ 0 \\ . \\ . \\ 0 \end{bmatrix}, A_{kn2} = \begin{bmatrix} \hat{A}_{kn2} & 1 & 0 & . & . & 1 & 0 \\ 0 & 0 & 0 & . & . & 0 & 0 \\ 0 & -w_1^2 & 0 & . & . & 0 & 0 \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ 0 & 0 & 0 & . & . & 0 & 1 \\ 0 & 0 & 0 & . & . & -w_\infty^2 & 0 \end{bmatrix}, \quad B_{kn2}$$

$$= \begin{bmatrix} \hat{B}_{kn2} + (1/2) i_{load1} \\ 0 \\ 0 \\ 0 \\ . \\ . \\ 0 \end{bmatrix}$$

Chapter 2

Appendix B

The derivation of (8) starting with (7) is delineated in detail below:

$$\nabla V_k(e) = \sum_{n=1}^{h} \alpha_{kn} \left((A_{knd} e(j) + B_{knd})^T P_{kn} (A_{knd} e(j) + B_{knd}) \right) - e(j)^T P_{kn} e(j))$$

$$= \sum_{n=1}^{h} \alpha_{kn} \left((e(j)^T A_{knd}^T + B_{knd}^T) P_{kn} (A_{knd} e(j) + B_{knd}) \right) - e(j)^T P_{kn} e(j))$$

$$= \sum_{n=1}^{h} \alpha_{kn} \left((e(j)^T A_{knd}^T P_{kn} + B_{knd}^T P_{kn}) (A_{knd} e(j) + B_{knd}) \right) - e(j)^T P_{kn} e(j))$$

$$\nabla V_k(e) = \sum_{n=1}^{h} \alpha_{kn} \left(e(j)^T A_{knd}^T P_{kn} A_{knd} e(j) + e(j)^T A_{knd}^T P_{kn} B_{knd} + B_{knd}^T P_{kn} A_{knd} e(j) + B_{knd}^T P_{kn} B_{knd} \right)$$

$$- e(j)^T P_{kn} e(j))$$

$$\nabla V_k(e) = \sum_{n=1}^{h} \alpha_{kn} \left(e(j)^T (A_{knd}^T P_{kn} A_{knd} - P_{kn}) e(j) + e(j)^T A_{knd}^T P_{kn} B_{knd} + B_{knd}^T P_{kn} A_{knd} e(j) + B_{knd}^T P_{kn} B_{knd} \right)$$

$$\nabla V_k(e) = \textstyle\sum_{n=1}^{h} \alpha_{kn} \begin{pmatrix} e(j) \\ 1 \end{pmatrix}^T \begin{bmatrix} (A_{knd}^T P_{kn} A_{knd} - P_{kn}) & A_{knd}^T P_{kn} B_{knd} \\ B_{knd}^T P_{kn} A_{knd} & B_{knd}^T P_{kn} B_{knd} \end{bmatrix} \begin{pmatrix} e(j) \\ 1 \end{pmatrix}. \quad \text{(A4)}$$

Chapter 2

Appendix C

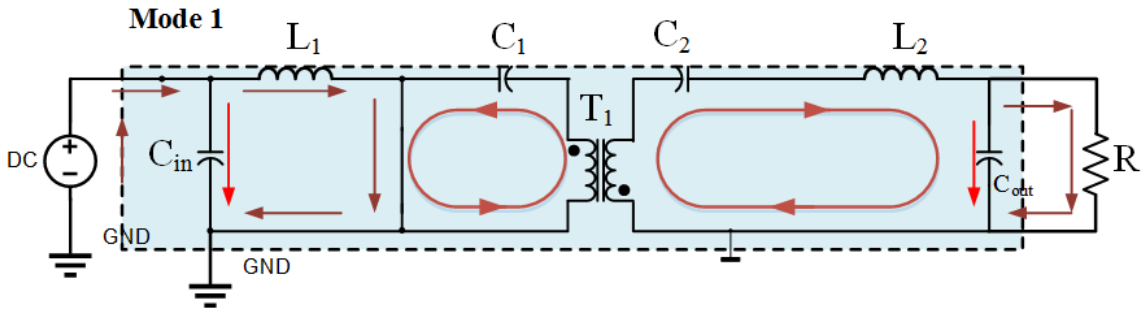
The modes of operation of the isolated Ćuk converter, which is the PES under consideration (i.e., Ćuk-PES), is discussed here succinctly. There are primarily two modes of operation, namely modes 1 and 2. The operation in the modes will be highlighted next.

Mode 1

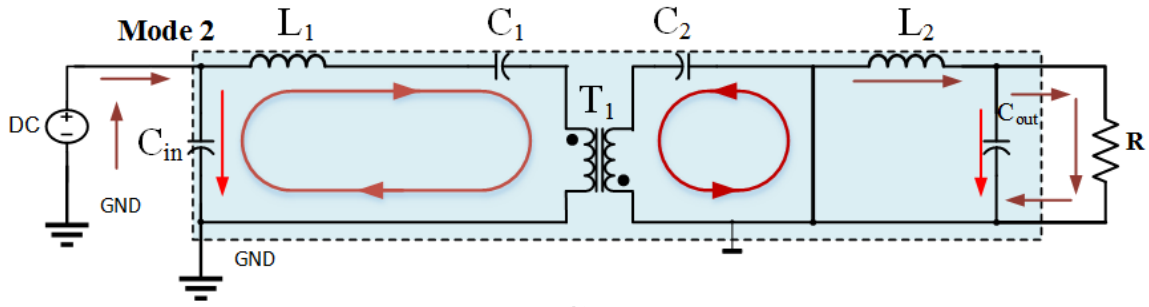
In mode 1, the primary switch of the Ćuk-PES is turned on. The current flowing through the primary side inductor L_1 increases and it stores energy. The capacitor C_1 discharges through the primary side switch resulting in a transfer of energy from the primary to the secondary side of the transformer. The energy stored in the capacitor C_2 is discharged to the circuit formed by L_2 , C_{out} and the load R. Figure A1a shows mode 1 of operation.

Mode 2

In mode 1, the primary switch of the Ćuk-PES is turned off and the secondary side switch is turned on. The primary inductor discharges to the primary and secondary blocking capacitors. The output inductor, which was charged in mode 1, relinquishes the charge to the output capacitor and the load R. Figure A1b shows mode 2 of operation.



(a)



(b)

Figure A1. (a) and (b) Modes of operation of the Ćuk-PES.

Chapter 2

Appendix D

The high-frequency transformer in the Ćuk-PES has a finite leakage of 300 *n*H referred to the primary side and a magnetizing inductance of 150 μH which are not incorporated in the prediction model. The leakage inductance is neglected given that it is significantly smaller compared to the series input inductance of the system. To test the efficacy of the reduced-order model used for prediction that does not encompass the magnetizing inductance (L_m), we compare the open-loop Bode plot of the prediction model with that obtained using Saber, which is a powerful system circuit simulator. A detailed simulation model using all the non-idealities, as shown in Figure 9, is constructed in Saber and the responses are compared. The responses, shown in Figure A2, almost match one another within the bandwidth of interest, thereby proving the efficacy of the prediction model.

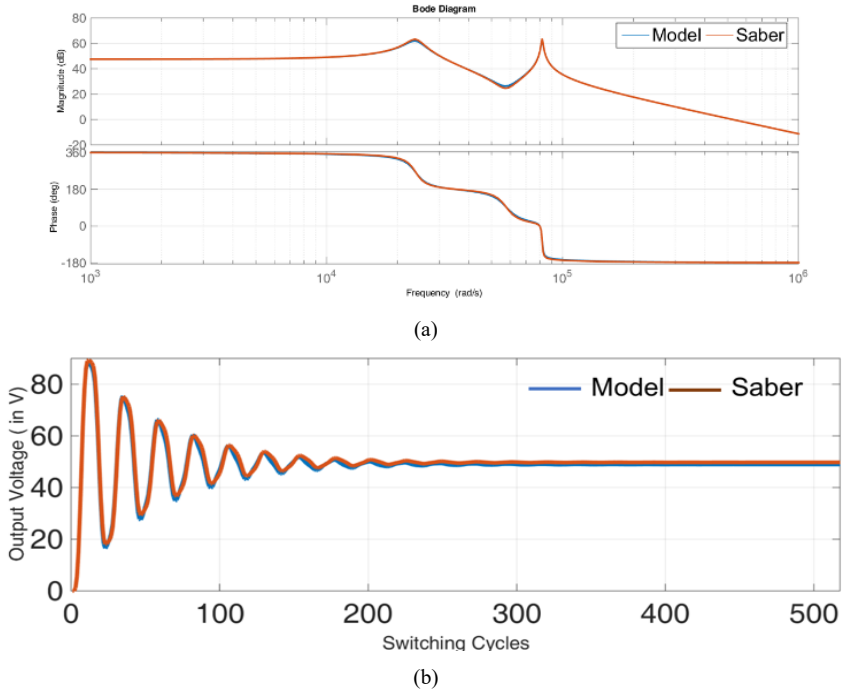


Figure A2. Comparison of (a) the open-loop Bode plot of $\hat{V}_{out}/\hat{\alpha}_{11}$ and (b) the output voltage predicted by the reduced-order model with that by Saber software simulation.

Chapter 2

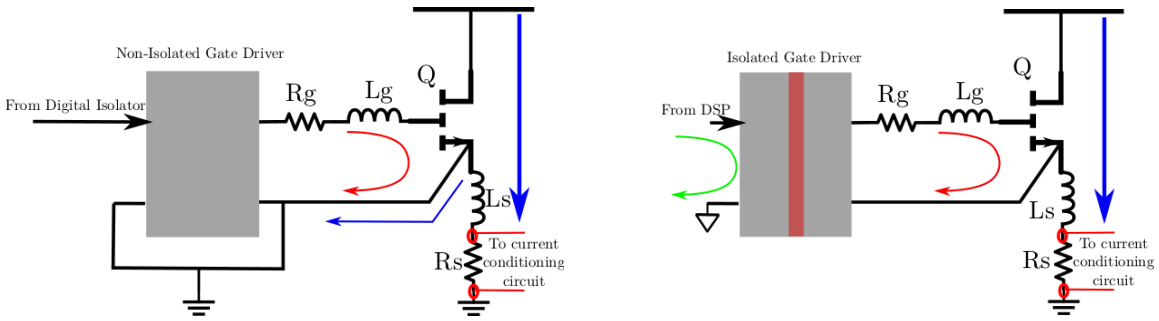
Appendix E

The protection scheme designed in this dissertation for the HF GaN-based PES is depicted in this Section. Apart from the protection features, most of the design intricacies are covered in [33].

High-speed bi-directional overcurrent and overvoltage protection schemes for a GaN-FET-based power electronics system (PES) are designed so that control algorithms can be seamlessly executed in the hardware set-up. Since low-cost resistive sensing is used as a current measurement technique at device source terminal, the effect of using isolated and non-isolated gate drivers for the GaN-FETs is explored. Drain-source differential voltage measurement is used for detecting the overvoltage fault. Current and voltage conditioning circuits along with the required analog logic for fault detection and rapid fault isolation have been delineated. Experimental results demonstrating the effectiveness of the designed protection scheme have been included in this Section.

AE1. Operating principle of overcurrent protection

Design of the overcurrent protection for GaN-based PES is particularly challenging because of their high $\frac{di}{dt}$ ratings. While switching large current, high $\frac{di}{dt}$ results in considerable voltage drop across the parasitic inductances and cause HF oscillations in the switching waveforms. Furthermore, adding current sense resistors in the HF current path adds to the already present PCB parasitic inductance and negatively impacts the magnitude of the HF oscillations. In case of a GaN-FETs featuring Kelvin source connection, if operated using a non-isolated gate driver, this increased parasitic inductance can result in a small portion of the device current to flow in the gate driver loop. Figure A3a shows a pictorial representation of various current flow paths while using a non-isolated gate driver and a current sense resistor (R_s). This small device current which interacts with the gate drive loop can disrupt the gate signals and cause oscillations in the gate circuit. One possible solution to this problem can be the use of isolated gate drivers with GaN-FETs devices featuring Kelvin source connection. Figure A3a shows a pictorial representation of the various current flow paths while using an isolated gate driver circuit. It can be observed that the power circuit and the gate driver circuit are completely isolated and do not interact with each other. This makes sure that all the current in the power circuit flows through R_s and exact current measurement can be obtained in the current conditioning circuit.



(a) (b)

Figure A3. Illustration of current flow paths (shown by arrows) in a GaN FET driven by (a) a non-isolated gate driver circuit and (b) an isolated gate driver circuit. Here, L_g represents the gate circuit leakage inductance, R_g is the gate resistance, L_s represents the PCB parasitic inductance and R_s is the sense resistor. While using a non-isolated gate driver circuit a small portion of device current can flow in the gate loop and cause HF oscillations. Using a non-isolated gate driver circuit, the gate driver loop can be completely isolated from the power loop.

AE2. Operating principle of overvoltage protection

In the overvoltage scheme, the voltage is differentially sensed across the drain to source of the GAN device. The sensed voltage is then fed to a comparator. Whenever the V_{ds} goes above certain threshold set externally, the comparator output goes high and disables all the Ćuk PES switches via a suitable logic circuitry.

AE3. Logic network

The logic network uses both combinational and sequential logic gates. On the event of overvoltage and overcurrent faults, all the gate drivers are disabled, and all the PWM signals are turned off. The logic schematic is portrayed in Figure A4. Simulation results are provided in Figure A5 which validate that in an event of a fault, rapidly turning-off all the devices in a grid-connected Ćuk PES, results in safely averting any GaN device failure.

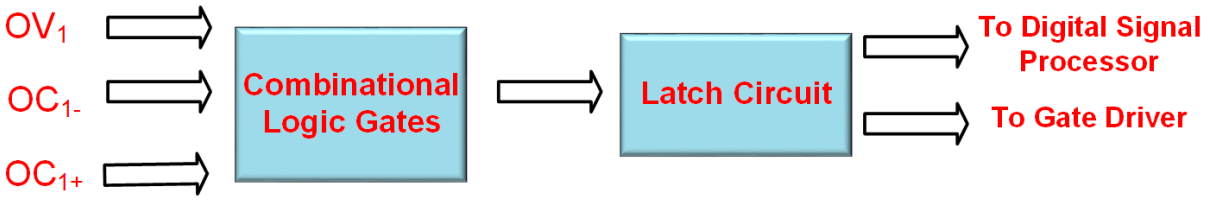


Figure A4. Illustration of the logic network. The bi-directional overcurrent and overvoltage signals pass through an array of combinational or gates and sequential latches to fire off the gate drivers in event of faults. A fault signal is also sent to the DSP to terminate the PWM switching.

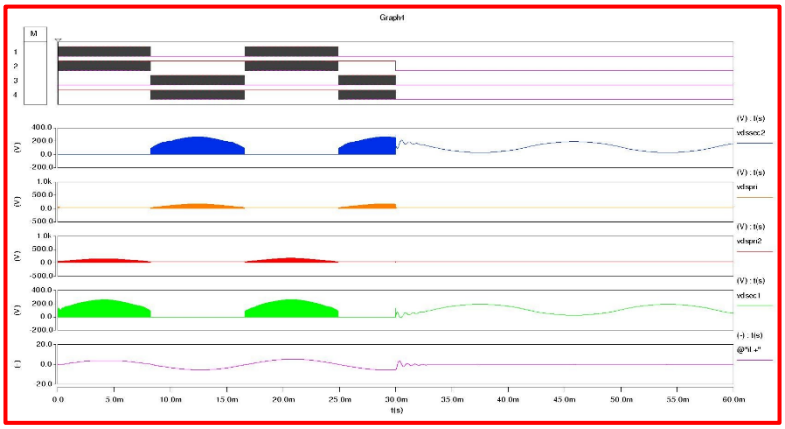


Figure A5. Illustration of the Ćuk PES voltages and currents, in grid-connected mode of inverter operation, during a fault scenario. Traces (1-9) from bottom to top are the grid current, device drain to source voltages (2-5), device gate to source voltages (6-9).

AE4. Results

The overcurrent and overvoltage protection schemes were validated in the experimental prototype of the Ćuk PES, as depicted in Figure A6. The power stage parameters for the designed circuit are given in Table I. The 1st and the 2nd sub-sections delineate the experimental results for the overcurrent and overvoltage protection, respectively. Subsequently, the basic results for the logic network is outlined.

Figure A6. Illustration of the developed experimental prototype. The overcurrent and overvoltage circuits are highlighted.

AE4.1. Overcurrent protection

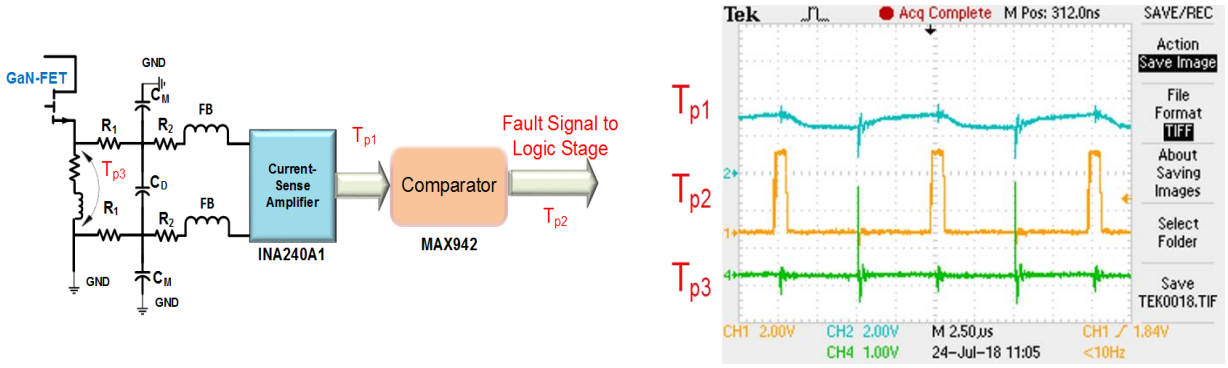


Figure A7. (a) Illustration of the overcurrent protection scheme for the GaN-based Ćuk PES. (b) Experimental waveforms at the points T_{p1}, T_{p2},T_{p3} probed in Figure A7.

Figure A7a shows the schematics of the bi-directional overcurrent protection and Figure A7b shows the signals obtained at the probed points.

AE4.2. Overvoltage protection

Figure A8a shows the schematics of the overvoltage protection and Figure A8b shows the result obtained at the probed points.

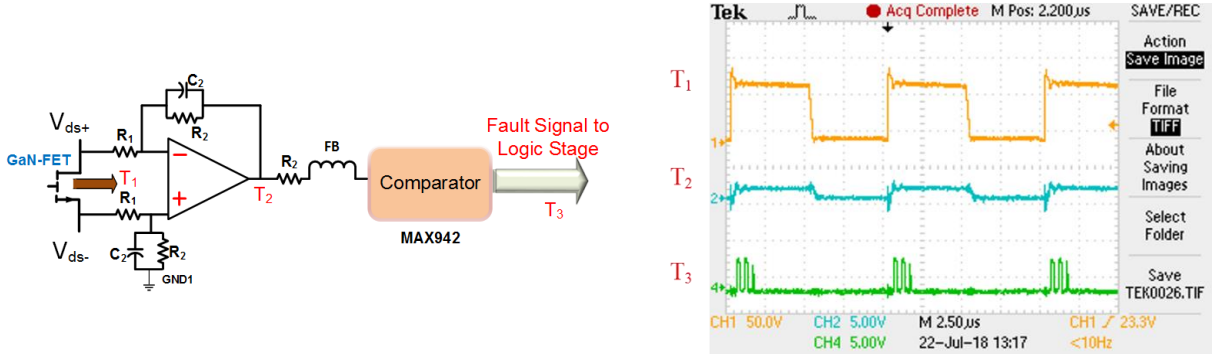


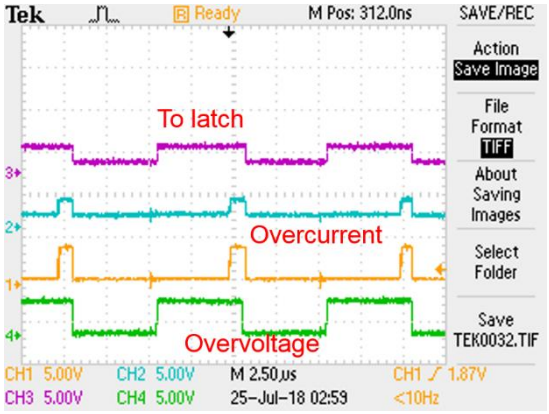
Figure A8. (a) Illustration of the overvoltage protection logic for the GaN-based Ćuk PES. (b) Experimental waveforms at the points T_1, T_2,T_3 probed in Figure A8.

AE4.3. Logic signals

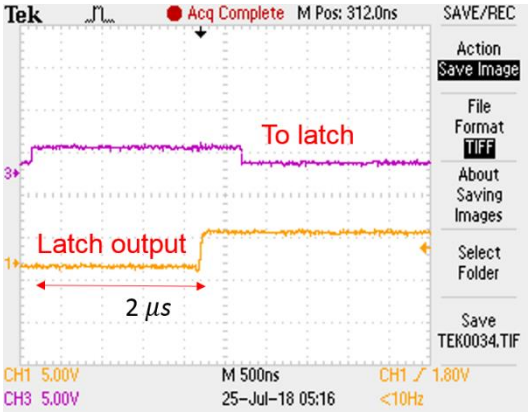
Figure A9 shows the logic signals obtained which disable the gate driver on an event of a fault. All results have been obtained at maximum power of 350 W of a single dc-dc HF GaN-based PES module. The different control signals, both analog and digital are fairly clean as shown in Figures A7-A9, which proves the efficacy of the protection scheme designed that precludes device loss at sustained PES operation at rated power and helps in reliable PES operation.

AE5. Conclusion

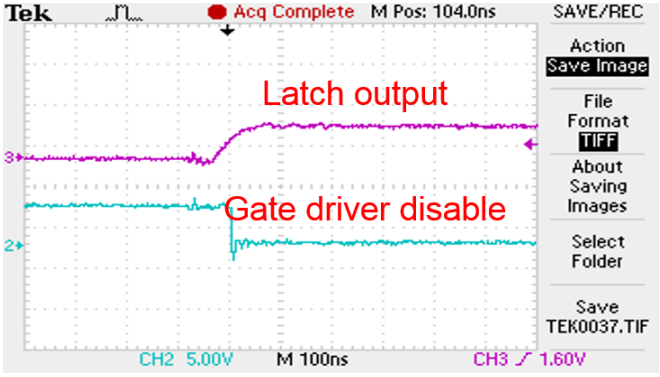
Experimental validation of a protection scheme for a GaN-FET-based HF PES is demonstrated in this Appendix. Unlike existing protection techniques which consider unidirectional PES operation, the overcurrent protection scheme encompasses bidirectional short-circuit faults. The schemes, overvoltage, and overcurrent, make use of low cost and readily available analog circuitry and does not compromise performance of the PES under consideration, even in presence of HF switching noise primarily associated with the rapid transitions of GaN-FETs.



(a)



(b)



(c)

Figure A9. (a) Illustration of the control signals produced by the logic network. The bottom three traces denote the faults due to overvoltage and overcurrent, and the topmost trace denotes the resultant signal sent to the latch. (b) Illustration of the control signals at the input and output of the latch circuit from top to bottom. (c) Illustration of the gate driver disable signal that is generated when latch output is set.

Chapter 2

Appendix F

The matrices described in Section 2.3.1.1 are delineated here. For simplification, the parameters of the two modules in Figure 27 are considered the same. R_{load} denotes the output resistance of the downstream converter. L_1, L_m and L_2 denote the inductances of the primary and secondary inductors and the magnetizing inductance of the HF transformer,

$A_{k_1} =$

$$= \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{2}{L_2} & \frac{1}{L_2} & \frac{-1}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{-1}{L_m} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{-2}{C_1} & \frac{1}{C_1} & \frac{-1}{R_dC_1} & 0 & 0 & \frac{1}{R_dC_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{R_dC_d} & 0 & 0 & \frac{-1}{R_dC_d} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{2}{L_2} & \frac{1}{L_2} & \frac{-1}{L_2} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_m} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-2}{C_1} & \frac{1}{C_1} & \frac{-1}{R_dC_1} & 0 & 0 & \frac{1}{R_dC_1} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_3} & 0 & 0 & 0 & \frac{-1}{R_{load}C_3} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_dC_d} & 0 & 0 & \frac{-1}{R_dC_d} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{K_P}{C_3} & 0 & 0 & 0 & (\frac{K_P}{C_3R_{load}} - K_I) & 0 & 0
\end{bmatrix}$$

respectively. The blocking capacitors of the modules have been denoted by C_1 and C_2. C_3/C_{out} denotes the output capacitor, R_d and C_d denotes the resistance and capacitance of the RC damper branch. K_p, K_I are the controller gains of the PI controller of the 2nd module and V_{ref} is the output voltage reference command for the 2nd module.

The matrices A_{k_1}, B_{k_1} , A_{k_2}, and B_{k_2} represent the fundamental switching sequence of the Ćuk PES for the two successive switching states. The matrices A_{k_1}, B_{k_1} represent the 1st switching state and A_{k_2}, B_{k_2} represent the 2nd switching state. The reduced order PES matrices A_r, B_r used for the state estimator and prediction model for the two

switching states (A_{r_1}, B_{r_1} for 1st state and A_{r_2}, B_{r_2} for 2nd state) will also be stated.

$$B_{k_1} = B_{k_2} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ K_I V_{ref} \end{bmatrix} A_{r_1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{2}{L_2} & \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_m} & 0 & 0 & 0 \\ 0 & \frac{-2}{C_1} & \frac{1}{C_1} & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} \\ 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & \frac{-1}{R_d C_d} \end{bmatrix}$$

$A_{k_2} =$

$$\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & \frac{-1}{2L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2L_m} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_1} & 0 & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_2} & 0 & \frac{-1}{2C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 & \frac{-1}{L_1} & \frac{-1}{2L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2L_m} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2C_2} & 0 & \frac{-1}{2C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_{load} C_3} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{K_P}{C_3} & 0 & 0 & 0 & (\frac{K_P}{C_3 R_{load}} - K_I) & 0 & 0 \end{bmatrix}$$

Appendix F (Continued)

$$A_{r_2} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & \frac{-1}{2L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2L_m} & 0 & 0 \\ 0 & \frac{1}{C_1} & 0 & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} \\ \frac{1}{2C_2} & 0 & \frac{-1}{2C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & 0 \end{bmatrix}$$

$$B_{r_1} = B_{r_2} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ -i_{load/C_3} \\ 0 \end{bmatrix}$$

Chapter 3

Appendix G

The matrices $\hat{A}_{kn}$ and $\hat{B}_{kn}$ for the two switching states of the Ćuk-PES, expressed as $\hat{A}_{kn1}$ and $\hat{B}_{kn1}$ and $\hat{A}_{kn2}$ and $\hat{B}_{kn2}$, respectively, are defined below, where the symbols of the passive components have been defined in Figure 44. R_d and C_d are the RC branch parameters referred to the primary side of the HFT.

$$\hat{A}_{kn1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{2}{L_2} & \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_m} & 0 & 0 & 0 \\ 0 & \frac{-2}{C_1} & \frac{1}{C_1} & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} \\ 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & \frac{-1}{R_3 C_3} & 0 \\ 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & \frac{-1}{R_d C_d} \end{bmatrix}, \hat{B}_{kn1} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \hat{A}_{kn2} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & \frac{-1}{2L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2L_m} & 0 & 0 \\ 0 & \frac{1}{C_1} & 0 & \frac{-1}{R_d C_1} & 0 & 0 & \frac{1}{R_d C_1} \\ \frac{1}{2C_2} & 0 & \frac{-1}{2C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & \frac{-1}{R_3 C_3} & 0 \\ 0 & 0 & 0 & \frac{1}{R_d C_d} & 0 & 0 & 0 \end{bmatrix}, \hat{B}_{kn2} = \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Chapter 3

Appendix H

For a dc/dc PES operating in steady state with a time horizon T_{kw_s}, any PES state (say $\hat{x}_1(t)$) can be generalized as a periodic series in time domain like:

$$\hat{x}_1(t) = \sum_{n_1=0}^{\infty} C_{n_1} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t)} \tag{A5}$$

where C_{n_1} is the magnitude of the n_1th harmonic of the time horizon T_{kw_s}. Now, instead of a fixed time horizon T_{kw_s}, we consider a new time horizon T_{kw} . As defined in

Figure 41, T_{kw} is formed of discrete time horizons $T_{kw_i}^{-1} = T_{kw_s}^{-1} + \Delta T_{kw}^{-1} v_m(w_m t)$. $T_{kw_i}^{-1}$ starts at $T_{kw_s}^{-1}$ for $i = 1$, reaches $T_{kw_i}^{-1} = T_{kw_s}^{-1} + \Delta T_{kw}^{-1}$ at $i = h_1/2$, and ends again at $T_{kw_i}^{-1} = T_{kw_s}^{-1}$ for $i = h_1$ as defined in

Figure 41 (check). If $v_m(w_m t) = \sin(w_m t)$, the PES state $\hat{x}_1(t)$ with the new horizon T_{kw} can again be written as a periodic series in time domain as:

$$\hat{x}_{1_{new}}(t) = \sum_{n_1=0}^{\infty} C_{n_1} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1}\right)t + n_1 \int_0^t (v_m(\tau)(d\tau))(\Delta T_{kw})^{-1})} \tag{A6}$$

$$\text{where} \qquad \Delta T_{kw}^{-1} = T_{kw_{h_{1/4}}}^{-1} - T_{kw_s}^{-1} \tag{A7}$$

Using mathematical manipulations formulated in [102] and [84], (A6) can be simplified to the form given by:

$$\hat{x}_{1_{new}}(t) = \sum_{n_1=0}^{\infty} \sum_{m_1=-\infty}^{\infty} C_{n_{1_{new}}} exp^{(2\pi j\left(n_1 T_{kw_s}^{-1} + m_1 T_{kw}^{-1}\right)t)} \tag{A8}$$

where

$$C_{n_{1_{new}}} = C_{m_1 n_1} \tag{A9a}$$

$$T_{kw} = \left(\frac{2\pi}{w_m}\right)^{-1} \tag{A9b}$$

$$C_{m_1} = j^{-1} J_{m_1}(n_1 \Delta T_{kw}^{-1} T_{kw}) \tag{A9c}$$

$$C_{m_1 n_1} = C_{n_1} C_{m_1} \exp\left(j n_1 \Delta T_{kw}^{-1} T_{kw}\right) \tag{A9d}$$

and J_{m_1} is the Jacobian function [102].

Chapter 4

Appendix I

AI1. Operating modes of the Ćuk PES

Figure A9 shows the modes of the HF non-isolated Ćuk PES in continuous conduction mode (CCM). During Mode-1, the current iL_a through the inductor L_a, and iL_b through the inductor L_b, flows through switch M_1 body diode, after the switch M_1 is turned off. After a certain period of deadtime, Mode-2 starts with the turn-on of the switch M_2, which now supports the entire current $iL_a + iL_b$. As reverse voltage $V_{ds_{M_1}}$ starts to build across the switch M_1, and hence its

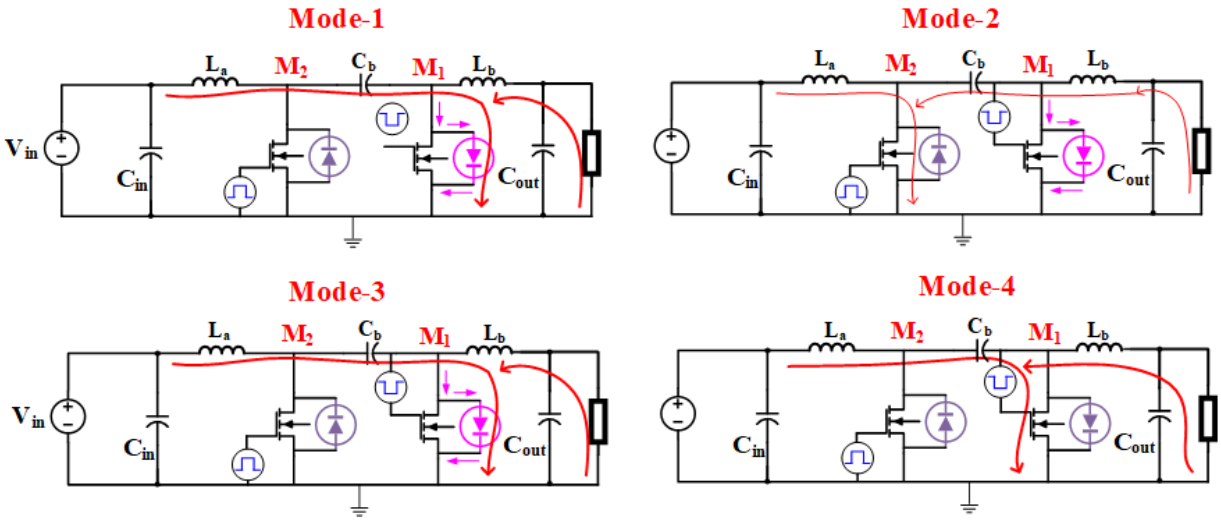


Figure A9. Figure showing modes of operation in Ćuk PES for CCM. STC operates only in Mode 2 and Mode 4 since modes 2 and 3 are soft switched and controlling the V_{gs} transition will have no effect on PES efficiency.

body-diode, the diode undergoes reverse recovery at the onset of Mode-2, which adds to the current $iL_a + iL_b$ through switch M_2. As Mode-2 ends, switch M_2 is turned off, and blocks voltage $V_{ds_{M_2}}$.The body-diode of M_1 again conducts during deadtime in Mode-3. During Mode-4, M_1 is turned on again in ZVS condition.

Chapter 4

Appendix J

With reference to Figure 70a, the dynamics of the Mosfet M_2 transitions is discussed in this Appendix. The work in the literature [90] for SiC Mosfets is mainly followed since it closely matches the application at hand. The important regions required for STC is focused only.

After the threshold voltage $V_{gs_{th}}$ at t_1, the drain current $I_{ds_{M_2}}$ rises following:

$$I_{ds_{M_2}} = g_{fs_{M_2}}\left[V_{gs}(t) - V_{gs_{th}}\right] \tag{A10}$$

where $g_{fs_{M_2}}$ is the transconductance of the SiC Mosfet. The drain current becomes $I_{L_a} + I_{L_b}$ at t_2. After t_2, the diode reverse recovery current of M_1 is added to $I_{L_a} + I_{L_b}$. We neglect the capacitor discharging current of M_2, $C_{ds_{M_2}} \frac{dV_{ds_{M_2}}}{dt}$ since $C_{ds_{M_2}} \frac{dV_{ds_{M_2}}}{dt} \ll I_{L_a} + I_{L_b}$. Let $I_{ds_{RR}}$ be the peak reverse recovery current of the body diode. Then the duration from t_2 to t_3 can be written as:

$$t_3\text{-}t_2 = \frac{(I_{L_a}+I_{L_b}+I_{ds_{RR}})\,(C_{gd_{M_2}}+C_{gs_{M_2}})}{g_{fs_{M_2}} I_{g_{M_2}}} \tag{A11}$$

The experiments are performed for a constant value of V_{ds}, and hence $C_{gd_{M_2}}, C_{gs_{M_2}}$ is constant. At t_3 the Mosfet M_2 reaches its gate-source plateau voltage which can be written as:

$$V_M = V_{gs_{th}} + (I_{L_a} + I_{L_b} + I_{ds_{RR}})/(\, g_{fs_{M_2}}) \tag{A12}$$

The gate current ($I_{g_{M_2}}$) in (8) can be written as:

$$I_{g_{M_2}} = \frac{V_E - 0.5\left(V_M + V_{gs_{th}}\right) - L_{cs_2}\dfrac{(I_{L_a} + I_{L_b} + I_{ds_{RR}})}{t_3 - t_2}}{R_{ext} + R_{init}} \tag{A13}$$

L_{cs_2} is the common source inductance, and $R_{ext} + R_{init}$ is the gate resistance. The time duration t_2-t_3 can be calculated using (8)-(10) as:

$$t_3\text{-}t_2 = \frac{(I_{L_a}+I_{L_b}+I_{ds_{RR}})\,(\left(C_{gd_{M_2}}+C_{gs_{M_2}}\right)(R_{ext}+R_{init})+g_{fs_{M_2}}L_{cs_2}}{g_{fs_{M_2}}(V_E-0.5\left(V_M+V_{gs_{th}}\right))} \tag{A14}$$

The peak reverse recovery current of the body diode can be approximated as

$$I_{ds_{RR}} = \sqrt{2(I_{L_a} + I_{L_b}) \frac{I_{dsRR-datasheet}}{T_{rr_{datsheet}}} \frac{Q_{rr-datasheet}}{I_{o-datasheet}}} \tag{A15}$$

In (A15), $Q_{rr-datasheet}, I_{o-datasheet}$ are the reverse recovery charge and test current levels from the datasheet, respectively. $I_{dsRR-datasheet}, T_{rr_{datsheet}}$ are the reverse recovery peak currents and times from the datasheet at the $I_{o-datasheet}$ test condition.

Then, we come to the next region t_3-t_4. At t_3, the non-linear capacitance $C_{gd_{M_2}}$ is at the lowest possible value and rate of fall of $v_{ds_{M_2}}$ is maximum.

$$t_4\text{-}t_3 = \frac{C_{gd_{M_2}}(t)\,(v_{ds_{M_2}}(t_4) - v_{ds_{M_2}}(t_3))}{V_E - V_M} \tag{A16}$$

At t_4, when the diode has reverse recovered, the voltage slope rate decreases, and the interval is given by :

$$t_6\text{-}t_4 = \frac{C_{gd_{M_2}}(t)\,(v_{ds_{M_2}}(t_6) - v_{ds_{M_2}}(t_4))}{V_E - V_M} \tag{A17}$$

Appendix K

Permission from the IEEE website (Rights Link) regarding Thesis/Dissertation reuse

This appendix presents the copyright permissions for the articles, whose contents were utilized in my dissertation. The list of the articles includes several journals, and conference publications: IEEE Transactions on Power Electronics'19,20,21, ECCE'19, and PEDG'16.

The copyright permissions for reusing the published materials are presented in Appendix K.

Appendix K (Continued)

IEEE Requesting permission to reuse content from an IEEE publication

Switching-Sequence Control of a Higher Order Power-Electronic System Driving a Pulsating Load

Author: Debanjan Chatterjee

Publication: IEEE Transactions on Power Electronics

Publisher: IEEE

Date: Jan. 2020

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

BACK CLOSE WINDOW

Appendix K (Continued)

Copyright Clearance Center RightsLink®

Home | Help | Email Support | Sign in | Create Account

IEEE Requesting permission to reuse content from an IEEE publication

Predictive Switching Sequence-based Control for Constant Power Load

Conference Proceedings: 2019 IEEE Energy Conversion Congress and Exposition (ECCE)

Author: Debanjan Chatterjee

Publisher: IEEE

Date: Sept. 2019

Copyright © 2019, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

BACK CLOSE WINDOW

Appendix K (Continued)

Control of Isolated Differential-Mode Single- and Three-Phase Ćuk Inverters at Module Level

Author: Harshit Soni

Publication: IEEE Transactions on Power Electronics

Publisher: IEEE

Date: Oct. 2018

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

BACK CLOSE WINDOW

Appendix K (Continued)

Optimal switching sequence based control of a differential-mode inverter

IEEE Requesting permission to reuse content from an IEEE publication

Conference Proceedings:
2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

Author: Debanjan Chatterjee

Publisher: IEEE

Date: June 2016

Copyright © 2016, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

BACK CLOSE WINDOW

REFERENCES

[1] S. K. Mazumder and K. Acharya, "Multiple Lyapunov Function Based Reaching Condition Analyses of Switching Power Converters," in *37th IEEE Power Electronics Specialists Conference*, pp. 1–8.

[2] D. Chatterjee and S. K. Mazumder, "Switching-Sequence Control of a Higher-Order Power-Electronic System Driving a Pulsating Load," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 1096–1110, 2020.

[3] N. Kumar, S. K. Mazumder, and A. Gupta, "SiC DC Fast Charger Control for Electric Vehicles," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 599–605.

[4] S. Vazquez *et al.*, "Model Predictive Control: A Review of Its Applications in Power Electronics," *IEEE Ind. Electron. Mag.*, vol. 8, no. 1, pp. 16–31, Mar. 2014.

[5] H. Soni, S. K. Mazumder, A. Gupta, D. Chatterjee, and A. Kulkarni, "Control of Isolated Differential-Mode Single- and Three-Phase Ćuk Inverters at Module Level," *IEEE Trans. Power Electron.*, ol. 33, no. 10, pp. 8872-8886, 2018.

[6] H. W. Gayek and L. R. Peaslee, "Behavior of Aircraft Generating Systems with Pulsating Loads," *Aerospace, IEEE Trans.*, vol. AS-3, no. 2, pp. 603–614, 1965.

[7] H. Ebrahimi, H. El-Kishky, M. Biswass, and M. Robinson, "Impact of pulsed power loads on advanced aircraft electric power systems with hybrid APU," *2016 IEEE Int. Power Modul. High Volt. Conf. IPMHVC 2016*, no. i, pp. 434–437, 2017.

[8] Z. Chen, "PI and sliding mode control of a Cuk converter," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3695–3703, 2012.

[9] S. Guo, X. Lin-Shi, B. Allard, Y. Gao, and Y. Ruan, "Digital sliding-mode controller for high-frequency dc/dc SMPS," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1120–1123, 2010.

[10] H. El Fadil and F. Giri, "Backstepping Based Control of PWM DC-DC Boost Power Converters," *2007 IEEE Int. Symp. Ind. Electron.*, pp. 395–400, 2007.

[11] H. Rodr, R. Ortega, and A. Astolfi, "Adaptive partial state feedback control of of the dc-to-dc Cuk converter," in ´ Proc. IEEE Amer. Control Conf., Jun. 2005, pp. 5121–5126.

[12] H. Sira-Ramirez and M. T. Prada-Rizzo, "Nonlinear feedback regulator design for the Cuk converter," IEEE Trans. Automat. Control, vol. 37, no. 8, pp. 1173–1180, Aug. 1992.

[13] S. K. Mazumder and K. Acharya, "Multiple Lyapunov Function Based Reaching Condition for Orbital Existence of Switching Power Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1449–1471, May 2008.

[14] A. Tajfar and S. K. Mazumder, "Sequence-Based Control of an Isolated DC/AC Matrix Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1757–1773, Feb. 2016.

[15] T. Geyer, "Computationally Efficient Model Predictive Direct Torque Control," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2804–2816, Oct. 2011.

[16] J. Rodriguez, P. Cortes, R. Kennel, and M. Kazrnierkowski, "Model predictive control -- a simple and powerful method to control power converters," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 41–49.

REFERENCES (Continued)

[17] S. Mariéthoz and M. Morari, "Explicit Model-Predictive Control of a PWM Inverter With an LCL Filter," vol. 56, no. 2, pp. 389–399, 2009.

[18] M. Votava, V. Smidl, T. Glasberger, and Z. Peroutka, "Model Predictive Control of Dual Inverter Respecting Temperature Limits of IGBTs Acknowledgment Keywords," *2016 18th Eur. Conf. Power Electron. Appl. (EPE'16 ECCE Eur.*, pp. 1–10, 2015.

[19] R. Vargas, U. Ammann, and J. Rodríguez, "Predictive approach to increase efficiency and reduce switching losses on matrix converters," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 894–902, 2009.

[20] L. Cheng *et al.*, "Model Predictive Control for DC-DC Boost Converters with Reduced-Prediction Horizon and Constant Switching Frequency," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 9064–9075, 2018.

[21] R. P. Aguilera *et al.*, "Selective Harmonic Elimination Model Predictive Control for Multilevel Power Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2416–2426, 2017.

[22] D. Limon, A. Ferramosca, I. Alvarado, and T. Alamo, "Nonlinear MPC for Tracking Piece-Wise Constant Reference Signals," *IEEE Trans. Automat. Contr.*, vol. 63, no. 11, pp. 3735–3750, 2018.

[23] T. Geyer, G. Papafotiou, and M. Morari, "Model Predictive Direct Torque Control—Part I: Concept, Algorithm, and Analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1894–1905, Jun. 2009.

[24] P. Karamanakos, T. Geyer, and S. Manias, "Direct Model Predictive Current Control Strategy of DC–DC Boost Converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 1, no. 4, pp. 337–346, Dec. 2013.

[25] P. Karamanakos, T. Geyer, and S. Manias, "Direct Voltage Control of DC–DC Boost Converters Using Enumeration-Based Model Predictive Control," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 968–978, Feb. 2014.

[26] P. Karamanakos, T. Geyer, and S. Manias, "Direct model predictive current control of DC-DC boost converters," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, p. DS2c.11-1-DS2c.11-8.

[27] J. Neely, R. DeCa, and S. Pekarek, "Real-time model predictive control of the Ćuk converter," in *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2010, pp. 1–8.

[28] F. M. Oettmeier, J. Neely, S. Pekarek, R. DeCarlo, and K. Uthaichana, "MPC of Switching in a Boost Converter Using a Hybrid State Model With a Sliding Mode Observer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 9, pp. 3453–3466, Sep. 2009.

[29] V. Grigore, J. Hatonen, J. Kyyra, and T. Suntio, "Dynamics of a buck converter with a constant power load," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, vol. 1, pp. 72–78.

[30] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant Power Loads and Negative Impedance Instability in Automotive Systems: Definition, Modeling, Stability, and Control of Power Electronic Converters and Motor Drives," *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112–1125, Jul. 2006.

[31] I. Kondratiev, E. Santi, R. Dougal, and G. Veselov, "Synergetic control for DC-DC buck converters with constant power load," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, pp. 3758–3764.

REFERENCES (Continued)

[32] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model Predictive Control A Simple and Powerful Method to Control Power Converters," *Ind. Electron. IEEE Trans.*, vol. 56, no. 6, pp. 1826–1838, 2009.

[33] A. Kulkarni, A. Gupta, and S. K. Mazumder, "Resolving Practical Design Issues in a Single-Phase Grid-Connected GaN-FET-Based Differential-Mode Inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3734–3751, May 2018.

[34] L. Xing, J. Sun, and S. Member, "Optimal damping of multistage EMI 1095 filters," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1220–1227, 1096 Mar. 2012.

[35] L. Xing, J. Sun, and S. Member, "Optimal Damping of Multistage EMI Filters," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1220–1227, 2012.

[36] Y. Lei *et al.*, "A 2-kW Single-Phase Seven-Level Flying Capacitor Multilevel Inverter with an Active Energy Buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017.

[37] A. Paredes, V. Sala, H. Ghorbani, and L. Romeral, "A novel active gate driver for silicon carbide MOSFET," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 3172–3177.

[38] S. Acharya, X. She, F. Tao, T. Frangieh, M. H. Todorovic, and R. Datta, "Active Gate Driver for SiC-MOSFET-Based PV Inverter with Enhanced Operating Range," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1677–1689, 2019.

[39] G. Tan, B. Kou, H. Wu, and L. Li, "Dynamic sensorless detection of linear electromagnetic UAV launch," *IEEE Trans. Plasma Sci.*, vol. 39, no. 1, pp. 399–404, 2011.

[40] Y. Komaru, Y. Inoue, S. Morimoto, and M. Sanada, "Comparative Study of Speed Ripple Reduction by Various Control Methods in PMSM Drive Systems with Pulsating Load," *2018 Int. Power Electron. Conf. (IPEC-Niigata 2018 -ECCE Asia)*, pp. 1329–1335, 2018.

[41] R. Cao, Y. Jin, M. Lu, and Z. Zhang, "Quantitative Comparison of Linear Flux-Switching Permanent Magnet Motor With Linear Induction Motor for Electromagnetic," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7569–7578, 2018.

[42] M. M. Jovanovic, C. S. Leu, and F. C. Y. Lee, "Zero-Voltage-Switched Multiresonant Converter for High-Power, Pulse-Load Applications," *IEEE Trans. Ind. Electron.*, vol. 37, no. 6, pp. 544–555, 1990.

[43] J. M. Crider and S. D. Sudhoff, "Reducing impact of pulsed power loads on microgrid power systems," *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 270–277, 2010.

[44] P. Alou, J. A. Cobos, O. Garcia, R. Prieto, and J. Uceda, "Coupling inductors for supplying pulsating loads with dc-dc converters," in Proc. 29th Annu. IEEE Power Electron. Spec. Conf., 1998, vol. 2, pp. 1790–1795.

[45] N. Vishwanathan and V. Ramanarayanan, "High voltage DC power supply topology for pulsed load applications with converter switching synchronized to load pulses," *Proc. Int. Conf. Power Electron. Drive Syst.*, vol. 1, pp. 618–623, 2003.

[46] J. T. Broach, "Converters for Supplying Pulsed Power Loads," *IEEE Trans. Ind. Appl.*, vol. IA-15, no. 1, pp. 85–91, 1979.

[47] X. Huang, X. Ruan, F. Du, F. Liu, and L. Zhang, "High Power and Low Voltage Power Supply for Low Frequency Pulsed Load," pp. 2859–2865, 2017.

[48] X. Huang, X. Ruan, F. Du, F. Liu, and L. Zhang, "A Pulsed Power Supply Adopting Active Capacitor Converter for Low-Voltage and Low-Frequency Pulsed Loads," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9219–9230, 2018.

[49] Q. Yang, L. Tan, W. Liu, and W. Im, "Adaptive critic design based cooperative control for pulsed power loads accommodation in shipboard power system," *IET Gener. Transm. Distrib.*, vol. 10, no. 11, pp. 2739–2747, 2016.

[50] M. M. Mardani, M. H. Khooban, A. Masoudian, and T. Dragicevic, "Model Predictive Control of DC-DC Converters to Mitigate the Effects of Pulsed Power Loads in Naval DC Microgrids," *IEEE Trans. Ind. Electron.*, vol. 0046, no. c, pp. 1–1, 2018.

[51] R. Redl and N. O. Sokal, "Near-Optimum Dynamic Regulation of DC-DC Converters Using Feed-Forward of Output Current and Input Voltage with Current-Mode Control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181–192, Jul. 1986.

[52] A. G. Beccuti, G. Papafotiou, and M. Morari, "Optimal Control of the Boost dc-dc Converter," in *Proceedings of the 44th IEEE Conference on Decision and Control*, pp. 4457–4462.

[53] P. Cortes *et al.*, "Guidelines for weighting factors design in Model Predictive Control of power converters and drives," *IEEE Int. Conf. Ind. Technol.*, pp. 1–7, 2009.

[54] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model Predictive Control for Power Converters and Drives: Advances and Trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb. 2017.

[55] P. Gahinet, A. Nemirovskii, A. J. Laub, and M. Chilali, "The LMI control toolbox," in *Proceedings of 1994 33rd IEEE Conference on Decision and Control*, vol. 3, pp. 2038–2041.

[56] J. G. Ciezki and R. W. Ashton, "The design of stabilizing controls for shipboard DC-to-DC buck choppers using feedback linearization techniques," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, vol. 1, pp. 335–341.

[57] Y. Li, K. R. Vannorsdel, A. J. Zirger, M. Norris, and D. Maksimovic, "Current Mode Control for Boost Converters With Constant Power Loads," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 59, no. 1, pp. 198–206, Jan. 2012.

[58] M. Cespedes, T. Beechner, L. Xing, and J. Sun, "Stabilization of constant-power loads by passive impedance damping," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 2174–2180.

[59] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, May 2003.

[60] P. A. Dahono, "A control method for DC-DC converter that has an LCL output filter based on new virtual capacitor and resistor concepts," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, pp. 36–42.

[61] A. M. Rahimi and A. Emadi, "Active Damping in DC/DC Power Electronic Converters: A Novel Method to Overcome the Problems of Constant Power Loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1428–1439, May 2009.

[62] D. Chatterjee and S. K. Mazumder, "Optimal switching sequence based control of a differential-mode

inverter," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1–8.

[63] L. A. Kamas and S. R. Sanders, "Parameter and state estimation in power electronic circuits," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, pp. 57–61.

[64] "GN001 application guide design with GaN enhancement mode HEMT," 1085 GaN Systems Inc., Ottawa, ON, Canada, 2018.

[65] T. Hegarty, "An overview of conducted EMI specifications for power 1087 supplies," Texas Instruments Whitepaper, Feb. 2, 2018.

[66] K. Raggl, S. Member, T. Nussbaumer, J. W. Kolar, and S. Member, "Guideline for a Simplified Differential-Mode EMI Filter Design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, 2010.

[67] A. Nagel and R. W. De Doncker, "Systematic design of EMI-filters for power converters," *Conf. Rec. - IAS Annu. Meet. (IEEE Ind. Appl. Soc.*, vol. 4, pp. 2523–2525, 2000.

[68] Z. Hao, "Simple solution for input filter stability issue in dc/dc converters," 1098 Application report, Texas Instruments, Dallas, TX, USA, Apr. 2019.

[69] G. Spiazzi and J. A. Pomilio, "Interaction between EMI filter and power factor preregulators with average current control: analysis and design considerations," *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 577–584, Jun. 1999.

[70] Liyu Yang *et al.*, "Modeling and characterization of a 1KW CCM PFC converter for conducted EMI prediction," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 2, pp. 763–769.

[71] K. Mainali and R. Oruganti, "Simple Analytical Models to Predict Conducted EMI Noise in a Power Electronic Converter," in *IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society*, 2007, pp. 1930–1936.

[72] S. Walder, X. Yuan, I. Laird, and J. J. O. Dalton, "Identification of the temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[73] P. Kong, Y. Jiang, and F. C. Lee, "Common Mode EMI Noise Characteristics of Low-Power AC–DC Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 731–738, Feb. 2012.

[74] B. van der Pol, "The fundamental principles of frequency modulation," *J. Inst. Electr. Eng. - Part III Radio Commun. Eng.*, vol. 93, no. 23, pp. 153–158, May 1946.

[75] J. Balcells, A. Santolaria, A. Orlandi, D. González, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, 2005.

[76] J. A. S. Lorenzo, "Tesi - SSCG methods of EMI emissions reduction applied to switching power converters," *Electron. Eng.*, no. April, p. 237, 2004.

[77] A. Santolaria, J. Balcells, and D. Gonzalez, "Theoretical & experimental results of power converter frequency modulation," in *IECON Proceedings (Industrial Electronics Conference)*, 2002, vol. 1, pp. 193–197.

REFERENCES (Continued)

[78] F. Lin and D. Y. Chen, "Reduction of Power Supply EMI Emission by Switching Frequency Modulation," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 132–137, 1994.

[79] A. Santolaria, "Effects of Switching Frequency Modulation on the Power Converter ' s Output Voltage," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2729–2737, 2009.

[80] D. Stepins, "Effect of Frequency Modulation on Input Current of Switch-Mode Power Converter," *IECON 2013 - 39th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 683–688, 2013.

[81] T. Geyer, "A Comparison of Control and Modulation Schemes for Medium-Voltage Drives: Emerging Predictive Control Concepts Versus PWM-Based Schemes," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1380–1389, May 2011.

[82] S. Vazquez, A. Marquez, R. Aguilera, D. Quevedo, J. I. Leon, and L. G. Franquelo, "Predictive Optimal Switching Sequence Direct Power Control for Grid-Connected Power Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2010–2020, 2015.

[83] S. Vazquez *et al.*, "Model Predictive Control: A Review of Its Applications in Power Electronics," *Ind. Electron. …*, no. March, pp. 16–31, 2014.

[84] B. van der Pol, "The fundamental principles of frequency modulation," *J. Inst. Electr. Eng. - Part III Radio Commun. Eng.*, vol. 93, no. 23, pp. 153–158, May 1946.

[85] Q. Ji, X. Ruan, and Z. Ye, "The worst conducted EMI spectrum of critical conduction mode boost PFC Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1230–1241, 2015.

[86] K. Fu, W. Chen, and S. Lin, "A general transformer evaluation method for common-mode noise behavior," *Energies*, vol. 12, no. 10, 2019.

[87] Hitachi Metals ,"FINEMET_CMC_Core_FT-3KM_FT-3K50T_K_Series.pdf .," pp. 1–4, 2014.

[88] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "A Hybrid Active Gate Drive for Switching Loss Reduction and Voltage Balancing of Series-Connected IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7469–7481, 2017.

[89] D. Chatterjee and S. K. Mazumder, "EMI Mitigation of a Cuk Based Power-Electronic System using Switching-Sequence-based Control," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2021.3059906.

[90] S. Eskandari, "Modeling and Loss Analysis of SiC Power Semiconductor Devices for Switching Converter," pp. 1–85, 2019.

[91] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, 2019.

[92] Y. Wang, Q. Zhang, J. Ying, and C. Sun, "Prediction of PIN diode reverse recovery," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, vol. 4, pp. 2956–2959, 2004.

[93] S. S. Lee, S. W. Choi, and G. W. Moon, "High-efficiency active-clamp forward converter with transient current build-up (TCB) ZVS technique," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 310–318, Feb. 2007.

[94] P. R. Palmer and A. N. Githiari, "The series connection of IGBT's with active voltage sharing," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 637–644, 1997.

[95] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC

MOSFET Switching Trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, 2017.

[96] S. Acharya, X. She, F. Tao, T. Frangieh, M. H. Todorovic, and R. Datta, "Active Gate Driver for SiC-MOSFET-Based PV Inverter With Enhanced Operating Range," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1677–1689, Mar. 2019.

[97] S. Zhao *et al.*, "Adaptive Multi-Level Active Gate Drivers for SiC Power Devices," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1882–1898, 2020.

[98] H. C. P. Dymond *et al.*, "A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, 2018.

[99] J. Wang, S. Mocevic, R. Burgos, and D. Boroyevich, "High-Scalability Enhanced Gate Drivers for SiC MOSFET Modules with Transient Immunity beyond 100 V/ns," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10180–10199, 2020.

[100] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," p. 188, 2009.

[101] Texas Instruments, "INA240 High- and Low-Side, Bidirectional, Zero-Drift, Current-Sense Amplifier With Enhanced PWM Rejection," 2016.

[102] J. Huang and R. Xiong, "Study on Modulating Carrier Frequency Twice in SPWM Single-Phase Inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3384–3392, Jul. 2014.

VITA

NAME: Debanjan Chatterjee

EDUCATION: B.E. Electrical Engineering, Jadavpur University, Kolkata, India, 2015

Ph.D. Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, IL, USA, 2021

MEMBERSHIP: IEEE

JOURNALS:

- D. Chatterjee and S. K. Mazumder**, "**Switching-sequence control of a higher-order power-electronic system driving a pulsating load**,"** ***IEEE Trans. Power Electron***., vol. 35, no. 1, pp. 1096–1110, 2020
- D. Chatterjee and S. K. Mazumder, "EMI Mitigation of a Ćuk Based Power-Electronic System using Switching-Sequence-based Control," ***IEEE Trans. Power Electron***., vol. 36, no. 9, pp. 10627-10644, Sept. 2021
- H. Soni, S. K. Mazumder, A. Gupta, D. Chatterjee, and A. Kulkarni, "Control of isolated differential-mode single- and three-phase Ćuk inverters at module level," ***IEEE Trans. Power Electron***., vol. 33, no. 10, pp. 8872–8886, 2018
- D. Chatterjee and S. K. Mazumder**, "**Switching transition control to improve efficiency of a dc/dc power-electronic system," ***IEEE Access***, doi: 10.1109/ACCESS.2021.3092017

CONFERENCE:

- D. Chatterjee and S. K. Mazumder, "Predictive switching sequence-based control for constant power load" ***2019 IEEE Energy Conversion Congress and Exposition (ECCE)***, pp. 1574–1583
- D. Chatterjee and S. K. Mazumder, "Optimal switching sequence-based control of a differential-mode inverter," ***2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG),*** 2016, pp. 1–8
- D. Chatterjee and S. K. Mazumder, "Turn-on Switching Transition Control using a GaN-FET based Active Gate Drive" ***2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG),*** 2020, accepted