Universal Battery Supercharger

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THESIS

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Dedicated to my family

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NK

PREFACE

This dissertation is an original intellectual product of the author, N. Kumar. All the work presented here was conducted in the Laboratory for Energy and Switching-Electronics Systems (LESES) at the University of Illinois at Chicago.

The results of our research have been previously published as journal, conference, and workshop articles in:

- IEEE Transactions on Power Electronics (Nikhil et al., 2020)
- IEEE Transactions on Power Electronics (Moien et al., 2021)
- IEEE Energy Conversion Congress and Exposition (ECCE'2018) (Kumar et al., 2018)
- IEEE Energy Conversion Congress and Exposition (ECCE'2018) (Kumar et al., 2019)

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Nikhil Kumar

March 15, 2021

CONTRIBUTION OF AUTHORS

Major parts of the results and discussions in this thesis are taken from my published or submitted papers with written permission from the journals (see Appendix A). Below, the contributions of all the co-authors are listed:

Authors' contributions in IEEE Transactions Power Electronics, ECCE'18, ECCE'19: N. Kumar, M. Mohamadi, and S. K. Mazumder conceived the main ideas and led the investigations. N.Kumar undertook the analytical analysis and experimental study. M. Mohamadi undertook the simulation study. N. Kumar, M. Mohamadi, and S. K. Mazumder contributed to the write-up of the manuscripts.

Authors' contributions in IEEE Transactions on Power Electronics, M. Mohamadi, S.K. Mazumder conceived the main idea and led the investigation. M. Mohamadi undertook the circuit design and performed the experimental analysis. M. Mohamadi, S.K. Mazumder, and N. Kumar contributed to the review and write-up of the manuscript.

Authors' contributions in Power Electronics for Distribution Generation System: N. Kumar, M. Mohamadi, S.K. Mazumder conceived the main idea. N. Kumar, and M. Mohamadi contributed to the circuit design and experimental study. N. Kumar, M. Mohamadi, S.K. Mazumder, Congbo Bao contributed to the review and write-up of the manuscript.

Authors' contributions in US patennt application: S.K. Mazumder conceived the main idea for the transformer-less, single-stage power module for off-board EV charging. N. Kumar, and M. Mohamadi contributed to the simulation analysis, circuit design and experimental results.

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LIST OF ABBREVIATIONS

ARPA-E	Advanced Research Project Agency-Energy
AWG	American Wire Gauge
CAD	Computer Aided Design
DMCR	Differential Mode Ćuk Rectifier
DMS	Discontinuous Modulation Scheme
DSP	Digital Signal Processor
EV	Electric Vehicles
EMI	Electromagnetic Interference
ePWM	Enhanced Pulse Width Modulator
FET	Field Effect Transistor
GaN	Gallium Nitride
GHG	Greenhouse Gases
HF	High Frequency
LF	Low Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PES	Power Electronics System
PFC	Power Factor Correction
PWM	Pulse Width Modulation
SiC	Silicon Carbide
SoC	State of Charge

LIST OF ABBREVIATIONS (Continued)

TVS	Transient Voltage Suppressor
WBG	Wide-bandgap
UBS	Universal Battery Supercharger

SUMMARY

In this dissertation, a universal battery supercharger (UBS) is presented that is based on a differential-mode-Cuk-rectifier (DMCR) topology. The UBS is targeted for DC fast charging application to reduce the range anxiety among the EV users. To fully understand the UBS (DMCR) topology, a comprehensive analysis of the high frequency and low frequency operating modes using an existing discontinues modulation scheme have been discussed in detail. However, due to presence of passives, the DMCR topology is prone to resonance frequency oscillations that makes the converter control complex and challenging. To mitigate this drawback two approaches; passive damping and multiloop control schemes are analyzed and experimentally validated. A scaled power UBS (sp-UBS) is designed to test the closed-loop control scheme and to parametric performance comparison between discrete magnetics and integrated magnetics. Finally, to extend the sp-UBS to 60-kW UBS, a pathway is through identifying critical components. To test the HCPCB design, SiC modules, integrated magnetics, a 20-kW UBS module was designed. Based on a preliminary CAD model, three such 20-kW UBS modules were integrated together to form a 60-kW UBS. Gradually, as power is increased on the 60- kW UBS prototype, several challenges were faced, and resolved. Steady-state and transient characterization results along with the parametric results are provided in detail.

Chapter 1

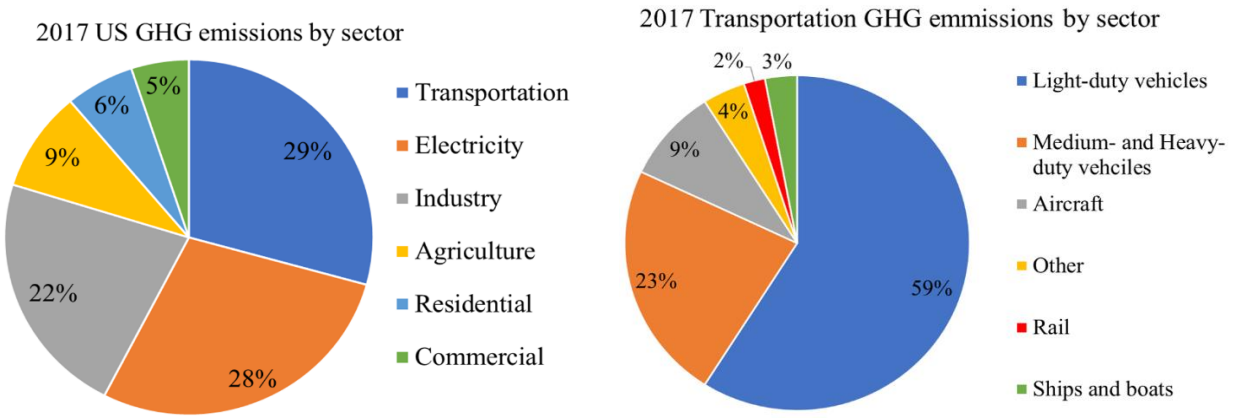
1. INTRODUCTION

Parts of this chapter, including figures and text, are based on my following papers:

- N. Kumar, S. K. Mazumder and A. Gupta, "SiC DC Fast Charger Control for Electric Vehicles," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018, pp. 599-605, doi: 10.1109/ECCE.2018.8558208.
- N. Kumar, M. Mohamadi and S. K. Mazumder, "Passive Damping Optimization of the Integrated-Magnetics-Based Differential-Mode Ćuk Rectifier," in *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10008-10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.
- S.K. Mazumder, N. Kumar, M. Mohamadi, “Transformer-less, single-stage power module for off-board EV charging,” Patent Application# PCT/US2020/057743, 2020.

1.1 Background

For the past 150 years, humans have relied heavily on coal, oil and other fossil-fuel based resources to accommodate their daily needs due to their ease of harnessing and widespread availability. Subsequently, this has allowed greenhouses gas (GHG) emissions to reach unprecedented levels. One of the largest contributors to the anthropogenic GHG emissions is transportation. According to the *Inventory of US Greenhouse Gas Emissions and Sinks* 1990-2017, transportation alone accounts for 29% of the GHG emissions as shown in Figure 1(a). Electricity production is another major sector that produces GHG emissions by burning coal and natural gas. Within the transportation sector, light-duty and heavy-duty vehicles are the largest contributors of GHG emissions as shown in Figure 1(b) [1][2]. As a result, rising environmental awareness and limited availability of these fossil-fuel based resources has led to the increased prices and paved a pathway for adoption of sustainable and clean energy.



(a) (b)

Figure 1. (a) 2017 US GHG emissions by sector (b) 2017 US transportation GHG emissions by sector [1].

In lieu of this, many nations have taken steps towards harnessing the renewable energy resources by creating solar, wind and hydro farms and reducing current usage of gasoline and diesel-based vehicles [3]. Moreover, to speed the adoption of zero-emission-vehicles, “green number plate” policy has been adopted which acts as an electric vehicle (EV) identifier and financial incentives are given to the drivers such as tax credits, discounted insurance, and high occupancy lane exemption [4][5].

A recent study by McKinsey& Company has shown that EVs penetration into the global vehicular market has crossed 1 million units in past seven years as presented in Figure 2 [6]. Besides the environmental concerns, another factor behind the rising mass adoption of EV’s can be attributed to the decline in the cost of batteries that has led to increased bulk production of EV’s and rise in public charging infrastructure.

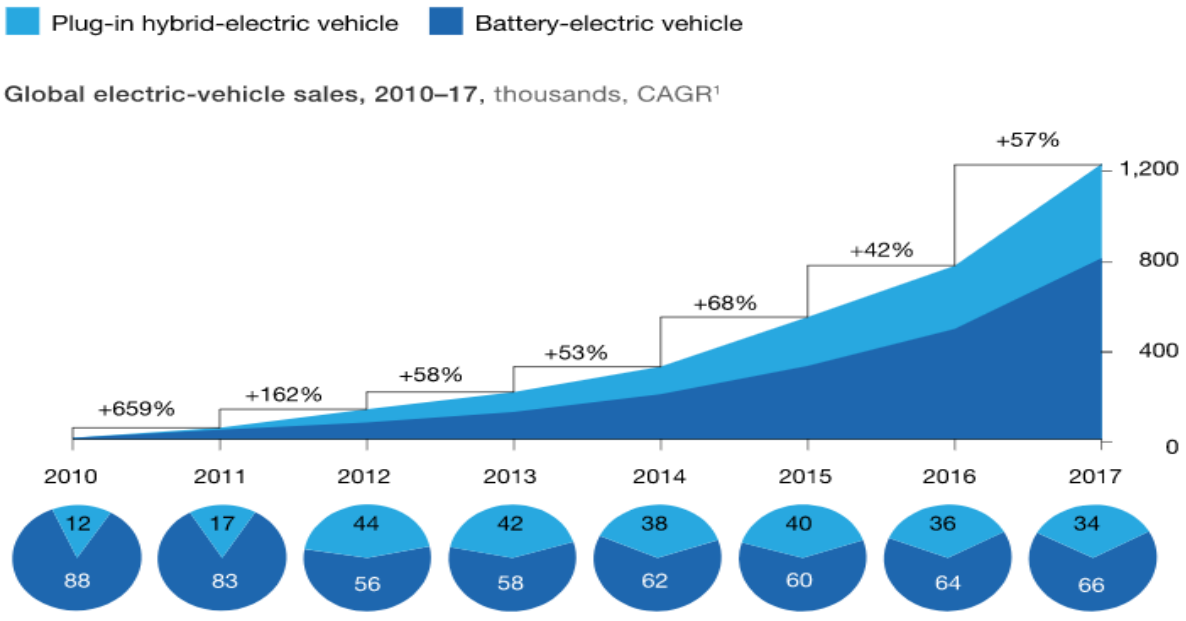
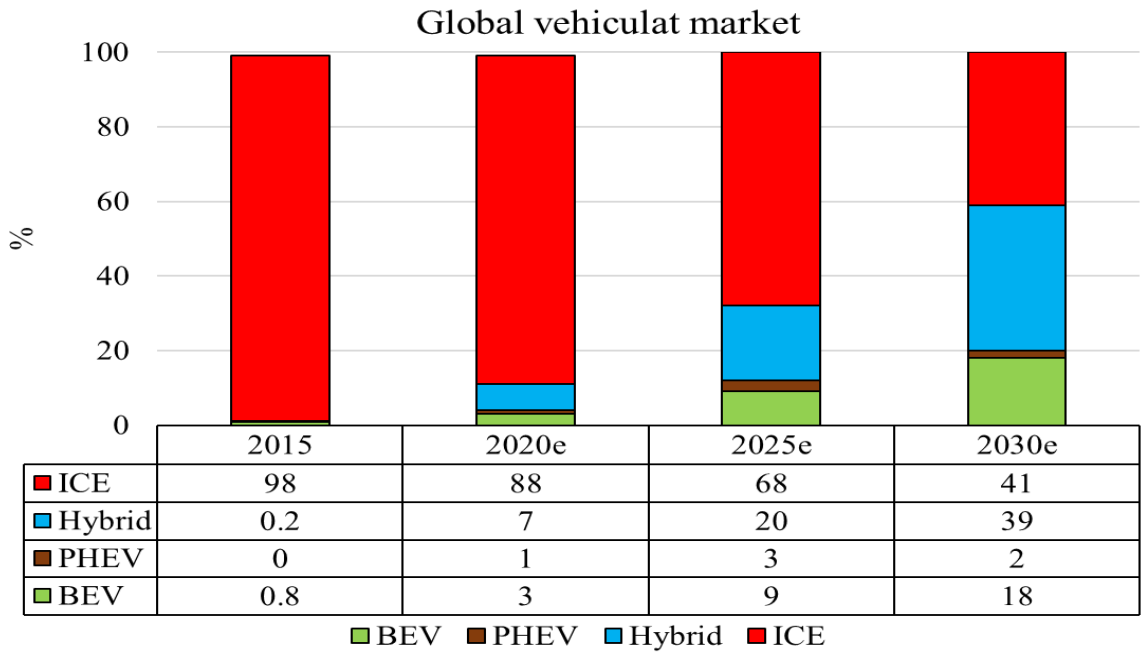


Figure 2. Global sales of the EV and PHEV from 2010-2017 [6].

Based on another study by JP Morgan shows that the number of EVs and hybrids will account for 60% of the global vehicular market by 2030 as shown in Figure 3 [7].



	2015	2020e	2025e	2030e
ICE	98	88	68	41
Hybrid	0.2	7	20	39
PHEV	0	1	3	2
BEV	0.8	3	9	18

Figure 3. JP Morgan study on global vehicular market [7].

Although, in recent years EV market has seen an exponential growth, one of the major challenges faced by the automotive/vehicular market is short driving range of EV's that causes "range-anxiety" among the EV users. This limitation is on to two accounts: low energy density of the EV batteries and slow charging rate which takes hours to recharge as shown in Figure 4 [8][9]. However, advancements in battery technology in the past decade have been remarkable. With the advent of high energy density Li-ion batteries, the driving range of the EVs have increased. Figure 5 illustrates the driving range of EVs on a single charge. It is seen that among others Tesla Model S 100 D has the highest driving range. However, it is also limited to only 335 miles. One possible solution to this problem is setting up a wide network of EV charging stations.

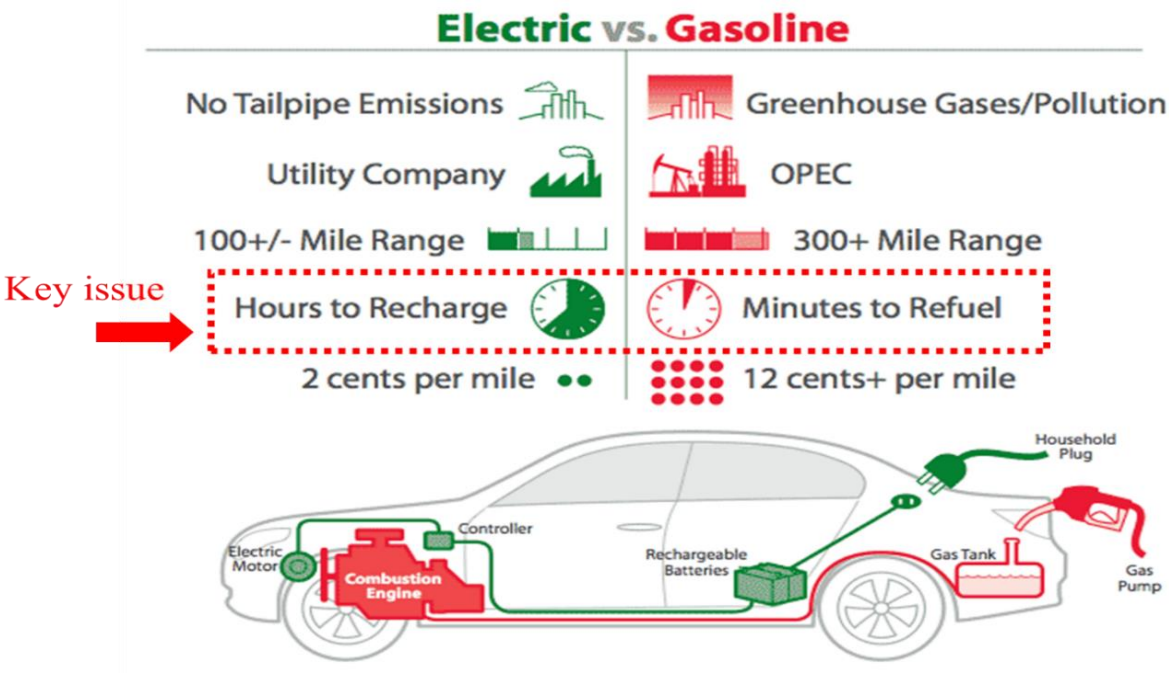


Figure 4. A comparison of EVs and gasoline-based vehicles.

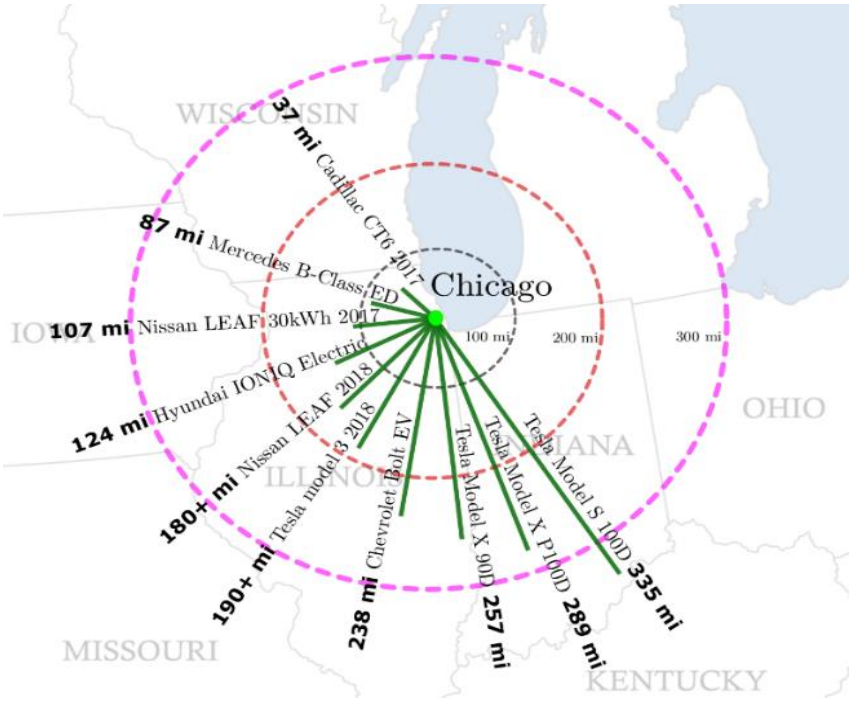


Figure 5. Driving range of various EVs on a single charge from Chicago [10].

However, for competing with the conventional gasoline-powered vehicles the EV charging stations have to be fast and charge the EV batteries in less than 15-30 mins. This has resulted in an increased demand for dc fast chargers.

1.2 Category of EV chargers

Based on the level of EV charging, EV battery chargers are placed in two categories a) On-board chargers b) off-board chargers [11]-[15]. Table I illustrates the type of chargers along with their power levels and limitations on the charge time and driving range.

Table I. Category of EV chargers

Type	Ratings	Estimated Charge Time and driving range
Level-1	120 Vac, 1.4 kW-1.9 kW, 16 A max.	Charge time: 17 hrs (20% to Full) Range: 2-5 miles/hour
Level-2	240 Vac, 3.3 kW-22 kW, 80 A max.	Charge time: 17 hrs (20% to Full) Range: 10-20 miles/hour
Level-3	480-600Vac, 50 kW-240 kW, 400 A max.	Charge time: 15-30 minutes (0% to 80%) Range: 100-200 miles/hour

A. On board chargers

On board chargers (OBC) reside in an EV and are connected to either 120 V (RMS) single-phase or 240 V (RMS) three-phase ac power source. They are further classified as level-1 and level-2 chargers [16]-[18].

Level-1 chargers are single-phase chargers and operate at 120-V (RMS) with a standard wall-

mounted outlet. Depending on the battery capacity, level-1 charger requires 12-17 hours to charge a battery to full capacity or provides a driving range of 2-5 miles/hour of charging. These charges usually found their use in residential applications.

Level-2 chargers provide relatively faster charging rates compared to level-1 chargers and can be used for both private and public facilities (offices, malls, commercial buildings). These chargers require a 240V (RMS) three-phase outlet. The output power of level-2 chargers varies between 3.3 kW – 22 kW and can provide maximum output current of 80 A . However, the charge duration of level-2 chargers lies in the range of 2-6 hours or provides of driving range of 10-20 miles/hour of charging.

B. Off board chargers

Off-board chargers are also termed as level-3 (L3) dc fast chargers. To address the charging duration and driving range of the EVs, recently focus has shifted towards the development of off-board DC fast chargers that bypass the OBC, and directly charge the EV on-board batteries. These chargers operate at 480-V (RMS) three–phase ac and provide regulated DC output at power levels varying between 50 kW to 240 kW. Such high-power levels are typically achieved by stacking multiple power converters in a modular fashion. As a result, these stacked power converters become bulkier to be a part of an EV, and due to the space limitations, they are installed in form of a charging station on highway rest areas or city refueling spots. The time taken to charge an EV battery from 20% to 80% of the state-of-charge (SOC) with a L3 charger varies between 15-30 minutes or provides a driving range of up to 200 miles/hour of charging, subjected to the battery ampacity and charging station output [19][20].

To achieve ac-dc conversion, conventionally diode-bridge rectifiers were used. Although, diode-bridge rectifiers provide cheapest form of ac-dc conversion, they draw non-sinusoidal current by injecting low-order harmonics into the utility grid and degrade the converter performance. To prevent the harmonic pollution, IEEE Std.519-2014 sets the guidelines that puts the limit on the maximum drawable low- and high-order harmonics currents with total harmonic distortion (THD) not exceeding 5% .

1.3 Overview of EV charging topologies

In contrast to the conventional rectifiers, various topologies have surfaced to achieve fast charging of an EV. Moreover, advancements in WBG technology, better magnetic materials and thermal management have enabled these topologies to push their performance limits in terms of efficiency, power-density, and overall weight. A typical L3 dc fast charger is shown in Figure 6.

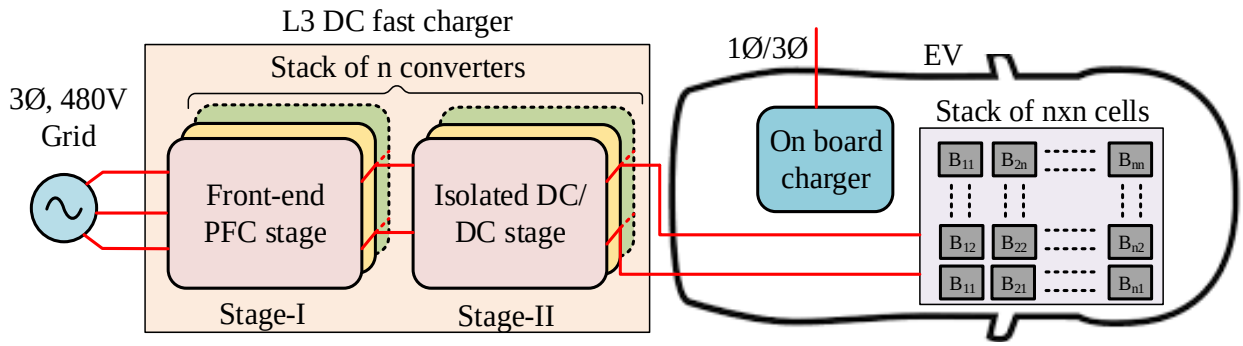
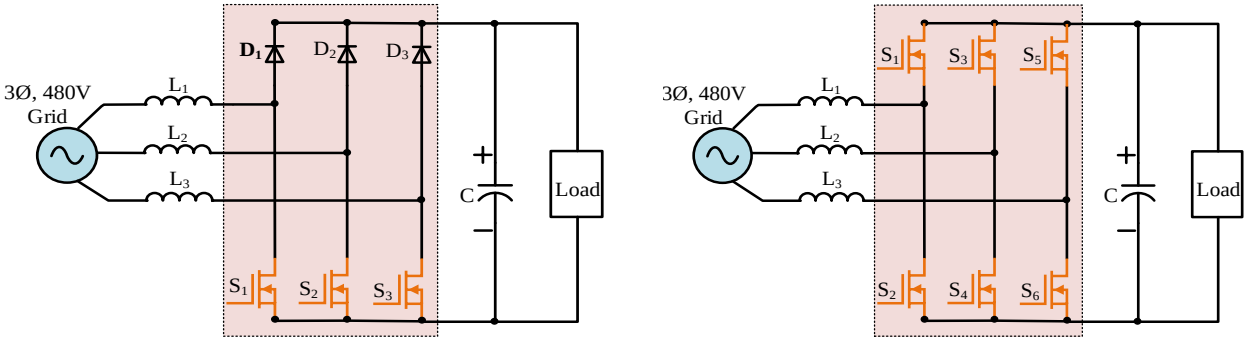


Figure 6. Architecture of a standard L3 dc fast charger.

A L3 dc fast charger achieves ac-dc conversion in two stages [21]-[25]. First-stage corresponds to an active front-end power- factor correction (PFC) converter that regulates the input current for achieving unity power factor (UPF) operation while the second-stage and is comprised of an

isolated dc-dc converter that regulates the output voltage. The architecture of the PFC stage in an EV charger is typically based on boost- and/or buck topology [26]. One of the popular variants of boost-derived topology is a three-phase bridgeless half or fully controlled boost converter as shown in Figure 7 (a) and Figure 7 (b) respectively. The active switches regulate the input line current while achieving lower THD and lower conduction losses in comparison to its diode-bridge counterpart. However, the converter has to operate in discontinuous conduction mode (DCM) to mitigate the reverse recovery of the body diode and avoid voltage overshoot while turning off. As a result, the filter inductors are designed to handle large peak-to-peak ripple current. However, pulsating nature of the output bus voltage generates high common-mode (CM) noise and electromagnetic interference (EMI), which is typically suppressed using large common-mode chokes [27]-[29].



(a) (b)

Figure 7. Bridgeless PFC boost converter (a) half-controlled, (b) fully-controlled.

Another variant of the PFC boost derived topology is interleaved PFC boost converter as shown in Figure 8. The topology is comprised of a diode bridge with boost converter cells connected in

parallel. The interleaving of the boost inductors is achieved by phase shifting the PWM of the active switch such that the sum of the ripple current gets reduced. This reduces the filtering

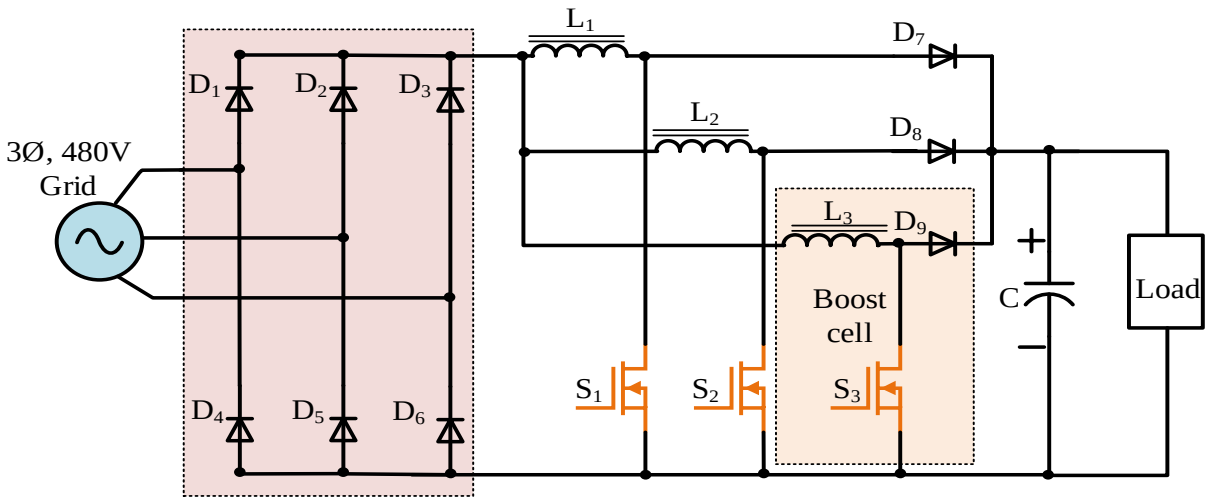


Figure 8. Three-phase interleaved boost converter.

requirements and makes the size of EMI filter small without sacrificing the efficiency. However, due to the heat management issues in the diode bridge, the topology does not scale up the power beyond 3-kW and are often used in level-1 on-board charging configuration. To avoid the input diode bridge and achieve higher power level, a bridgeless interleaved PFC boost converter has been proposed in [30]-[32].

The second-stage of a L3 EV charger is comprised of an isolated dc-dc converter [33]-[35]. For bidirectional power flow application, isolated dual-active bridge (DAB) converter is commonly used as shown in Figure 9. The isolated DAB topology includes two active full-bridge circuits, a series inductor L, and a HF transformer for galvanic isolation between input and the output terminals. The phase-shift modulation allows the inductor current to discharge and charge the output capacitance C_{oss} of the incoming (turning-on) and outgoing (turning-off) device

respectively.

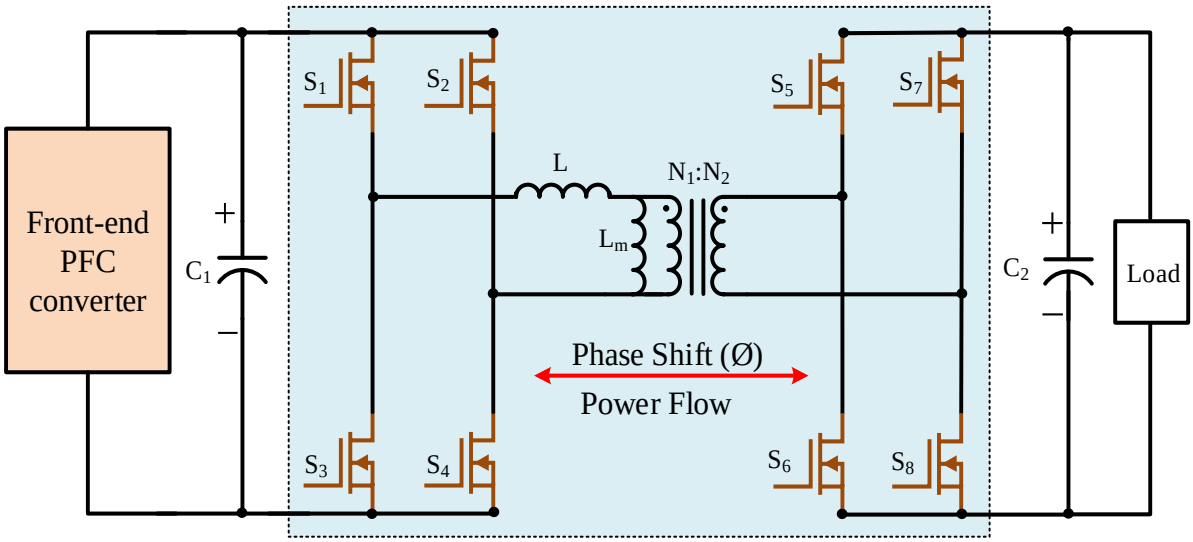


Figure 9. Isolated dual active bridge (DAB) dc-dc converter.

This allows devices to be switched at zero-voltage (ZVS), thereby enhancing the efficiency of the converter. The simplicity in design, and high power density coupled with inherent soft-switching makes the DAB an attractive solution for high-power EV charging applications However, it suffers from limited ZVS range and higher circulating current at light loads. To achieve ZVS for a wide operating region, a number of techniques such as extended-phase modulation and triple-phase modulation have been proposed in [36][37]. Another variant of the isolated dc-dc converter topology is based on the resonant dc-dc converters. Resonant converter topologies achieve very low switching losses that enables it to operate at higher switching frequencies and is an attractive alternative to the DAB. Figure 10 displays an isolated series resonant LLC dc-dc converter.

Carefully selected values of the resonant tank L_r, L_m, and C_r allows the devices to be soft-

switched (ZVS). This is achieved by operating the converter in the inductive region such that the

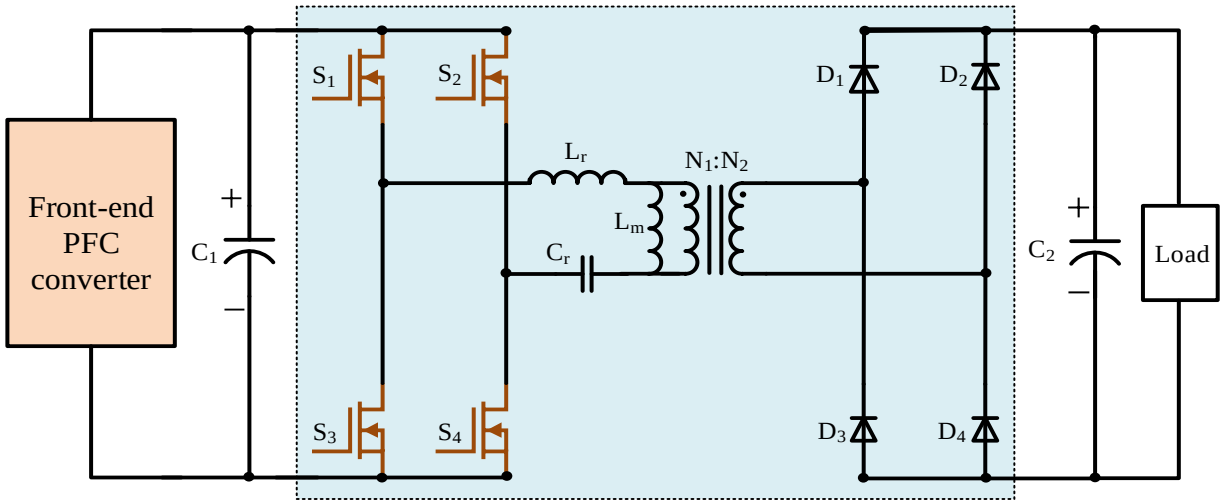


Figure 10. Isolated series-resonant LLC unidirectional dc-dc converter.

current through the resonating inductor lags the switching nodal voltage. However, soft-switching is quite sensitive to the loading conditions. At light loads, the switching frequency has to be increased much higher than the resonating frequency to keep the output voltage regulated. Further, as the input voltage is increased, circulating energy increases and as a result the switches turn off at higher current, increasing turn-off losses [38][39]. Apart from DAB, and LLC, other single-stage topologies such as Vienna rectifier, multilevel converters such as neutral-point-clamped (NPC), and active neutral-point clamped (ANPC) topologies have been proposed in [40][41]. Though apart from achieving soft-switching, these topologies claim to reduce the device stress, however, end up using more devices that reduces the reliability.

1.4 Objective

In this thesis, a UBS is presented for dc fast charging application that is based on a three-phase differential-mode Ćuk rectifier (DMCR) as shown in Figure 11. DMCR has some advantage over other topologies, such as single-stage conversion with fewer switches, bidirectional power flow capability and continuous input and continuous output current [42]-[46] with buck and boost capability. It is a promising configuration for renewable-/alternative-energy applications with isolated and non-isolated topological realizations [47][48]. In non-isolated realization,

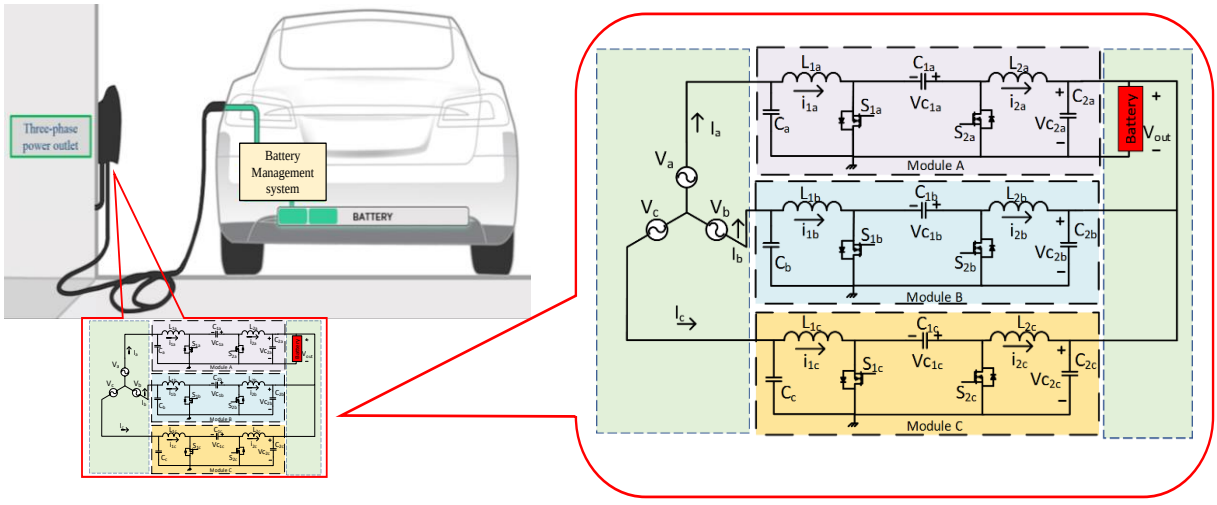


Figure 11. Universal Battery Supercharger (UBS) for L3 DC fast charging application.

the lack of transformer and symmetry of the converter leads to the identical applied voltage across the ac-side and dc-side inductors, thus making them a suitable candidate for magnetic integration [49]-[51]. The integrated magnetics (IM) provides various advantages in terms of a) enhancing the power density and specific weight of the converter, b) lowering the total harmonic distortion (THD) by ripple cancellation, and c) improving efficiency by lowering the core loss. This is

typically achieved by coupling of the ac-and dc-side inductors windings to achieve maximum flux cancellation. However, the topology has its own challenges. Nonlinear nature of the DMCR coupled with higher-order dynamics, makes the converter control complex and challenging [52]-[54]. Further, absence of damping in the ac-link path gives rise to LC oscillations, and if not controlled, may degrade the overall performance of the converter. To dampen these oscillations, passive damping technique that employs an RC network in parallel to the ac-link capacitance is used. Other techniques, such as active damping methodology, suppress these oscillations by adding an anti-resonant component to the duty-cycle modulation, and typically requires an additional sensing mechanism.

To evaluate the DMCR topology as a candidate for DC fast charging application, first an overview of the topology along with its modulation scheme and HF operating modes are discussed in Chapter 2. Second, to understand the dynamics of DMCR and to address the associated control challenges, Chapter 3 presents a small-signal analysis that leads to the development of control architecture for achieving PFC and output voltage tracking. With the goal to design and develop 60-kW UBS, in Chapter 4, first, a scaled-power prototype (sp-UBS) is designed and validated for its operational feasibility. To test the effectiveness of the integrated magnetics (IM) with discrete magnetics (DM), parametric performance results comparing the ripple, THD, and efficiency are provided. After careful evaluation of the sp-UBS, a systematic approach for the design and development of the 60-kW UBS is presented. The developed prototype is tested and the experimental results displaying tracking performance, power quality, efficiency are presented.. The thesis is concluded in Chapter 5 with some propositions for the future work.

Chapter 2

2. DMCR TOPOLOGY AND MODES OF OPERATION

Parts of this chapter, including figures and text, are based on my following papers:

- N. Kumar, M. Mohamadi and S. Mazumder, "Experimental Validation of Single-Stage Three-Phase Non-Isolated Cuk Rectifier," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 2744-2751, doi: 10.1109/ECCE.2019.8912485.
- N. Kumar, M. Mohamadi and S. K. Mazumder, "Passive Damping Optimization of the Integrated-Magnetics-Based Differential-Mode Ćuk Rectifier," in *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10008-10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.
- S.K. Mazumder, N. Kumar, M. Mohamadi, “Transformer-less, single-stage power module for off-board EV charging,” Patent Application# PCT/US2020/057743, 2020.

2.1 Differential-Mode-Ćuk-Rectifier (DMCR) topology

The differential-mode-Ćuk-rectifier (DMCR) is comprised of three Ćuk converter modules; module A, module B, and module C. As shown in Figure 12, input of the Ćuk converter modules are connected differentially to the three-phase ac power supply while the outputs are connected in parallel configuration to the load. Each Ćuk converter module consists of two inductors (L_{1a}, L_{2a}), three capacitors (C_a, C_{1a}, C_{2a}), and two devices (S_{1a}, S_{2a}). The two inductors L_{1a} and L_{2a} can be categorized as ac-side inductor and dc-side inductor respectively. The two capacitors C_a and C_{1a} are high-frequency ac-link capacitors while the third capacitor C_{2a} is a low-frequency dc-link capacitor. Switches S_{1a} and S_{2a} are SiC MOSFETs and are connected in half-bridge configuration.

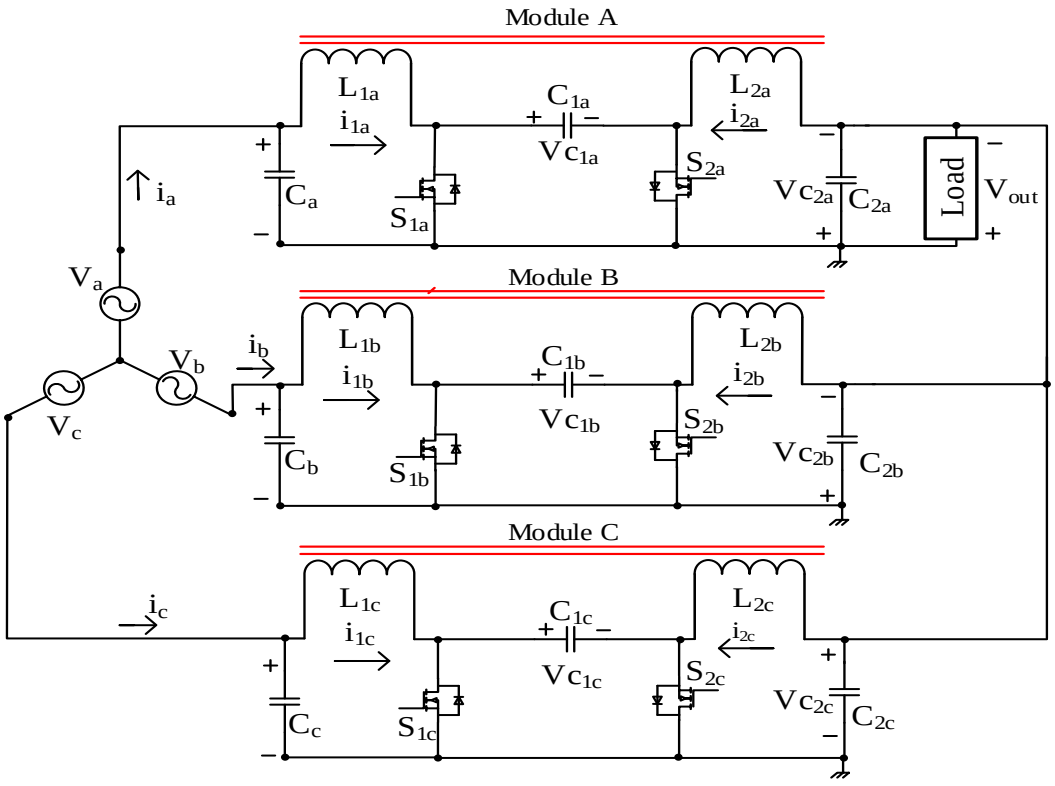


Figure 12. Three-phase differential-mode Ćuk rectifier schematic representation [55].

2.2 DMCR switching scheme

To demonstrate the basic operation of the DMCR and for the estimation of the device and magnetic losses, switches S_{1a}, S_{2a}, S_{1b}, S_{2b}, S_{1c}, and S_{2c} are considered to be hard-switched. Based on the hard-switching scheme, a pulse width modulation (PWM) technique is used. In literature, modulation schemes such as continuous modulation scheme (CMS) and discontinuous modulation scheme (DMS) have been employed for differential-mode Ćuk inverter [56][57]. A comparison between CMS and DMS have been shown in [5][6], which clearly indicates the superiority of DMS over CMS. Based on the DMS, each module does the high-frequency (HF) switching for *2/3rd* of the line cycle and maintains a constant switch configuration for rest of the *1/3rd* line cycle as shown in Figure 13. The duty-cycle modulation duty_a, duty_b, and duty_c are provided to switches S_{2a}, S_{2b}, and S_{2c} respectively.

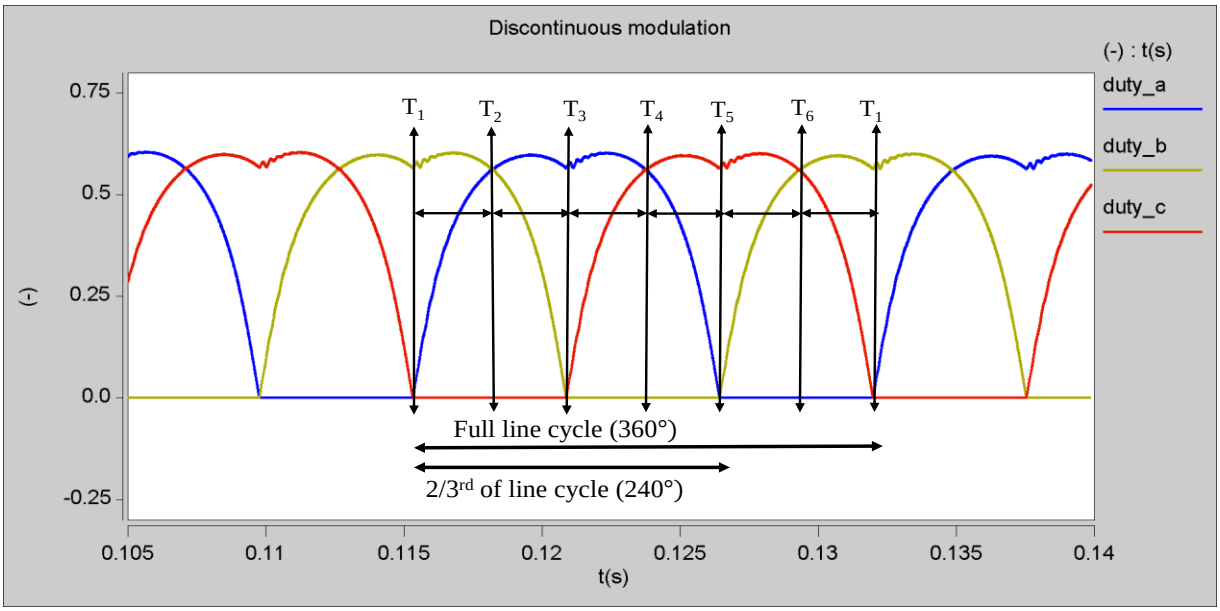


Figure 13. Duty-cycle modulation signal of phase a, b, and c in blue, yellow, and red respectively.

2.3 DMCR HF operating modes

Using Figure 13 and Figure 14, Table 1 displays the duration of activation of each mode in a 60-Hz line cycle. Based on the DMS, four HF operating modes are identified as shown in Figure 15. As evident from Table 1, during the time interval of $T_1 \leq t < T_2$, modes M1, M2, and M3 are active while in the time interval of $T_2 \leq t < T_3$, modes M4, M2, and M3 are active.

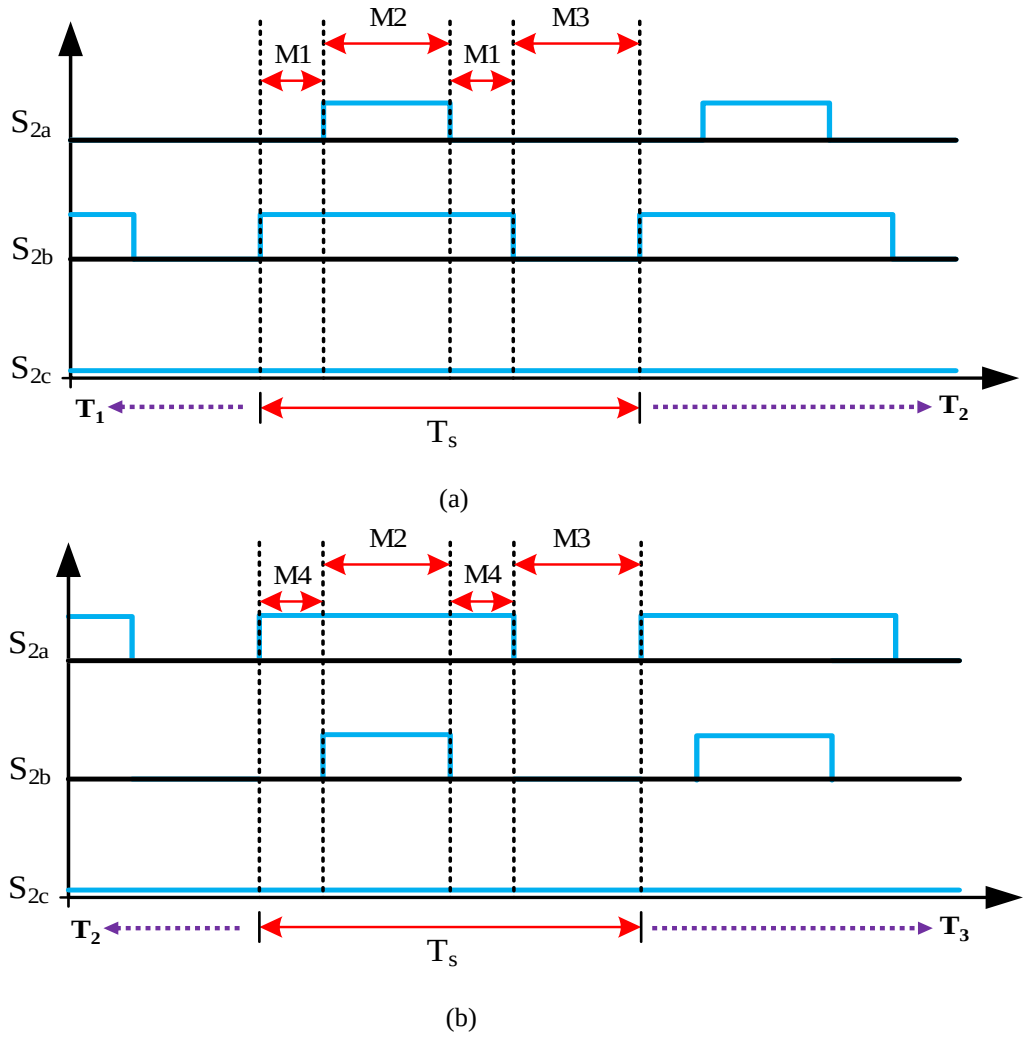


Figure 14. HF switching states during time interval $T_1 \leq t < T_3$ (a) M1, M2, and M3 (b) M1, M2, and M4.

Thus, in the duration of $T_1 \leq t < T_3$, module A and module B does HF switching while phase C maintains a constant switch configuration. The modes are repeated in a similar manner in the subsequent time intervals. Figure 15 represents the switching states of six switches during each mode of operation.

Table II. HF modes of operation of the DMCR based on Figures 13 and 14.

Duration		Modes		
HF transition from phase C to phase A (phase B maintains HF switching)				
$T_1 \leq t < T_2$	1/6th of the line cycle (60°)	M1	M2	M3
$T_2 \leq t < T_3$	1/6th of the line cycle (60°)	M4	M2	M3
HF transition from phase B to phase C (phase A maintains HF switching)				
$T_3 \leq t < T_4$	1/6th of the line cycle (60°)	M1	M2	M3
$T_4 \leq t < T_5$	1/6th of the line cycle (60°)	M4	M2	M3
HF transition from phase A to phase B (phase C maintains HF switching)				
$T_5 \leq t < T_6$	1/6th of the line cycle (60°)	M1	M2	M3
$T_6 \leq t < T_1$	1/6th of the line cycle (60°)	M4	M2	M3

Mode M1 ($T_1 \leq t < T_2$):

As shown in Table 1 and Figure 13, mode M1 starts at the beginning of the time T_1, when phase C relinquishes the control and is taken over by phase A. At this time the module C switches S_{1c} (on) and S_{2c} (off) maintains a constant switch configuration for *1/3*rd of the line cycle (T_1 to T_3) and duty cycle of module A starts to pick up. The equivalent circuit for mode M1 is shown in Figure 15(a). Throughout this duration, module A and module B does HF switching and module C carries the line current, $I_c = I_a + I_b$. Red and blue signals represent the flow of low-frequency and high-frequency current components respectively. In mode M1, the dc-side inductor L_{2a} is charged by the ac-link capacitor C_{1a} while ac-side inductor L_{1a} gets charged by the ac-supply. Further at $t = T_1$, the ac-side inductor L_{1b} discharges into the ac-link capacitor C_{1b} while the dc-side inductor L_{2b} charges the dc-link capacitor C_{2b}.

Mode M2 ($T_1 \leq t < T_2$):

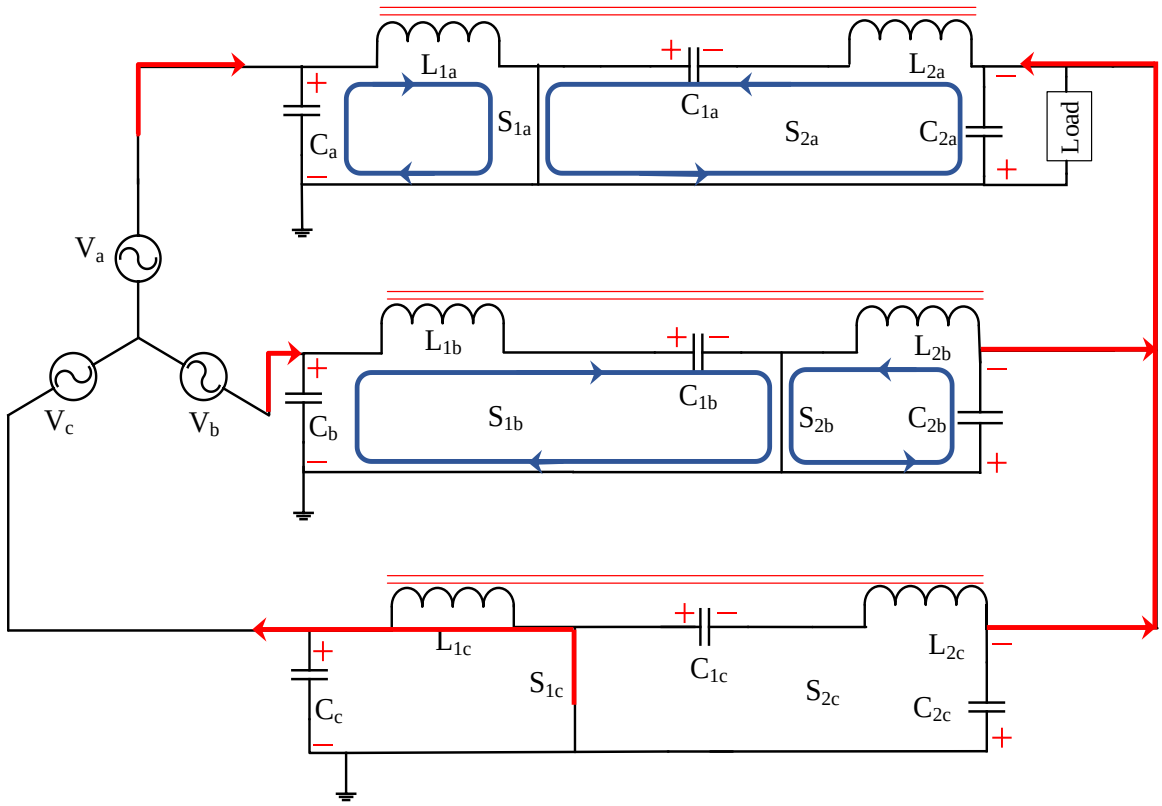
As evident from the gate pulses shown in Figure 14, mode M2 occurs when S_{2a} and S_{2b} are in the ON state. In this mode, dc-side inductors L_{2a} and L_{2b} discharge into the dc-link capacitors C_{2a} and C_{2b} respectively. The equivalent circuit for mode M2 is shown in Figure 15 (b).

Mode M3 ($T_1 \leq t < T_2$):

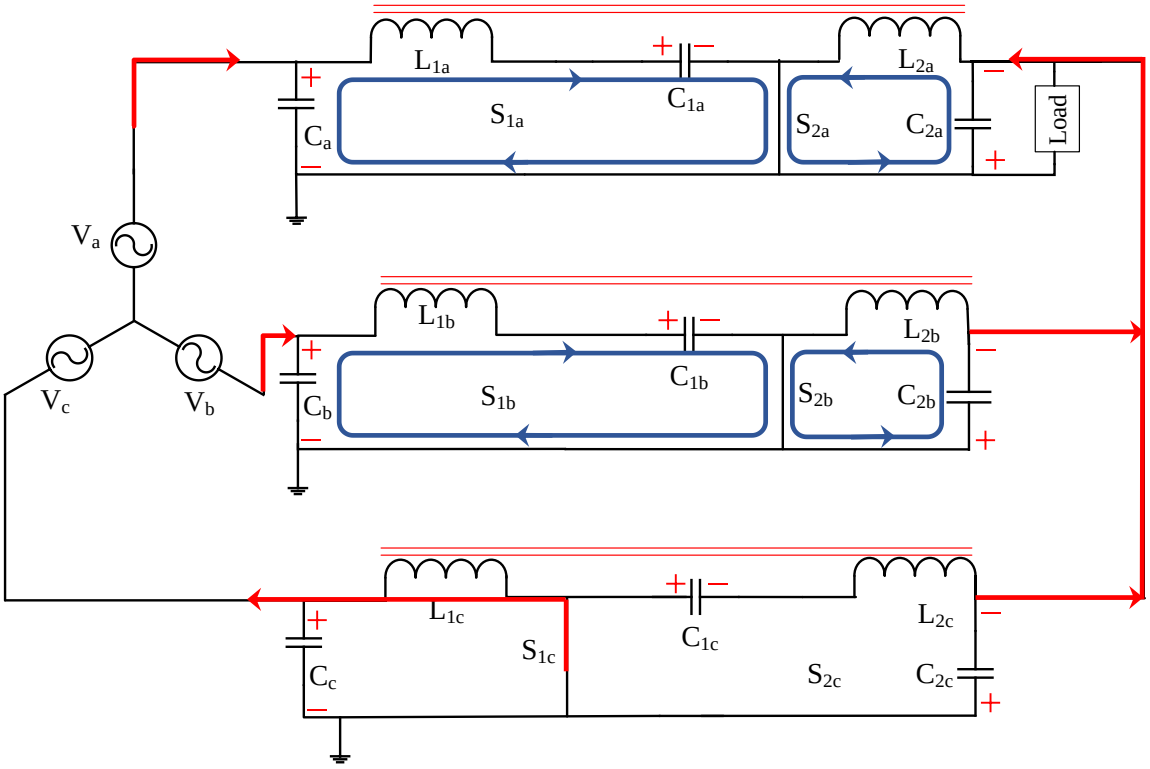
This mode occurs when both the switches S_{2a} and S_{2b} are in the OFF state as shown in Figure 14. In this mode, the blocking capacitors C_{1a} and C_{1b} discharge into dc-side inductors L_{2a} and L_{2b} while ac-side inductors L_{1a} and L_{1b} gets charged by input voltage V_a and V_b respectively. The equivalent circuit for mode M3 is shown in Figure 15 (c).

Mode M4 ($T_2 \leq t < T_3$):

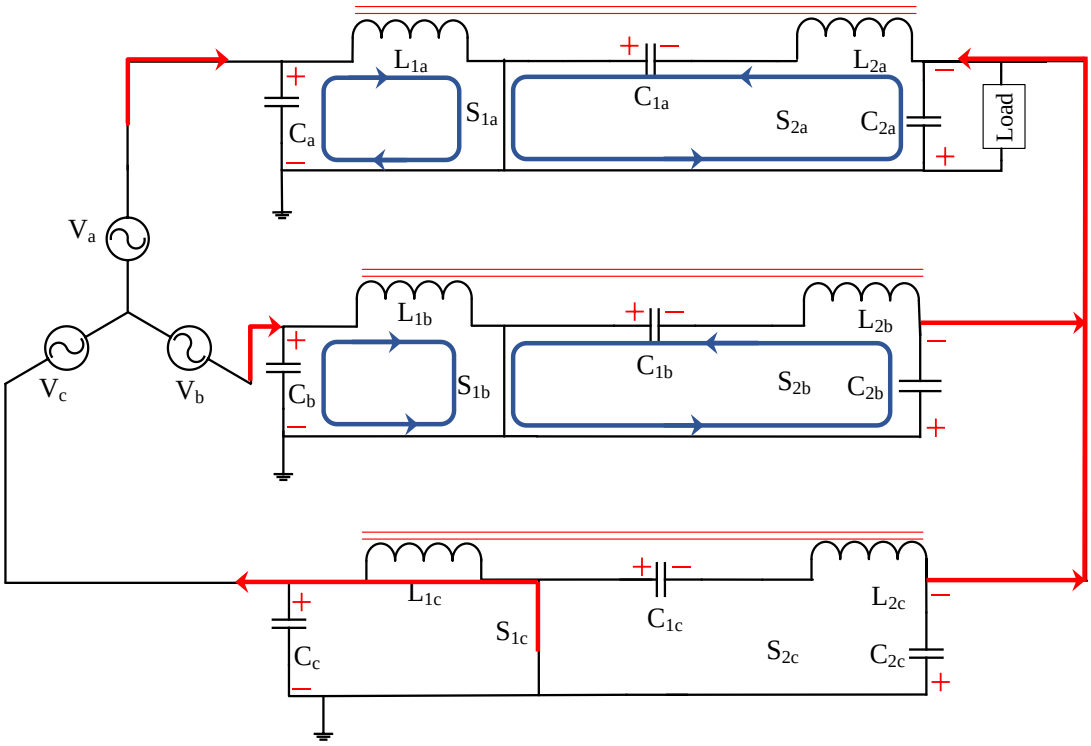
This mode is similar to mode M1 except now, the duty-cycle of module A is higher than module B as shown in Figure 13. The gate pulses corresponding to this time interval is shown in Figure 14 (b). Again, in this mode, the dc-side inductor L_{2a} discharge the dc-link capacitor C_{2a}, while ac-side inductor L_{1a} charges the ac-link capacitor C_{1a}. At the same time, ac-side inductor L_{1b} gets charged by V_b, ac-link capacitor C_{1b} discharges into dc-side inductor L_{2b}. The equivalent circuit for mode M3 is shown in Figure 15 (d).



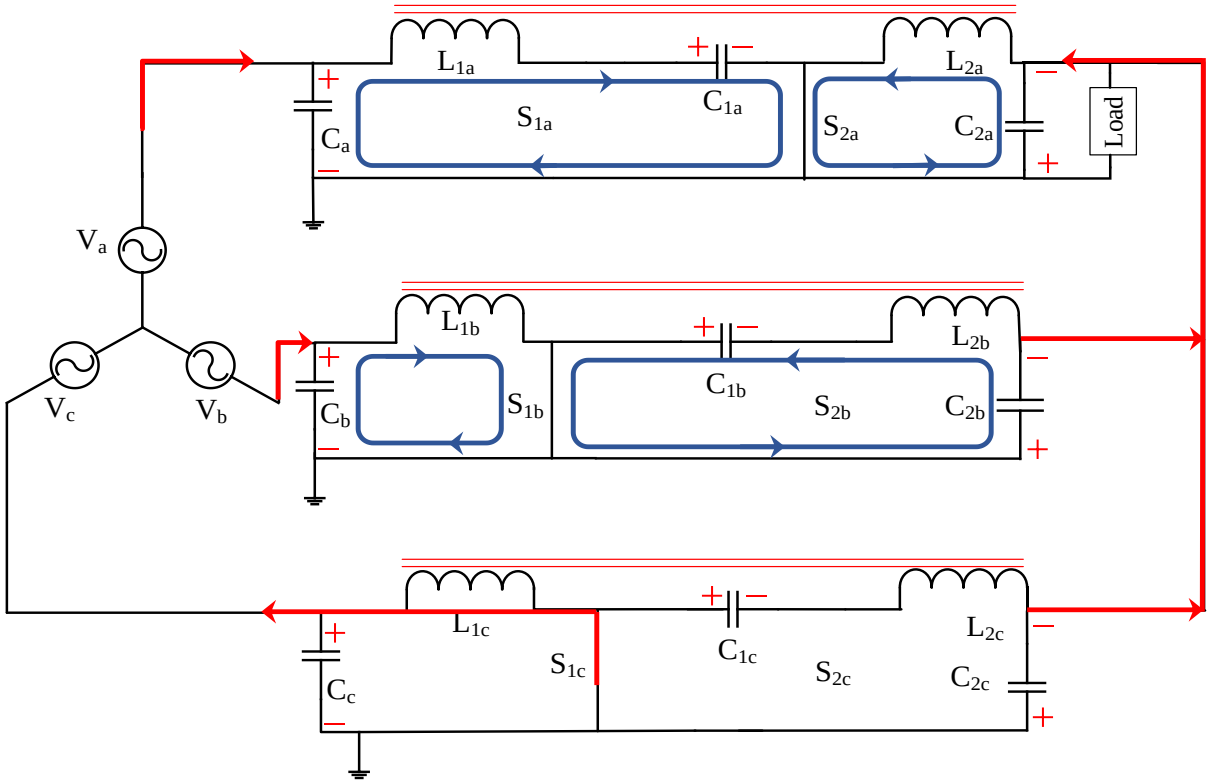
(a)


L1a
C1a
L2a
S1a
S2a
C2a
Load
Ca
Va
L1b
C1b
L2b
Vc
Vb
S1b
S2b
C2b
Cb
L1c
C1c
L2c
S1c
S2c
C2c
Cc

(b)


L1a
C1a
L2a
S1a
S2a
C2a
Load
Ca
Va
L1b
C1b
L2b
Vc
Vb
S1b
S2b
C2b
Cb
L1c
C1c
L2c
S1c
S2c
C2c
Cc

(c)



(d)

Figure 15. HF modes of operation of the DMCR in $^{1}/_{3}$ rd of the 60-Hz line cycle $T_1 \leq t < T_3$ (a) Mode M1, (b) Mode M2, (c) Mode M3, and (d) Mode M4.

2.4 Piece-wise power flow in the DMCR

Figures 16 and 17 displays a piecewise flow of active (circulating) power and instantaneous power in the DMCR modules respectively. The flow of active and circulating power are represented by arrows in red and yellow. The power distribution curve in Figure 17 has been divided into four zones for depicting the power-flow in figure 16. As shown in Figure 16 (a) and Figure 17, between the time interval $0 \leq t < t_1$ rated power is shared amongst module A and module B, while module C is inactive.

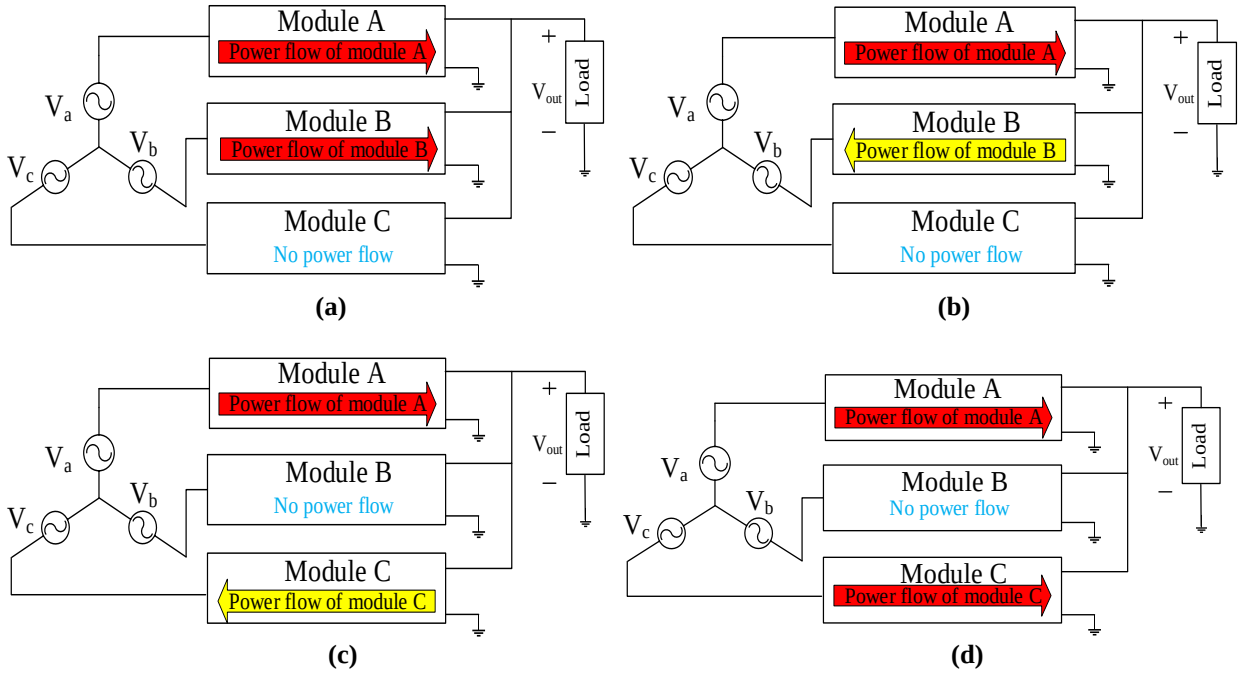


Figure 16. Representation of active power flow (red) and circulating power flow (yellow) in the DMCR. (a) Rated power is shared amongst module A and module B. (b) Flow of active power and circulating power through Module A and Module B respectively. (c) Flow of active power and circulating power through Module A and Module C respectively. (d) Rated power is shared amongst module A and module C.

In other words, on an average each module provides half of the rated active power in this time duration. In the second time interval $t_1 \leq t < t_2$, the module A alone provides full-rated power, while a small amount of circulating power flows in module B as shown in Figure 16 (b) and 17. In the next time interval $t_2 \leq t < t_3$, as module C starts to pick up, module A still provides full-rated power and a small amount of circulating power flows through module C as shown in Figure 16 (c) and Figure 17. In Figure 16 (c) and 17, between the time interval $t_3 \leq t < t_4$, once again the full-rated power is shared amongst module A and module C. It is noted from the power distribution curve that each module has to be designed for handling the full-rated power in a 60-Hz line cycle.

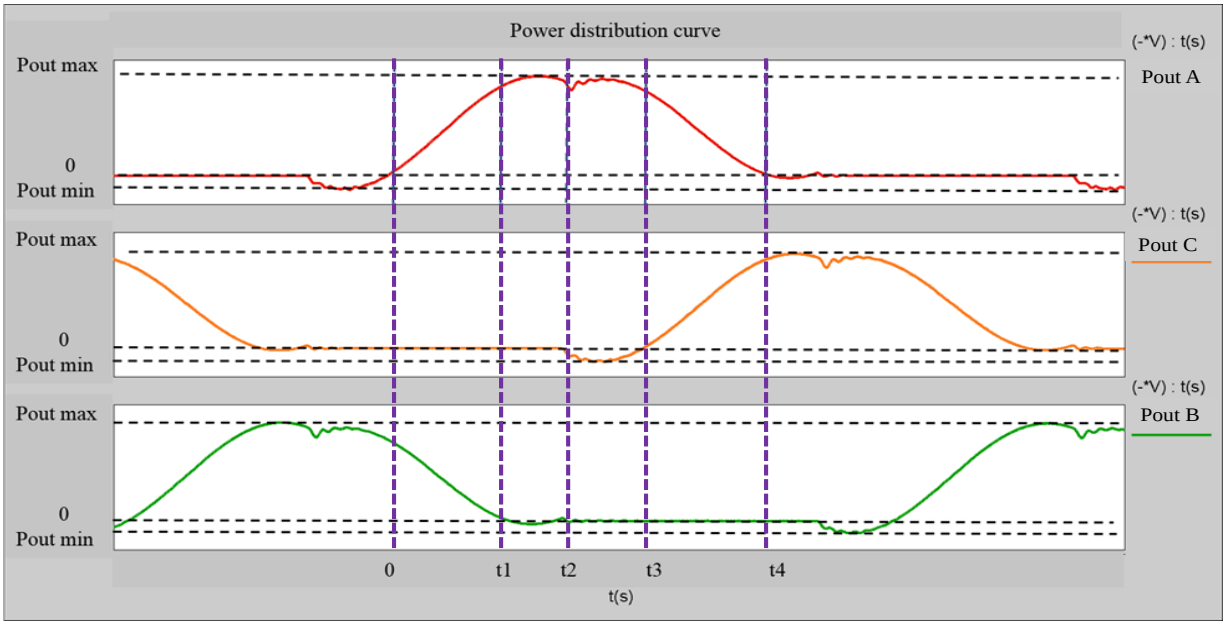


Figure 17. Instantaneous power flow through module C (red), module B (orange) and module A (green).

Chapter 3

3. DMCR CONTROL

Parts of this chapter, including figures and text, are based on my following papers:

- N. Kumar, M. Mohamadi and S. K. Mazumder, "Passive Damping Optimization of the Integrated-Magnetics-Based Differential-Mode Ćuk Rectifier," in *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10008-10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.
- S.K. Mazumder, N. Kumar, M. Mohamadi, “Transformer-less, single-stage power module for off-board EV charging,” Patent Application# PCT/US2020/057743, 2020.

3.1 Overview of Battery charging control

An EV battery can be charged in three modes of operation; a) constant current (CC), b) constant voltage (CV), and c) combination of CC and CV. Combination of CC and CV mode of charging is the most effective way to achieve fast charging without sacrificing the battery lifetime. As defined by the standard IEEE 2030.1.1-2015 [58], to achieve fast charging of EV, first, the battery is charged in CC mode at a higher C-rate and is limited by the battery maximum ampacity and internal temperature rise.

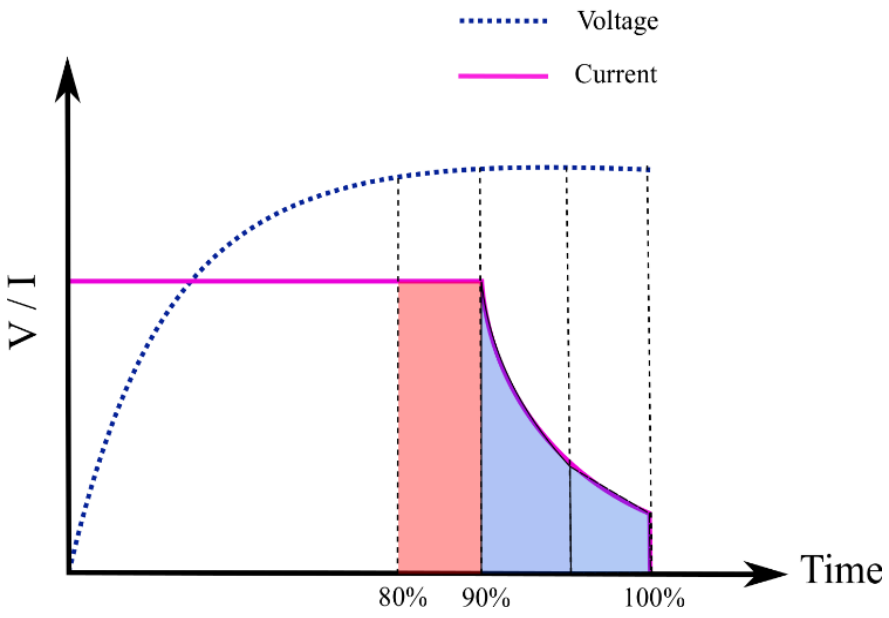


Figure 18. Constant-current (CC) and constant-voltage (CV) mode of charging [59].

After reaching a particular safe voltage, the charging control shifts to the CV mode of operation as the charging current gradually reduces. The charging duration as dictated by level-3 dc fast chargers corresponds to the CC mode of operation as bulk of the charge is provided in this mode. As shown in Figure 18, the CC mode charges the battery from 20 % state of charge (SOC) to 80 % SOC while

rest of the charge is provided in CV mode of operation and usually takes 40-50 mins to achieve 100% SOC. The charging process is terminated when the charging current reaches to 12.5% of its rated value.

3.2 DMCR control

To achieve power factor correction for unity-power factor operation and output voltage mode control, a standard dual loop control architecture is used with current control being the inner loop and output voltage control being the outer loop. However, before diving into the control architecture, a small-signal model is first constructed to understand the Ćuk converter dynamics with respect to the duty-cycle perturbation. Figure 19 display a circuit schematic representation of the DMCR module.

3.2.1 Small signal model of the Ćuk converter

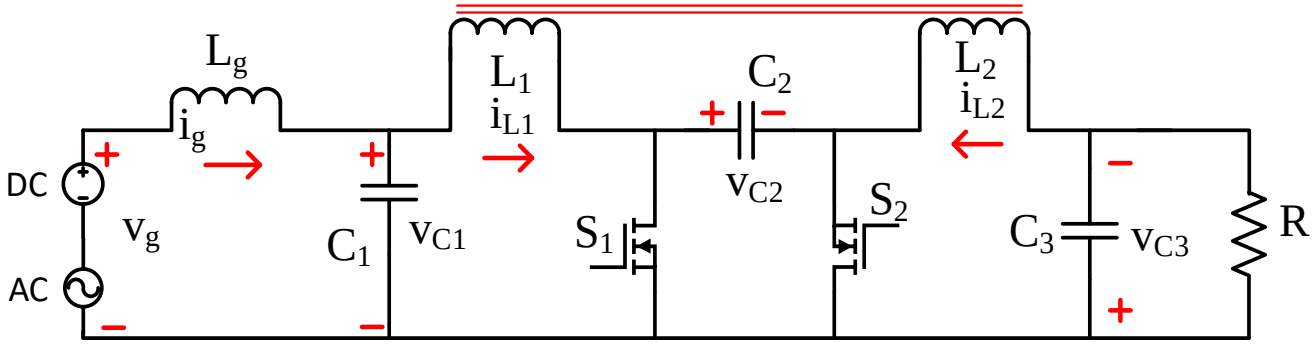


Figure 19. Circuit representation of the IM based Ćuk converter.

Using the state-space averaging technique, the state equations of the DMCR can be written as follows,

$$\dot{x} = Ax + Bu \tag{1}$$

$$y = Cx + Du \tag{2}$$

where $x^T = [i_{L1} \quad i_{L2} \quad v_{c1} \quad v_{c2} \quad v_{c3} \quad i_g]^T$, $y = i_g$, and $u = V_g$

During the first subinterval when switches S_1 and S_2 are in the ON and OFF state respectively, the state matrices are expressed as follows;

$$\dot{x} = A_1 x + B_1 u \tag{3}$$

$$y = C_1 x + D_1 u, \tag{4}$$

where matrices A_1, B_1, C_1, and D_1 are defined as follows;

$$A_1 = \begin{bmatrix} 0 & 0 & \frac{L_2}{(L_1L_2 - M^2)} & \frac{-M}{(L_1L_2 - M^2)} & \frac{M}{(L_1L_2 - M^2)} & 0 \\ 0 & 0 & \frac{-M}{(L_1L_2 - M^2)} & \frac{L_1}{(L_1L_2 - M^2)} & \frac{-L_1}{(L_1L_2 - M^2)} & 0 \\ \frac{-1}{C_1} & 0 & 0 & 0 & 0 & \frac{1}{C_1} \\ 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{RC_3} & 0 \\ 0 & 0 & \frac{-1}{L_g} & 0 & 0 & 0 \end{bmatrix}$$

$$B_1{}^T = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{L_g} \end{bmatrix}^T$$

$$C_1 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]$$

$$D_1 = 0$$

During the second subinterval when switches S_{1a} and S_{2a} are in the OFF and ON state respectively, the state matrices are expressed as follows;

$$\dot{x} = A_2 x + B_2 u \tag{5}$$

$$y = C_2 x + D_2 u, \tag{6}$$

where matrices A_2, B_2, C_2, and D_2 are defined as follows;

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{L_2}{(L_1L_2 - M^2)} & \frac{-L_2}{(L_1L_2 - M^2)} & \frac{M}{(L_1L_2 - M^2)} & 0 \\ 0 & 0 & \frac{-M}{(L_1L_2 - M^2)} & \frac{M}{(L_1L_2 - M^2)} & \frac{-L_1}{(L_1L_2 - M^2)} & 0 \\ \frac{-1}{C_1} & 0 & 0 & 0 & 0 & \frac{1}{C_1} \\ \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{RC_3} & 0 \\ 0 & 0 & \frac{-1}{L_g} & 0 & 0 & 0 \end{bmatrix}$$

$$B_2{}^T = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{L_g} \end{bmatrix}^T$$

$$C_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$D_2 = 0$$

Using the equations above, the state equation of the small-signal model are,

$$\dot{x} = A\hat{x} + B\hat{u} + \{(A_1 - A_2)X + (B_1 - B_2)U\}\,\hat{d} \tag{7}$$

$$y = C\hat{x} + D\hat{u} + \{(C_1 - C_2)X + (D_1 - D_2)U\}\,\hat{d}, \tag{8}$$

where $A = A_1 d + A_2(1-d)$, $B = B_1 d + B_2(1-d)$, and $X = -A^{-1}BV_{in}$.

Symbol M reprsents the coupled inductance and is expressed in terms of the coupling factor (c) as follows,

$$M = c\sqrt{L_1 L_2}$$

The grid-current ($\hat{i_g}$) to duty-cycle ($\hat{d}$) transfer function (G_{id}) for the IM based DMCR can be expressed by the following equation,

$$G_{id} = \frac{N(s)}{D(s)} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (9)$$

The coefficients of numerator and denominator are provided in Appendix B. Due to the implicit nature and complexity of the polynomial $D(s)$, an approximate qualitative analysis is carried out. For simplicity, the ac- and dc-side inductances L_1 and L_2 are considered to be the same. Using the small-signal approximation and chosen parameters as displayed in Table III, frequency response of the G_{id} is shown in Figure 20.

Table III. Power-stage parameters used for simulation and small-signal analysis.

Parameter	L_1	L_2	M	L_g	C_1	C_2	C_3	R
Value	$200\mu H$	$200\mu H$	$100\mu H$	$1mH$	$6.8\mu F$	$1.5\mu F$	$1mF$	15Ω

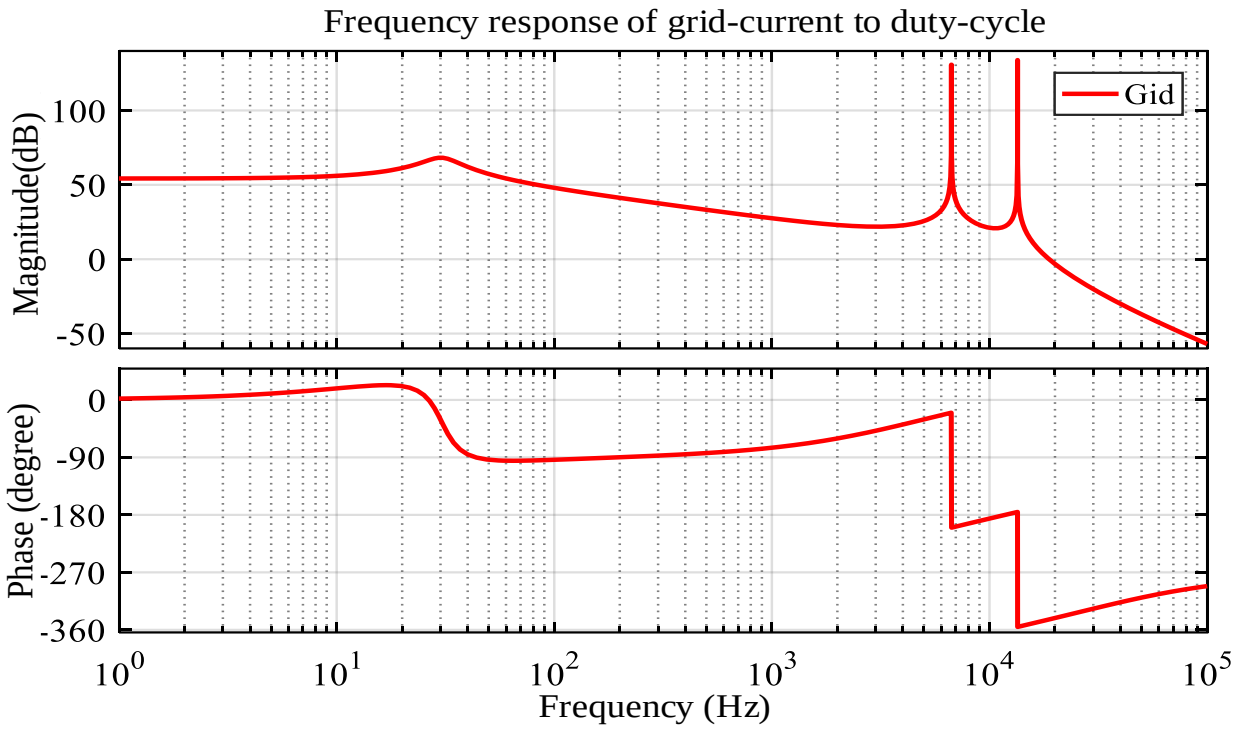
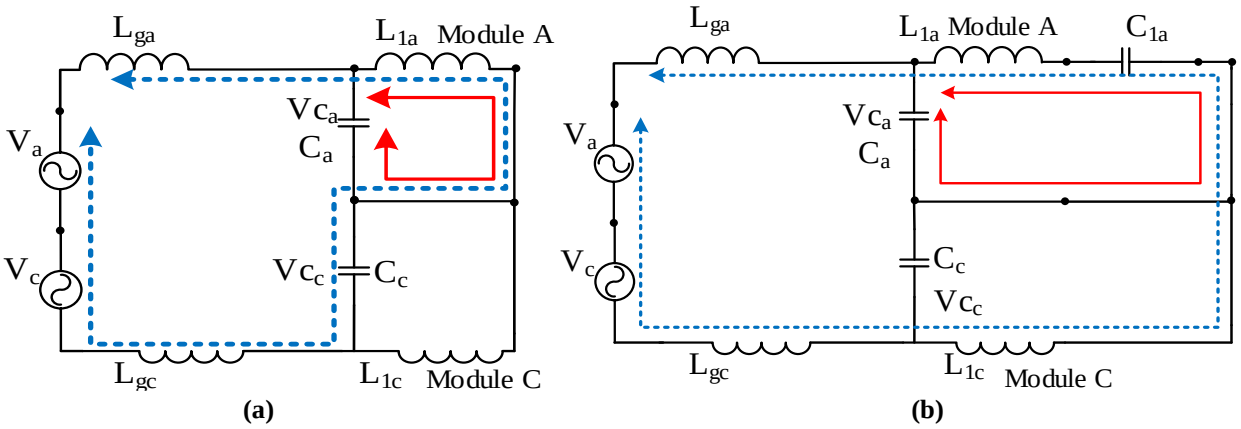


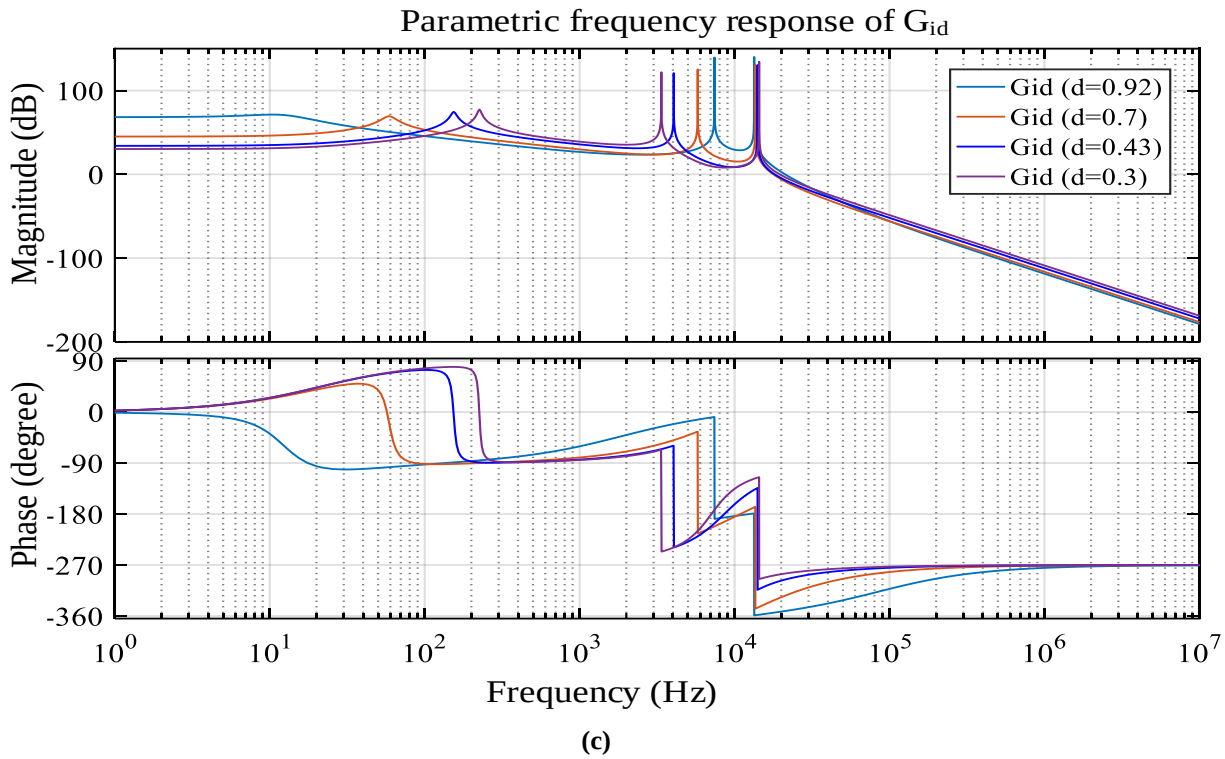
Figure 20. Open-loop frequency response of the grid-current to duty-cycle (G_{id}).

As evident from the Figure, the open-loop frequency response of G_{id} consists of three right-half plane (RHP) zeros and six left-half plane (LHP) poles (three complex conjugate pole pairs). It is noted that the frequency response has two sharp resonance peaks at 7.5 kHz and 15 kHz close to each other and results in sharp phase drop below 180° at crossover frequency. These resonance oscillations arises mainly due to the switching of the C_2 and its interaction with the L_g, L_1, and C_1 that manifests in the form of a pair of complex conjugate zeros and poles in close proximity of each other. If these resonance peaks resides within the close-loop control bandwidth, it gives rise to uncontrollable LC oscillations that deteriorates the input current quality and compromise overall performance of the converter.

3.2.2 LC resonance oscillations

Following the DMS for the DMCR, Figures 21 (a) and 21 (b) displays the resonance paths when modulating switch S_{1a} turns ON and OFF respectively, while 21 (c) represents the frequency response of the G_{id} for different duty-cycles. It is assumed that for *1/3rd* of the 60-Hz line cycle, module A, and module B are undergoing HF switching while module C maintains a constant switch configuration. Module B is not considered in the resonance path as it would behave in the same manner as module A for *1/3rd* of the 60-Hz line cycle. It is seen from Figures 21 (a) and 21 (b) that there exists two resonance paths for each switch position. The path in red corresponds to the highest resonance frequency while the path in blue corresponds to the lower resonance frequency and are a function of the duty-cycle as evident from Figure 21 (c). Due to the absence of damping in the ac-link path, these oscillations cannot be mitigated by the standard compensator alone and requires either insertion of a damping network also known as passive damping or need additional sensing states to control ac-link voltage across either C_1 or C_2 along with the control of the grid-current i_g .





(c)

Figure 21. Resonance path when switch S_{1a} (a) ON, (b) OFF. (c) Frequency response of G_{id} with variation in duty-cycle depicting duty-cycle dependent resonance frequency oscillations.

This method of compensation is known as active damping [60]-[64]. Other alternative approach is to employ notch filters that cancels the effect of poles and zeros at resonance frequencies and are usually cascaded with grid-current controller. However, this methodology would require multiple such resonant filters as a result of varying resonance frequency. Though, this methodology does not require any additional sensing elements, it increases the computational delay of the digital loop and makes the compensator tuning procedure strenuous [65][66] .

3.2.3 RC damping

The passive damping approach to mitigate the LC resonance frequency oscillations usually employs and RC network in parallel to the C_2 or C_1, as both of the ac-link capacitances participate

in the resonance path as shown in Figures 20 (a) and 20 (b) [67]. To analyze the effect of RC damping on the dynamics of the Ćuk converter, a small-signal model of the converter with RC damper in parallel to ac-link capacitance as shown in Figure 22 is constructed.

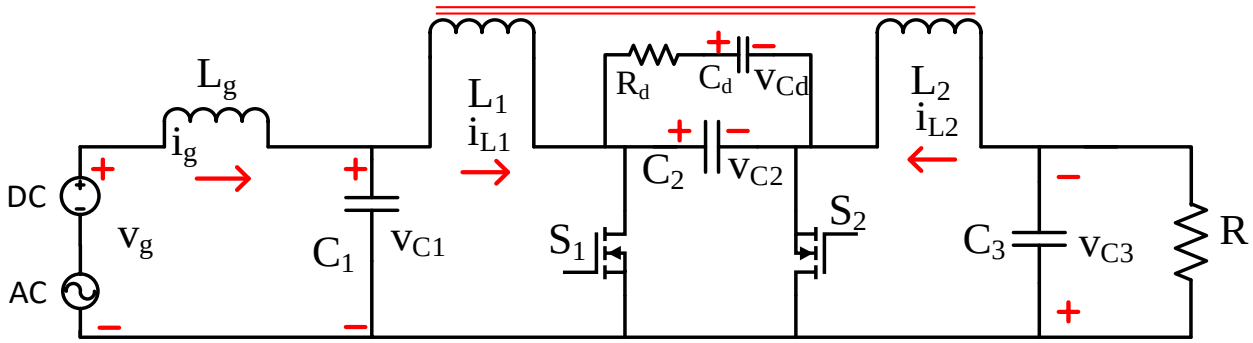


Figure 22. Circuit representation of the single module of IM based Ćuk converter with RC damper across the ac-link capacitance.

Using the state-space averaging technique, the input-current to duty cycle transfer function (G_{id-RC}) for the IM based DMCR can be expressed by following equation,

$$G_{id-RC} = \frac{P(s)}{Q(s)} = \frac{x_4 s^4 + x_3 s^3 + x_2 s^2 + x_1 s + x_0}{y_7 s^7 + y_6 s^6 + y_5 s^5 + y_4 s^4 + y_3 s^3 + y_2 s^2 + y_1 s + y_0} \quad (10)$$

Addition of RC damper in converter topology introduces one zero and one pole near the second peak of the G_{id} as shown in Figure 23. However, in contrast to the dc-dc operation, for inverter and rectifier applications, continuously varying operating conditions introduces duty-cycle dependent oscillations. In order to suppress these duty-cycle dependent oscillations, the value of R_d and C_d are so selected such that it provides low impedance path alternative to the ac-link capacitors up to the system maximum resonance frequency and also provides high impedance to the energy transfer at the switching frequency. Based on the chosen parameters and taking varying operating conditions into account, the maximum resonance frequency is calculated to be 15 kHz.

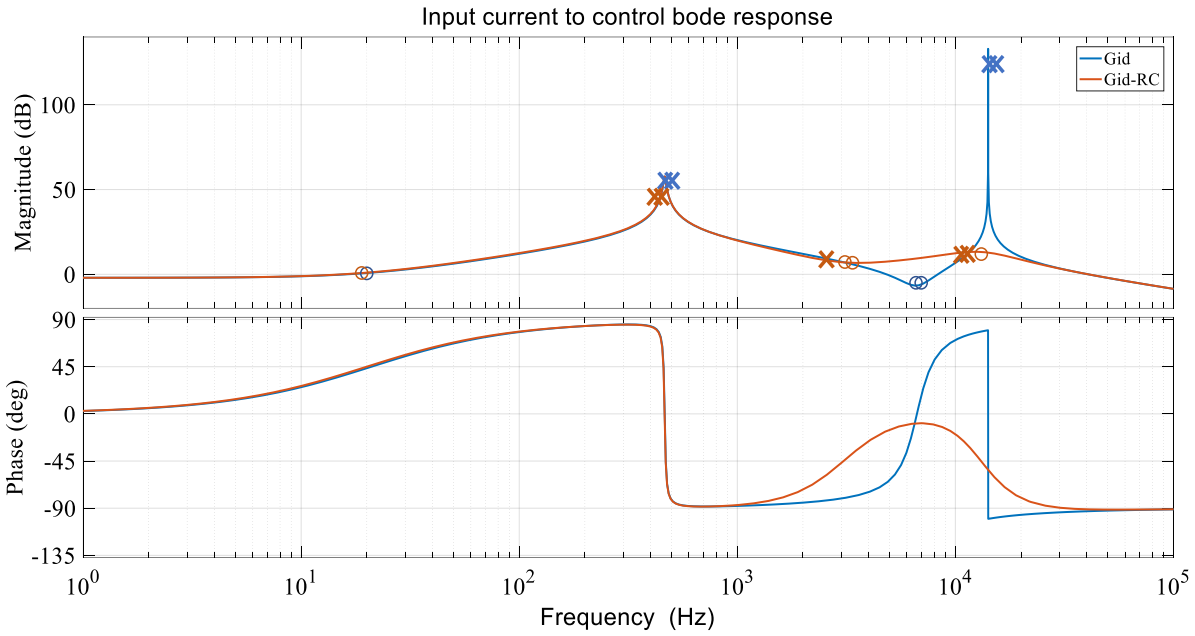


Figure 23. Input current to duty cycle bode response with/without RC in orange and blue respectively.

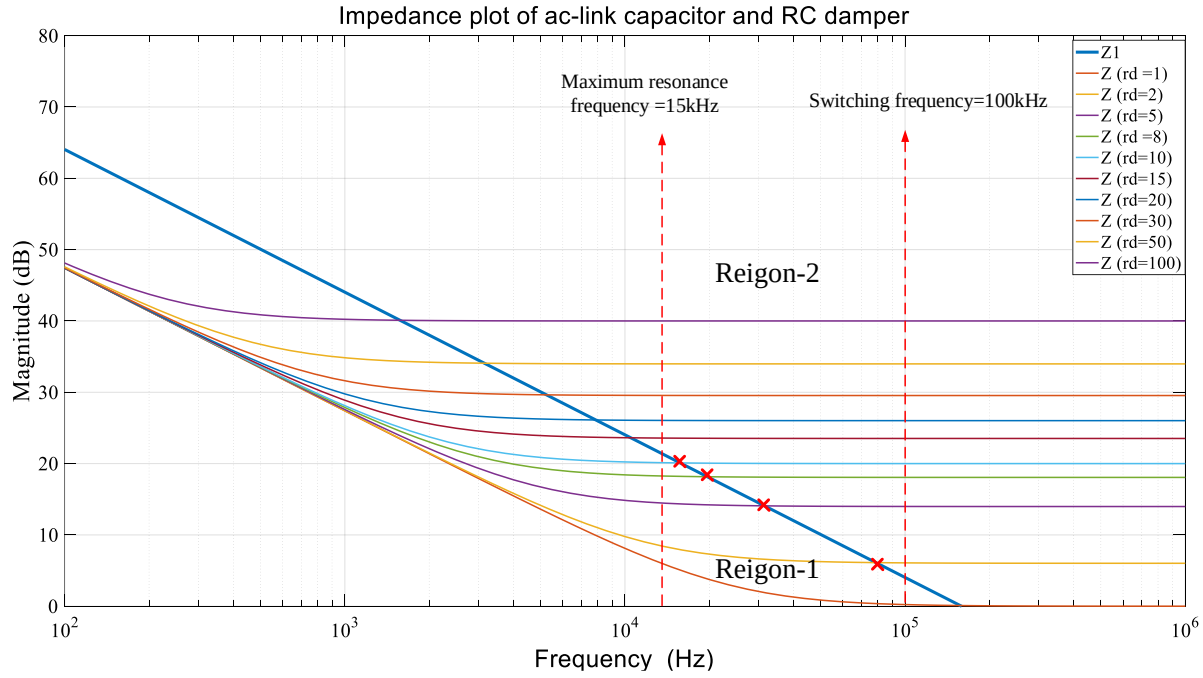


Figure 24. Impedance plot of ac-link capacitor and RC damper. The lower bound and upper bound on the value of R_d and C_d is found to be (10 Ω, 6.8 μF) and (2 Ω, 6.8 μF) respectively.

To determine the value of R_d and C_d that provides equal or lower impedance up to 15 kHz, a parametric plot of the impedance of the ac-link capacitor (Z_1) and RC damper at different values of R_d is shown in Figure 24. The intersection of impedance Z_1 in blue with two red dotted markers sets the upper and lower bound on the value of R_d for a given C_d . Using Figure 24, any value of $R_d \epsilon[1,10]$ Ω can be chosen to achieve damping of the resonance frequency oscillations. Further, it can be inferred from Figure 24, that the lowest R_d provides overall better damping from the control performance viewpoint but will also allow the energy transfer at switching frequency ergo bypassing the C_1.

B. Power loss in RC damper

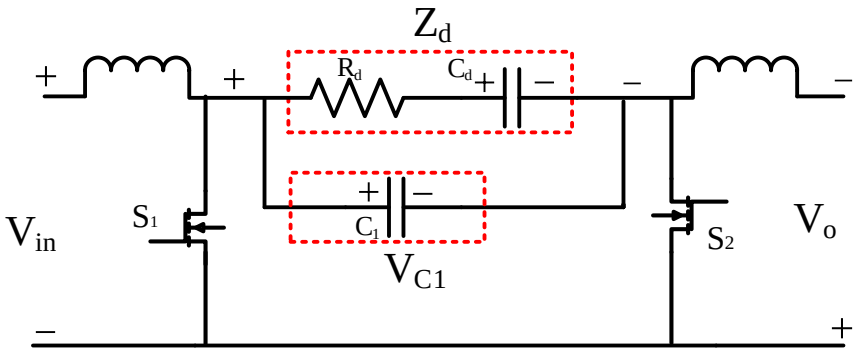
Though employing an RC damping scheme improves the converter frequency response by snubbing the intra-modular interactions, it incurs some power loss and lowers the efficiency. Figure 25 (a) displays the RC damping network across the ac-link capacitance. By using

$$i_{cd,rms}\big|_{60\ Hz} = \frac{V_{c1,rms}\big|_{60\ Hz}}{Z_d} = \frac{jV_{c1,rms}(\omega C_d)}{1+j\omega R_d C_d} \tag{11}$$

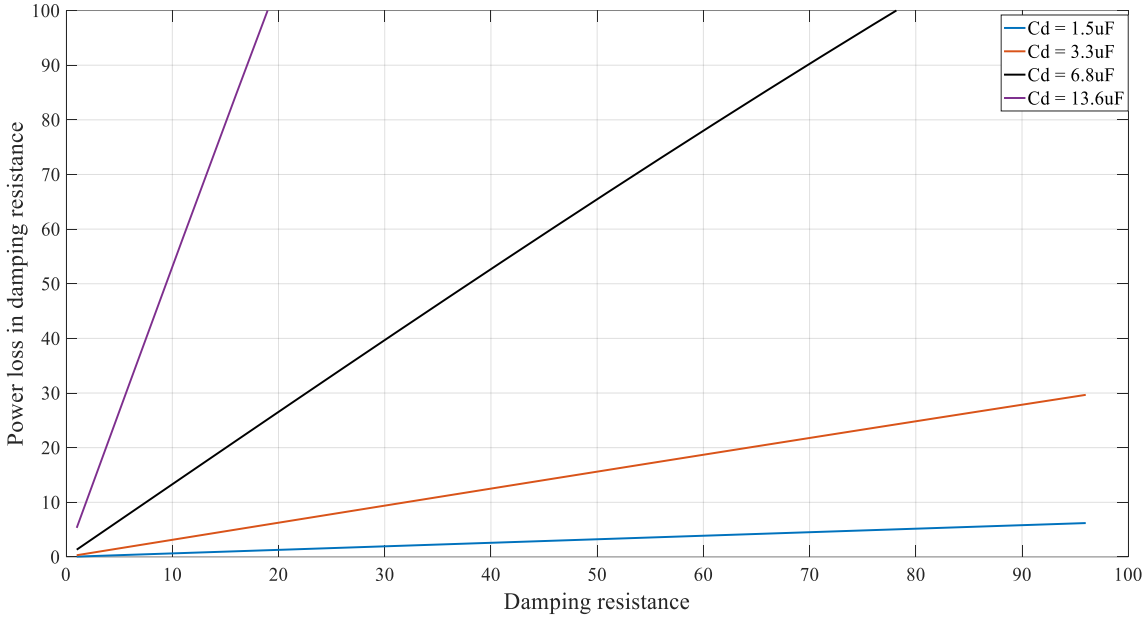
where $Z_d = \frac{{V_{c1,rms}}^2(\omega^2 {C_d}^2)R_d}{1+\omega^2 {R_d}^2 {C_d}^2}$, the total loss in R_d is found to be

$$P_{Rd} = Real(i_{cd,rms}^2) \tag{12}$$

Figure 25 (b) displays P_{Rd} with variation in R_d and C_d. It is noted that, P_{Rd} increases quadratically with higher C_d compared to R_d. Thus, from an efficiency standpoint, higher value of C_d should be avoided. This trade-off between the control performance and efficiency leads to the optimization of the R_d and C_d. To achieve satisfactory PFC operation with input current THD < 5 % a higher value of R_d is used.



(a)



(b)

Figure 25. (a) RC damper in parallel to the ac-link capacitor. (b) Parametric plot of power loss in damping resistor R_d with variation in damping capacitance C_d.

This trade-off between the control performance and efficiency leads to the optimization of the R_d and C_d. Next, using the RC network damping scheme to address the LC resonance, a standard control architecture is discussed in the next section.

3.3 Control architecture

The control architecture for the DMCR as shown in Figure 26 is comprised of two control loops. The outer DC loop consists of a constant voltage mode control followed by a constant current mode control for CC and CV mode of operation respectively. The PFC loop is a grid current mode control that tracks the current reference as generated by the DC loop and is responsible for ensuring the PFC operation and mitigation of low-order harmonics presented in the feedback currents i_a, i_b, and i_c .

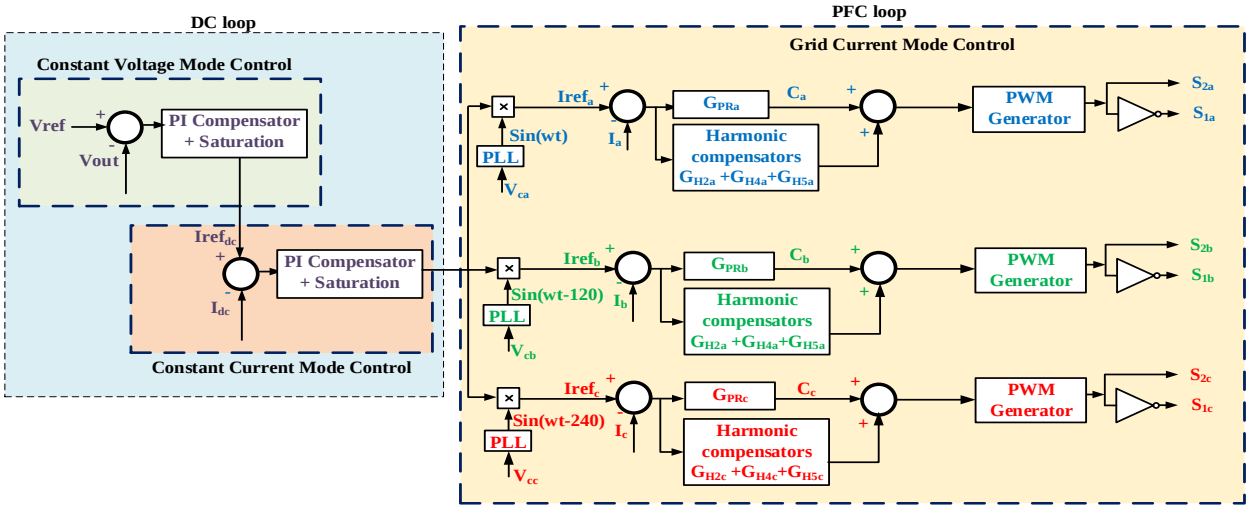


Figure 26. A standard dual-loop control architecture of the DMCR without inverse transformation.

3.3.1 DC loop

The CC and CV mode control is comprised of a proportional-integral (PI) compensator. The proportional (K_p) and integral (K_i) gains of the PI compensator are selected such that CC/CV mode of charging is achieved while achieving an optimum start-up performance. During the CC mode of operation, output of the constant voltage mode control is saturated and is clamped to the

maximum ampacity of the charger that acts as the charger current reference. As the battery voltage reaches close to the desired voltage set-point, output of the constant voltage mode control gradually reduces, thereby reducing the charger current reference and enabling the CV mode of operation as sown in Figure 27.

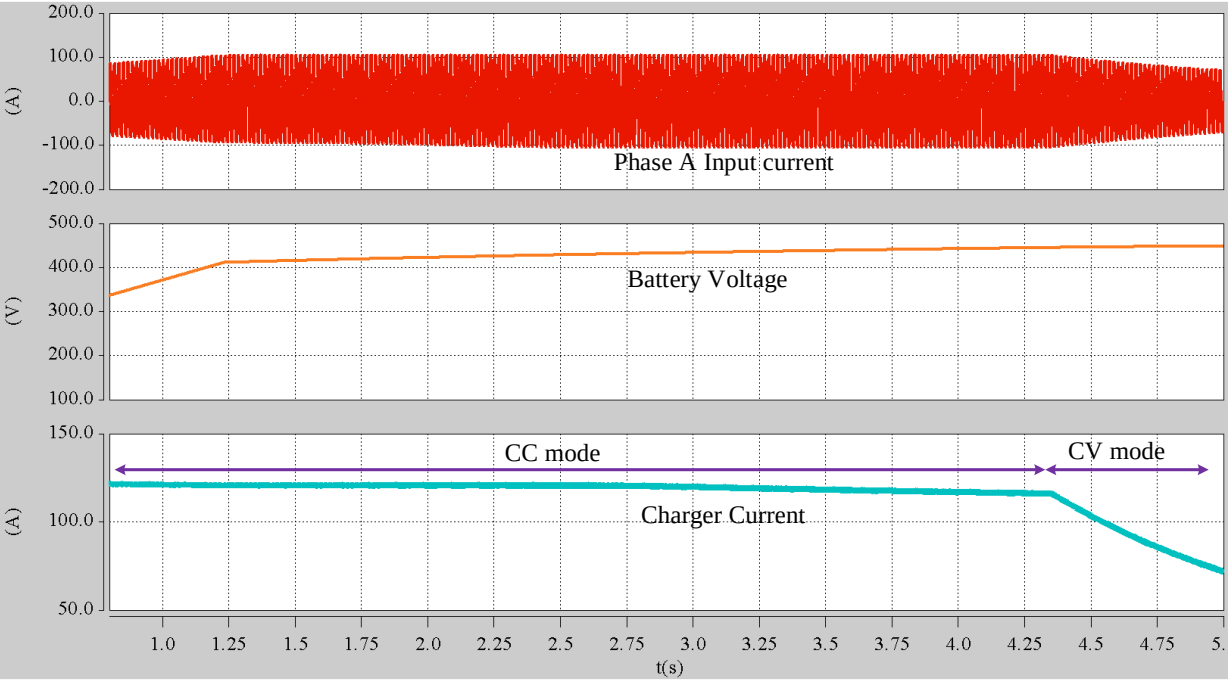


Figure 27. Simulation snippet of the CC/CV mode of charging with phase A input current (red), battery voltage (orange), and charger current (blue).

3.3.2 PFC loop

Next, the PFC loop as shown in Figure 28 is comprised of a proportional-resonant (PR) compensator and multiple harmonic compensators for grid current control.

A. Phase-locked loop (PLL)

The PLL is achieved by sensing the modular input capacitor voltages V_{ca}, V_{cb}, and V_{cc}. After sensing, these modular voltages are first converted from three-phase system (abc) to synchronous

rotating reference frame (dq) using Clarke and Park transformation and are expressed by (1) and (2) respectively;

$$\begin{bmatrix} \overrightarrow{V_\alpha} \\ \overrightarrow{V_\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} \overrightarrow{V_{ca}} \\ \overrightarrow{V_{cb}} \\ \overrightarrow{V_{cc}} \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} \overrightarrow{V_d} \\ \overrightarrow{V_q} \end{bmatrix} = \begin{bmatrix} \cos\theta_c & -\sin\theta_c \\ \sin\theta_c & \cos\theta_c \end{bmatrix}\begin{bmatrix} \overrightarrow{V_\alpha} \\ \overrightarrow{V_\beta} \end{bmatrix} \tag{14}$$

where $\begin{bmatrix} \overrightarrow{V_{ca}} \\ \overrightarrow{V_{cb}} \\ \overrightarrow{V_{cc}} \end{bmatrix} = \begin{bmatrix} V_m \sin\omega t \\ V_m \sin(\omega t - 120°) \\ V_m \sin(\omega t - 240°) \end{bmatrix}$ and θ_c is the PLL angle. On combining (1) and (2), $\overrightarrow{V_d}$ and $\overrightarrow{V_q}$ can be expressed as

$$\overrightarrow{V_d} = \sqrt{\frac{2}{3}}\cos(\omega t - \theta_c),\ \overrightarrow{V_q} = \sqrt{\frac{2}{3}}\sin(\omega t - \theta_c) \tag{15}$$

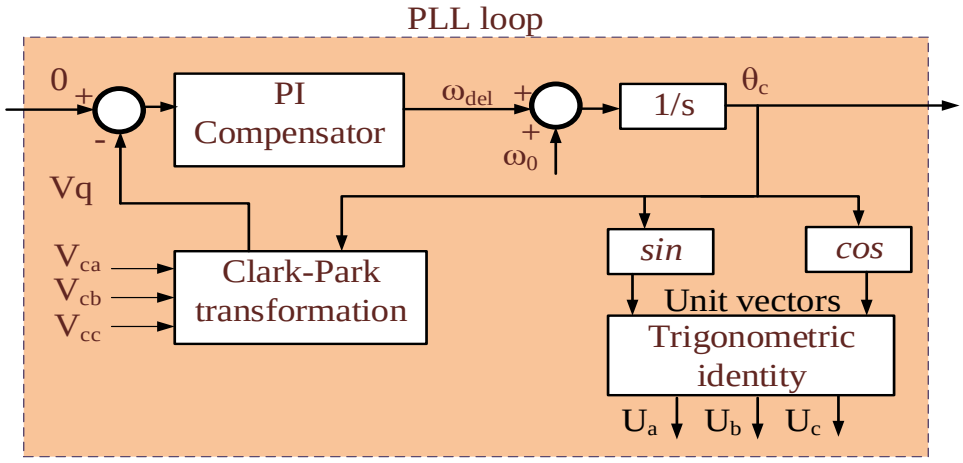


Figure 28. Phase-locked loop (PLL) structure.

To achieve phase locking, θ_c must be close to the instantaneous voltage phasor angle ωt. This

condition can only be satisfied by making $\overrightarrow{V_q} \cong 0$. A simplified structure of the PLL loop is shown in Figure 28 [68][69]. The obtained θ_c is then used to generate three sinusoidal unit vectors U_a, U_b, and U_c phase shifted by $120°$.

B. PR and harmonic compensator

Next, to track the sinusoidal current reference, a combination of PR compensator and harmonic compensators are used [70]-[72]. The PR compensator is tuned at the grid fundamental frequency of 60 Hz and is responsible for tracking the input current references $Iref_a$, $Iref_b$, and $Iref_c$ as generated by the phase-locked loop (PLL). The transfer function of an ideal PR compensator is given by,

$$G_{PR(ideal)}(s) = k_p + \frac{k_i s}{s^2 + {w_o}^2}$$

where k_p, k_i, and w_o represents proportional gain, integral gain, and resonant-frequency. However, the PR compensator provides infinite gain at the resonant-frequency which causes stability problems during its practical implementation. Therefore, a more non-ideal version of the PR compensator is expressed as,

$$G_{PR(non-ideal)}(s) = k_p + \frac{2k_i w_c s}{s^2 + 2w_c s + {w_o}^2}$$

where w_c is the cut–off (3dB) band of the compensator. Though, PR compensator might be able to track the fundamental frequency component, however, due to the non-linearity of the converter, low-order dominant harmonics such as 2^{nd}, 4^{th}, and 5^{th} are drawn from the utility grid that are required to reduce the total harmonic distortion (THD) and to comply with the limits on drawable harmonic current specified by the IEEE Std.519-2014. To suppress these harmonics, multiple

harmonic compensators are used that provides finite gain at the harmonic frequency. The transfer function of a harmonic compensator (G_{HC}) is given by,

$$G_{HC(non-ideal)}(s) = \frac{2k_i w_c s}{s^2+2w_c s+(nw_o)^2}$$

where *n* represents the n^{th} harmonic. The number of harmonic compensators that are added in parallel to the PR compensator is determined by the number of low-order harmonics presented in the three-phase input currents i_a, i_b, and i_c. The tuning of the PR compensator and the harmonic compensators are so done such that optimum trade-off between the phase-margin and bandwidth is achieved. Although harmonic compensators suppress baseband harmonics, the tuning of these harmonic compensators is a non-trivial task. Further, once the harmonic compensator parameters are tuned, same values may or may not be applicable for the hardware prototype. Therefore, it is beneficial to use an approach that reduces the number of harmonic compensators.

C. Static inverse transformation:

Two key control challenges for the grid current control are to ensure unity-power-factor (UPF) operation and to ensure low THD for the current drawn from the utility grid. Harmonics in the DMCR arises due to inherent nonlinearity of the converter. Consequently, the voltage at the point of common coupling is rarely sinusoidal and harmonic currents propagate through the power system and cause harmonic pollution that need to be mitigated to comply with standard IEEE 519-2014. To address this issue, a nonlinear inverse transformation is added in the original control scheme shown in Figure 28 that yields a linear relationship between the transformed duty ratio and the output voltage under steady state, thereby mitigating harmonics. The modified part of the control architecture is shown by red envelope in Figure 29. Further, the transformation also

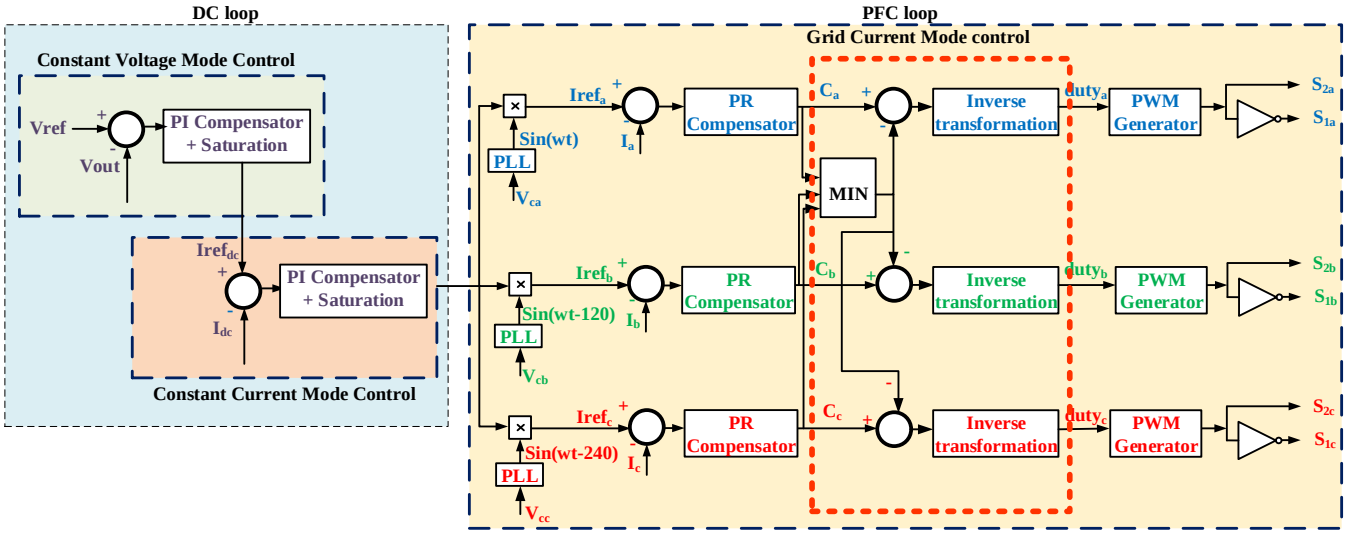


Figure 29. A standard dual-loop control architecture of the DMCR with feedforward and inverse transformation.

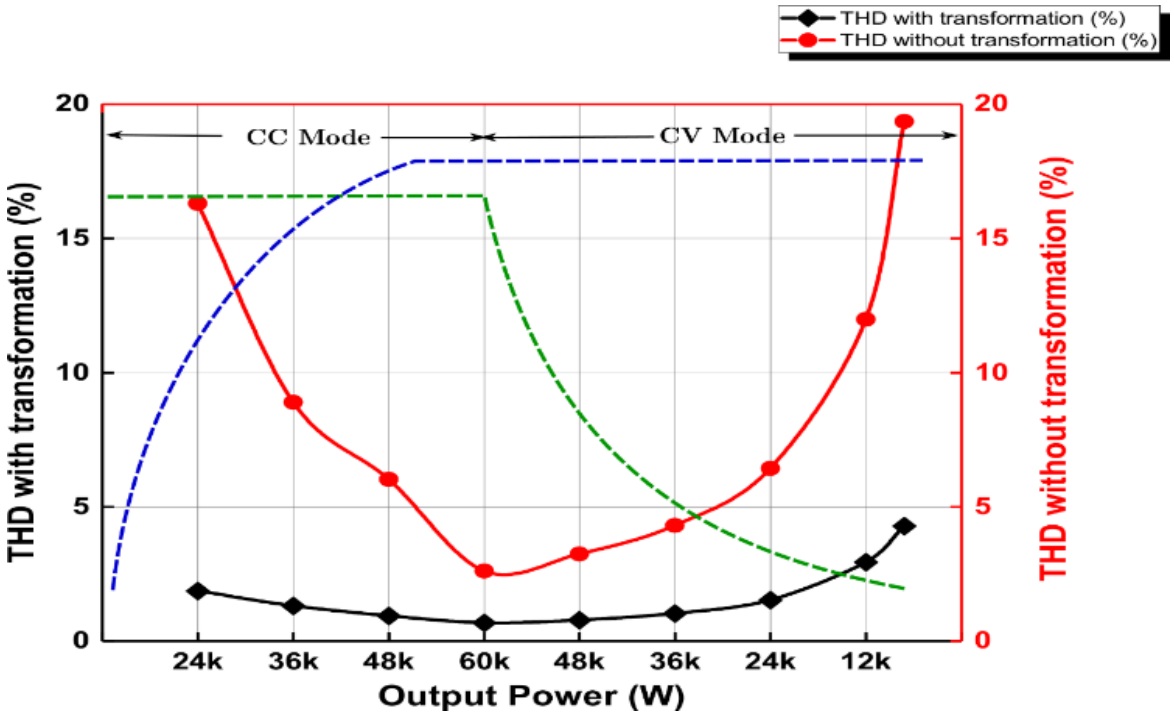


Figure 30. Total Harmonic Distortion (THD) vs output power with (blue) and without (orange) using feedforward and inverse transformation.

mitigates the necessity for using multiple harmonic compensators. Additionally, a feedforward term is added to improve the steady-state tracking performance and to minimize the control effort in the event of a disturbance. A comparison of THD with and without using the inverse transformation is displayed in Figure 30.

3.3.3 Closed –loop control Bode plot

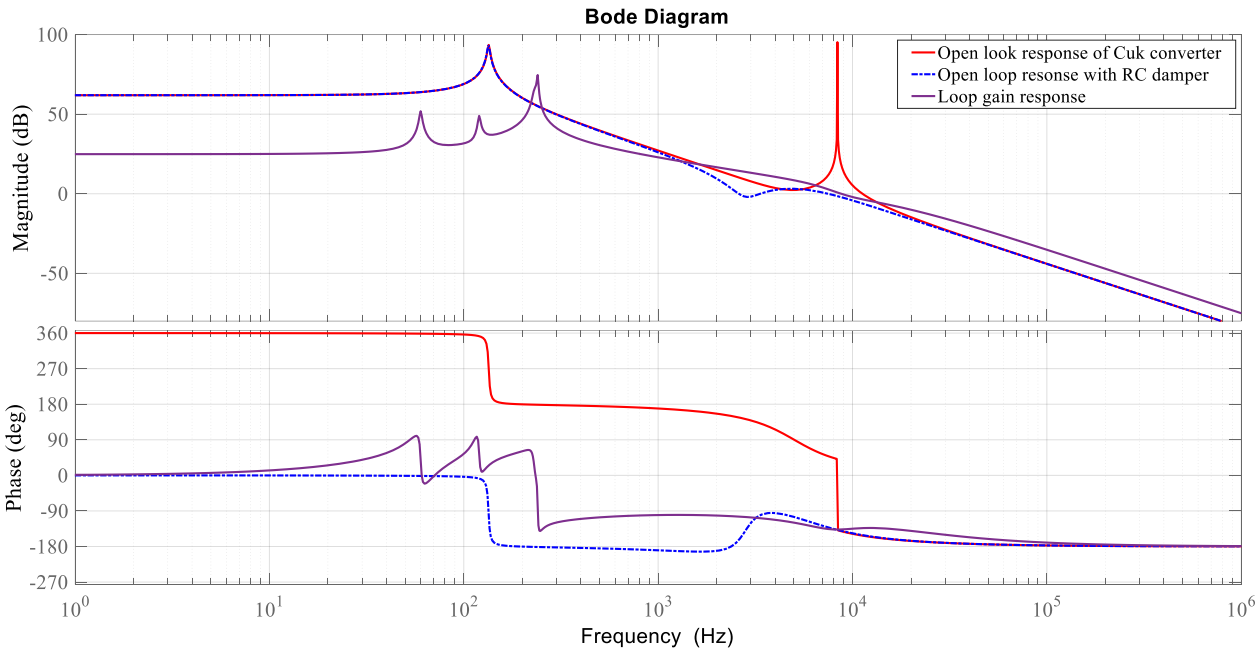


Figure 31. Bode diagram of the duty-to-output transfer function of the Ćuk converter. Blue and red curve represents open loop response with/without RC damper. Purple curve represents the bode response of the loop gain.

Figure 31 in orange displays the response of the grid-current feedback loop with multiple resonant controller. The resonant controller provides high gain at the frequency of interest and

does not alter the phase response of the overall system.

3.3.4 Active damping

Figure 32 displays the closed-loop control architecture for grid-current tracking. The feedback loop uses a standard PR and high-order harmonic compensator for grid-current tracking and to comply with harmonic limits of IEEE-519 Std, while the feedforward term that employs a lead-lag compensator is added to the generated duty-ratio command for damping the resonance frequency oscillations. The transfer functions G_{PR}, $G_{lead-lag}$ are represented as,

$$G_{PR} = \frac{K_p s^2 + w_c(K_p + K_r)s + K_p w_0^2}{s^2 + w_c s + w_0^2}$$

$$G_{lead-lag} = K_d \frac{1 + {}^{s}/_{w_z}}{1 + {}^{s}/_{w_p}}$$

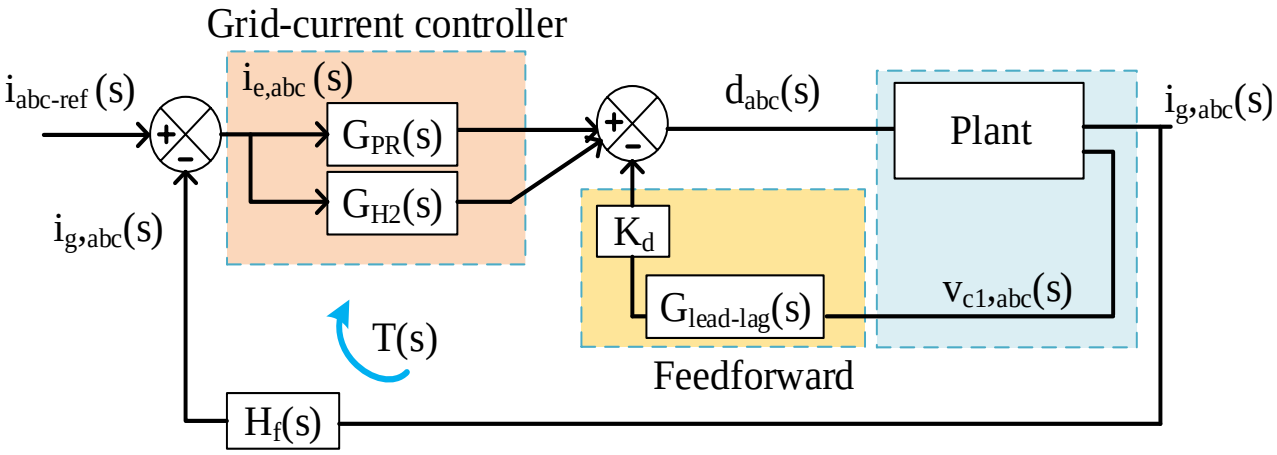


Figure 32. Representation of control architecture of the DMCR employing PRC and high-order harmonic compensator for grid-current tracking and feedforward compensation using V_(c-abc).

Figure 33 displays a comparison of frequency response of the grid current to duty ratio (G_{ig-d}) without damping, with RC damping, and feedforward for a given operating conditions and PR

compensator parameters. It is seen from the curve in green that the feedback loop $T_{vc}(s)$ smoothens the phase drop at resonance frequency and provides a finite phase margin at the crossover frequency. Further, it is noted that mitigation of the resonance peaks provides room for achieving higher bandwidth without incurring oscillations.

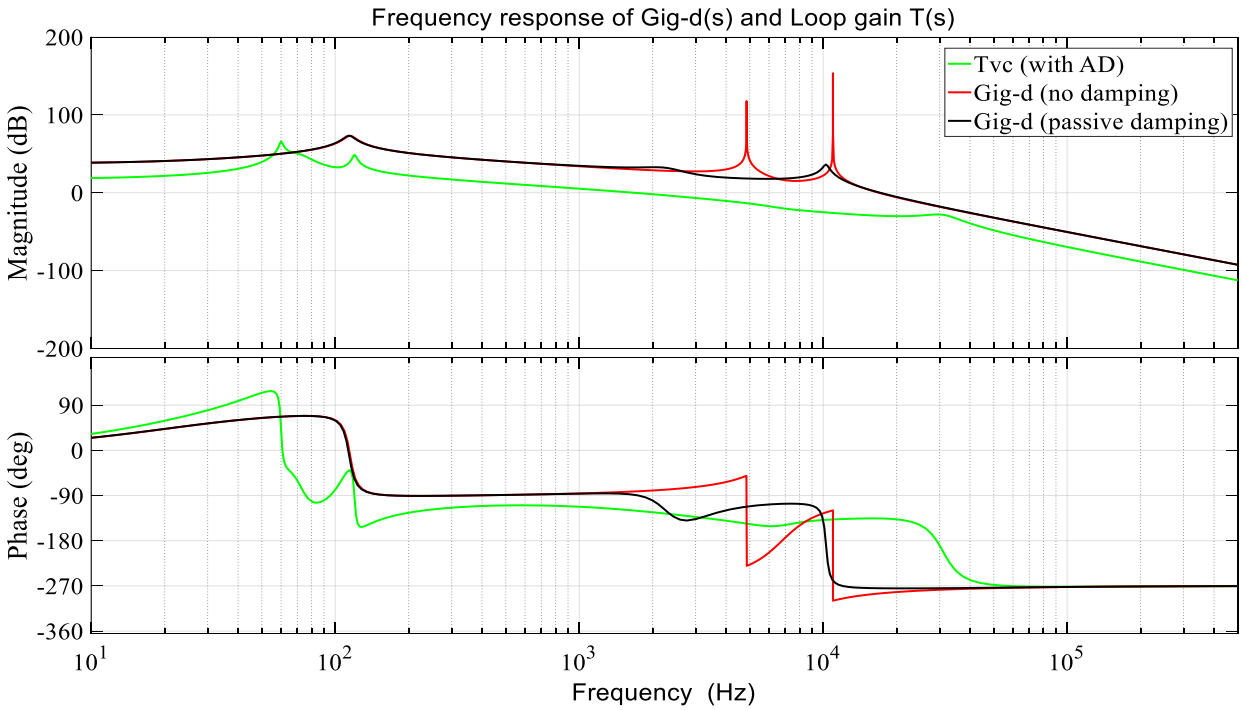


Figure 33. A comparison of frequency response of grid current to duty-ratio without damping, with passive damping, and active damping in red, black, and green respectively.

However, digital implementation of the control architecture as shown in Figure 32 gives rise to computational delay and affects the system pole-zero locations. To study the effect of the inner loop, zero-order hold discretization method was used to transform from s- to z-domain with sampling time period of 20μs. Following the control architecture as shown in Fig. 4, the transfer function of the loop gain (L_p) in z- domain is represented by (1),

$$L_p = (G_{PR} + G_{H2})(z)\frac{G_{ig-d}(z)H}{(1-G_{vc-d}(z)G_{lead-lag}(z)K_d)} \quad (1)$$

Using (1), a parametric pole-zero map of the L_p with variation in gain K_d is plotted as shown in Figure 34 for a given duty-ratio and fixed K_p.

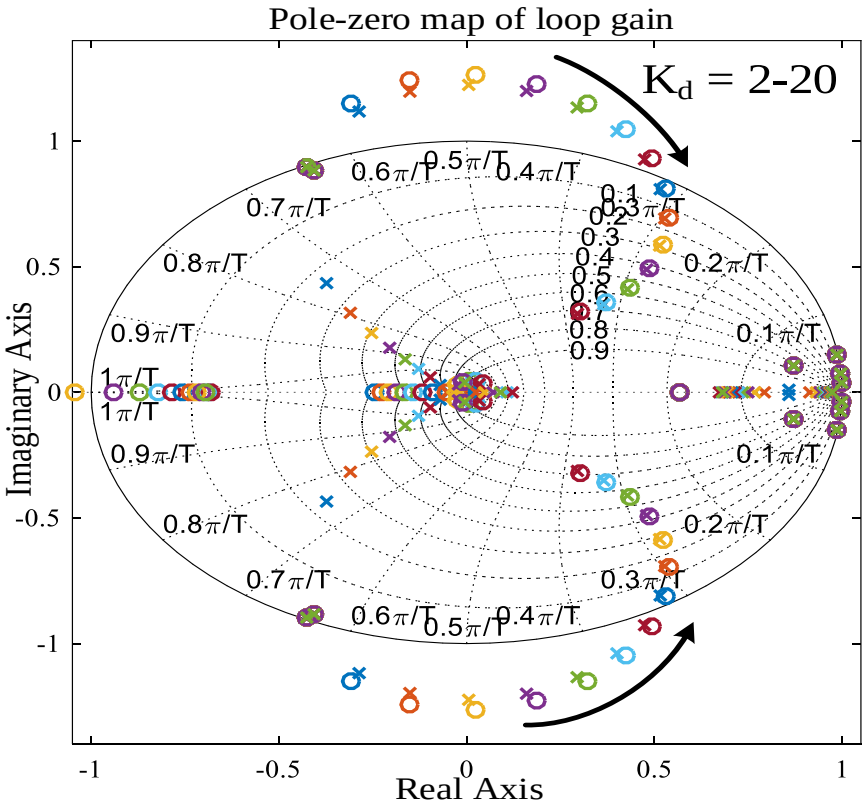


Figure 34. Pole-zero map of loop gain employing PR compensator and lead-lag compensation loop. Gain K_d is varied from 2-20 keeping the duty-ratio and K_p fixed at 0.35 and 10 respectively.

However, it is imperative to access the stability of the entire system for different duty-ratios to mitigate the duty-ratio dependent oscillations. In boost-derived converter, usually the worst-case conditions occurs at the highest-duty ratios, i.e. when boosting a low-input voltage to a high-output voltage. Figure 35 displays a PZ map of the L_p for a duty-ratio variation ranging from 0.99-0.7 at

two sets of gain $K_d = \{10, 12\}$. It is seen that, higher K_d is much effective in bringing back the unstable poles back into the unit-circle at high duty-ratios.

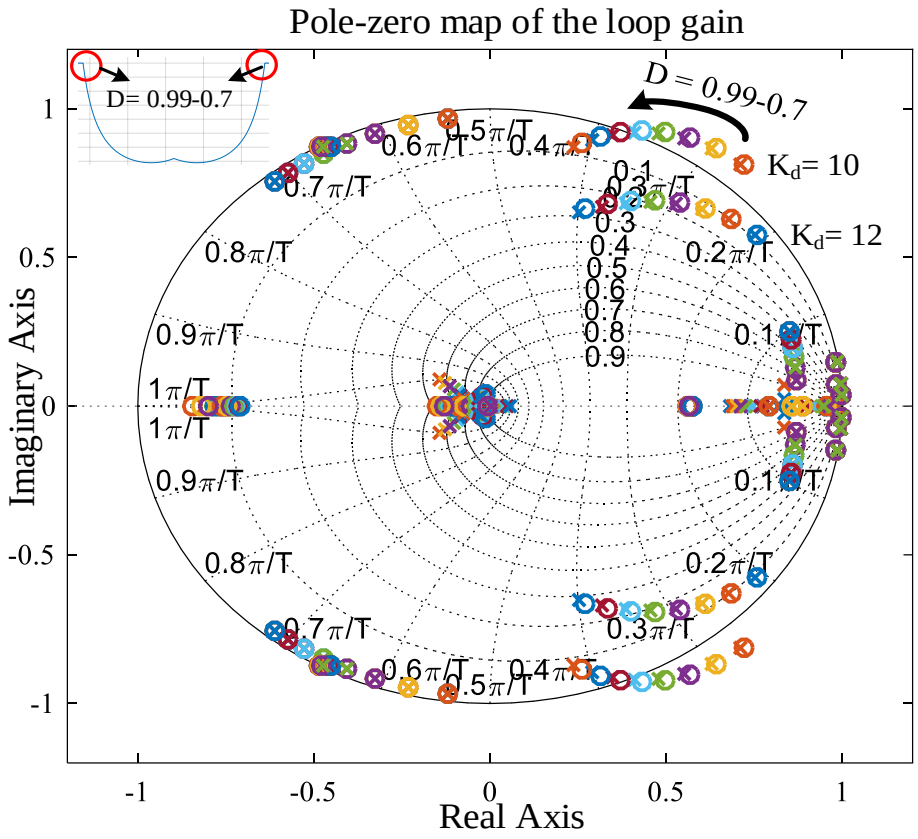


Figure 35. Pole-zero map of loop gain employing PR compensator and lead-lag compensation loop. Duty-ratio is varied from 0.99-0.7 for two sets of gain K_d= 10 and 12 keeping the K_p fixed at 10 respectively.

Further, it is inferred from Figures 34 and 35 that, higher K_d also limits the performance of the loop gain by limiting the closed-loop bandwidth owing to the fact that pole-zero frequencies in s-domain manifests itself in form of distance of the respective pole-zero from the origin of the unit-circle in z-domain. However, this limitation can be compensated by increasing the parameter K_p of the PRC which would not have been possible without damping.

Chapter 4

4. HARDWARE IMPLEMENTATION

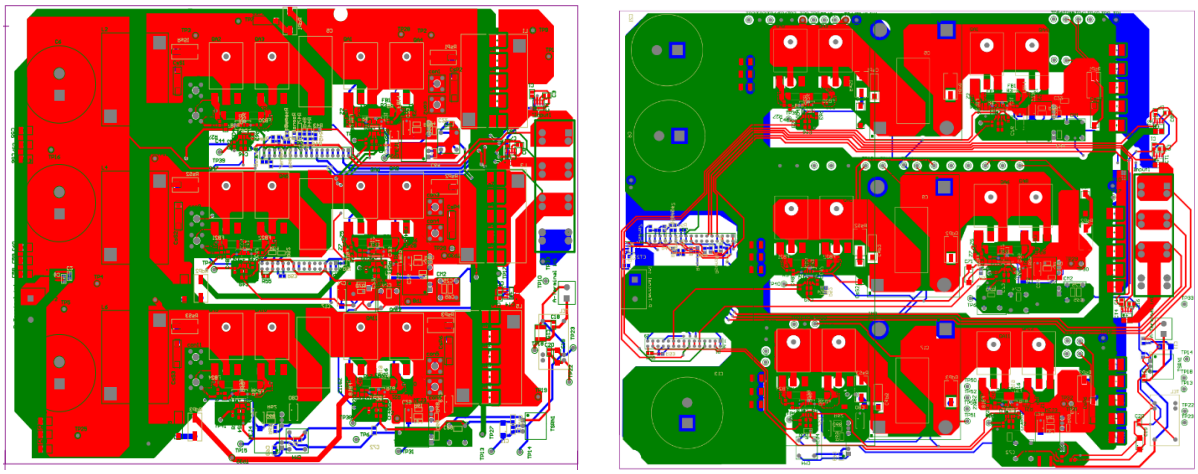
Parts of this chapter, including figures and text, are based on my following papers:

- N. Kumar, M. Mohamadi and S. Mazumder, "Experimental Validation of Single-Stage Three-Phase Non-Isolated Cuk Rectifier," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 2744-2751, doi: 10.1109/ECCE.2019.8912485.
- N. Kumar, M. Mohamadi and S. K. Mazumder, "Passive Damping Optimization of the Integrated-Magnetics-Based Differential-Mode Ćuk Rectifier," in *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10008-10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.
- S.K. Mazumder, N. Kumar, M. Mohamadi, “Transformer-less, single-stage power module for off-board EV charging,” Patent Application# PCT/US2020/057743, 2020.
- M. Mohamadi, S.K Mazumder, and N.Kumar, “Integrated Magnetics Design for a Three-Phase Differential-Mode Rectifier”, accepted in IEEE Transactions on Power Electronics.
- N. Kumar, M. Mohamadi, and S. K. Mazumder, "High Performance Off-Board DC Fast Charger” accepted in *IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG).*

This chapter outlines the design and development of the scaled-power UBS (sp-UBS) and high-power UBS experimental prototype to validate the operational feasibility of the DMCR and its proposed control architecture. To test and evaluate the developed active damping algorithm against no damping/RC damping for loss mitigation and performance improvement, efficiency and THD parametric plots are provided. Further, evaluation of integrated magnetics (IM) against discrete magnetics (DM) is performed by developing two prototypes of sp-UBS. To scale the power from sp- to high-power UBS, a pathway is provided, and a detailed design procedure is delineated. Component selection for the UBS is done based on extensive simulations for the worst-case scenario and following the design of sp-UBS. Finally, experimental results displaying charging curves and performance parametric plots are provided at rated power.

4.1 Sp-UBS Power board

Two different power boards were made for performance evaluation between IM and DM in the sp-UBS context. The PCB layout for these two boards are shown in Figures 36 (a) and (b).



(a) **(b)**

Figure 36. (a) PCB layout of the DM based sp-UBS (b) PCB layout of the IM based sp-UBS.

The PCBs for both the boards are based on the four-layer design to have the freedom of implementing different planes and to minimize the interference among low power signals, high power signals, digital ground plane, and power ground plane. Designing power board PCB comes with many challenges, mainly the HF current planes which need to be placed on the board optimally to avoid overlapping of different signals, induction of noise signals on one another, and minimizing the parasitic components in the process.

The sp-UBS power board comprises of:

(i) Magnetic components

(ii) Capacitive components

(iii) Devices, gate drives, and power supplies

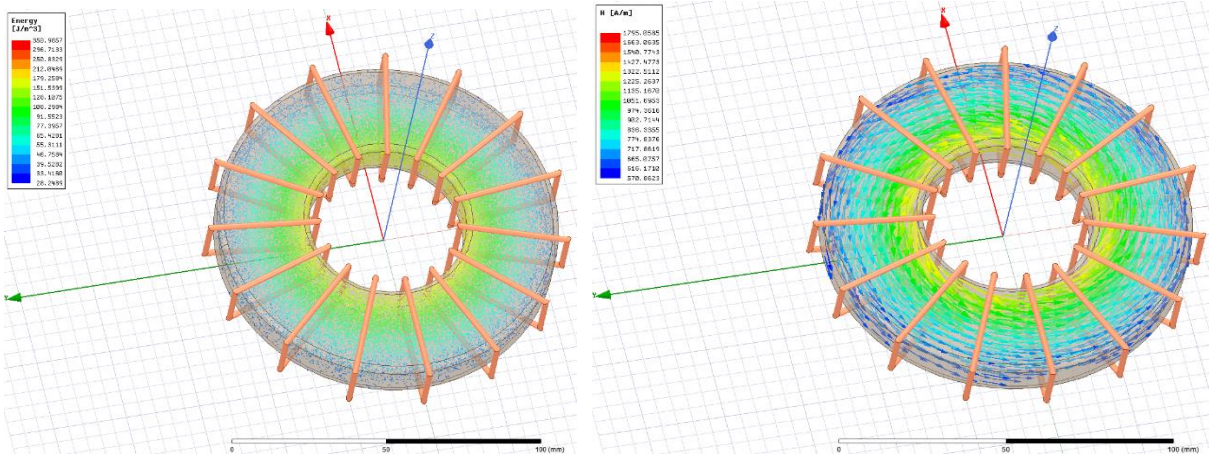
(iv) Sensor board

(v) Digital signal processor (DSP)

A. Magnetics

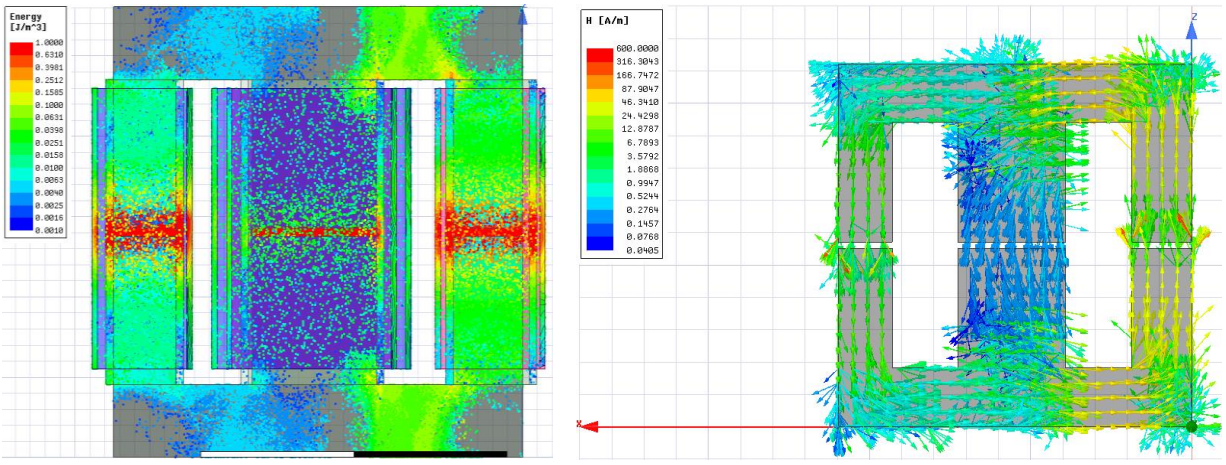
In this section, a brief comparison of the DM and IM is provided. The core that is selected for DM based sp-UBS is based on High-Flux toroidal geometry while for IM based sp-UBS Kool-Mu E-E core is used. Figure 37 (a) and 37 (b) displays the energy distribution and magnetizing force (H) for the chosen toroidal core. It is seen that the magnetization energy and magnetizing force are concentrated more towards the center of the toroidal core. Due to the limited energy density of toroidal cores, they have tendency to saturate early. However, in contrast to the toroidal core, for a given stored energy, E-E/E-I core provide advantage in terms of higher

energy density that results in the reduction of its overall effective volume. This boosts up the power density of the converter significantly.



(a) **(b)**

Figure 37. (a) Inductive energy distribution in the toroidal core, (b) Distribution of magnetizing force in the toroidal core.



(a) **(b)**

Figure 38. Inductive energy distribution in the EE-core and air-gap, (b) Distribution of magnetizing force in the EE-core.

The E-E core configuration. provides the provision for including air-gap to increase the stored energy. Figures 38 (a) and 38 (b) displays the energy distribution and magnetizing force (H) for the chosen E-E core, respectively. With reference to Figures 38 (a) and 38 (b), to achieve HF ripple mitigation, the ac-side inductor winding is distributed between the leftmost and middle limb while dc-side inductor winding is placed on the middle and rightmost limb of the EE-core. Further, an air-gap of 0.762 mm was added in the path length of the E-E core to achieve desired inductance and coupling factor of 0.5. It is seen from Figure 38 (a), that the inductive energy is concentrated more in the leftmost and rightmost limb compared to the middle limb of the E-core. This is due to the cancellation of resulting magnetizing force in the middle limb of the E-E core as generated by ac-and dc-side inductors and is shown in Figure 38 (b).

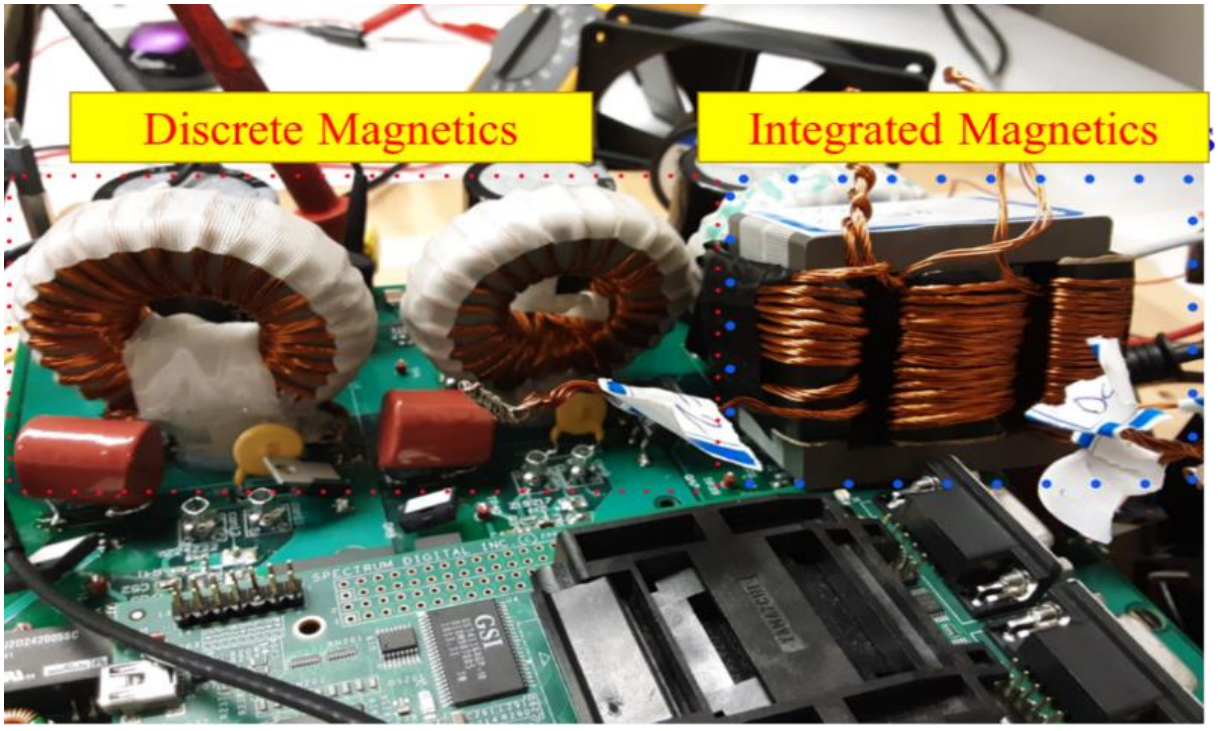


Figure 39. Comparison of discrete and integrated magnetic for 2-kW experimental prototype of three-phase Ćuk rectifier.

Such winding arrangement ensures that only a part of the magnetic flux is linked between the ac- and dc-side inductor. The red shaded region in the rightmost and leftmost limb of the EE-core represents energy stored in the air-gap which is much higher than the core. Including the air-gap reduces the effective inductance and requires more turns to compensate. This compensation increases the conduction losses. Thus, a trade-off is required between enhanced power density and higher efficiency. Figure 39 displays the size comparison between the toroidal core and the E-E core.

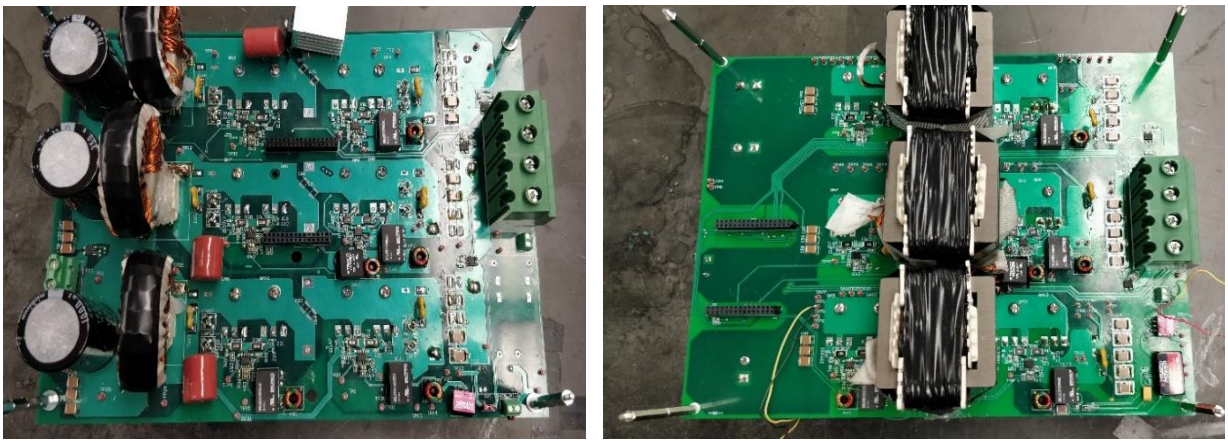
B. Capacitors

Apart from magnetics, DM and IM based sp-UBS module comprises of many capacitor elements: namely the main ones are stipulated in Table IV. In this table different design aspects of the capacitors are shown. The specifications for each capacitive element comes from the purpose that they serve in the power circuit and the performance that they need to project in the circuit.

Table IV. List of capacitors used in the scaled power prototype of the sp-UBS.

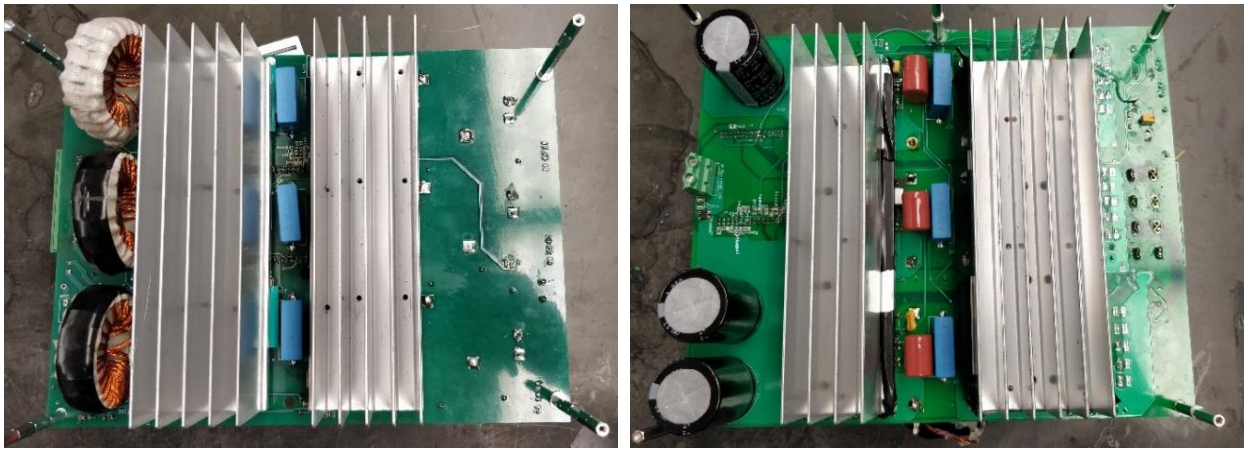
Purpose	Type	Capacitance	Voltage
Blocking	Film	1.5 μF	450 V
Damping	Film	6.8 μF	450 V
Snubber	Ceramic	330 pF	1 kV
Output	Electrolytic	1000 μF	450 V
Input	Ceramic-SMD	10 μF	250 V
HF output	Ceramic-SMD	10 μF	450 V

C. Switching device, gate driver and power-stage



(a) **(b)**

Figure 40. Top view of the populated (a) discrete, and (b) integrated magnetics based sp-UBS



(a) **(b)**

Figure 41. Bottom view of the populated (a) discrete and (b) integrated magnetics based sp-UBS.

C2M0080120D 1200 V, 36 A SiC MOSFETs are used as switching components in the sp-UBS. The ac-side and dc-side devices each are put in parallel to achieve higher currerent rating and lower conduction loss during the ON state. A capitative-isolation based gate driver circuit is used to drive each MOSFET pair in the circuit. The part number of the gate drives is Si8271GB-IS. Voltage-divider circuits are used to sense input voltage and output voltage of each module. ACS712-30

hall-effect current sensors are used to sense input ac current and output dc current. Dc-dc power bricks were used to supply dc-bias to the gate driver ICs. The digital PWM signals are obtained from the sensor board (which will be discussed subsequently) and the sensed voltages and currents are sent to the sensor board. The gate circuit design, along with the layout, was given careful consideration to reduce the impact of the HF oscillations on the gate signals due to gate loop parasitic inductances. The incorporation of isolated gate drivers helped the cause by separating the gate and power loop currents so that they do not interact with one another and mitigate the faulty-turn-on of the MOSFETs. Figures 40 and 41 displays the top and bottom view of the populated DM and IM based sp-UBS. Table V displays the power-stage parameters of the DM and IM based sp-UBS shown in Figures 40 and 41.

Table V. The power-stage-parameters for the sp-UBS.

Input voltage (line to line) ($V_a = V_b = V_c$)	208 V RMS
Output voltage (V_{out})	Up to 200 V dc
Output power	3 kW (1 kW per module)
Input inductance ($L_{1a} = L_{1b} = L_{1c}$)	100 μH
Output inductance ($L_{2a} = L_{2b} = L_{2c}$)	100 μH
Input capacitance ($C_a = C_b = C_c$)	6.6 μF
Output capacitance ($C_{2a} = C_{2b} = C_{2c}$)	3 mF
Blocking capacitance ($C_{1a} = C_{1b} = C_{1c}$)	1.5 μF
Switching frequency (f_s)	100 kHz

D. Sensor board and DSK card

The interface board acts as an interface between the digital controller and the power board as shown in Figure 42. It houses the sensing circuit for input modular voltages, input current, output current, and output voltage. The input current of the sp-UBS is sensed using Hall-effect current sensor. The bandwidth of these current sensors are 80 kHz. The input modular voltage and output voltage are sensed for generating three 120°phase shifted unit vectors for PFC operation using PLL. The voltage sensing is done based on the resistive divider network which is low-pass filtered using op-amps to remove unwanted HF noise. The corner frequency of the low-pass filter is set at 10-kHz. These sensed signals are analog in nature and are converted to digital by a 12-bit analog to digital converter (ADC). The sensor board also outputs the PWM signals generated by the digital controller which is converted to a nominal voltage to be used by the gate drivers using digital isolators. The sensor board also has a digital to analog converter (DAC) for measuring the duty cycle waveform, voltage and current feedback signals. The control algorithm for the three-phase sp-UBS is implemented on an eZdsp EVM board from spectrum digital consisting of TMS320F28335 digital signal processor (DSP) as shown in Figure 42 (b). The EVM board communicates with the PC using code composer studio version 3.3, and a J-TAG cable. The duty cycles generated by the processor is used to drive the SiC-based sp-UBS operating at switching frequency ($f_s = 1/T_s$) of 100 kHz

(a) **(b)**

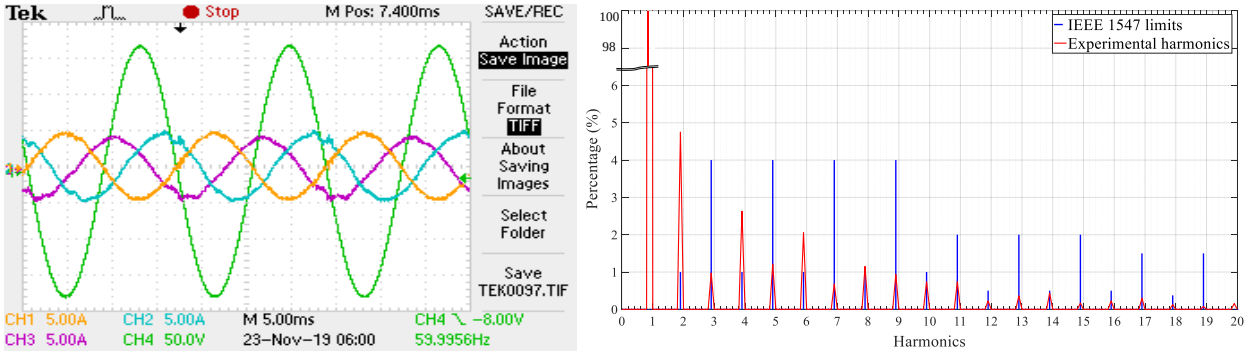
Figure 42. (a) Populated sensor board PCB that interfaces to the sp-UBS power and DSP control boards (b) TMS320F28335 off-the-shelf DSP control board for implementing the sp-UBS control algorithm.

4.2 Experimental results

A. Without RC damping

Figure 43 (a) displays the steady-state waveform of the three-phase input currents and phase A input voltage. The hardware prototype was first operated in current control mode. In this test, the rectifier was operated at input rated voltage of 208 V (RMS) line-to-line and the current reference was set at 4 A-peak. The proposed control architecture was able to track the current reference in phase with the input voltage. The total harmonic distortion (THD) and power factor at power level of 1-kW was found to be 6.68 % and 0.998 respectively. Further the efficiency of the rectifier at power level of 1-kW was found to be 92.2%. These measurements were taken using the power analyzer.

Figure 43 (b) displays a comparison of the harmonic spectrum of phase-A current and limits on the allowable harmonics in ac-grid [73] in red and blue respectively. It is seen, the odd harmonics that arise due to the inter-modular interaction among the rectifier modules are below the specified limits. However, the even harmonics that arise due to the non-linearity of the converter topology



(a) (b)

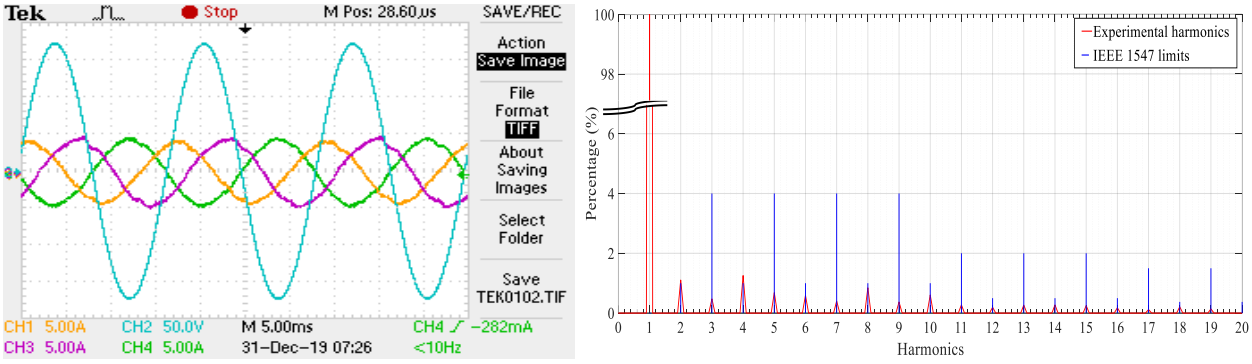
Figure 43. (a) three-phase input current waveforms without RC. Signals in orange, blue, and purple are phase A, B, and C input currents (5A/div) respectively. Signal in green is phase A line-to-neutral voltage (50V/div). (b) Comparison of the phase A input current harmonic spectrum with the IEEE 1547-2003 standard. The experimental result is without using RC damper in the ac switching link.

are higher than the set standard. As evident from Figure 43 (a), the THD of the input current waveform at rated voltage is observed to be 6.68 % which is higher than the set value of 5 % based on IEEE 519-2014 standard. Moreover, it is noted that the operational feasibility of the converter gets compromised at higher power without RC damping.

B. With RC damping

As discussed in Section II, introducing a RC damper in parallel to the ac-link capacitor, snubs the intra-modular interactions and improves the power quality of the signal, however, at the expense of slight reduction in efficiency. The DMCR is operated at an input rated voltage of 208 V line-to-line RMS and the current reference is set at 4-A peak. Figure 44 (a) displays the steady-state input current waveforms at a power level of 1-kW. The THD and PF is observed to be 3% and 0.997, respectively.

Figure 44 (b) displays the amplitude of the harmonic components present in the input current of phase A. It is seen that the amplitude of each harmonic component complies with the maximum



(a) (b)

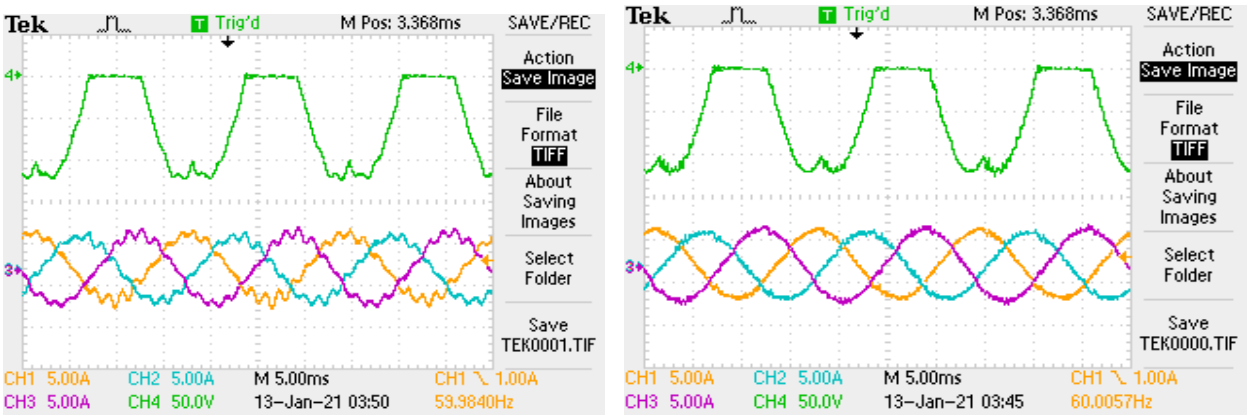
Figure 44. (a) three-phase input current waveforms with RC. Signals in yellow, blue, and purple are phase A, B, and C input currents (10A/div) respectively. Signal in green is phase A line-to-neutral voltage (100V/div). (b) Comparison of the phase A input current harmonic spectrum with the IEEE 1547-2003 standard. The experimental result is with using RC damper in the ac switching link.

allowable limits on drawable harmonic current as specified by the IEEE 1547-2003 standard. A modest reduction in efficiency is observed at a power level of 1-kW in comparison to without RC-damper scenario. Based on the measurements, the RC damper incurs approximately 15 W of losses.

4.2.1 Performance comparison of active damping with RC and no damping

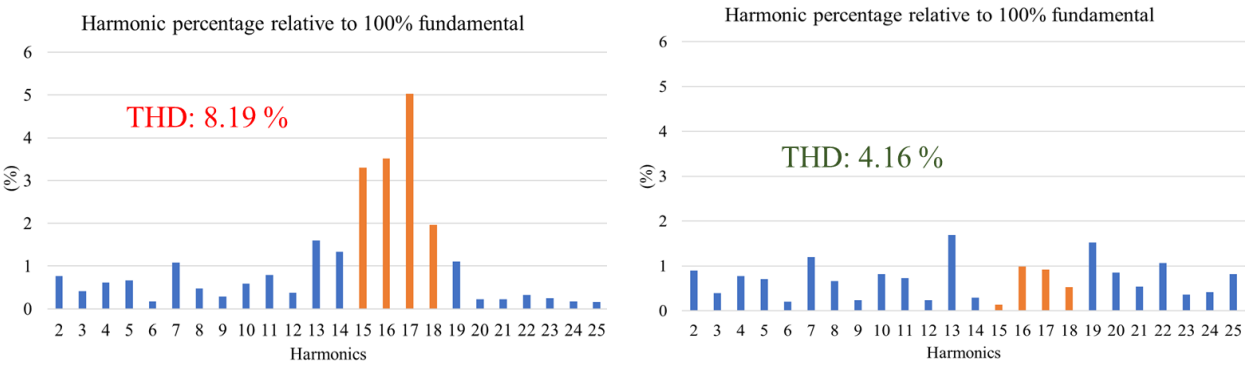
Figures 45 (a) and 45 (b) displays the experimental three-phase time-domain line-current waveforms with input current control and feedforward compensation respectively while Figures 46 (a) and 46 (b) displays the respective harmonies spectrum for phase A. It is seen that even though PRC and harmonic compensators keep the low-order harmonics (2nd,4th etc.) within the limits of IEEE Std-1547, resonance oscillations in the range of 15^{th}-18^{th} harmonic violates these limits and deteriorates the power quality as evident from time-domain waveforms in Figure 7(a). Upon implementation of the feedforward compensation, the resonance oscillations are mitigated and THD of the input current is reduced to 4.16 %. The notches in the line current in Fig. 8(b) is

the effect of the DMS that occurs every 1/3rd of the 60-Hz line cycle.



(a) **(b)**

Figure 45. Steady-state time domain waveforms for phase A, B, and C in yellow, blue, and purple respectively. (a) without damping, (b) with multiloop control. Signal in green is input modular voltage of phase A.



(a) **(b)**

Figure 46. Phase A input current harmonic spectrum, (a) no damping, (b) with multiloop control.

Next, to evaluate the improvement in the converter performance a parametric comparison of efficiency and THD using feedforward (in orange) and passive damping (in blue) is carried out as shown in Figures. 47 (a) and 47 (b) respectively. The values of damping resistance and capacitance (R_d and C_d) is chosen to be 8Ω and 6.8μF respectively and are placed across the ac-link capacitance. A considerable improvement of 2.5% in efficiency is observed at rated power of 1-kW while the THD of the input current is approximately the same. Also, the PF for both the

scenarios is observed to be 0.99.

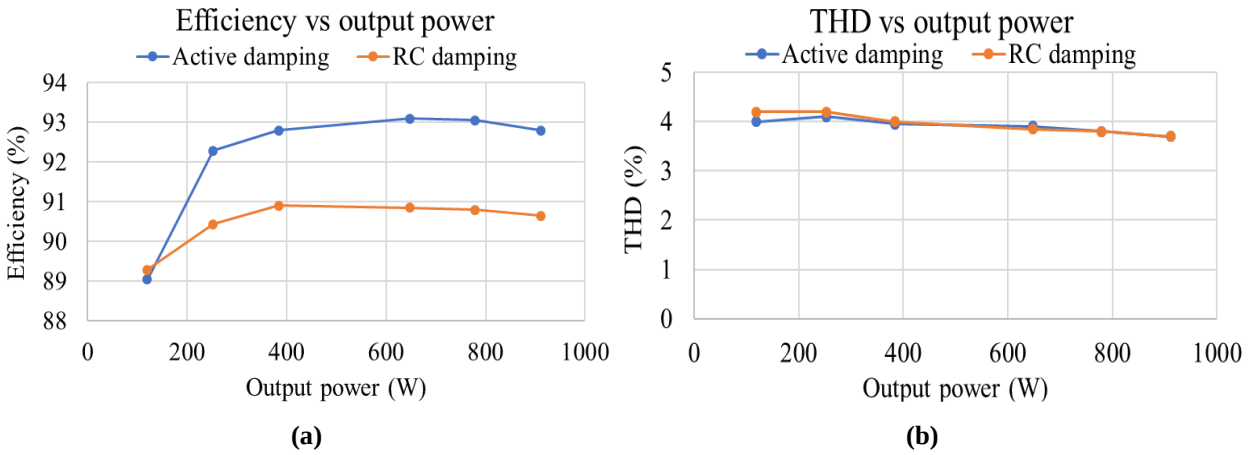


Figure 47. (a) Efficiency vs power (b) THD vs power characterization with passive damping (orange),and multiloop control scheme (blue)

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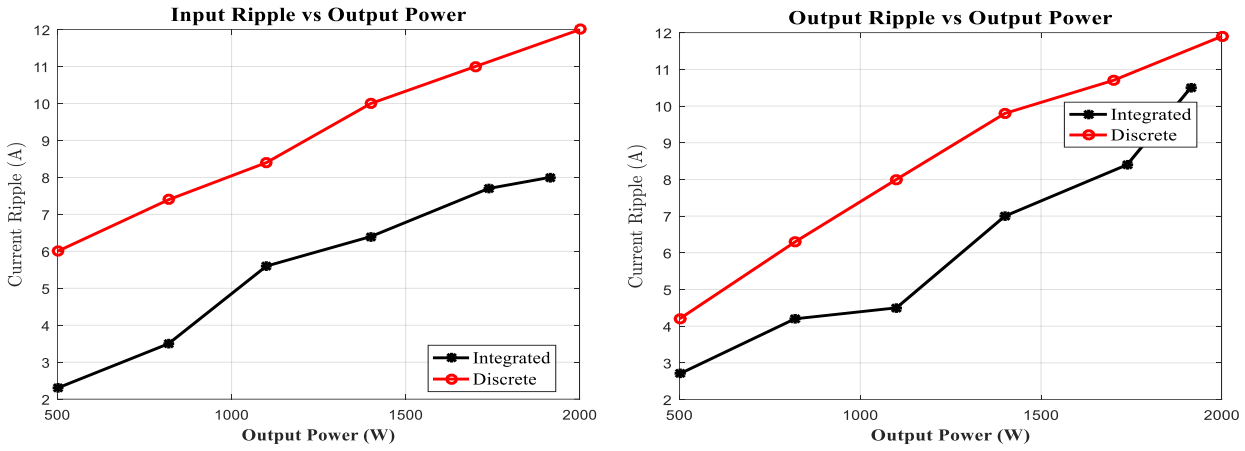
4.2.2 Parametric performance comparison of DM and IM based sp-UBS

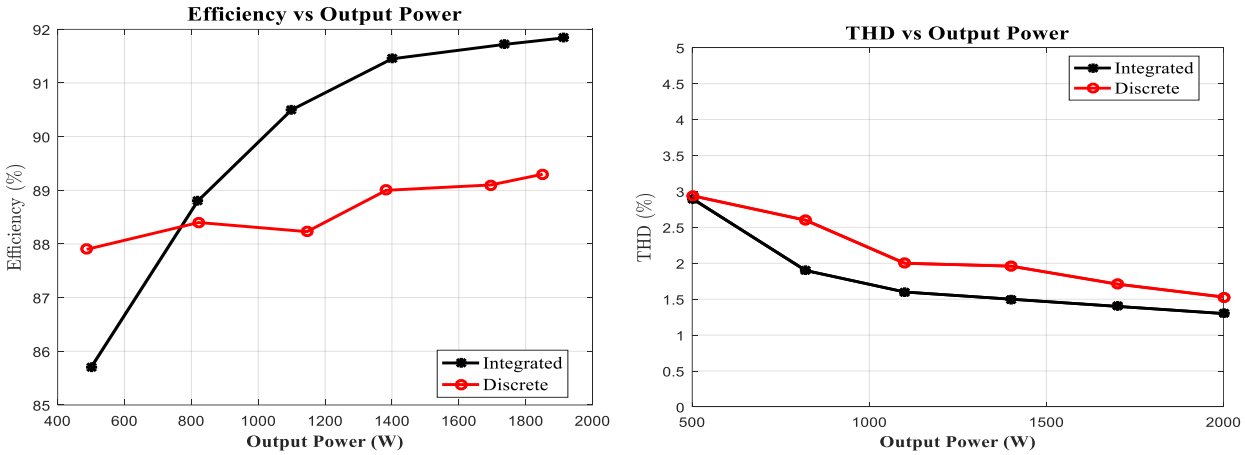
In this section the performance characteristics of the sp-UBS with DM and IM are compared and evaluated. The DMCR is operated with the set reference current of 8 A-peak. Figures 48 (a) and 48 (b) displays the variation of ac-side and dc-side inductor ripple current with output power for the IM and DM respectively. It is seen that, with a coupling coefficient of 0.45, the resultant ripple current for the integrated magnetics based sp-UBS reduces approximately by 30 %.

Figure 49 (a) shows the efficiency and comparison as power is increased from 500-W to 2-kW. The efficiency with the integrated magnetics at 2 kW is roughly 3% higher than the discrete magnetics counterpart. The improvement in efficiency is owing to the reduction in inductor ripple current that affects device switching loss, conduction loss, and magnetics core losses. Figure 49 (b) displays the variation in THD at different power levels. Both prototypes projects THD lower than 5%. The THD of the integrated magnetics based sp-UBS is less than its discrete counterpart



(a) **(b)**

Figure 48. Inductor ripple current comparison with IM and DM (a) ac-side ripple current , (b) dc-side ripple current.



(a) **(b)**

Figure 49. A comparison of efficiency of IM and DM based DMCR at different power levels.

by 0.2 % - 0.4 %. This is owing to the fact that, the THD is calculated by using RMS of all the harmonic components presented in the input current. Since, due to the coupling the switching frequency ripple current is reduced as evident from Figures 48 (a) and (b), its contribution to the THD is also reduced.

4.3 60-kW UBS

After the validation of the proposed control architecture on the sp-UBS, in this section, a detailed design and development of the 60-kW UBS is outlined. Figure 50 depicts a pathway to scale-up the power from 2 kW sp-UBS to rated power of 60 kW UBS for DC fast charging. The pathway is through identifying some of the critical components that are required to achieve performance targets in terms of efficiency, power-density, and specific weight.

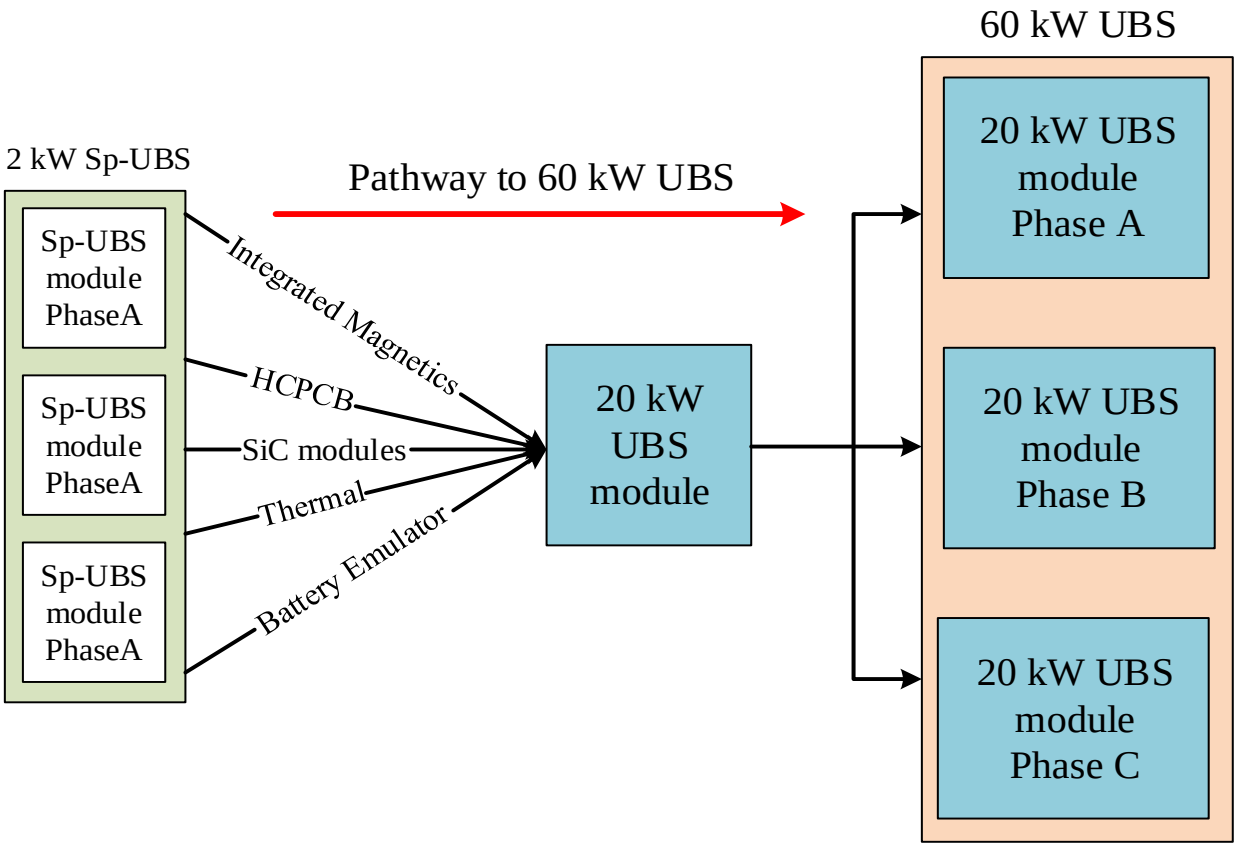
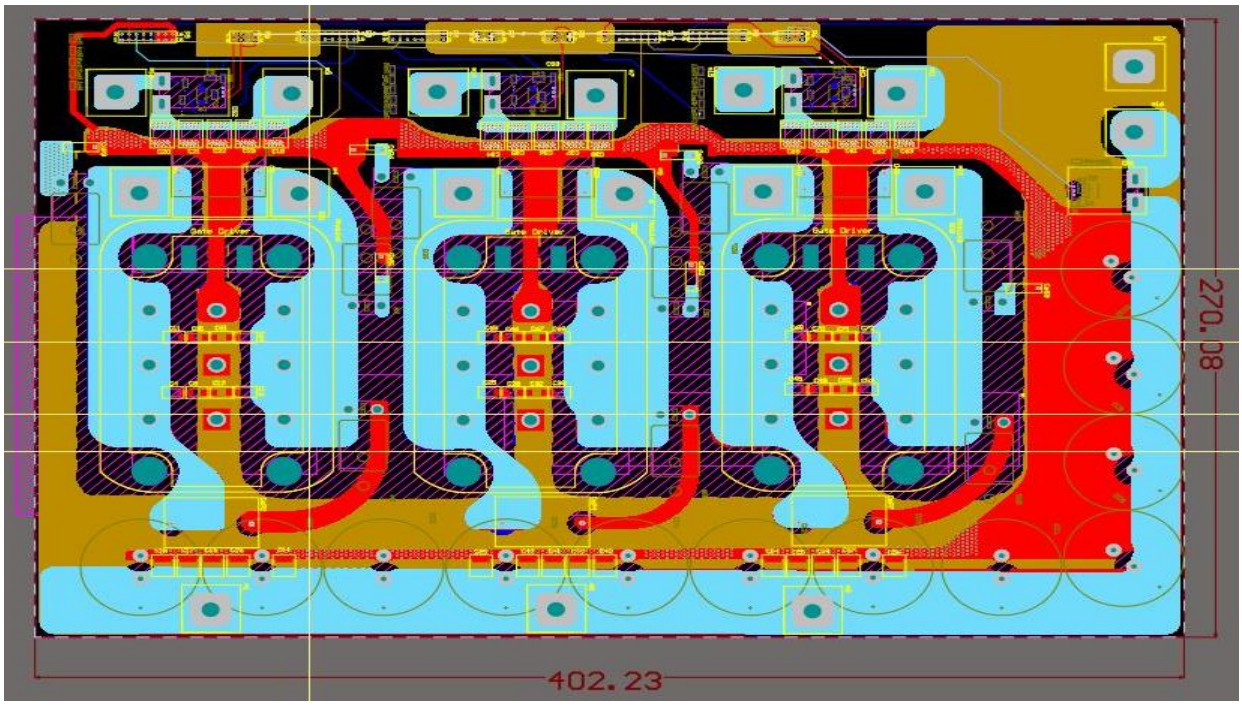


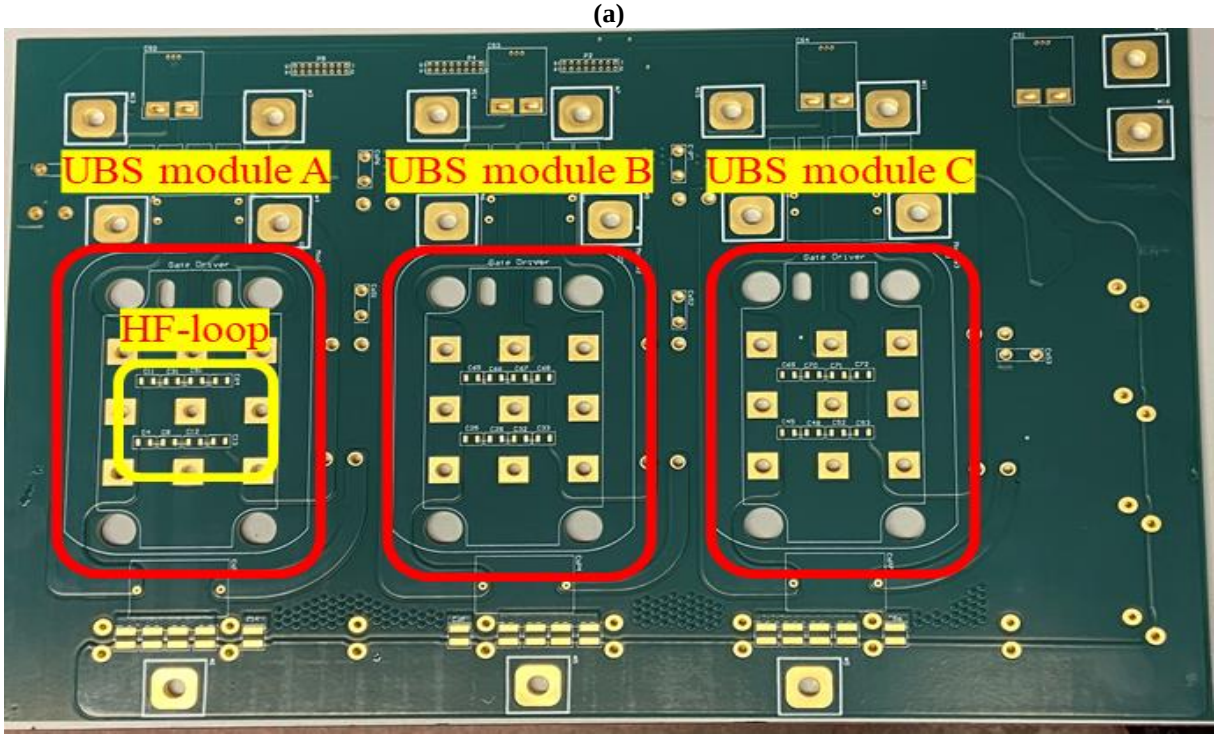
Figure 50. Transitional pathway for scaling the power from 2-kW to 60-kW.

A. High-current PCB (HCPCB)

High current PCBs are also known as heavy/extreme copper PCBs and uses copper weights



(a)



(b)

Figure 51. (a) HCPCB Layout of the 60-kW DMCR based UBS. (b) Finished design of the HCPCB.

ranging from 4 Oz/ft^2 to 32 Oz/ft^2.The minimum thickness and the width of the copper is a function of the required ampacity (I_m) and maximum permissible conductor temperature rise and is represented by the following empirical relationship [],

$$I_m = k(\triangleq T)^{0.44}(Wt)^{0.725}$$

where, I_m, T, W, and t represents current, allowable conductor temperature rise, width, and thickness of the conductor. Constant k is defined to be 0.048 for outer layers and is de-rated by 50% for same amount of heating of the inner layers. For the 60-kW DMCR based UBS, semiconductor switches conducts the maximum current (I_{ds}), and is an ideal sum of instantaneous ac-and dc-side inductor currents. Based on the simulations, the I_{ds} is observed to be 330 A. Adding 25% overhead to the I_{ds}, the thickness and width of the copper is decided based on the maximum $\triangleq T$ and standard IPC-221A [74]. For 20℃ conductor temperature rise and to support approximately 400 A, copper width and thickness were chosen to be 1500 mils and 16 Oz/ft^2 respectively. Further, to prevent the localized heating of the inner layers, thermal vias are provided and 16-Oz copper is evenly distributed among all the layers. Another important aspect of a high-power PCB design is the electrical clearance between the conductors. In the DMCR based UBS, the switching device blocks the maximum voltage (V_{ds}) and is an ideal sum of peak-input and output voltages. At an input and output voltage of 480 VLL (RMS) and 500 VDC, the switching devices blocks maximum voltage of 1178 V. Using the standard IPC-221A, a clearance of 162 mils between the conductors on the inner layers, that can sustain up to 2.5 kV is provided. Much higher electrical clearance of 250 mils on the outer layer is provided to avoid any electrical breakdown due to condensed moisture or external contaminants. The overall HCPCB design is

based on 4-layers with 16-Oz copper and 2-Oz copper coexisting on the same plane for routing of high-voltage power and low-voltage control signals respectively as shown in Figure 51 (a). Figure 51 (b) displays the finished version of the HCPCB.

B. SiC modules

Compared to Si, WBG devices has higher bandgap and superior thermal conductivity that makes them suitable for high voltage, high-power applications as shown in Figure 52 (a). While 650 V GaN devices has been dominant in low-voltage, class of 1200 V and 1700 V SiC MOSFETs are being used for pushing the performance limits in high-voltage, high-power applications. For high-power electronics system (PES), SiC power modules provides maximum current throughput while operating at elevated temperatures.

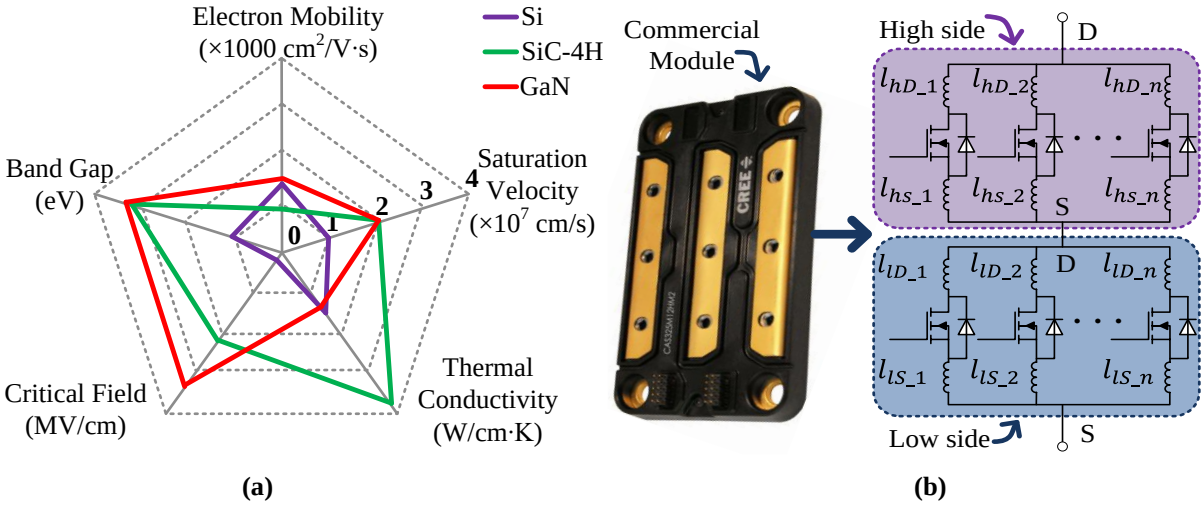


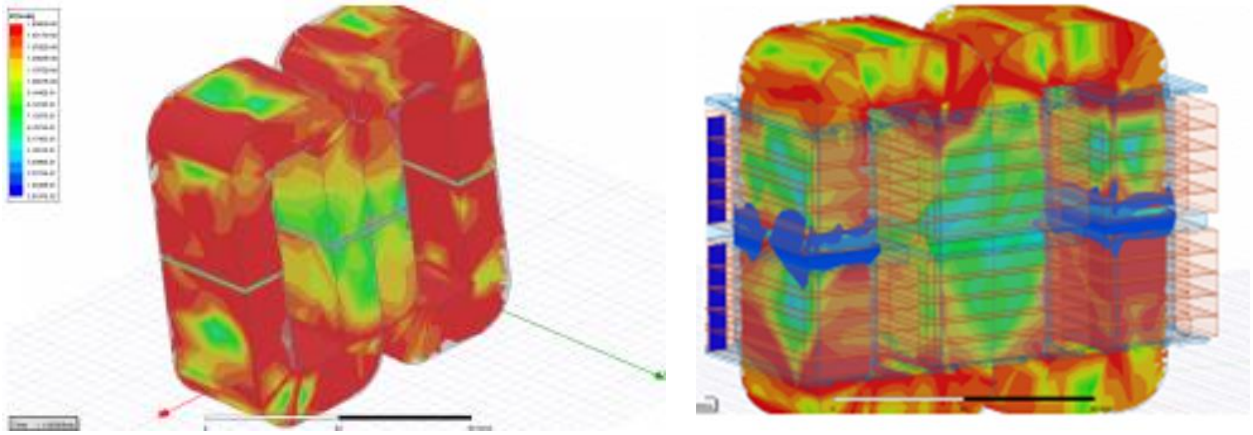
Figure 52. (a) Physical and electrical properties of Si, SiC and GaN-based power devices[4] (b) Depiction of SiC module from CREE with several parallel dies.

This is usually done by housing multiple SiC dies in parallel that enhances its ampacity and power handling capability as shown in Figure 52 (b). However, paralleling multiple dies also gives rise

to higher packaging/stray inductance and higher gate-source commutation delay, that limits the device transition-time and consequently high-switching frequency operation. To sustain a maximum nominal switch current I_{ds} of 330 A and blocking voltage V_{ds} of 1200 V, a 1700V SiC module are used.

C. Magnetics

Apart from switching devices, magnetics is one of the major components that affects the efficiency, volume, and weight of a power electronic system (PES). Magnetic materials such as ferrite, iron-powder, metglas cores enhance the performance of magnetics. Based on the analytical calculation and ANSYS simulation, AMCC 200 C-core is used for realizing the IM for the UBS. Figure 53 (a) and (b) displays the energy distribution and magnetic flux density of the AMCC 200 C-core at dc current and peak input voltage of 120 A dc and 678 V respectively.



(a) **(b)**

Figure 53. (a) Energy distribution in the AMCC 200 E-core. (b) Magnetic flux density of the AMCC 200 E-core at dc output current and peak input voltage of 120 A dc and 678 V respectively.

D. Thermal

In EV applications, available volume and weight of various components are of essence. Efforts are made to shrink the components to make EV's more spacious and light weight. This require the manufacturers to move towards electronics having higher form factor and lower specific weight which in-turn, creates a design challenge for finding the most-efficient yet cost-effective modes of removing excess heat for keeping the critical components within optimum operating temperature ranges. Apart from conventional air-cooled heat sinks, liquid cooled cold plates have gained widespread acceptance and have emerged as an attractive alternative for high-power and high-density PES. Liquid cooling takes advantage of the higher density, thermal conductivity and heat capacity of the liquid in comparison to air. Figure 54 outlines a schematic representation of a liquid cooling loop for contact cooling. The cold-plate is from the Wieland-Microcool []. The double-sided nature provides ease of mounting of SiC modules and IM on top and bottom side respectively. Further, this arrangement also allows IM to dissipate heat in the cold plate. Figure 55 (a) and (b) shows the thermal capture of the IM core of phases A, and B and temperature of the HCPCB switching traces. The

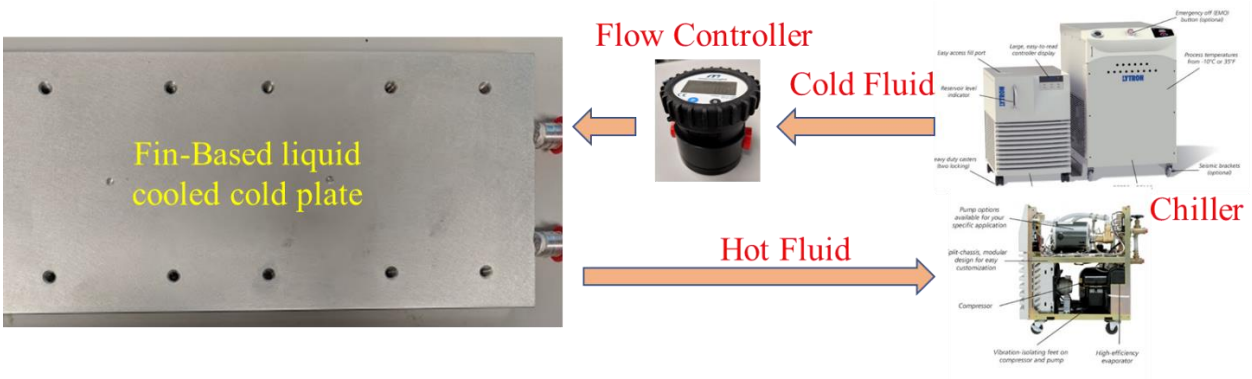
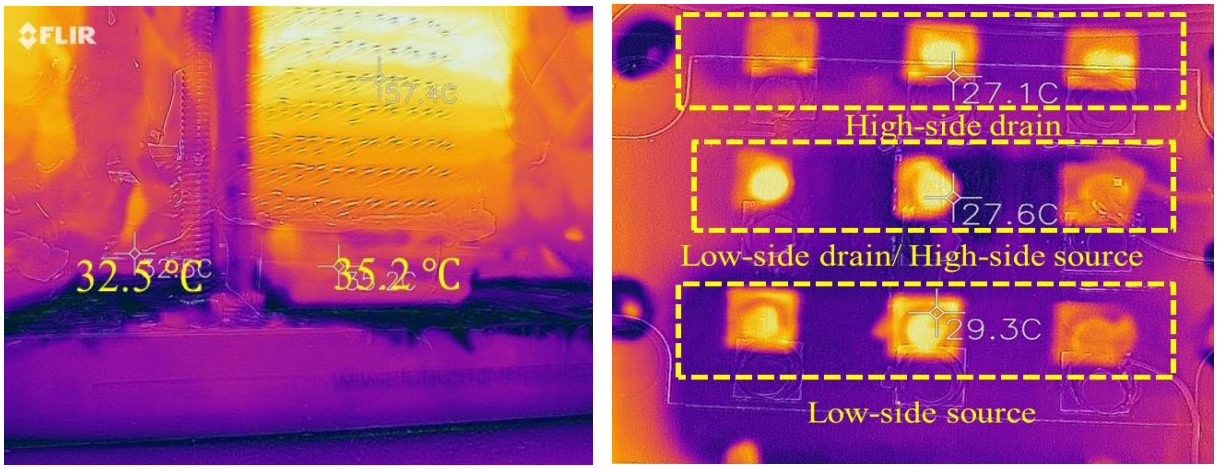


Figure 54. Schematic representation of the liquid cooling loop using the cold-plate. An additional flowmeter is used to regulate the liquid pressure.



(a) **(b)**

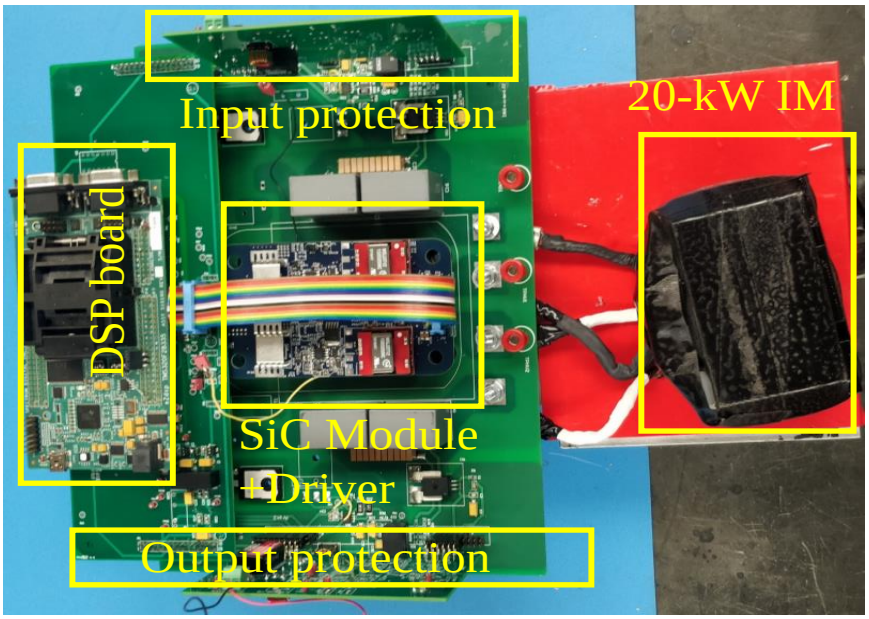
Figure 55. Thermal capture of the IM core of Phase A and B. (b) thermal capture of the HCPCB switching traces.

E. Battery emulator

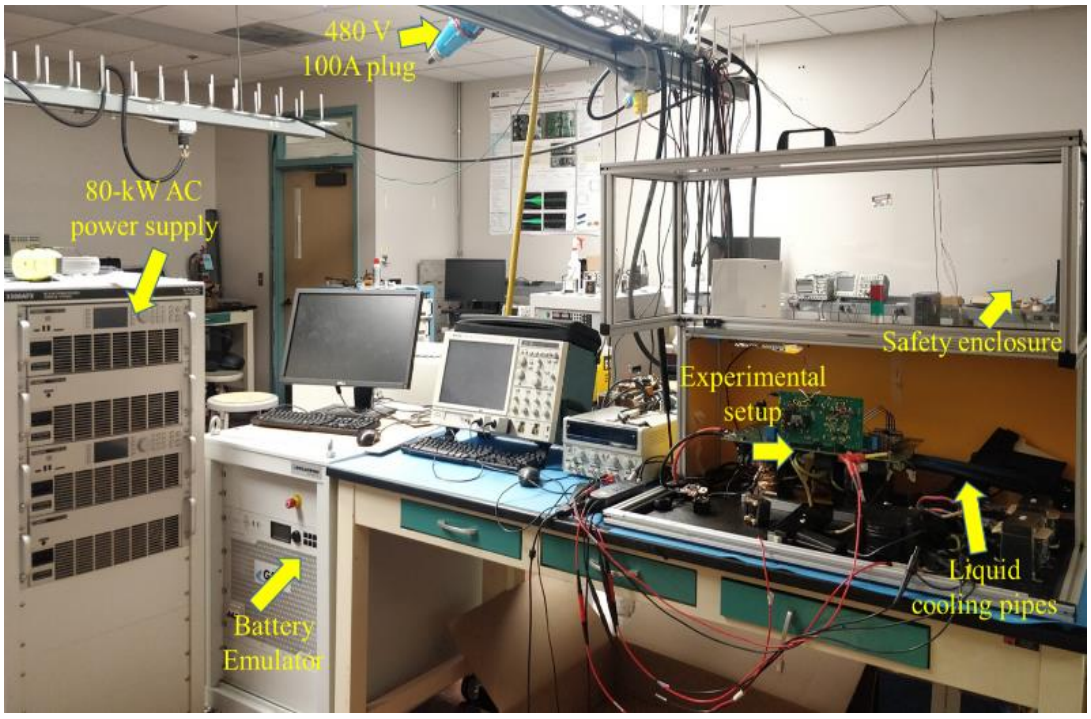
To test the CC and CV mode of operation for the rated power, two 32 kW battery emulator were connected in parallel, and were used as a load. These battery emulators can be characterized as a Ni-Cd, Li-ion or a Lead-acid battery.

4.3.1 20 kW UBS submodule and DC-DC operational characterization

To validate the feasibility of the high-power design and to characterize the critical components, a 20-kW UBS module is designed and tested in DC-DC mode. Figure 56 (a) and (b) shows the experimental prototype and test bench for high-power testing. The 20-kW UBS module is comprised of 1700V SiC module in half-bridge configuration, isolated/bipolar gate driver, one integrated magnetics, and liquid cooled cold-plate. The gate driving signals are generated by digital signal processor TMS320F28335. Battery emulator is used as a load. The experimental tests are performed using the safety enclosure and following other safety protocols.



(a)



(b)

Figure 56. (a) Populated experimental prototype of 20 kW UBS module based on HCPCB design, (b) Experimental test bench for conducting high-power test.

Figure 57. Switching waveforms of ac-side (purple) and dc-side (green) device in steady-state at drain-to-source $V_{ds}of$ 1000 V. The switching frequency of the module is kept at 50-kHz.

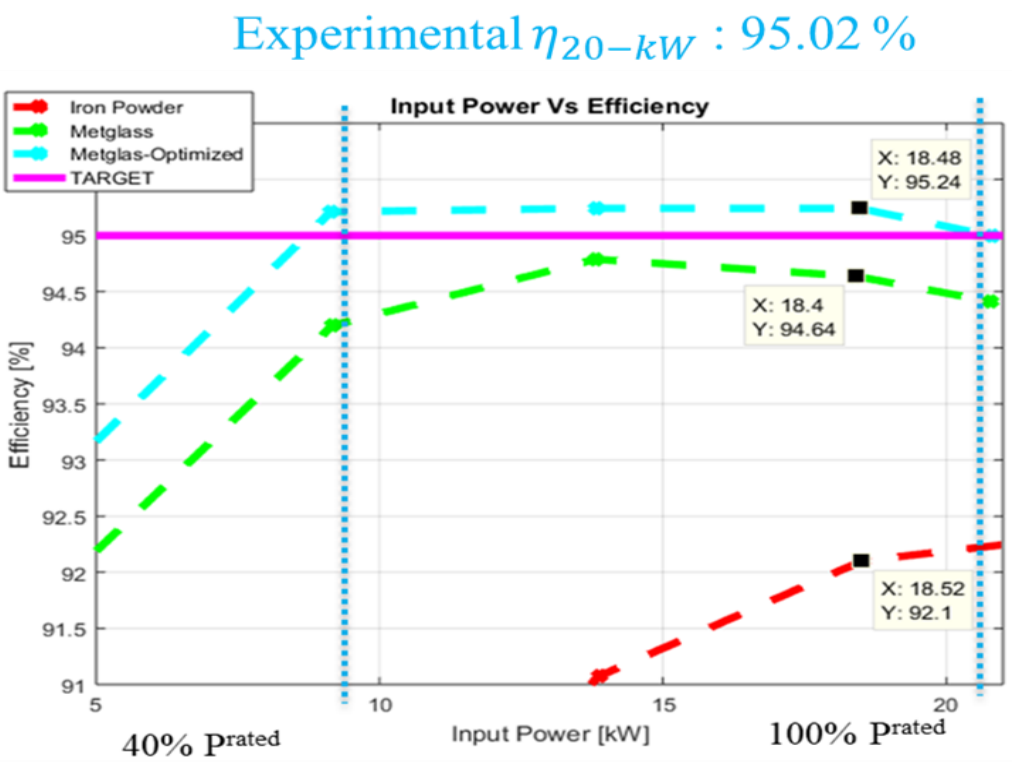
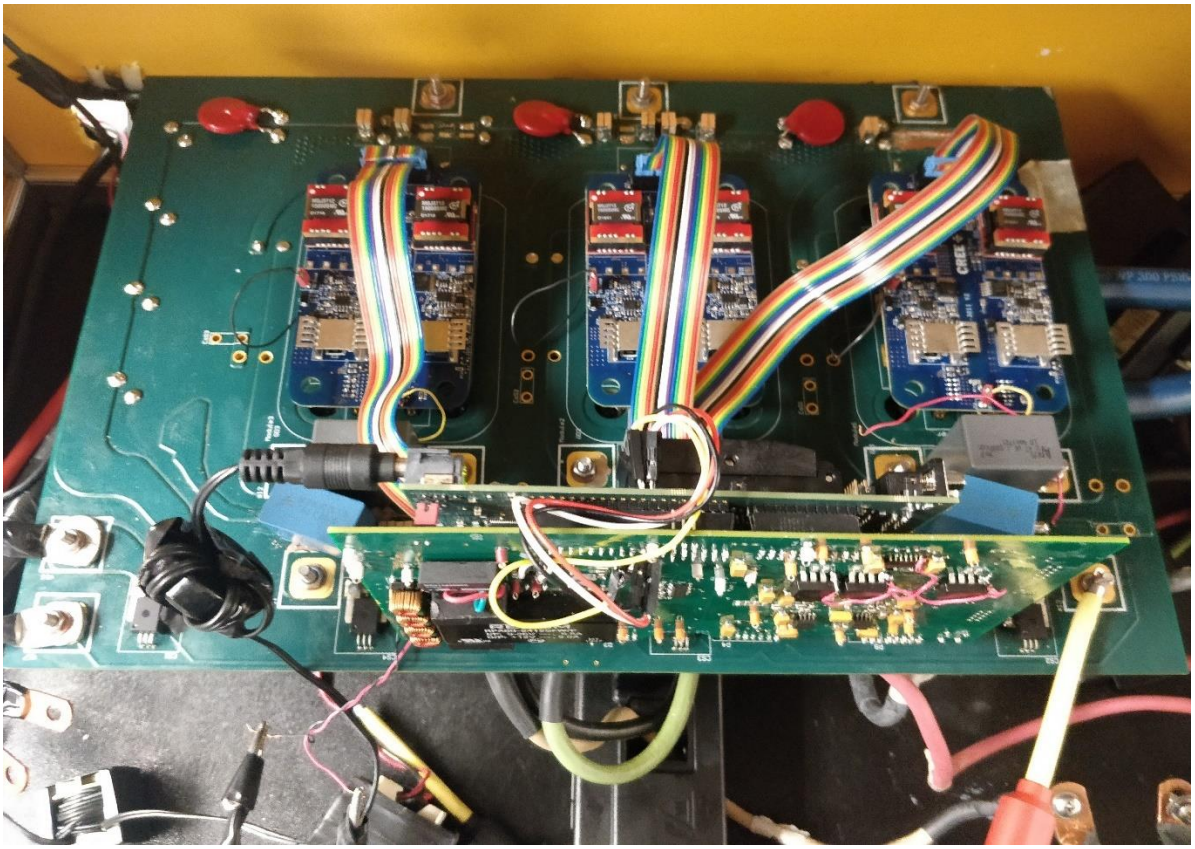
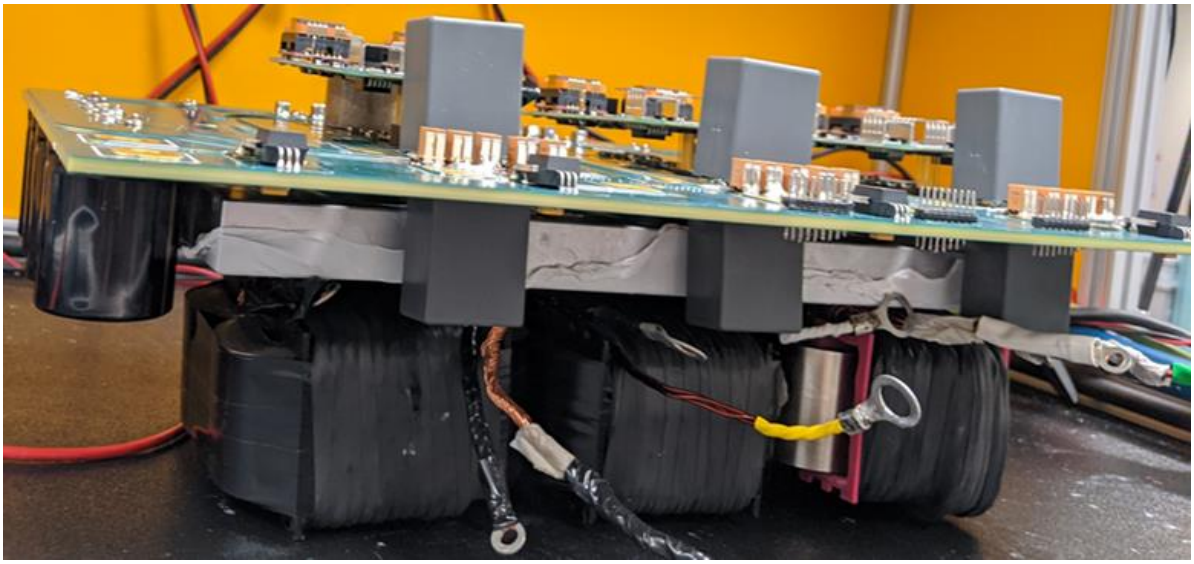


Figure 58. Characterization of the efficiency vs power from 20 % rated power to full rated power

Next, Figure 57 displays the switching waveforms in steady-state at an input and output voltage of 500 V. Multiple efficiency-power characterization tests were carried out to improve the peak efficiency of each UBs module as shown in Figure 58. The curve in red has peak efficiency at 92.1 % without any optimization. The other two curves in green and blue shows significant improvement in the efficiency due to better magnetic material. Replacing the iron powder core with Metglas core improves the efficiency by 2.5 %. Further optimization of the IM design increases the peak efficiency to 95.24 % and stays constant from 40% rated power to full rated power of the UBS module. The decrement in the efficiency near full-rated power is due to increased conduction losses.



(a)



(b)

Figure 59. Experimental prototype of the 60-kW UBS. (a) top view displaying the position of the three SiC gate drivers and their respective modules. (b), side-view displaying position of the three IMs.

4.3.2 60-kW UBS module and AC-DC operational characterization

Three 20-kW UBS submodules are integrated together on the HCPCB to validate the operational characterization and functional feasibility of the UBS as shown in Figure 59.

Table VI. Power-stage parameters of 60-kW UBS

Input voltage (line to line) ($V_{ab} = V_{bc} = V_{ca}$)	480 V RMS
Output voltage (V_{out})	Up to 500 V dc
Output power	60-kW (20-kW per module)
Input inductance ($L_{1a} = L_{1b} = L_{1c}$)	75 µH
Output inductance ($L_{2a} = L_{2b} = L_{2c}$)	75 µH
Input capacitance ($C_a = C_b = C_c$)	2.2 µF
Output capacitance ($C_{2a} = C_{2b} = C_{2c}$)	4.7 mF

Blocking capacitance ($C_{1a} = C_{1b} = C_{1c}$)	1.5 μF
Switching frequency (f_s)	50 kHz

Table VI displays the power-stage-parameters for the 60-kW UBS. To test the operational cahracteristics of the UBS from 20 % of the rated power to full rated power, first the converter input voltage was increased to 480 V L-L RMS at an input current of 20 A-peak. Gradually the current reference is increased to-100 A-peak to achieve input power of 60-kW. However, there were several challenges that were resolved during the power increments.

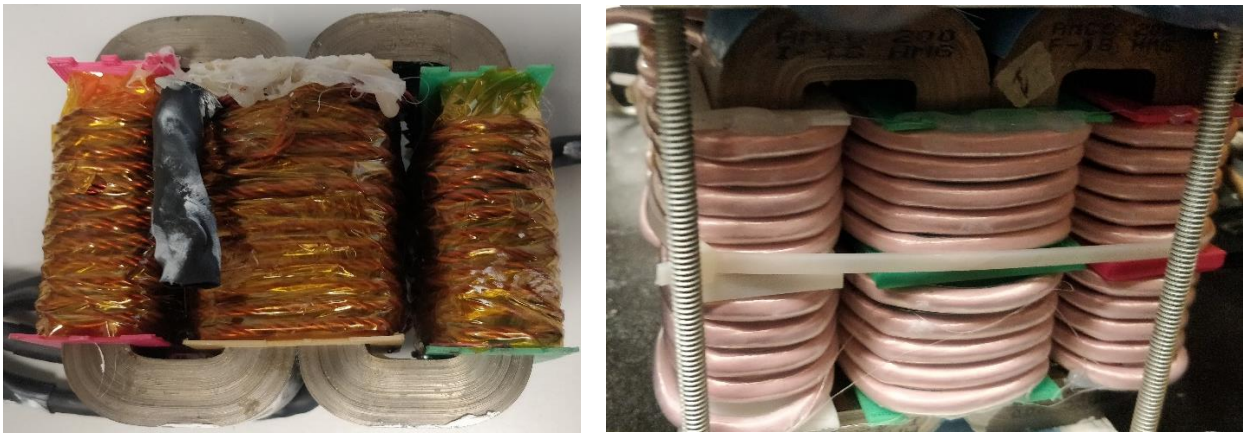
Challenges:

(i) Presence of third-harmonic: Due to mismatch in the scaled feedback input voltage amplitudes in a PLL, the conversion from abc to a d-q coordinate system gives rise to an additional zero vector. The zero vector distorts the reference current vector as generated by the PLL and manifest itself in the form of third-harmonic. Consequently, this affects the feedback current. To mitigate this challenge, the PLL gains must be tuned at the highest operating voltage.

(ii) Dead time: A higher dead time between the switching of the devices results in loss of duty cycle near the zero crossing. As a result, the gate-to-source voltage does not recognize small duty-cycle widths and does not switch the device and affects the THD of the input current. This effect becomes more pronounced with the devices of high transition time (rise time and fall time) since to ensure no overlap of drain to-source voltage (V_{ds}) between HS and LS devices during transition, a large dead time is required. A lower dead-time can improve the THD however, it results in shorting of the ac-link capacitor which in turns dips the output voltage and results in loss of efficiency. In lieu of this, the dead time is optimized on the current setup and is kept at 300 *n*s.

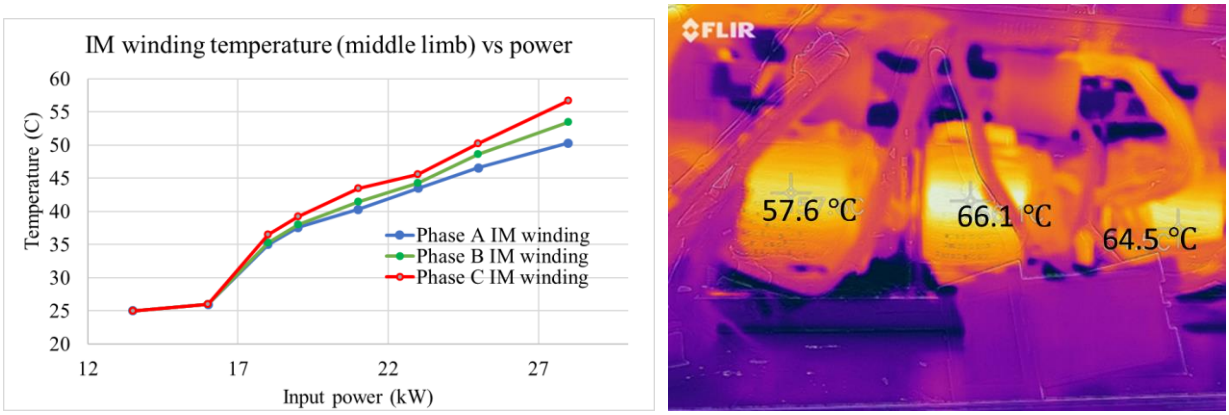
(iii) Sensor feedback gain optimization: As the input current reference amplitude increases, the dominating resonant poles and zeros creeps inside the system bandwidth and give rise to the resonance oscillations. Thus, the sensor feedback gains are optimized such that the resonating poles and zeros stays outside the control bandwidth.

(iv) IM windings: The ac-and dc-side inductors in the DMCR supports ac and dc currents in addition to the ripple current. Previously, in the version A IM of inductance 200μH, and 0.5 coupling factor, 7, 16-AWG Litz wire strands were used as shown in the Figure 60 (a). As the current reference is gradually increased from 25 A-peak to 50 A-peak, conduction loss in the IM windings increases. As evident from Figure 61 (a), the temperature rises from 25℃ to 60℃ . Figure 61 (b) displays the thermal capture of the winding at 55 A-peak. The winding temperature reaches 66℃ approximately. To mitigate this challenge, 1300, 40-AWG Litz wire strands were wound together by the New England Wire Technologies. However, due to the sheer size of the overall winding, it is practically infeasible to achieve 200μH without increasing the window area/size of the core. Thus, keeping the core dimensions and weight same, a trade-off between core loss and conduction loss was worked out. In the version B IM, an inductance of 75 μH is achieved with lesser number of turns as shown in Figure 60 (b). This reduced the dc and ac resistance of the winding by approximately 75% i.e. from 30.36 mΩ to 8.23 mΩ. The winding temperature at 60 A-peak was observed to be at 40℃.



(a) **(b)**

Figure 60. (a) version A IM of inductance 200 uH with 30, 26-AWG Litz wire strands, (b) version B IM of inductance 75 uH with 600, 40-AWG Litz wire strands.

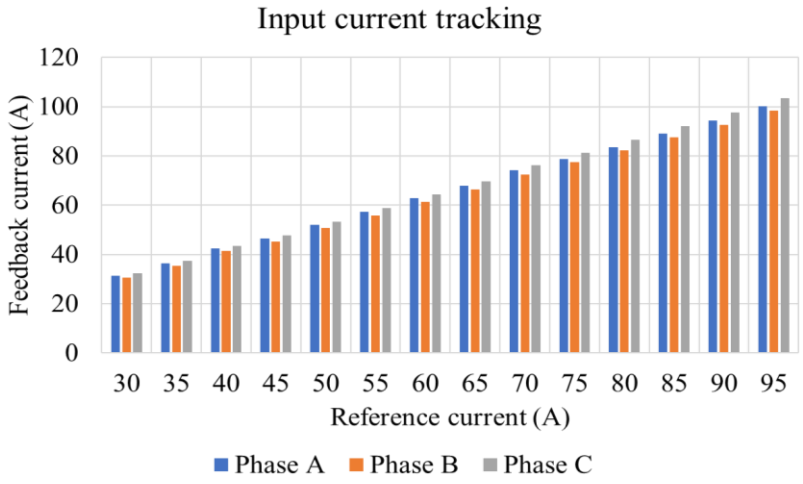


(a) **(b)**

Figure 61. (a) Ac-side winding temperature profile of three phase A, B, and C. (b) Thermal capture of the copper windings of phase A, B, and C at 57.6℃, 66.1 ℃, 70.1 ℃ respectively at 32.3-kW.

Parameter	Value
Voltage	480 Vrms (L-L)
Current	95 A-peak
K_p (PLL)	0.2
K_i (PLL)	100
$K_{p,abc}$ (PR)	4.5
$K_{r,abc}$ (PR)	500
$K_{r2,abc}$ (PR)	500

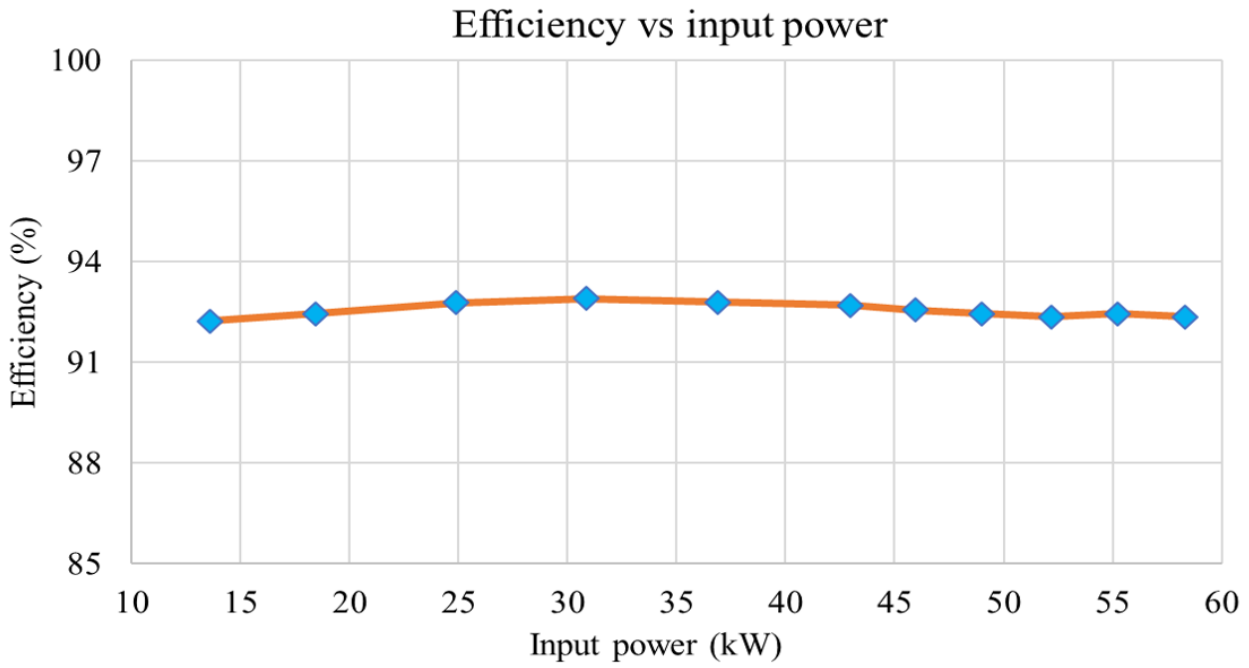
(a)



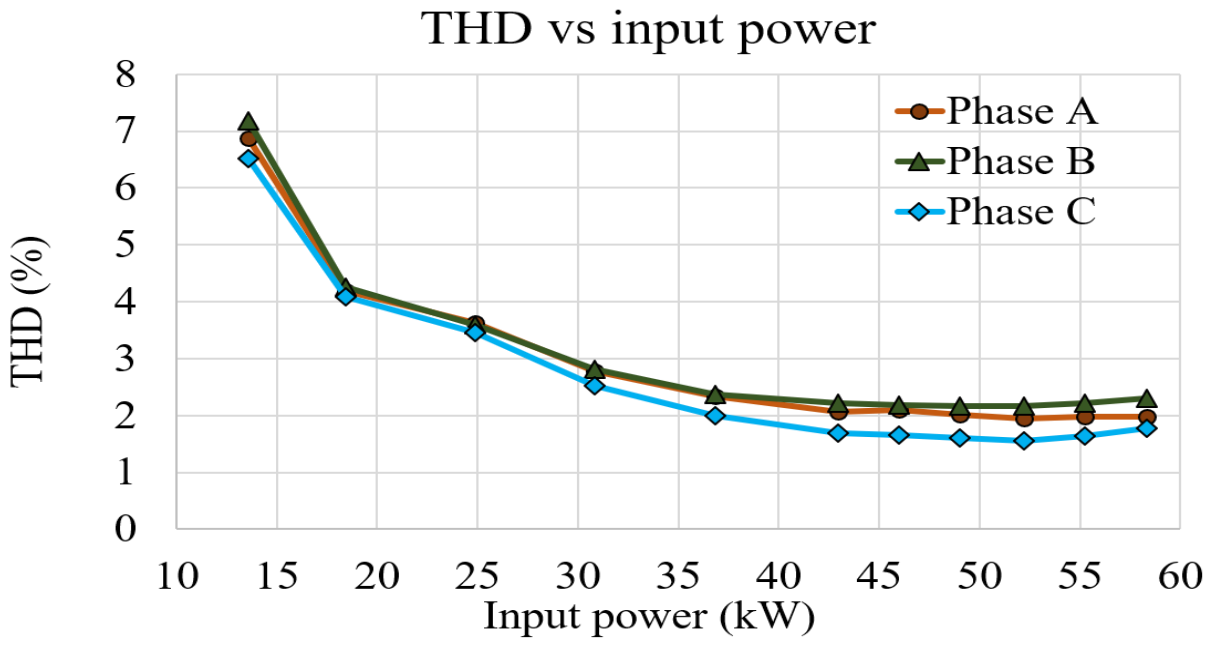
(b)

Figure 62. (a) Closed loop control gains, (b) input current feedback vs input current reference for phase A, B, and C

To demonstrate the operational functionality at 60-kW, power level of the UBS is increased gradually by increasing the input current reference. Figure 62 (a) displays the control gains that were tuned for achieving PFC and tracking the input current references of all the three phases. Figure 62 (b) displays a comparison of the tracking reference and feedback current. The mismatch in the phase current is owing to the dissimilarity in the passives between the UBS submodules. Figure 63 displays a parametric plot of the efficiency and THD of phase A, B, and C with input power variation. The UBS with hard-switching reaches a peak of 93% efficiency at 30-kW and is plateaued at 92.5 % from 20% to 100 % of the rated power. The THD of the phase A (brown), B



(a)



(b)

Figure 63. Parametric plots captured at input voltage and charger current of 480 Vrms (L-L) and 120 A dc respectively. (a) efficiency, (b) THD.

(green), and C (blue) reduces from 7% to 2% on an average as the power is increased to the rated power. The reduction in THD is the result of increment in fundamental current component. Figure 64 displays the steady-state time-domain waveform for input currents phase A (yellow), phase B (blue), phase C (purple), and L-N voltage of phase A (green) at the rated power of 60-kW.

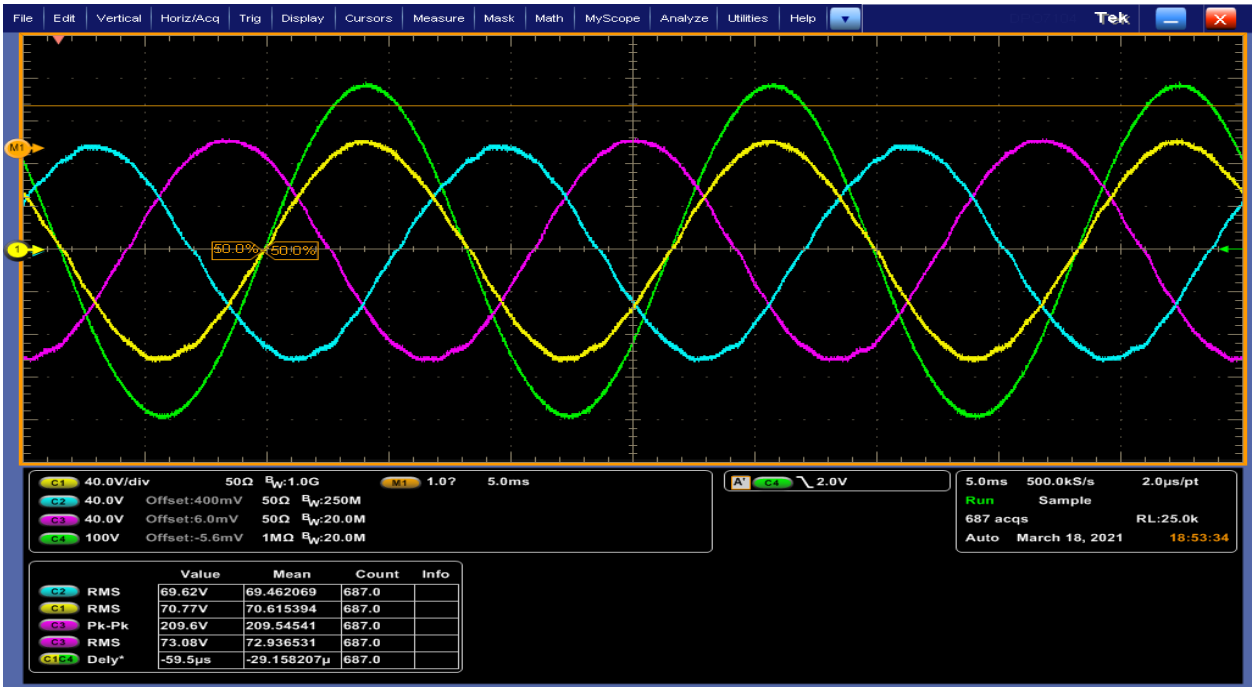


Figure 64. Three-phase steady state time-domain phase currents and phase A L-N voltage.

Figure 65 displays the sequence of increasing the power on the UBS setup during the initial testing phase. The signals in yellow, green, and purple represents phase A current, phase A voltage, and output voltage respectively. As evident from Figure 65, the UBS setup is turned ON at lower input voltage of 40 Vrms (L-L) and is ramped up to 480 Vrms (L-L) in 15s. In this duration, the input current is able to maintain its tracking reference of 20 A due to current-control mode of operation. When the input voltage reaches 480 Vrms (L-L), input power is increased from 13.5 kW to 60-kW by increasing the current reference from 20 A-peak to 100 A-peak. Figure 66

displays the transient susceptibility of the UBS. A step transient of 50 % of the rated input voltage was given to measure the current control response time.

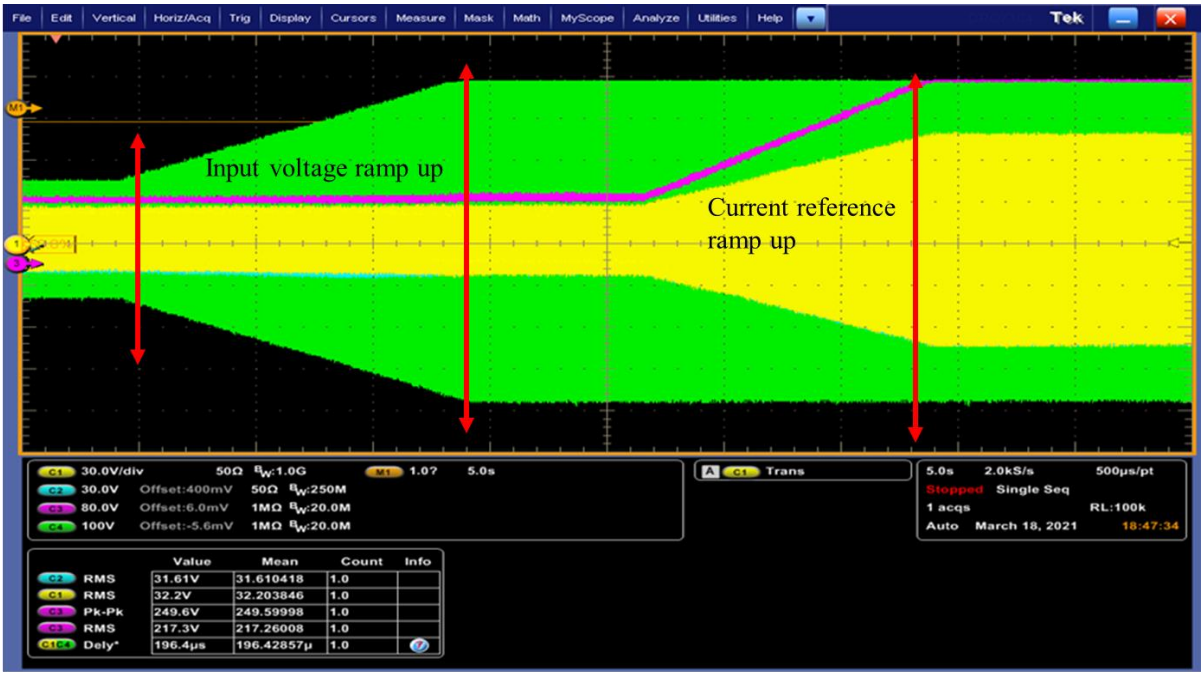


Figure 65. Sequence of increasing power on the UBS setup from 20 % of the rated power to full-rated power.

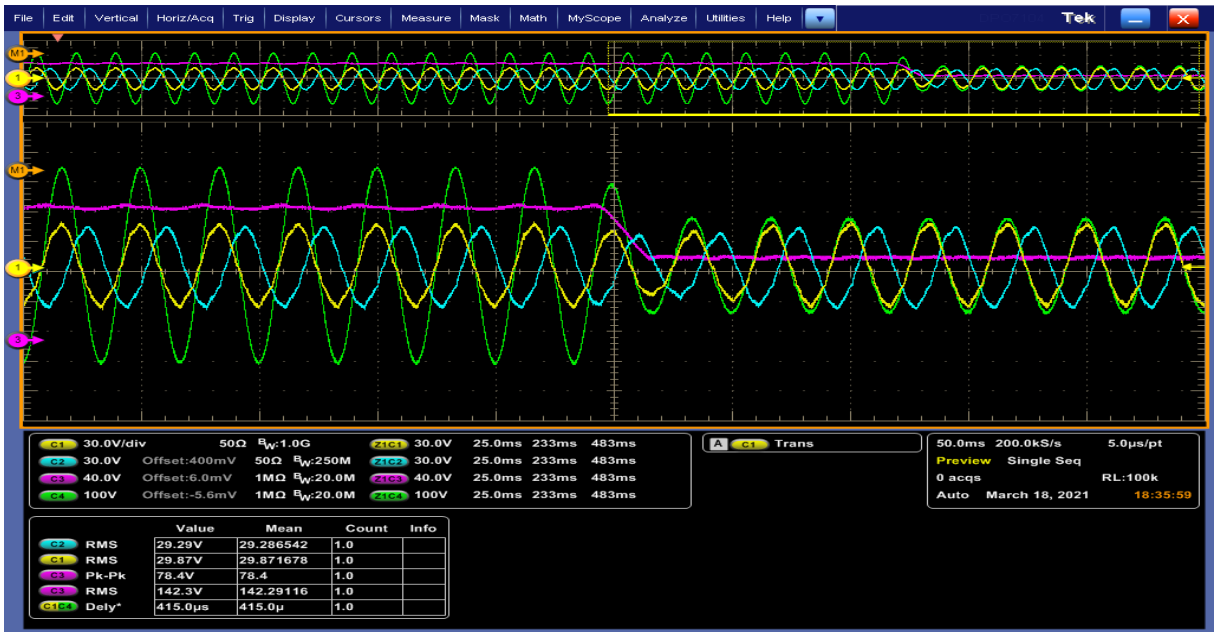


Figure 66. Transient susceptibility of the closed-loop current control for a step transient of 50% of the rated input voltage.

Chapter 5

5. CONCLUSIONS AND FUTURE WORK

5.1 Summary and Contributions

L3 chargers/DC fast chargers alleviates the range anxiety among the EV users by reducing the charging duration. In this dissertation, a three-phase differential-mode-Cuk-rectifier (DMCR) topology is proposed as a universal battery supercharger (UBS) for achieving DC fast charging of EVs. Advantages of the DMCR topology and its application for achieving performance in terms of efficiency, weight, and size as a cost-effective solution have been discussed succinctly.

To validate the operating principle of the DMCR, an existing DMS PWM scheme is used. HF and LF operating modes are delineated alongwith the piece-wise power flow through the DMCR modules. To control the DMCR in a rectifying mode of operation for EV charging, the input current must be drawn in UPF fashion with the grid voltage. To achieve this, a PLL followed by a simple PR and low-order harmonic compensator is designed for achieving PFC and tracking of the input current references. A feedforward compensation with inverse transformation is used to mitigate the low-order harmonics that arises due to the gain non-linearity of the DMCR. However due to the HF mode of operation, passive elements of the DMCR and grid filters interacts with each other and give rise to resonance frequency oscillations. These oscillations if unchecked, renders the operational and functional feasibility of the. In chapter 3, two methods of mitigating the resonance frequency oscillations have been discussed. One approach is based on insertion of a physical RC damper in the resonance path to dampen the oscillations. However, this causes

conduction loss and tank the efficiency of the converter. The other approach is based on a multiloop control that uses a standard feedforward lag-lead compensation. The multiloop control based approach is lossless scheme however requires control algorithm modification. Advantages of each approach are discussed. Experimental validation of both approaches on the same power-stage board

Finally, in chapter 4, experimental validation of the proposed DMCR topology for L3 EV charging applications is delineated. First, to test the basic control architecture and verify the modes of operation, a sp-UBS of 3-kW power-stage board was designed. The purpose of the board was to verify the functional feasibility, control architecture, operating modes, and a comparison between DM and IM. Further, to mitigate the resonance frequency oscillations, two damping schemes; passive damping, and multiloop control scheme were experimentally tested and validated.

High power 60-kW prototype of the DMCR is developed following the UBS CAD model design. First, a 20-kW submodule of the DMCR is designed using a HCPCB approach and tested. The HCPCB allows high power and low power circuit to co-exist on the same PCB. To support such power levels at high frequency, 1700 V SiC modules with dedicated isolated gate drivers were used Finally, three such 20-kW submodules were integrated together on a HCPCB to form a 60-kW UBS prototype. The prototype is tested with two 32-kW battery emulators at an input voltage of 480 Vrms(L-L) and output current of 120 A dc. Challenges in increasing the power from 3-kW to 60-kW are discussed in detail. Experimental results encompassing, steady-state, transient, start-up sequence waveforms are provided. Thermal captures of the device, magnetics and PCB at rated power are presented.

5.2 Future Work

The research work delineated in this dissertation can be extended to encompass the following future works:

- One of the challenges on the hard-switching DMCR topology is efficiency, which can be further be improved using soft-switching scheme by operating the converter in BCM or DCM.
- Protection schemes against DC fault, AC fault, converter faults and their effect on UBS can be verified and tested.
- Transformerless nature of the DMCR allow higher common-mode leakage current. Techniques to reduce the leakage current can be studied further.

6. APPENDICES

APPENDIX A

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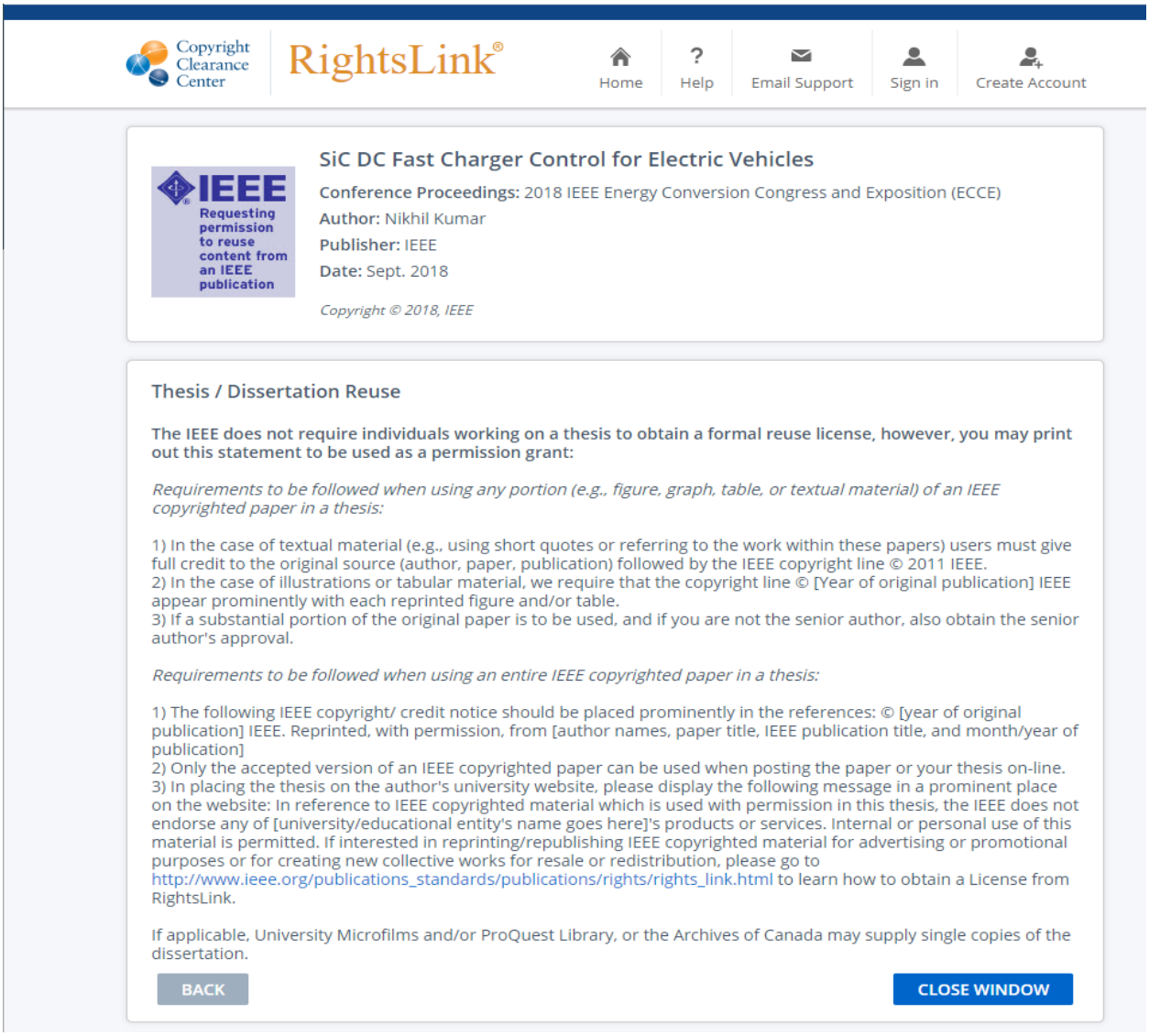

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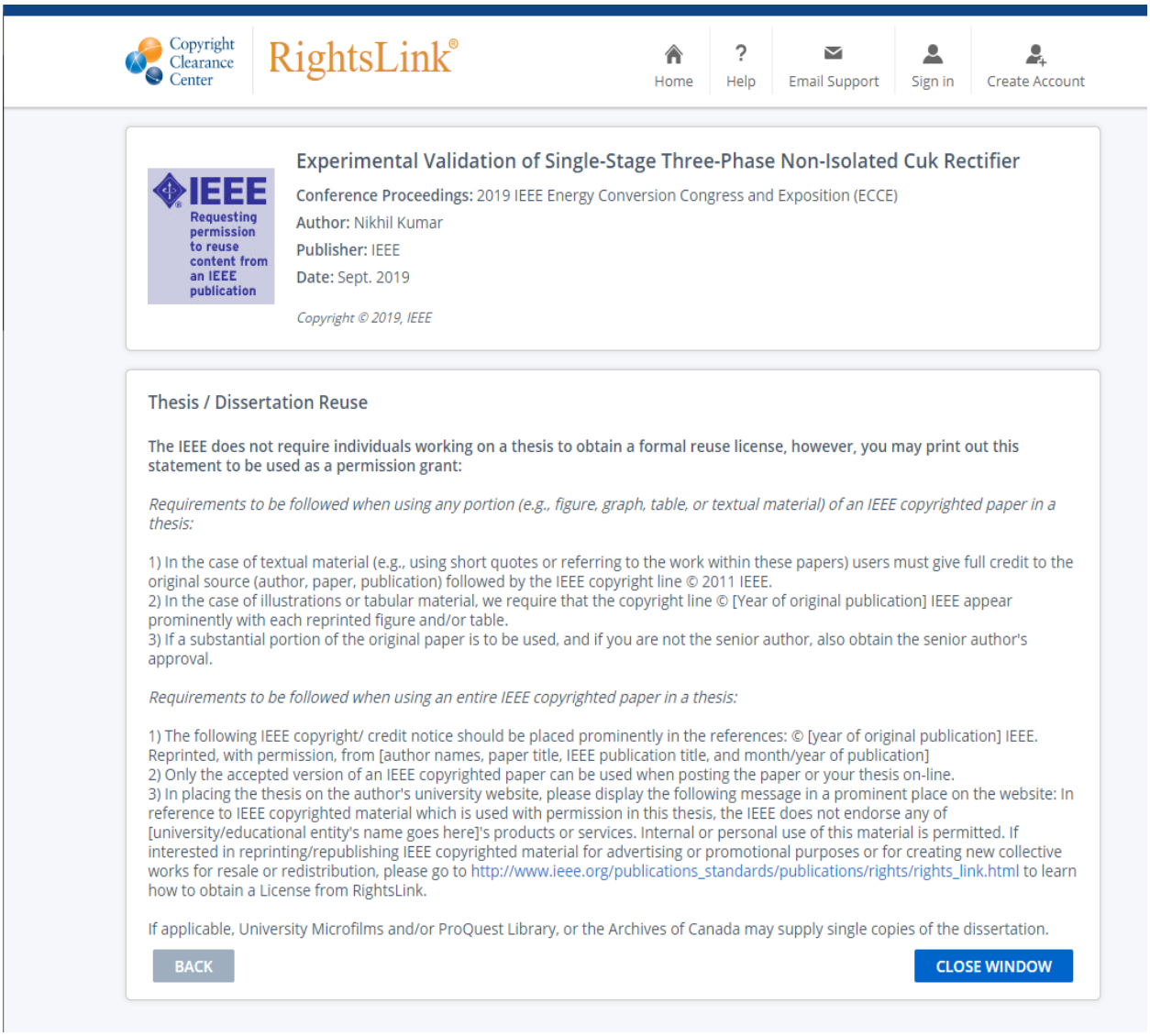

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Conference Proceedings: 2019 IEEE Energy Conversion Congress and Exposition (ECCE)

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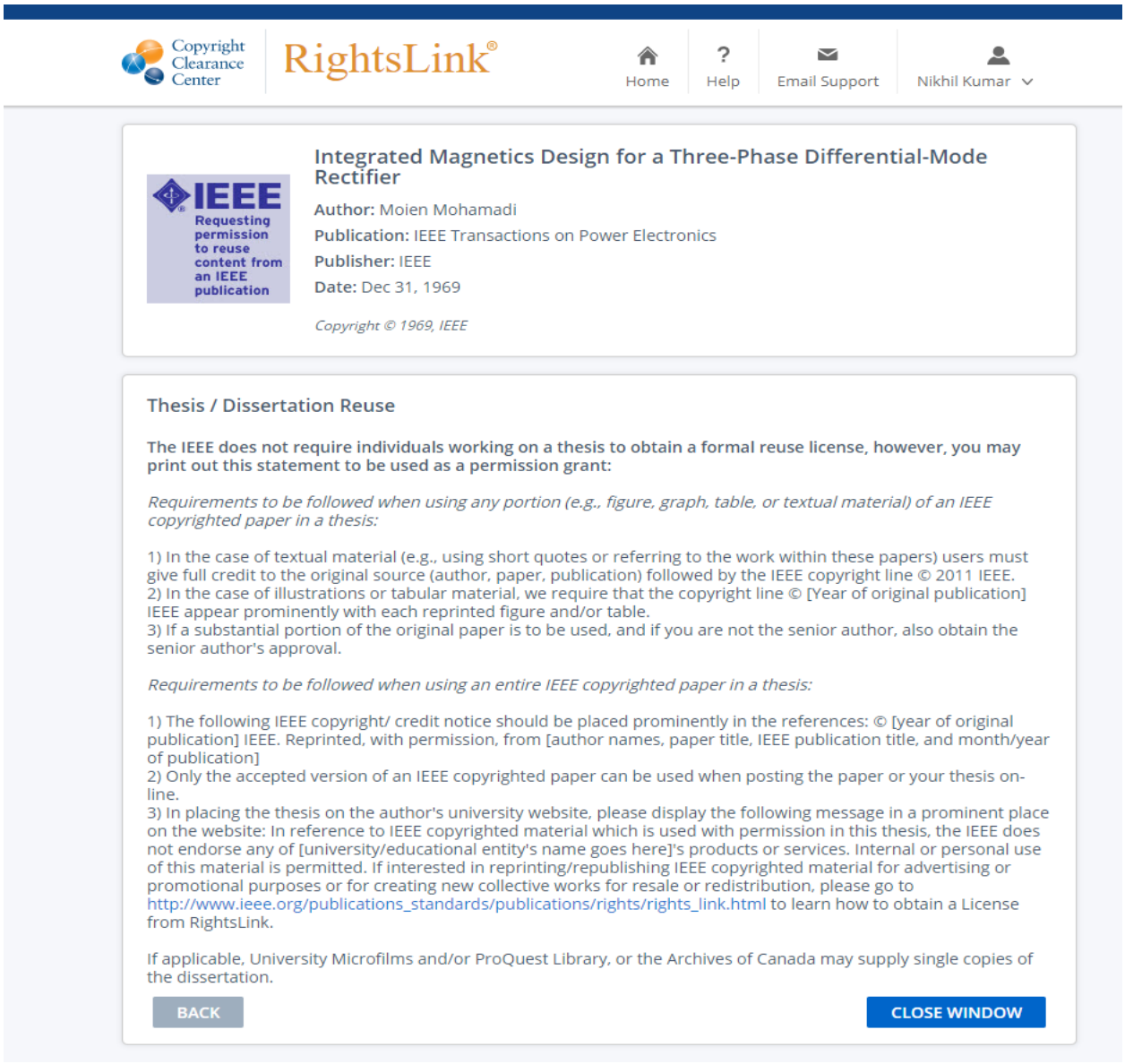
APPENDIX A (Continued)

APPENDIX A (Continued)



APPENDIX B

The coefficients of the grid-current ($\hat{i_g}$) to duty-cycle ($\hat{d}$) transfer function (G_{id}) for the IM based DMCR are presented below.

A. Numerator coefficients

$$a_0 = 2RV_{in}D^2M^2 - 2L_1L_2RV_{in}D^2 - 2RV_{in}DM^2 + 2L_1L_2RV_{in}D$$

$$a_1 = D^2MV_{in}k - D^2L_2V_{in}k - C_2M^2R^2V_{in} + DL_2V_{in}k + C_2L_1L_2R^2V_{in} + C_2DM^2R^2V_{in} - C_3DM^2R^2V_{in} + C_3D^2M^2R^2V_{in} - C_2DL_1L_2R^2V_{in} + C_3DL_1L_2R^2V_{in} - C_3D^2L_1L_2R^2V_{in}$$

$$a_2 = C_2L_2RV_{in}k - C_2MRV_{in}k - C_2DL_2RV_{in}k + C_3DL_2RV_{in}k + C_2DMRV_{in}k - C_3D^2L_2RV_{in}k + C_3D^2MRV_{in}k$$

$$a_3 = C_2C_3L_2R^2V_{in}k - C_2C_3MR^2V_{in}k - C_2C_3DL_2R^2V_{in}k + C_2C_3DMR^2V_{in}k$$

B. Denominator coefficients

$$b_0 = -D^4M^2R^2 + L_1L_2D^4R^2 + 4D^3M^2R^2 - 4L_1L_2D^3R^2 - D^2M^2R^2 + 6L_1L_2D^2R^2 + 4DM^2R^2 - 4L_1L_2DR^2 - M^2R^2 + L_1L_2 * R^2$$

$$b_1 = L_2Rk + D^2L_1Rk + 6D^2L_2Rk - 2D^3L_1Rk - 4D^3L_2Rk + D^4L_1Rk + D^4L_2Rk - 6D^2MRk + 6D^3MRk - 2D^4MRk - D^2L_gM^2R + 2D^3L_gM^2R - D^4L_gM^2R - 4DL_2Rk + 2DMRk + D^2L_1L_2L_gR - 2D^3L_1L_2L_gR + D^4L_1L_2L_gR$$

APPENDIX B (Continued)

$$b_2 = C_2L_1R^2k + C_3L_2R^2k - C_1L_gM^2R^2 - C_2L_gM^2R^2 + C_1L_1L_2L_gR^2 + C_2L_1L_2L_gR^2 - 2C_2DL_1R^2k - 4C_3DL_2R^2k + 2C_3DMR^2k + 4C_1DL_gM^2R^2 + 2C_2DL_gM^2R^2 + C_2D^2L_1R^2k + C_3D^2L_1R^2k + 6C_3D^2L_2R^2k - 2C_3D^3L_1R^2k - 4C_3D^3L_2R^2k + C_3D^4L_1R^2k + C_3D^4L_2R^2k - 6C_3D^2MR^2k + 6C_3D^3MR^2k - 2C_3D^4MR^2k - 6C_1D^2L_gM^2R^2 + 4C_1D^3L_gM^2R^2 - C_2D^2L_gM^2R^2 - C_1D^4L_gM^2R^2 - C_3D^2L_gM^2R^2 + 2C_3D^3L_gM^2R^2 - C_3D^4L_gM^2R^2 - 4C_1DL_1L_2L_gR^2 - 2C_2DL_1L_2L_gR^2 + 6C_1D^2L_1L_2L_gR^2 - 4C_1D^3L_1L_2L_gR^2 + C_2D^2L_1L_2L_gR^2 + C_1D^4L_1L_2L_gR^2 + C_3D^2L_1L_2L_gR^2 - 2C_3D^3L_1L_2L_gR^2 + C_3D^4L_1L_2L_gR^2$$

$$b_3 = C_2Rk^2 - 2C_2DRk^2 + C_2D^2Rk^2 + C_1L_2L_gRk + C_2L_2L_gRk - 4C_1DL_2L_gRk - 2C_2DL_2L_gRk + 2C_1DL_gMRk + C_1D^2L_1L_gRk + 6C_1D^2L_2L_gRk - 2C_1D^3L_1L_gRk - 4C_1D^3L_2L_gRk + C_1D^4L_1L_gRk + C_2D^2L_2L_gRk + C_1D^4L_2L_gRk - 6C_1D^2L_gMRk + 6C_1D^3L_gMRk - 2C_1D^4L_gMRk$$

$$b_4 = C_2C_3R^2k^2 + C_2C_3D^2R^2k^2 - 2C_2C_3DR^2k^2 + C_1C_2L_1L_gR^2k + C_1C_3L_2L_gR^2k + C_2C_3L_2L_gR^2k + C_1C_2D^2L_1L_gR^2k + C_1C_3D^2L_1L_gR^2k + 6C_1C_3D^2L_2L_gR^2k - 2C_1C_3D^3L_1L_gR^2k - 4C_1C_3D^3L_2L_gR^2k + C_1C_3D^4L_1L_gR^2k + C_2C_3D^2L_2L_gR^2k + C_1C_3D^4L_2L_gR^2k - 6C_1C_3D^2L_gMR^2k + 6C_1C_3D^3L_gMR^2k - 2C_1C_3D^4L_gMR^2k - 2C_1C_2DL_1L_gR^2k - 4C_1C_3DL_2L_gR^2k - 2C_2C_3DL_2L_gR^2k + 2C_1C_3DL_gMR^2k$$

APPENDIX B (Continued)

$$b_5 = C_1C_2L_gRD^2k^2 - 2C_1C_2L_gRDk^2 + C_1C_2L_gRk^2$$

$$b_6 = C_1C_2C_3L_gD^2R^2k^2 - 2C_1C_2C_3L_gDR^2k^2 + C_1C_2C_3L_gR^2k^2$$

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